CAEN
*Tools for Discovery*

# A5203(B)/DT5203

*64/128 Channel picoTDC unit for FERS-5200*


JANUS FERS CAEN | CAEN FERSlib | 10/100 MbE | TDLINK | USB 2.0 | WEB INTERFACE

## Overview

The A5203 (or desktop DT5203 version) is a front-end TDC module of the FERS-5200 platform, optimized for time measurements with the high-resolution picoTDC ASIC developed at CERN. The base A5203 model features 64 input channels, while the A5203B version includes a mezzanine board to extend functionality to 128 channels.

Each channel receives LVDS signals and measures the Time of Arrival (ToA) and, optionally, the Time over Threshold (ToT) thanks to the trailing edge acquisition, at resolutions down to 3.125 ps. Four acquisition modes are supported:

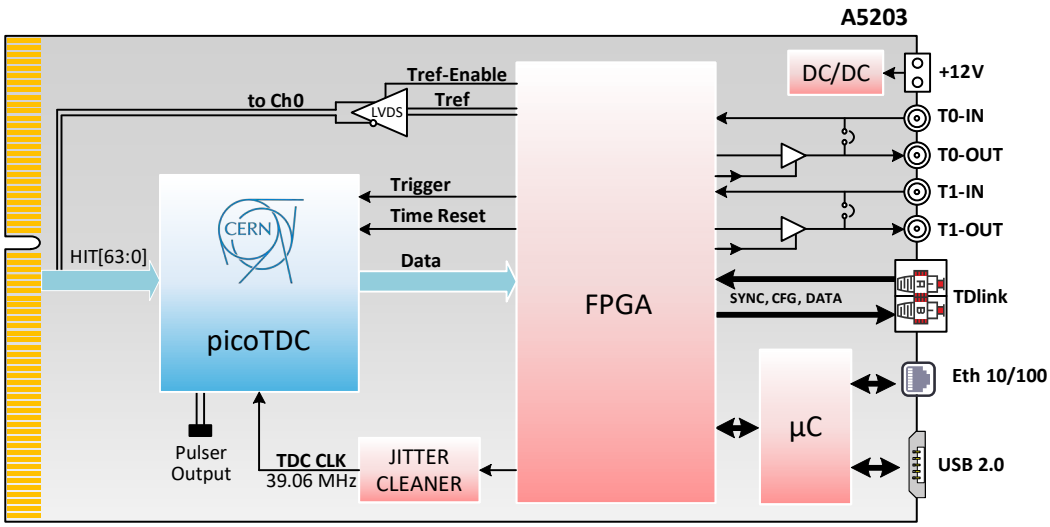
- Common Start
- Common Stop
- Streaming
- Trigger Matching

Integration with JANUS 5203 open source software provides full control of acquisition settings, synchronization, and data visualization, making the module ideal for fast-timing and multi-hit experiments requiring scalable channel density and deterministic timing. The FERSlib open source library is also available for custom-made software.

The offer is completed by a useful set of adapters to easily connect signals with flat cables to the high-density input edge-connector of the A5203. The A5256 adapter allows to use 16+1 single-ended signals on LEMO connectors and discriminate them thanks to the embedded fast voltage comparators with programmable threshold.

## Highlights

- Up to 128 channels with picoTDC ASICs (64 ch in A5203 / DT5203, 128 ch in A5203B)
- Input signal: LVDS, with 1.2 V common mode, and 1.45 V absolute voltage (DC coupled)
- Sub-10 ps RMS timing resolution with programmable LSB (min. 3.125 ps)
- Acquisition modes: Common Start, Common Stop, Streaming, Trigger Matching
- 56-bit coarse timestamp for global synchronization (25.6 ns LSB)
- USB 2.0, 10/100T Ethernet, and 3.125 Gbps TDlink (for DT5215 and DT5216connection) communication interfaces
- Daisy chain support for clock and sync signals
- Compact form factors: OEM board (A5203), desktop (DT5203), or extended A5203B
- Fully compatible with JANUS (5203 version)
- supported by the CAEN FERSlib Library, C/C++ software API




*Simplified block diagram of the A5203/DT5203 FERS-5200 unit.*

## Operating Modes

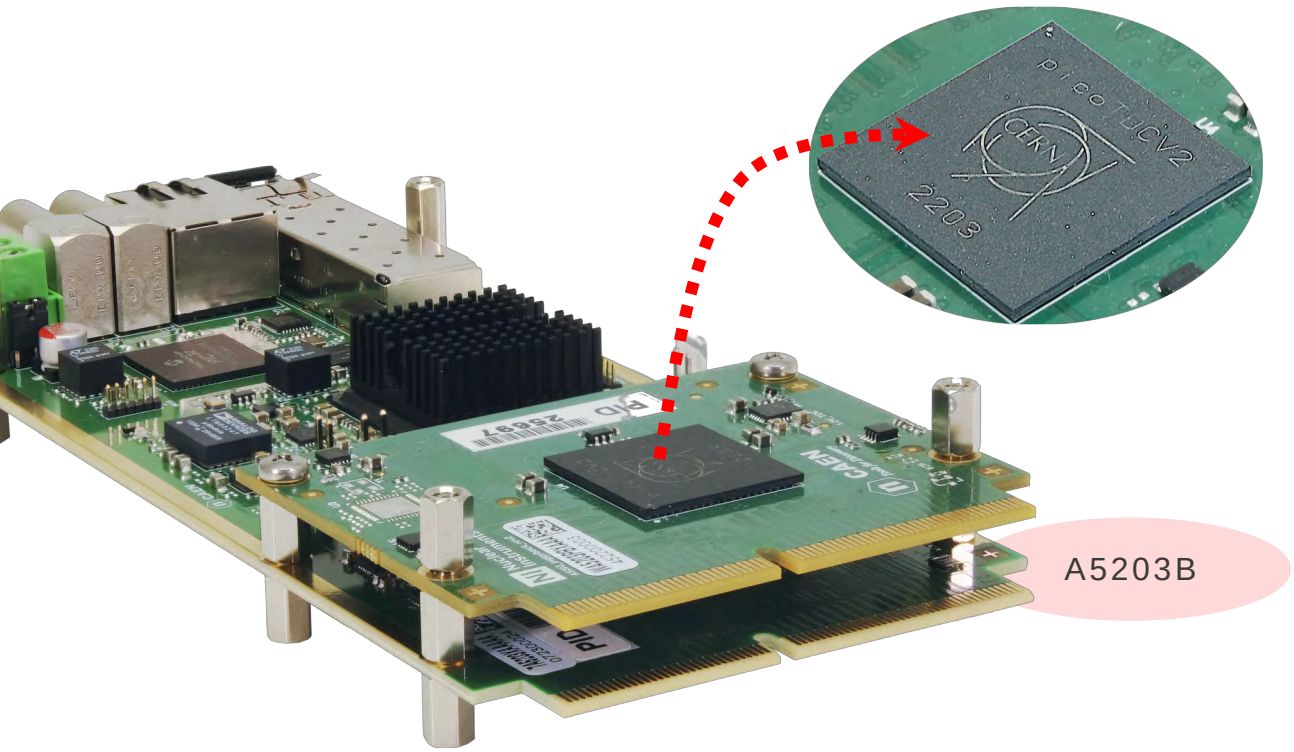
The A5203(B)/DT5203 supports four acquisition modes, selectable via software, depending on the experimental needs. Each mode is optimized for specific time measurement scenarios and is fully supported by the Janus 5203 software and FERSlib APIs.

Common Start Mode: In this mode, a signal on a reference channel (typically channel 0) defines the start of an acquisition window. Each of the remaining channels records the first hit occurring after this common start (inside the acquisition window). The measured quantity is the time difference ΔT between the reference and the hit. Multi-hit recording is not supported: only the first hit per channel inside the gate is recorded. A coarse timestamp (56-bit, 12.8 ns LSB) and fine timestamp (3.125 ps LSB) are provided. This mode is ideal for stop detectors in TOF set-ups.

Common Stop Mode: In this mode, a signal on a reference channel (typically channel 0) defines the stop of an acquisition window. Each of the remaining channels records the last hit occurring before this common stop. The measured quantity is the time difference ΔT between the hit and the reference. Multi-hit recording is not supported: only the last hit per channel inside the gate is recorded. A coarse timestamp (56-bit, 12.8 ns LSB) and fine timestamp (3.125 ps LSB) are provided.

Streaming Mode: In Streaming mode, the module records all input hits without requiring a trigger. Hits are timestamped with 64-bit absolute times, combining a coarse counter and fine timing at 3.125 ps resolution.

Trigger Matching Mode: In this flexible mode, multiple hits per channel are captured within a programmable acquisition window defined by an external or internal trigger. All hits inside the window are time-referenced to the trigger timestamp (25.6 ns LSB), while time difference between hits and the trigger timestamp retain the full 3.125 ps resolution. This mode enables multi-hit capture and is ideal for high-rate experiments.




The A5203(B)/DT5203 supports several measurement modes, selectable depending on the acquisition scenario and data throughput requirements:

LEAD ONLY: Records only the leading edge of each hit with maximum resolution (3.125 ps LSB). Ideal for applications needing precise ToA only.

LEAD ToT8: Stores leading edge plus 8-bit ToT value, providing coarse amplitude information. Slightly reduced dynamic range for ToA.

LEAD ToT11: Same as above, but with 11-bit ToT. Useful for applications requiring finer ToT resolution.

LEAD TRAIL: Saves both leading and trailing edges of each hit in two separate event words. Allows software-level ToT calculation with extended dynamic range, but doubles data throughput.

All measurement modes produce 32-bit event words and support configurable packetization. Depending on the acquisition mode, only a subset of measurement modes may be available. Refer to the JANUS 5203 software documentation (UM9636) for detailed compatibility.

## Connectivity

The A5203(B)/DT5203 modules feature multiple communication interfaces for data acquisition, and system control and integration:

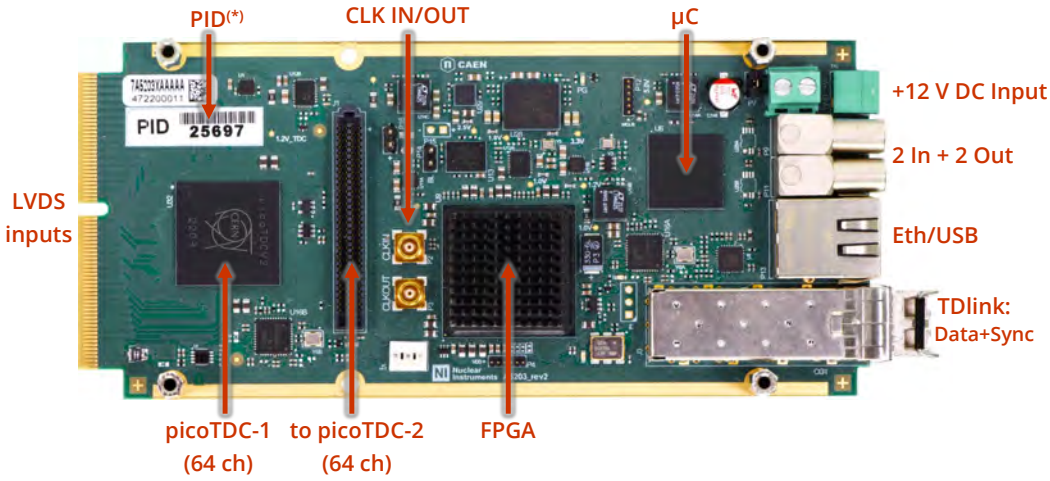
USB 2.0 (Micro-USB type B): direct connection to host PC for configuration and readout in standalone setups.

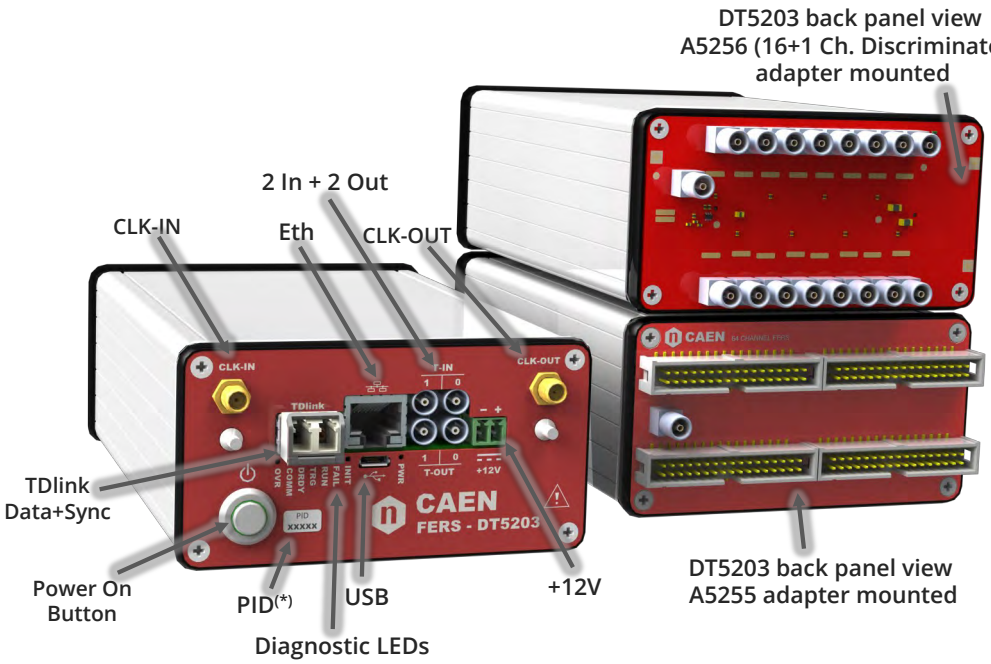
Ethernet 10/100 Mbps (RJ-45): direct connection to host PC for configuration and readout in standalone setups. Web interface for IP management (DHCP option).

TDlink Optical Interface (3.125 Gbps): high-speed optical link running TDlink CAEN proprietary protocol designed for scalable multi-board systems embedding the DT5215/DT5216 Concentrator Boards. It supports data transfer, synchronization signals, and broadcast commands (e.g. run, start/stop). Up to 16 boards can be daisy-chained per optical ring with the DT5215 (supporting up to 128 units), and up to 8 boards for the single DT5216 link, LC connector, OM2/OM3 fiber compatible.

Front Panel LEMO I/Os: 2 inputs (T0-IN, T1-IN), supporting both LVTTL and NIM levels, 2 outputs (T0-OUT, T1-OUT), LVTTL standard. These lines are used for external triggers, trigger propagation and user-defined logic signals. The inputs are 50 Ω terminated and support jumper-based reconfiguration for daisy-chain or wired-OR topologies.

SMA/MCX clock I/Os: CLK-IN and CLK-OUT allow deterministic clock distribution across boards. Daisy-chain configuration supported.



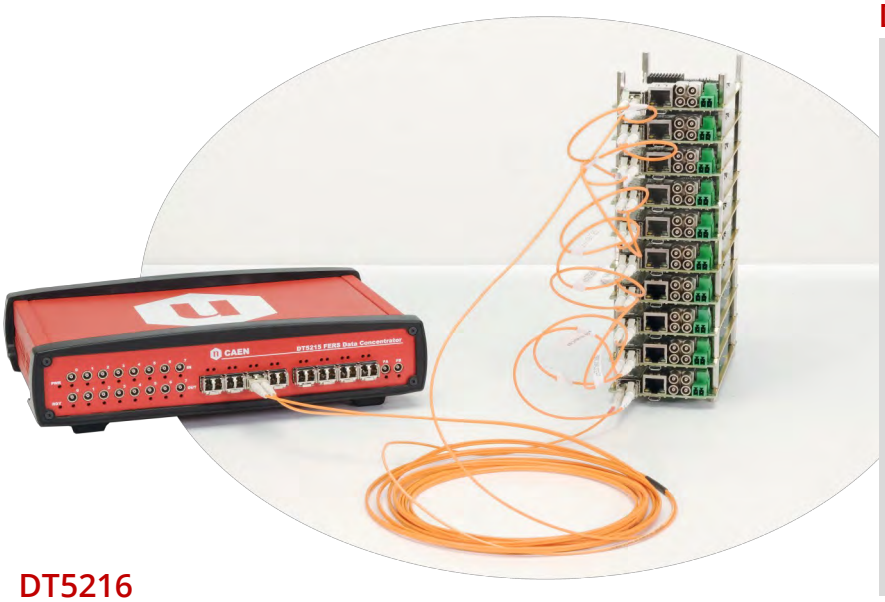

(*) PID (Product IDentifier)

The PID is a unique, incremental number greater than 10000 assigned to every CAEN product. This unique identifier is affixed to the product on an adhesive label composed of the "PID" prefix followed by the incremental number. The PID can also be read by the attached CODE39 barcode.

## Synchronization

- Daisy chain and wired-OR configurations supported for scalable trigger distribution across multiple modules
- Integrated support for optical link interconnect (3.125 Gbps – TDlink proprietary protocol) to enable synchronized acquisition of up to 128 modules via DT5215 Concentrator Board and up to 8 modules via DT5216
- When connected in Daisy chain to the DT5215 / DT5216, first board picoTDC clock propagation to the other boards in Daisy chain to improve time resolution
- Thanks to the DT5215 / DT5216, deterministic time alignment enabled by distributed 56-bit timestamp counter (12.8 ns LSB) with synchronization via external timestamp reset (GPS, 15MHz clk) only DT5215
- Multiple DT5215 units can be interconnected for large distributed FERS installations

## DT5215 and DT5216 – FERS Concentrator Boards



### DT5215

- Centralized control of FERS-5200 front-end modules
- 8 optical TDlink outputs (3.125 Gbps), each supporting up to 16 daisy-chained modules
  - Up to 128 modules (8192 channels)
- Host interfaces: USB 3.0, 1 GbE, 10 GbE
- Synchronization via RJ45 SYNC ports, internal or external GPS-ready clock
- Deterministic timing with 6.4 ns skew compensation
- Integrated web interface for configuration
- Fully supported by JANUS-5202 software on Windows® and Linux®

### DT5216

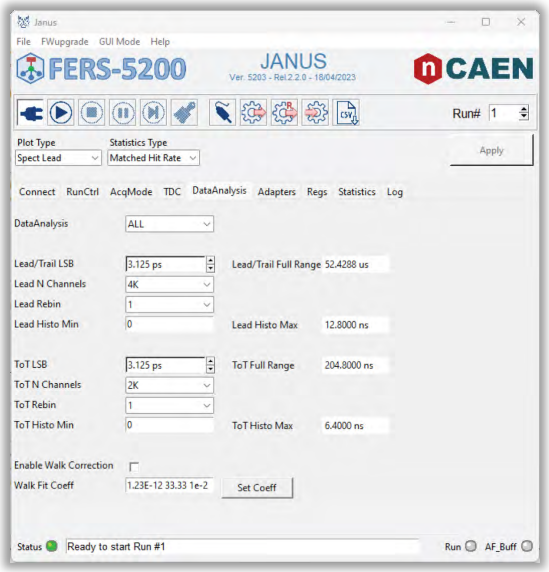
- Centralized control of FERS-5200 front-end modules
- 1 optical TDlink output supporting up to 8 daisy-chained modules
  - Up to 512 channels
- Host interface: USB 3.0
- Deterministic timing with 6.4 ns skew compensation
- Full software support via JANUS-5202 on Windows® and Linux®


DT5215 is a concentrator board for FERS-5200 systems, acting as a central hub for data acquisition and synchronization. It features 8 high-speed optical TDlink outputs (3.125 Gbps, CAEN proprietary protocol), each capable of connecting up to 16 daisy-chained front-end modules. In total, it can manage up to 128 FERS units, corresponding to 8192/16384 channels. Configuration is handled through a built-in web interface. The DT5215 provides multiple host connections, including USB 3.0, 1 GbE, and 10 GbE, and supports both internal and external (GPS-ready) synchronization.

DT5216 is the compact counterpart, designed for smaller setups. It offers a single TDlink output supporting up to 8 FERS modules (512/1024 channels). While limited in scalability, it ensures the same reliability and flexibility in integration, making it well suited for compact or medium-scale systems. DT5216 provides USB 3.0 connectivity for data readout.

Both models implement deterministic time alignment with 6.4 ns skew compensation and support the broadcast execution of system commands (Run Start/Stop, timestamp reset).

JANUS 5202 software fully supports both models in Windows® and Linux® environments.




## JANUS FERS-5200 DAQ Software

www.caen.it/products/janus/

- Model-dependent GUI for a quick and easy start
- Open-Source for user customization
- Management of the acquisition parameters of all connected boards
- Multi parametric Jobs and Runs with time or counts preset
- Data saving of lists in .bin, .txt and .csv formats
- Statistics and Plots visualization
- Available for Windows® and Linux® platforms

JANUS 5203 is the official readout software developed by CAEN for the A5203(B)/DT5203 modules. It provides full control over configuration parameters, acquisition modes, and real-time monitoring. The software is available both as a command-line tool (C-based) and a Python-based GUI that includes configuration panels, live histograms, and run control.

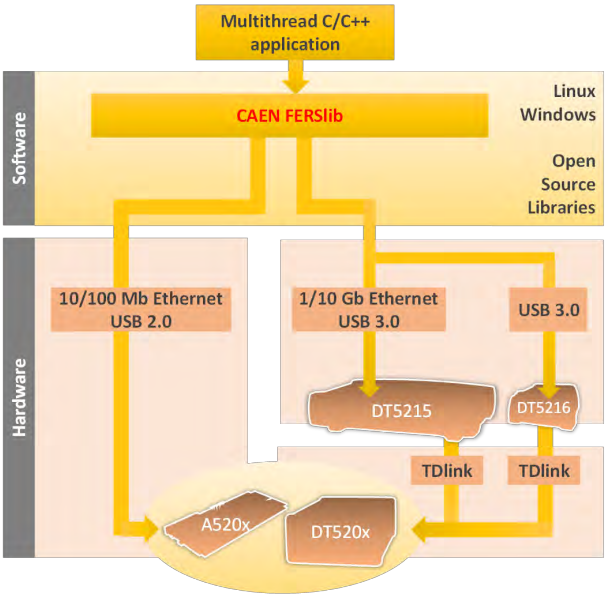
Supported features include hit-rate visualization, ToA/ToT histograms, list-mode data export, and synchronized acquisition from multiple modules. JANUS 5203 also provides slow control, timestamping, and board identification. The system is compatible with both Windows® and Linux®, and supports integration with the DT5215 and DT5216(*) concentrator board for large-scale setups.

(*) Coming Soon

## CAEN FERSlib Library

https://www.caen.it/products/caen-ferslib-library/

- Full control and data acquisition for CAEN FERS-5200 boards
- Supports all acquisition modes: spectroscopy, timing (ToA/ToT), and counting modes
- Manages all FERS unit communication interfaces
- .Supports system connection via TDLink to the DT5215 and DT5216
- Designed for integration in custom DAQ frameworks
- Available in C/C++ for Windows® and Linux® platforms




The A5203(B)/DT5203 module is natively supported by the CAEN FERS Library, a C/C++ software API designed for the full configuration, control, and data acquisition of boards within the FERS-5200 family. The library is compliant with the C99 and C++14 standards, and is available for integration in custom DAQ software environments on both Windows® and Linux® platforms.

The FERS Library provides a rich set of data structures and low-level routines to manage acquisition in all supported modes (Common Start, Common Stop, Streaming, Trigger Matching). Core features include:

- Board and chain discovery, initialization, and status monitoring
- Full configuration control through the Config_t structure
- Native support for concentrator board and TDlink chains

Demo Codes are present inside the lib package to give a starting point for software creation.

# Technical Specifications

## General Features

| TDC Inputs | A5203 / DT5203 | A5203B |
|---|---|---|
| Number of Channels | 64 | 128 |
| Connector | nr.1 edge connector type HSEC8-170<br>Optional front panel adapter (A5255)<br>for ribbon cable input, already mounted on DT5203 | nr.2 edge connector type HSEC8-170 |
| Input Type | Differential LVDS, 1.2 V common mode (DC-coupled)<br>Voltage range: −40 mV to +1450 mV<br>Differential voltage: 140 mV to 450 mV<br>100 Ω input termination | |
| **Timing Resolution** | | |
| LSB | 3.125 ps (minimum picoTDC programmable resolution) | |
| Fixed amplitude pulses: | $\Delta T_{RMS}$ ~5 ps (LVDS input)<br>$\Delta T_{RMS}$ ~7 ps (with A5256 fast discriminator) | |
| Variable amplitude pulses | $\Delta T_{RMS}$ ~20 ps (after ToT walk correction) ) | |
| **Timestamping** | | |
| Coarse | 56-bit counter, 12.8 ns LSB | |
| Fine | PicoTDC timestamp with programmable resolution (min. 3.125 ps) | |
| **Dynamic Range** | | |
| LEAD ONLY | up to 26 bits (≈210 µs) | |
| LEAD ToT8 | ToA up to 19 bits, ToT 8 bits | |
| LEAD ToT11 | ToA up to 16 bits, ToT 11 bits | |
| LEAD TRAIL | full 26-bit timing for both edges | |
| Extended to 64 bits in streaming mode with FPGA time base | | |

## Operating Modes

**Common Start**

- Measures $\Delta T = T_{hit} - T_{ref}$
- Only the first hit after the reference trigger is recorded
- ToT optional
- Multi-hit not supported

**Common Stop**

- Measures $\Delta T = T_{ref} - T_{hit}$
- Only the last hit before stop is recorded
- Same logic and timing performance as Common Start

**Streaming**

- Continuous acquisition of all hits without trigger
- Absolute timestamps (64-bit)
- Supports LEAD, LEAD TRAIL, and (soon) LEAD ToT

**Trigger Matching**

- Multi-hit per channel acquisition inside a programmable time window
- All hits referred to a coarse timestamp (25.6 ns LSB), internal or external trigger
- Maintains full 3.125 ps resolution for relative time

# Technical Specifications (continued)

## Fiters

**Zero Suppression via ToT**

- Channel-by-channel, available in all gated modes
- Reduces event size by removing empty channels (trigger acquisition windows with no Bias)

## Acquisition Memory

Local Event Buffering: Events are buffered locally in FPGA memory before transfer. No long-term acquisition storage.

## Communication Interfaces

**USB 2.0**

A micro-USB type B port allows direct connection to a host PC. It is ideal for standalone operation, offering easy access to configuration and acquisition control via the Janus 5203 software

**Ethernet 10/100 Mbps**

This interface supports both configuration and real-time data transfer, allowing integration in networked DAQ setups.

**TDlink Optical Interface ( to the DT5215 / DT5216 only)**

A high-speed 3.125 Gbps optical link designed for scalable and distributed FERS-5200 installations. TDlink supports synchronized readout, command broadcasting (e.g. start/stop run), and slow control for up to 16 modules in daisy-chain (ring) topology. (up to 8 modules in case of DT5216).

## Trigger and Synchronization

**Digital I/O (LEMO-compatible)**

Four programmable lines (T0-IN, T1-IN, T0-OUT, T1-OUT) support input/output functions such as global trigger, external time reference (Tref), and veto. Accepts LVTTL or NIM levels; outputs are LVTTL with 50 Ω termination.

**Trigger Logic**

Internal logic supports external triggers (periodic, manual, T0/T1-IN). Internal programmable periodic trigger generator (from 25.6 ns to ~55 s).

**Timestamping**

56-bit coarse timestamp counter with 12.8 ns LSB, plus fine timestamp from picoTDC with 3.125 ps LSB. Full 64-bit absolute timing supported in streaming mode.

**Synchronization**

Modules can be synchronized via TDlink, external triggers, or timestamp reset signals. Multiple DT5215 concentrators can coordinate distributed systems via future S-LINK interface.

## Firmware and FPGA

**FPGA**

| | |
|---|---|
| Device | Xilinx® Artix-7 XC7A75T-1FGG676C. Handles buffering, synchronization, trigger logic, and data formatting |
| Upgrades | Performed via Janus 5203 software. Firmware (.ffu) files can be uploaded directly to the onboard Flash memory. Version and build info are displayed in the web interface or Janus GUI |

# Technical Specifications (continued)

## Software

| JANUS 5203 | |
|---|---|
| GUI | Cross-platform Python-based interface with basic and advanced modes. Features include live histogramming (ToA, ToT), configuration panels, multi-board support, and real-time run control. |
| Console Interface | Command-line acquisition and scripting via JanusC executable. Ideal for automation or headless setups. |

| Web Interface |
|---|
| Accessible via browser at 192.168.50.3 for basic configuration, IP setup, and diagnostics |

| FERSlib Library SDK |
|---|
| Open-source C/C++ SDK under LGPL v3 license. Supports integration in user DAQ systems with full event structure for ToA, ToT, and trigger data. Compatible with both Windows® and Linux® platforms. |

## Mechanical

| | A5203 | A5203B | DT5203 |
|---|---|---|---|
| Form Factor | OEM module without enclosure | OEM module without enclosure | Desktop<br>Enclosure: Aluminium housing with integrated fan |
| Weight | 140 g | 163g | 503 g |
| Dimensions | 73.0 W × 20.0 H × 165.5 L $mm^3$ | 73.0 W × 20.0 H × 164.5 L $mm^3$ | 106.5 W × 56.5 H × 187.5 L $mm^3$ |
| | Requires external ventilation | Includes additional mezzanine board<br>Stackable via metal spacers<br>Requires external ventilation | Includes A5255 adapter for front-panel connectivity<br>Fan included in the case |

## Environmental

| | |
|---|---|
| Environmental | Indoor use |
| Operating Temperature | 0°C ÷ +40°C |
| Storage Temperature | -10°C ÷ +60°C |
| Operating Humidity | 10% ÷ 90% RH non condensing |
| Storage Humidity | 5% ÷ 90% RH non condensing |
| Pollution Degree | 2 |
| Overvoltage Category | II |
| EMC Environment | Commercial and light industrial |
| IP Degree | Enclosure (desktop models), not for wet location |

## Regulatory

| | | |
|---|---|---|
| Compliance | EMC: | CE 2014/30/EU Electromagnetic compatibility Directive |
| | Safety: | CE 2014/35/EU Low Voltage Directive |

## Power Requirements

| Input Voltage | + 12 V DC | Accepted Voltage Range: | +7 V to +15 V |
|---|---|---|---|

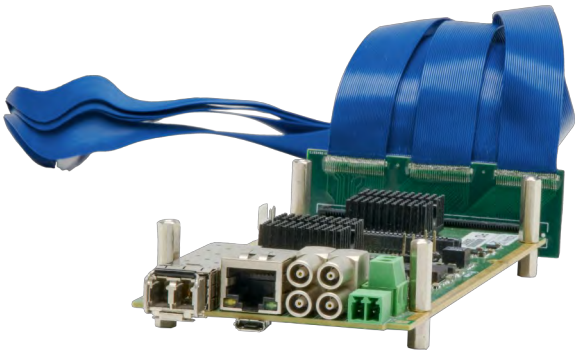
| | A5203 | A5203B | DT5203 |
|---|---|---|---|
| Power Consumption | 700 mA<br>≈ 8.4 W | TBD | 700 mA<br>≈ 8.4 W |
| Power Supply | requires external DC source | requires external DC source | includes 12 V / 45 W AC-DC adapter and cable |
| Power connector | DC jack | DC jack | DC jack |

## Safety Notes

- A5203/A5203B is ESD-sensitive and must be handled in EPA environments
- Use appropriate shielding and avoid operation in explosive or wet conditions
- Always provide sufficient ventilation to prevent overheating

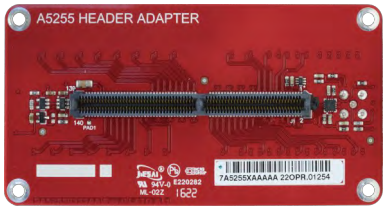
## A5260 – Remotization cable for FERS-5200 boards

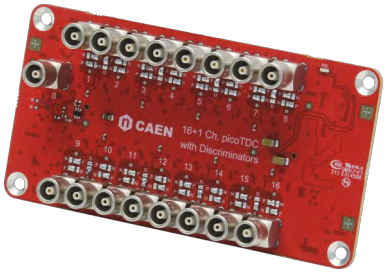
The A5260 flat cable has been designed to allow the remotization of the edge card connector of FERS-5200 boards. On one side, the cable features a Samtec HSEC8-170-01-S-DV-A connector mating directly to the edge card connector of FERS-5200 boards. On the other side, the cable features edge card connectors type HSEC8-170 (140 contacts with 0.8 mm pitch) mating directly to FERS-5200 header adapters (e.g. A5255, A5256). Thanks to this cable, detectors can be moved up to one meter (A5260B) away from the readout electronics without experiencing a significant signal degradation.



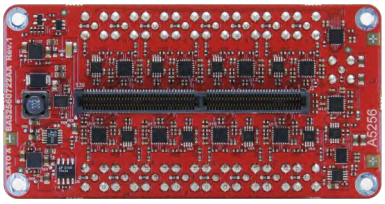

## A5255 – 17x2 pin 2.54 mm pitch Quad Connector for A5203/DT5203

The A5255 is a  four 17×2 pin, 2.54 mm pitch header adapter (64 channels in total) for flat cables. It provides an auxiliary LEMO connector for NIM/TTL signals, driving channel 0, that is the common time reference (selection between NIM/LVTTL  via solder jumpers).



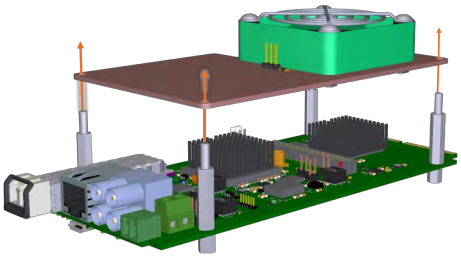

## A5256 – 16+1 Channels Discriminator for A5203/DT5203



The CAEN Mod.A5256 is a 16+1 channels adapter for A5203/DT5203 board. It provides dual threshold, leading edge discriminators for analog single-ended signals on LEMO coaxial connectors. It includes ultra-fast comparators with programmable thresholds (DAC) and accepts both positive and negative analog pulses, as well as NIM/TTL logic signals. It features a dedicated connector for Channel 0 to be used as a common time reference (Tref). The dual threshold allows for a better ToT to amplitude conversion and walk correction, as well as pulse shape discrimination.


## A5270 – FERS cooling fan

The CAEN Mod. A5270 is a fan for the FERS-5200 system, to be mounted on the top or on the side of A5203(B) boards. It is powered by the HV fan connector of A5203(B) units. The speed of the fan can be changed thanks to a jumper on the top of the board.



## Ordering Option

| Description | Code |
|---|---|
| A5203 - 64 Channel pico-TDC unit for FERS-5200 | WA5203XAAAAA |
| A5203B - 128 Channel pico-TDC unit for FERS-5200 | WA5203BXAAAA |
| DT5203 - Desktop 64 Channel pico-TDC unit for FERS-5200 | WDT5203XAAAA |
| ***Accessories*** | |
| A5260 - Remotization cable for FERS-5200 boards - 50 cm | WA5260XAAAAA |
| A5260B - Remotization cable for FERS-5200 boards - 100 cm | WA5260BXAAAA |
| A5255 – 17x2 pin 2.54 mm pitch Quad Connector for A5203/DT5203 | WA5255XAAAAA |
| A5256 – 16+1 ch pos/neg Discriminator for A5203 | WA5256XAAAAA |
| A5270 - FERS cooling fan | WA5270FANXAA |

# A5203(B)/DT5203 64/128 Channel picoTDC unit for FERS-5200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DT5203

A5203