CAEN
Tools for Discovery

A5202/DT5202

64 Channel Citiroc unit
for FERS-5200

Overview

The A5202 (or desktop DT5202 version) is a front-end readout unit designed for the FERS-5200 platform. It integrates 64 readout channels based on Citiroc-1A ASICs, providing analog front-end and digital processing optimized for Silicon Photomultiplier (SiPM) detectors. Each channel includes programmable amplification, shaping, and discrimination, enabling high-resolution pulse analysis.

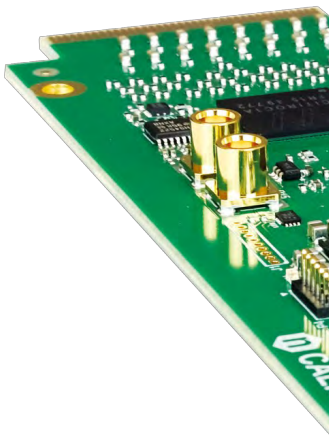
The module supports Spectroscopy (PHA), Timing, and Counting acquisition modes, fully configurable via the Janus 5202 software suite. Thanks to the onboard high-voltage generator and programmable trimming, the A5202 provides accurate and stable biasing of the connected SiPM, ensuring optimal operating conditions and consistent detector response.

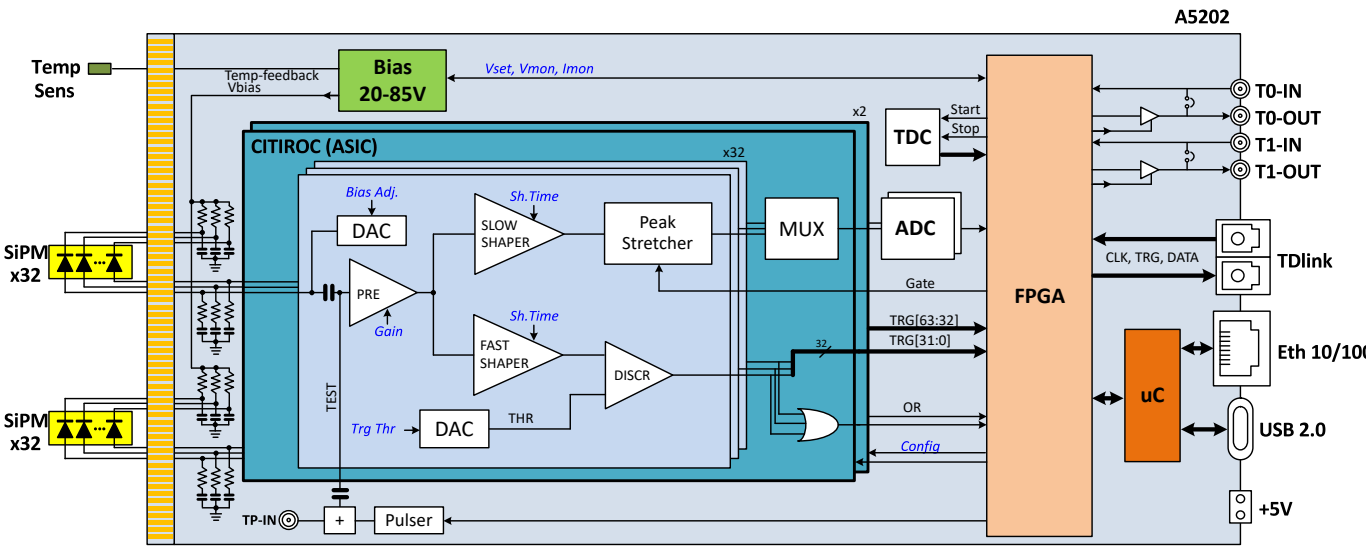
The unit supports USB 2.0, Ethernet 10 /100T, and a high-speed optical link interface (TDlink*). Integration into distributed systems is enabled via daisy-chained synchronization, making the A5202 ideal for scalable detector arrays.

* *CAEN proprietary protocol*

Highlights

- 64-channel readout based on Citiroc-1A ASICs
- Integrated preamplifier, fast/slow shapers, discriminators, ADC, and trigger logic per channel
- Acquisition modes: Spectroscopy (PHA), Timing (ToA/ToT), Counting
- Internal self-trigger and external trigger support (LEMO connection)
- Programmable 20÷85 V SiPM bias with 8-bit individual adjustment and temperature compensation
- Software-selectable shaping times and gains
- Interfaces: USB 2.0, 10/100T Ethernet, optical link (TDlink) @ 3.125 Gbps
- Daisy-chain capability for trigger and sync distribution
- Available in two versions: A5202 (assembled board) and DT5202 (aluminum enclosure).
- Fully supported by JANUS 5202 acquisition software and FERSlib (Windows® / Linux®)





Simplified block diagram of the A5202/DT5202 FERS-5200 unit

Operating Modes

The A5202/DT5202 supports multiple acquisition modes to meet the needs of various experimental setups:

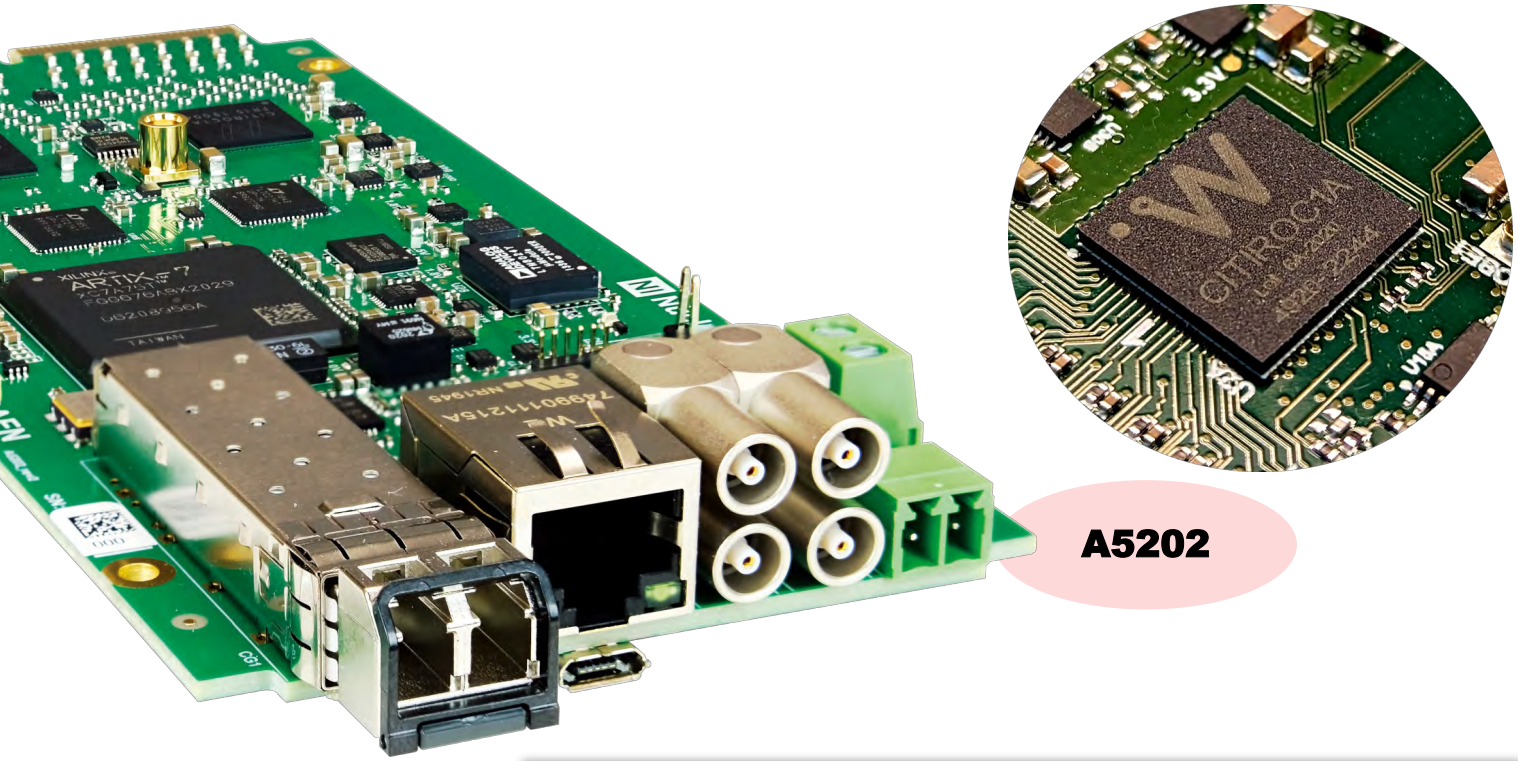
Spectroscopy Mode (PHA): used for energy measurements. Signals pass through the slow shaper and peak-hold circuit. A global bunch trigger (external or internal) controls the acquisition. Each valid peak is acquired and time stamped .

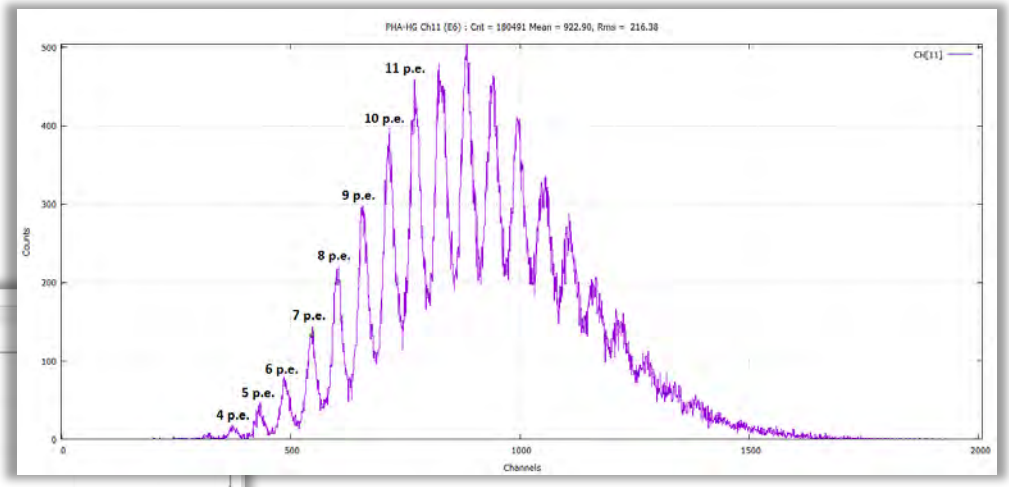
Counting Mode: used for event counting above programmable thresholds. Each channel counts independently, suitable for rate monitoring or threshold scans.

Timing Mode: used for precise time-of-arrival (ToA) and time-over-threshold (ToT) measurements. Based on fast shaper and discriminator output. Provides sub-nanosecond resolution.

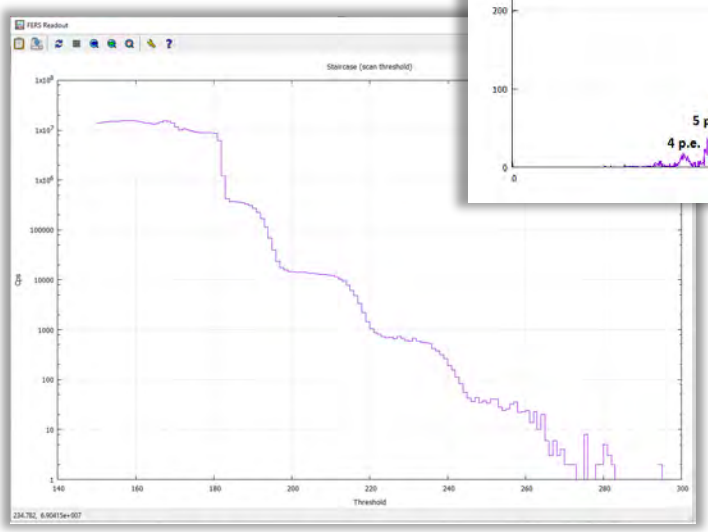
Spectroscopy and Timing Mode: This hybrid mode combines the capabilities of both PHA and timing. For each bunch trigger, the module performs energy conversion across all channels while also recording ToA and ToT information.

All modes are configurable via JANUS 5202 and FERSlib, which manage data flow, channel masking, triggering logic, and synchronization.





Pulse height amplitude spectrum with the association of each peak to the correspondent number of photoelectrons triggered



Count rate as a function of the channel self-trigger threshold (staircase) acquired in dark conditions. Each step corresponds to a different number of photoelectrons triggered

Connectivity

The A5202/DT5202 modules feature multiple communication interfaces for data acquisition, and system control and integration:

USB 2.0 (Micro-USB type B): direct connection to host PC for configuration and readout in standalone setups.

Ethernet 10/100 Mbps (RJ-45): direct connection to host PC for configuration and readout in standalone setups. Web interface for IP management (DHCP option).

TDlink Optical Interface (3.125 Gbps): high-speed optical link running TDlink CAEN proprietary protocol designed for scalable multi-board systems embedding the DT5215/DT5216 Concentrator Boards. It supports data transfer, synchronization signals, and broadcast commands (e.g. run, start/stop). Up to 16 boards can be daisy-chained per optical ring with the DT5215 (supporting up to 128 units), and up to 8 boards for the single DT5216 link, LC connector, OM2/OM3 fiber compatible.

Front Panel LEMO I/Os: 2 inputs (T0-IN, T1-IN), supporting both LVTTL and NIM levels, 2 outputs (T0-OUT, T1-OUT), LVTTL standard. These lines are used for external triggers, trigger propagation and user-defined logic signals. The inputs are 50 Ω terminated and support jumper-based reconfiguration for daisy-chain or wired-OR topologies.

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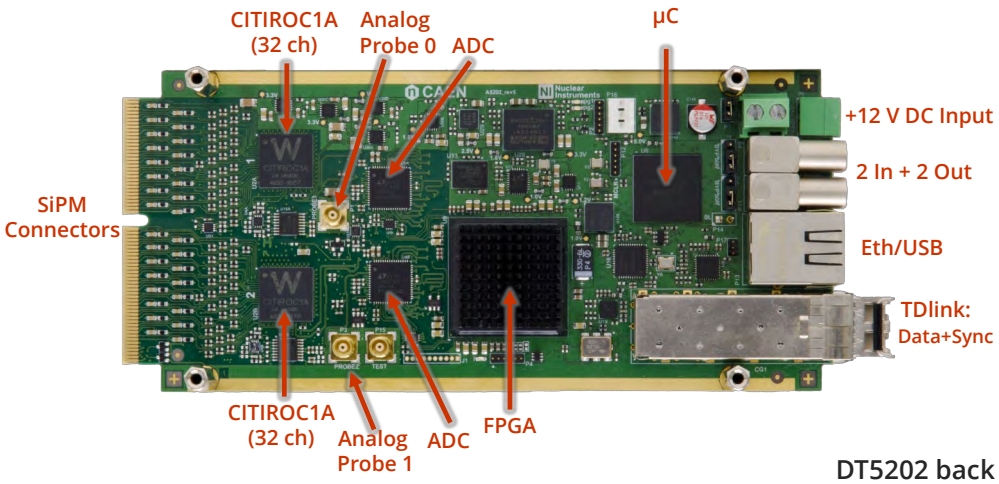
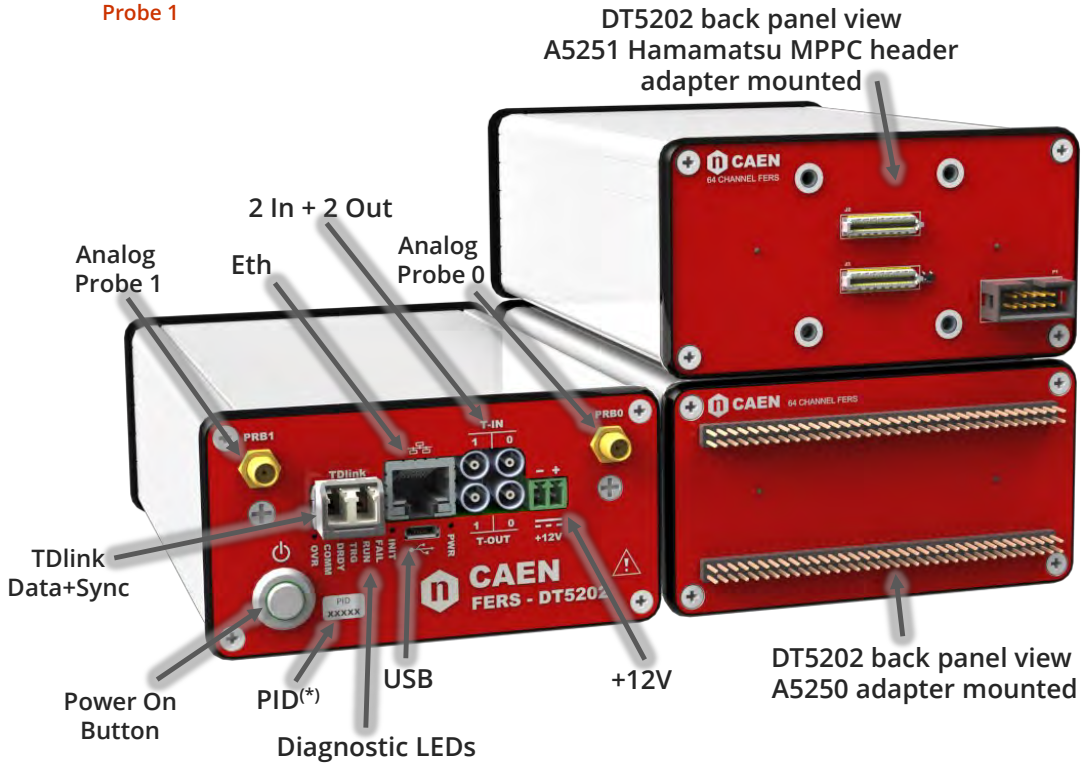
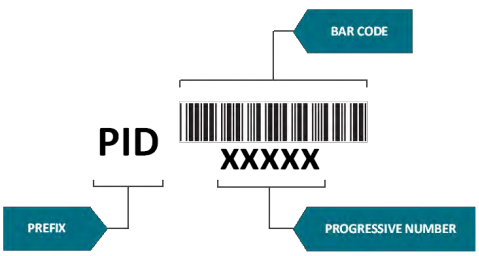






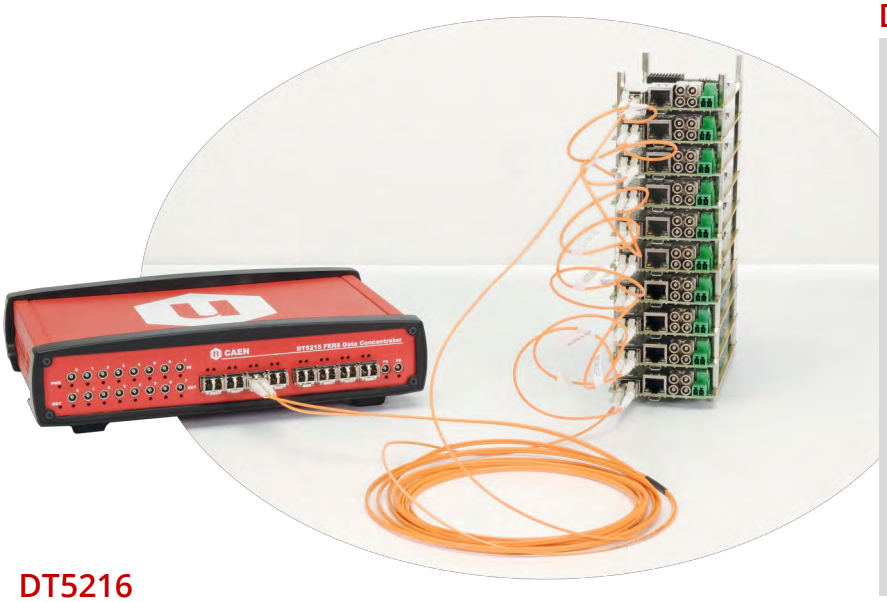
(*) PID (Product IDentifier)

The PID is a unique, incremental number greater than 10000 assigned to every CAEN product. This unique identifier is affixed to the product on an adhesive label composed of the "PID" prefix followed by the incremental number. The PID can also be read by the attached CODE39 barcode.

Synchronization

- Daisy chain and wired-OR configurations via LEMO T-IN/T-OUT supported for scalable trigger distribution across multiple modules
- Integrated support for optical link interconnect (3.125 Gbps – TDlink proprietary protocol) to enable synchronized acquisition of up to 128 modules via DT5215 Concentrator Board and up to 8 modules via DT5216
- Deterministic time alignment via distributed 56-bit timestamp counter (12.8 ns LSB), with external timestamp reset; DT5215 supports synchronization via external reference clock or GPS-disciplined sources
- Multiple DT5215 units can be interconnected for large distributed FERS installations

DT5215 and DT5216 – FERS Concentrator Boards



DT5215

- Centralized control of FERS-5200 front-end modules
- 8 TDlink connection (3.125 Gbps), each supporting up to 16 daisy-chained modules
- Up to 128 modules (8192 channels)
- Host interfaces: USB 3.0, 1 GbE, 10 GbE
- Synchronization via RJ45 SYNC ports, internal or external GPS-ready clock
- Deterministic timing with 6.4 ns skew compensation
- Integrated web interface for configuration
- Fully supported by JANUS-5202 software and FERSlib on Windows® and Linux®

DT5216

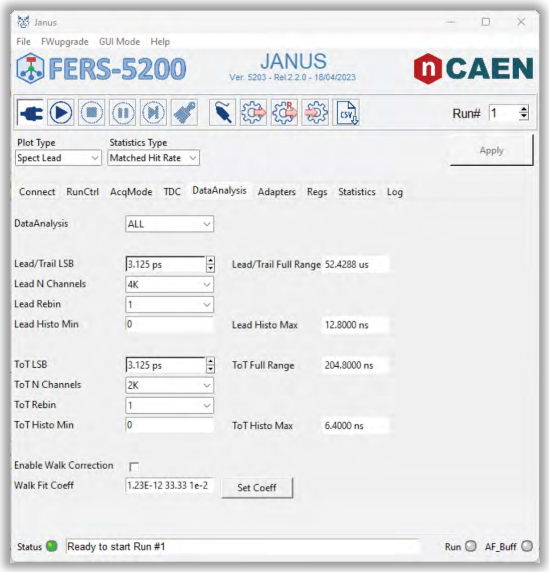
- Centralized control of FERS-5200 front-end modules
- 1 TDlink connection supporting up to 8 daisy-chained modules
- Up to 512 channels
- Host interface: USB 3.0
- Deterministic timing with 6.4 ns skew compensation
- Full software support via JANUS-5202 and FERSlib on Windows® and Linux®
- Performant and compact Setup

DT5215 is a concentrator board for FERS-5200 systems, acting as a central hub for data acquisition and synchronization. It features 8 high-speed optical TDlink (3.125 Gbps, CAEN proprietary protocol), each capable of connecting up to 16 daisy-chained front-end modules. In total, it can manage up to 128 FERS units, corresponding to 8192 channels. Configuration is handled through a built-in web interface. The DT5215 provides multiple host connections, including USB 3.0, 1 GbE, and 10 GbE, and supports both internal and external (GPS-ready) synchronization.

DT5216 is the compact counterpart, designed for smaller setups. It offers a single TDlink supporting up to 8 FERS modules (512 channels). While limited in scalability, it ensures the same reliability and flexibility in integration, making it well suited for compact or medium-scale systems. DT5216 provides USB 3.0 connectivity for data readout.

Both models implement deterministic time alignment with 6.4 ns skew compensation and support the broadcast execution of system commands (Run Start/Stop, timestamp reset).

JANUS 5202 software and FERSlib library fully support both models in Windows® and Linux® environments.



JANUS FERS-5200 DAQ Software

www.caen.it/products/janus/

- Model-dependent GUI for a quick and easy start
- Open-Source for user customization
- Management of the acquisition parameters of all connected boards
- Multi parametric Jobs and Runs with time or counts preset
- Data saving of lists in .bin, .txt and .csv formats
- Statistics and plots visualization
- Available for Windows® and Linux® platforms

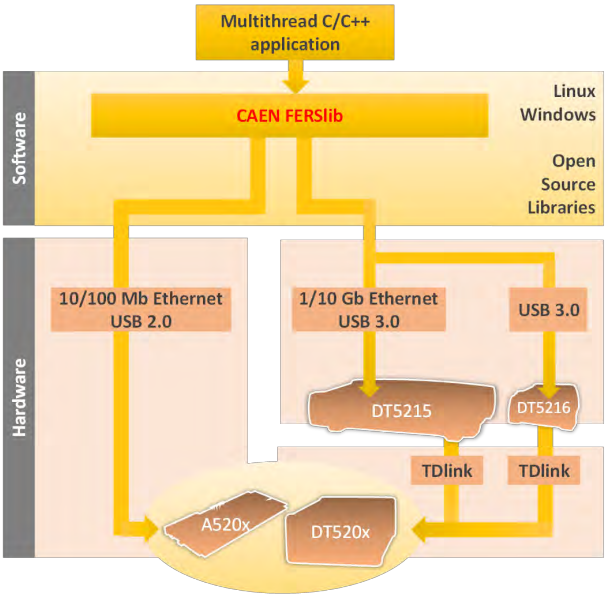
JANUS 5202 is the official readout software developed by CAEN for the A5202/DT5202 modules. It provides full control over configuration parameters, acquisition modes, and real-time monitoring. The software is available both as a command-line tool (C-based) and a Python-based GUI that includes configuration panels, live histograms, and run control.

Supported features include hit-rate visualization, ToA/ToT histograms, list-mode data export, and synchronized acquisition from multiple modules. JANUS 5202 also provides slow control, timestamping, and board identification. The system supports integration with the DT5215 and DT5216 concentrator boards for large-scale setups.

CAEN FERSlib Library

https://www.caen.it/products/caen-ferslib-library/

- Full control and data acquisition for CAEN FERS-5200 boards
- Supports all acquisition modes: spectroscopy, timing (ToA/ToT), and counting modes
- Manages all FERS unit communication interfaces
- Supports system connection via TDLink to the DT5215 and DT5216
- Designed for integration in custom DAQ frameworks
- Available in C/C++ for Windows® and Linux® platforms



The A5202/DT5202 module is natively supported by the CAEN FERS Library, a C/C++ software API designed for the full configuration, control, and data acquisition of boards within the FERS-5200 family. The library is compliant with the C99 and C++17 standards, and is available for integration in custom DAQ software environments on both Windows® and Linux® platforms.

The FERS Library provides a rich set of data structures and low-level routines to manage acquisition in all supported modes (Spectroscopy (PHA), Timing, and Counting). Core features include:

- Board and chain discovery, initialization, and status monitoring
- Full configuration control
- Native support for concentrator board and TDlink chains

Demo Codes are present inside the lib package to give a starting point for software creation.

Technical Specifications

General Features

Number of Channels	64 (2 CITIROC 1A chips)
ASIC	CITIROC 1A: 32– channel Scientific instrumentation SiPM read-out chip
Input Type	2 x double row strip header (35+35 pin, 0.8 mm pitch) providing 64 SiPM anode–cathode pairs, one temperature sensor, and multiple ground contacts
Input Signal Polarity	Positive
Charge Measurement	Each channel of CITIROC 1A embeds two independent programmable variable-gain preamplifiers ensuring a wide coverage of the dynamic range: LG (Low Gain) and HG (High Gain)
Dynamic Range	160 fC to 400 pC (1 to 2500 photoelectrons @ 10^6 SiPM gain)
Gain configuration via JANUS	Programmable via feedback capacitor Cf: 25 fF to 1575 fF (step: 25 fF) LG gain: 1.5 pF/Cf (max gain = 60) HG gain: 15 pF/Cf (max gain = 600)
Shaping Times	Each channel preamplifier is followed by a variable shaper with an adjustable time constant: SSH (Slow Shaper), FSH (Fast Shaper)
SSH (Slow Shaper) FSH (Fast Shaper)	7 options from 12.5 ns to 87.5 ns 15 ns (fixed)
Trigger Logic	For each channel, CITIROC 1A provides a programmable trigger line that can be connected to either the HG or LG preamplifier. It includes a fast shaper with a 15 ns peaking time, followed by two discriminators: “Charge” and “Time”
Thresholds setting	Coarse: Common for all channel set by two 10-bit DAC Fine: set by 4-bit DAC on each discriminator to compensate non-uniformities
Programmable trigger logic	AND, OR, Majority, AND2_OR32, OR32_AND2

System Performance

Spectroscopy Mode (PHA)

- Common trigger acquisition
- Max trigger rate: ~100 kHz
- Minimum conversion time (shaping-time dependent): ~10 µs
- Channel-by-channel digital threshold for Zero Suppression (ZS)

Counting Mode

- Individual channel counters
- Gated acquisition via internal periodic window or external trigger
- Max counting rate: ~20 Mcps per channel

Timing Mode

- Time of Arrival (ToA) with respect to a comon time reference signal and Time- over-Threshold (ToT)
- Resolution: 0.5 ns LSB (typ. 250 ps RMS)
- Continuous streaming with no intrinsic dead time

Spectroscopy + Timing

- Full spectroscopy + timing (ToA/ToT) per common trigger
- Both the PHA and timing information are available for each bunch trigger

High Voltage Power Supply

Single channel PCB mounted A7585D High Voltage Power Supply:
- Common SiPM bias voltage: 20 ÷ 85 V
- Settling precision: ± 20 mV
- Individual channel adjustment: 8-bit (2.5V or 4.5V dynamic range)
- Max. output bias current: 10 mA (software programmable limit)
- Programmable temperature compensation

Technical Specifications (continued)

Communication Interfaces

USB 2.0

A micro-USB type B port allows direct connection to a host PC. It is ideal for standalone operation, offering easy access to configuration and acquisition control via software and library.

Ethernet 10/100 Mbps

The RJ-45 connector enables remote operation over local networks. This interface supports both configuration and real-time data transfer, allowing integration in networked DAQ setups.

TDlink Optical Interface (to the DT5215 / DT5216 only)

A high-speed 3.125 Gbps optical link designed for scalable and distributed FERS-5200 installations. TDlink supports synchronized readout, command broadcasting (e.g. start/stop run), and slow control for up to 16 modules in daisy-chain (ring) topology (up to 8 modules in case of DT5216).

Trigger and Synchronization

Self-Triggering:

Each of the 64 channels features an independent discriminator with programmable thresholds (10-bit coarse + 4-bit fine DACs). These self-triggers can be used individually (e.g. for counting or timing), or logically combined through programmable logic (OR, AND, Majority). The resulting signal can serve either as a global bunch trigger for Spectroscopy acquisition or as a Time Reference (Tref) in Timing mode.

External Trigger Inputs

Two front-panel LEMO inputs (T0-IN and T1-IN) accept LVTTL or NIM logic levels. These can be used to inject a global external trigger or to synchronize multiple boards using daisy chain or wired-OR topologies. Both inputs are 50 Ω terminated by default and can be reconfigured via onboard jumpers.

Trigger Logic Options

Self-triggers can be combined via programmable logic (AND, OR, MAJORITY) to form internal trigger conditions or to generate time references for time stamping.

Timestamping and Synchronization

A 56-bit internal counter with 12.8 ns step provides timestamping capabilities for all acquisition modes. Synchronization across multiple modules is achieved via external timestamp reset signals or distributed through the TDlink optical interface and the DT5215 (or DT5216) concentrator board, ensuring global timestamp coherence in systems of up to 128 (or 8) boards.

Firmware and FPGA

FPGA	
Device	Xilinx® Artix-7 XC7A75T-1FGG676C. Supports Spectroscopy, Timing, Counting, and Spectroscopy + Timing modes
Upgrades	Firmware upgradeable via USB, Ethernet and TDlink Performed via JANUS 5202 software. Firmware (.ffu) files can be uploaded directly to the onboard Flash memory. Version and build info are displayed in the web interface or Janus GUI
Operation	FPGA Internal logic includes trigger handling, peak-sensing chain control (hold/mux/ADC), data formatting Fully controlled via Janus 5202 and FERS Library

Software

Readout Software

- Full control and acquisition via JANUS 5202 and FERS Library
- Supports all acquisition modes: Spectroscopy, Timing, Counting, Spectroscopy + Timing
- Real-time plots, statistics, threshold/gain tuning

Web Interface

- Accessible via Ethernet
- Board configuration and network setup
- Useful for quick diagnostics and connection testing

FERSlib Library SDK

- **FERS Library:** C/C++ SDK for custom integration
- Compatible with Windows® and Linux®
- Includes data structures for all event types (PHA, ToA/ToT, Counting)
- Open-source, LGPL v3 license

Technical Specifications (continued)

Mechanical

	A5202	DT5202
Form Factor	OEM module without enclosure Stackable via metal spacers	Desktop Enclosure: Aluminium housing with rubber end-frames Includes mounted A5250 adapter
Weight	132 g	503 g
Dimensions	73.0 W × 20.0 H × 164.5 L mm^3	103.0 W × 55.5 H × 187.5 L mm^3

Environmental

Environmental	Indoor use
Operating Temperature	0°C ÷ +40°C
Storage Temperature	-10°C ÷ +60°C
Operating Humidity	10% ÷ 90% RH non condensing
Storage Humidity	5% ÷ 90% RH non condensing
Pollution Degree	2
Overvoltage Category	II
EMC Environment	Commercial and light industrial
IP Degree	Enclosure (desktop models), not for wet location

Regulatory

Compliance	EMC: Safety:	CE 2014/30/EU Electromagnetic compatibility Directive CE 2014/35/EU Low Voltage Directive

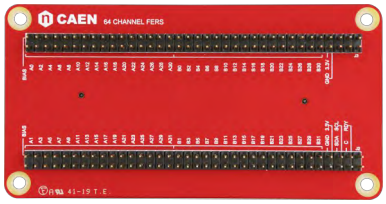
Power Requirements

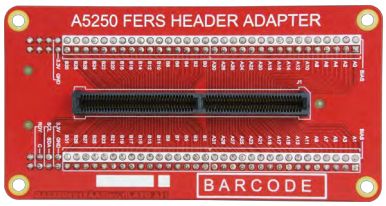
Input Voltage	+ 12 V DC	Accepted Voltage Range:	+7 V to +15 V
Typical consumption (full operation) Idle consumption (HV OFF, no SiPMs)	750 mA @ +12 V ≈ 9 W 685 mA @ +12 V ≈ 8.2 W		

	A5202	DT5202
Power Supply	requires external DC source	includes 12 V / 45 W AC-DC adapter and cable
Power connector	DC 691361300002 WURTH ELEKTRONIK	DC jack

Safety Notes

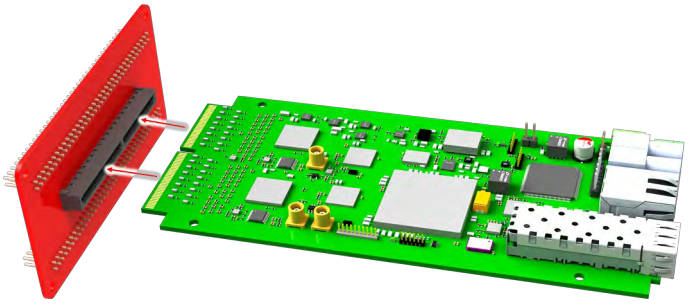
- Use only with proper shielding
- Do not operate in wet or explosive environments
- Handle A5202 as ESD-sensitive device

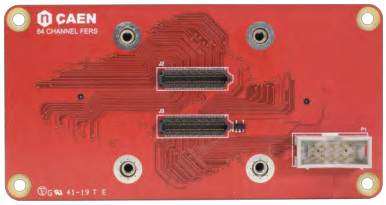




A5250 – 2.54 mm pin header adapter for A5202/DT5202

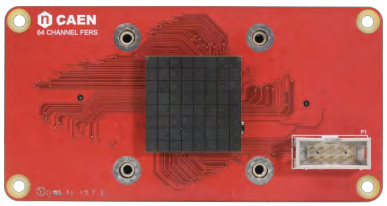
The A5250 adapter is compliant with A5202 and DT5202 boards. It converts the HSEC8-170 edge connector to a 2.54 mm pin header, exposing 32 bias/signal pairs per strip, plus ground and temperature sensor connectors. It comes pre-mounted on the DT5202 back panel.



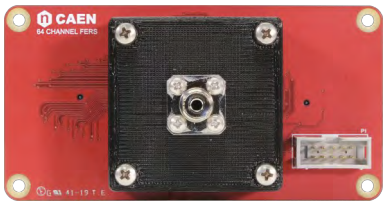


A5251– MPPC header adapter for 8x8 Hamamatsu S13361 SiPM matrix

The A5251 adapter is compliant with A5202/DT5202 boards. It mechanically adapts from the input edge card connector (type HSEC8-170) to a couple of Samtec SS4-40-3.0-L-D-K-TR connectors. The adapter is suited for biasing and reading out an 8×8 Hamamatsu S13361-3050AE-08 SiPM matrix. The A5251 is equipped with a TMP37 temperature sensor. A dark plastic box is also included in the delivered kit, which is ideal for shielding environmental light and pulsing the matrix via the fiber optic connector placed on top of it. A 5x2 pin (2.54 mm pitch) connector is included in the adapter and brings several grounds, the I2C lines (not yet supported) and the signals for an additional temperature sensor (different form the internal TMP37).

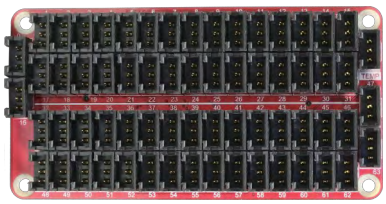


Front view with Hamamatsu SiPM matrix S13361-3050AE-08 mounted



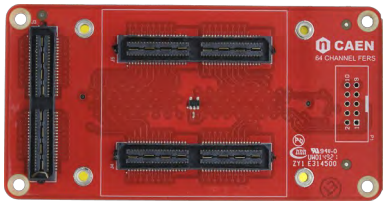
Front view with Dark box mounted

A5253 – 3-pin header adapter



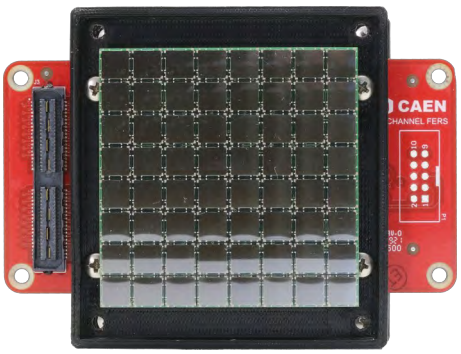
The A5253 header adapter is compliant with A5202/DT5202 FERS-5200 boards. It mechanically adapts from the input edge card connector (type HSEC8-170) to 65 3-pin connectors (AMPMODU type 3-102203-4). Each 3-pin connector mates to an AMPMODU type 102241-1 (as the one present in A5261 cables). Of the headers mounted, 64 allows reading out and biasing as many SiPMs, while 1 allows reading out an external temperature sensor. The A5253 header adapter was designed to allow the reading out of remote SiPMs, by having the channels and associated cables unbundled rather than grouped in a single flat cable.

A5254 – 8x8 OnSemi SiPM Array Adapter



The A5254 adapter is compliant with A5202/DT5202 boards. It mechanically adapts from the input edge card connector (type HSEC8-170) to a couple of Samtec QSE−040−01−F−D−A connectors. The adapter is suited for biasing and reading out 8x8 OnSemi (ex SensL) ARRAYJ-60035-64P-PCB or ARRAYC-60035-64P-PCB SiPMs matrices. Moreover, this adapter provides access to the individual fast output of the cells on a side Samtec QSE−040−01−F−D−A connector.

The A5254 is equipped with a TMP37 temperature sensor. A dark plastic box is also included in the delivered kit, which is ideal for shielding environmental light and pulsing the matrix via the fiber optic connector placed on top of it. The A5254 is also arranged for housing a 5x2 pin (2.54 mm pitch) connector, where could be connected several grounds, the I2C lines and the signals for an additional temperature sensor (different form the internal TMP37).



Front view with OnSemi ARRAYC-60035-64P-PCB SiPMs matrix mounted

A5202/DT5202 Cables

A5260 – Remotization cable for FERS-5200 boards

The A5260 flat cable has been designed to allow the remotization of the edge card connector of FERS-5200 boards. On one side, the cable features a Samtec HSEC8-170-01-S-DV-A connector mating directly to the edge card connector of FERS-5200 boards. On the other side, the cable features edge card connectors type HSEC8-170 (140 contacts with 0.8 mm pitch) mating directly to FERS-5200 header adapters . Thanks to this cable, detectors can be moved up to one meter (A5260B) away from the readout electronics without experiencing a significant signal degradation.

A5261 – SiPM remotization cable for A5253

The CAEN Model A5261 is a cable assembly designed to enable remote SiPM readout for A5202/DT5202 boards. Each A5261 cable is terminated on both ends with AMPMODU type 102241-1 connectors, which mate with AMPMODU type 3-102203-4 three-pin connectors installed on the A5253 FERS-5200 adapter. Each cable carries three lines (anode, cathode, and ground), allowing both readout and biasing of a single remote SiPM.

A5202 setup with A5253 adapter and A5261 cable connected to a SiPM-coupled Scintillating Tile.

Ordering Option

Description	Code
A5202 - 64 Channel Citiroc unit for FERS-5200	WA5202XAAAAA
DT5202 - Desktop 64 Channel Citiroc unit for FERS-5200	WDT5202XAAAA
Accessories	
A5250 - 2.54 mm pin header adapter for A5202/A5204	WA5250FHAXAA
A5251 - MPPC header adapter for A5202/DT5202	WA5251FMAXAA
A5253 - 3-pin header adapter for A5202/A5204	WA5253F3AXAA
A5253 Kit – A5253 adapter and 64 SiPM remotization CABLES	WKA5253X64AA
A5254 – SensL Array Adapter for A5202/DT5202	WA5254FSAXAA
A5260 - Remotization cable for FERS-5200 boards - 50 cm	WA5260XAAAAA
A5260B - Remotization cable for FERS-5200 boards - 100 cm	WA5260BXAAAA
A5261 – SiPM Remotization cable (0.7 m) for A5253	WA5261XAAAAA

A5202/DT5202 64 Channel Citiroc unit for FERS-5200

CAEN S.p.A.
Via Vetraia 11
55049 - Viareggio - Italy
Phone +39.0584.388.398
Fax +39.0584.388.959
info@caen.it - **www.caen.it**

CAEN GmbH
Brunnenweg 9
64331 Weiterstadt, Germany
Phone +49 (0)212.254.4077
Mobile +49 (0)151.16.548.484
info@caen-de.com - **www.caen-de.com**

CAEN Technologies, Inc.
1 Edgewater Street - Suite 101
Staten Island, NY 10305 - USA
Phone +1.718.981.0401
Fax +1.718.556.9185
info@caentechnologies.com
www.caentechnologies.com

CAENspa India Private Limited
B205, BLDG42, B Wing,
Azad Nagar Sangam CHS,
Mhada Layout, Azad Nagar, Andheri West
Mumbai, Maharashtra 400053, India
info@caen-india.in - **www.caen-india.in**

DT5202

A5202