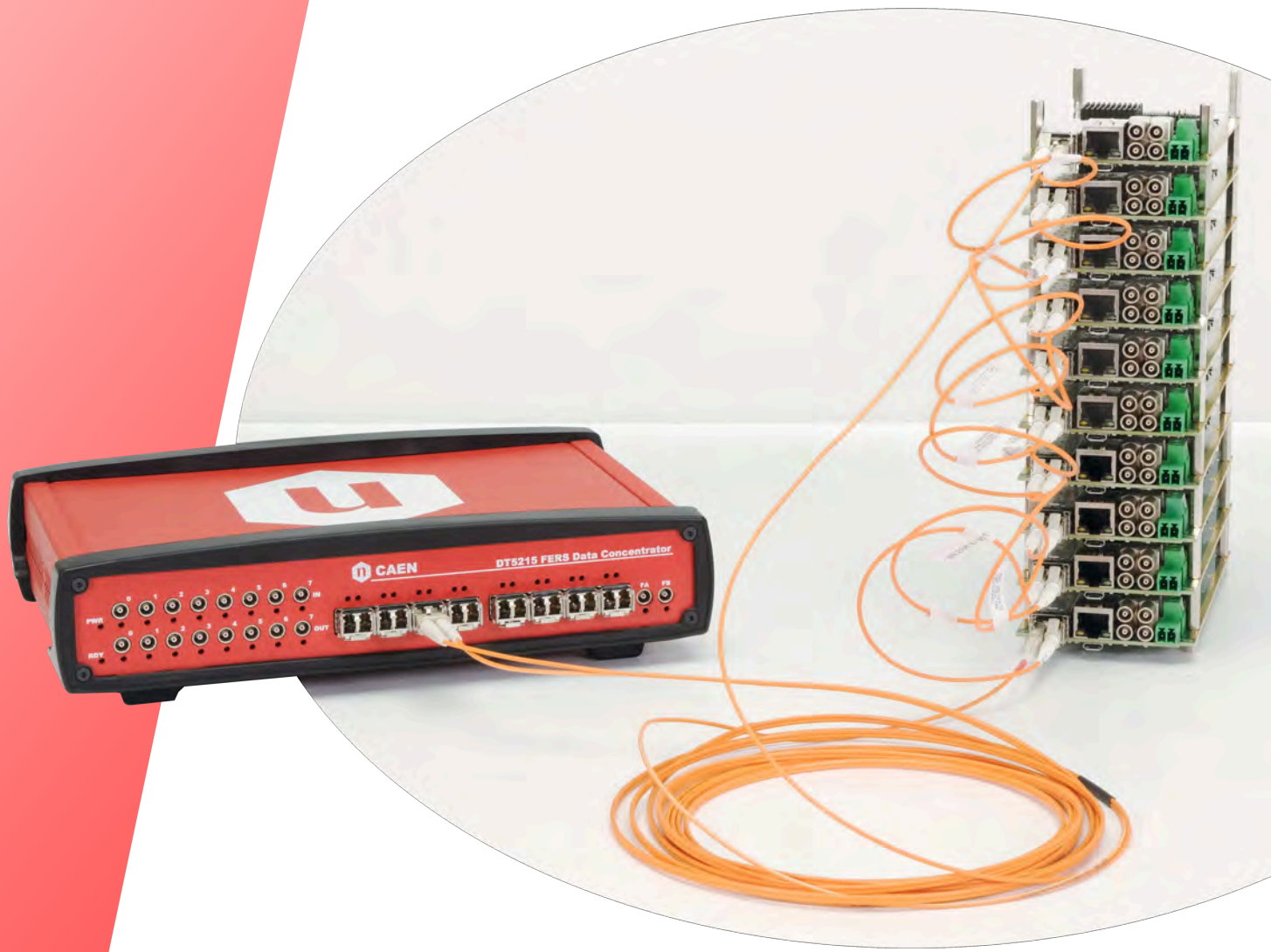
CAEN
Tools for Discovery

FERS 5200

Front-End Readout System

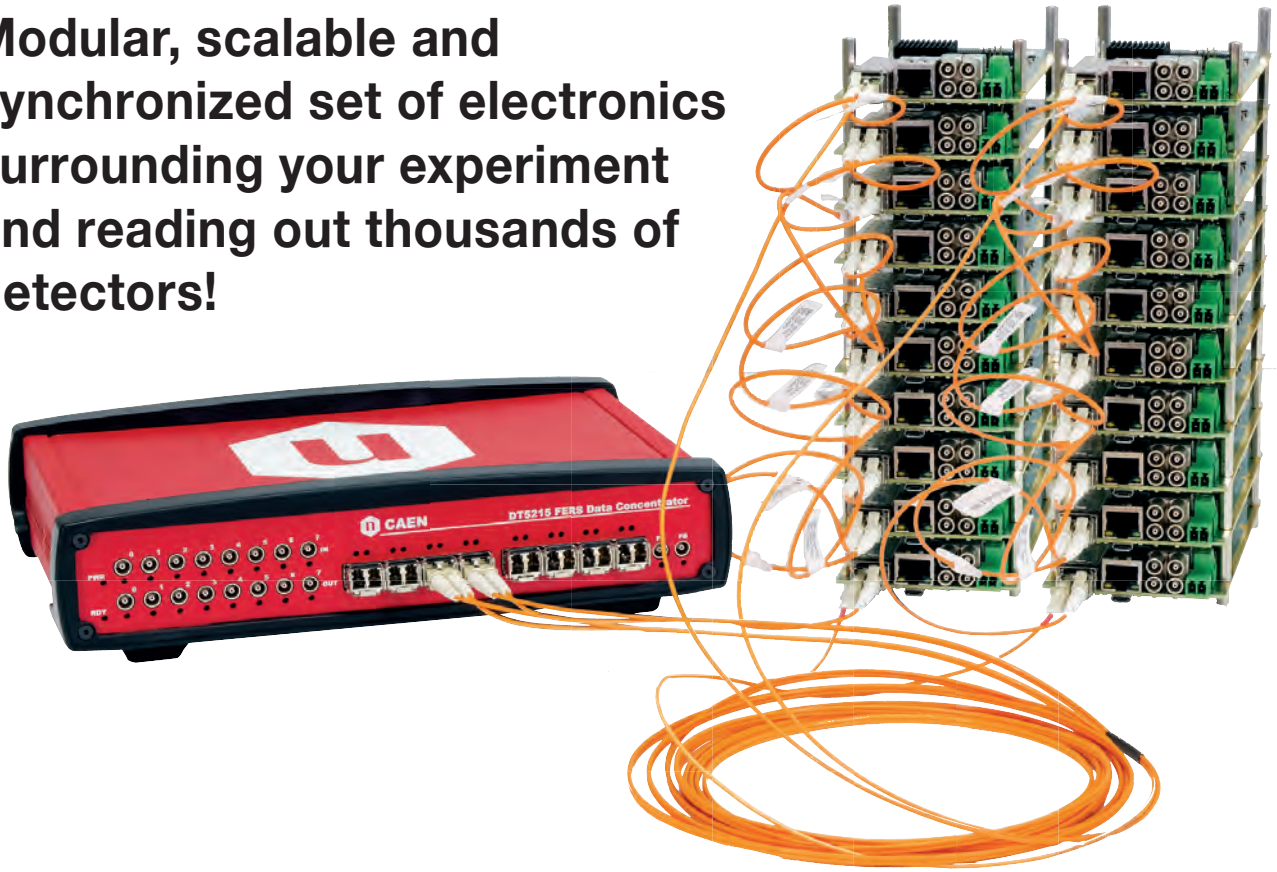


MULTI BOARD SYNC
USB 3.0
1 GbE
10 GbE
WEB INTERFACE
JANUS FERS CAEN
CAEN FERSlib

FERS-5200 FAMILY

MODULAR FRONT-END READOUT SYSTEM

Modular, scalable and synchronized set of electronics surrounding your experiment and reading out thousands of detectors!



- **Modular front-end readout system based on high-density ASICs (CITIROC, picoTDC, RADIOROC, PSIROC, etc.)**
- **High channel count (64/128 ch per board) with low power and low cost per channel**
- **Scalable architecture: from standalone boards to synchronized networks with thousands of channels**
- **Optical daisy-chain synchronization via DT5215/DT5216* concentrators**
- **Managed via Janus software (customized per board type)**
- **Unified C++ control API with FERSlib for acquisition and slow control**
- **Ideal for SiPMs, PMTs, silicon strips, GEMs, wire chambers, and more**

*** COMING SOON**

HIGH CHANNEL DENSITY POWERED BY ASIC FRONT-ENDS

At the core of each FERS board is a carefully selected ASIC, chosen by CAEN to match the characteristics of specific detector technologies. Leveraging commercial chips such as CITIROC, picoTDC, and RADIOROC, FERS boards provide compact front-end solutions with 64 or 128 acquisition channels per module—optimizing both cost-per-channel and power efficiency.

The board-level design is the result of CAEN's long-standing collaboration with Nuclear Instruments, where electronics are engineered specifically around the chosen ASIC to ensure optimal analog performance and full digital integration. Starting with the A5204, FERS boards adopt a common PCB layout that ensures long-term compatibility with future Weeroc ASICs, thanks to their pin-to-pin equivalence. This strategy streamlines development while maintaining support for next-generation features without redesigning the entire system—ensuring continuity, scalability, and reliability.

A SCALABLE AND MODULAR READOUT ARCHITECTURE

FERS is designed to seamlessly scale from compact lab setups to large-scale experiments with thousands of channels. Each board integrates analog front-end, digitization or time stamping, acquisition logic, and communication interface into a compact, self-contained module. To offer maximum flexibility, FERS boards are available in two hardware configurations: the naked version, optimized for integration into mechanical frames and dense detector planes, and the desktop version, ideal for standalone use during prototyping, testing, or small-scale experiments.

Single-board systems can be powered and controlled directly via Ethernet/USB, while multi-board installations rely on a robust synchronization and data routing infrastructure based on optical TDlink connections and the use of DT5215 or DT5216 concentrators. These units ensure precise distribution of clock and control signals across the acquisition chain.

Importantly, the DT5215 also allows synchronization of the FERS system with external instrumentation, including CAEN digitizer families and GPS-based timing sources, enabling full integration into hybrid DAQ environments where precise time alignment is critical.

This architectural flexibility allows users to reuse the same FERS electronics across different scales and use cases, with minimal reconfiguration. Whether you're reading out a few SiPMs on the bench or managing timing for a large calorimeter array, FERS ensures consistency, precision, and ease of deployment—making it an ideal solution for both R&D environments and production-grade detector systems.

UNIFIED SOFTWARE CONTROL: JANUS & FERSLIB

FERS boards are controlled via Janus, CAEN's acquisition software tailored to each board type. Janus provides a graphical interface for configuration, monitoring, run control, and data visualization. Every board has its own version of Janus, optimized for its specific acquisition modes and parameters—whether you're working with pulse-height analysis, counting, TDC or streaming data. For advanced integration, the FERSlib C++ API allows users to develop custom acquisition and control applications. FERSlib abstracts hardware complexity, providing uniform access to registers, data buffers, and synchronization logic across the entire FERS ecosystem. Together, Janus and FERSlib streamline both development and operation, making the system accessible for users at all levels.

CONNECTIVITY & CONTROL HIGHLIGHTS

	10/100 Mb Ethernet	RJ-45 port on every FERS unit. Provides TCP/IP control and data at up to ~2–3 MB/s, ideal for standalone tests, firmware updates and fast prototyping. IP address, DHCP and basic health metrics are set in the on-board Web Interface.
	TDlink Optical Link	Optical link running proprietay TDlink protocol over duplex fiber (3.125 Gb/s) that combines clock, slow-control and data. One DT5215 hub fans out 8 links, each daisy-chaining up to 16 boards, for 128 units/ >8 k channels with <20 ps jitter and <6.4 ns fixed skew.
	USB 2.0	Micro-USB (front-ends) or USB-C (DT5215). Sustains ~ 3 MB/s and supports firmware upgrades or quick lab setups; synchronization is limited to single-board use.
	Embedded Web Interface	A browser-based GUI is available on all FERS boards. For single units, it allows network configuration and real-time status monitoring. On the DT5215 concentrator, it also provides TDlink control, log file download, and one-click FPGA/CPU firmware upgrade—no additional software required.
	USB 3.0, 1 GbE, 10 GbE	DT5215 equipped with USB 3.0, 1 Gb Ethernet, and 10 Gb Ethernet interfaces for data acquisition. USB 3.0 and 10 GbE support data rates up to ~300 MB/s, while 1 GbE offers ~100 MB/s—ideal for a wide range of system configurations.

A5202/DT5202

CITIROC-BASED 64 CH SIPM READOUT & BIAS

Flexible readout for single SiPMs or arrays. Full support for 64-channel matrices.

The A5202 (naked board) and DT5202 (desktop version) are compact, high-density front-end modules designed for the direct readout of Silicon Photomultipliers (SiPMs) within the CAEN FERS-5200 platform. Each unit integrates two Citiroc-1A ASICs, providing a total of 64 channels with complete analog signal conditioning and peak detection. Each channel includes a preamplifier, a fast shaper followed by a discriminator, and a slow shaper connected to a peak-and-hold circuit. The peak amplitude is acquired sequentially from each Citiroc-1A via a 13-bit external ADC under FPGA control, enabling accurate energy (pulse height) measurements. The fast shaper output is used to implement self-triggering per channel, as well as for Time over Threshold measurements, event counting, and the generation of a bunch trigger to start energy acquisition.

The module features a built-in A7585D programmable high-voltage supply to bias the connected SiPMs individually, eliminating the need for external HV sources.

The A5202/DT5202 can operate in standalone mode via USB or Ethernet for configuration and basic data acquisition. In larger systems, it connects via the TDlink protocol over optical fiber, which handles data readout, slow control, and synchronization to a DT5215 concentrator board. This allows multiple FERS units to operate in a fully synchronized and scalable acquisition system based on a common reference clock.

The system is fully supported by the Janus 5202 open-source software, which provides intuitive GUI and console-based control for configuration and data acquisition. For advanced integration, CAEN also provides the FERSlib C++ library, enabling users to develop custom applications and DAQ systems. A wide selection of input adapters, remote cabling options, and mechanical accessories is available to ensure compatibility with various SiPM formats and experimental setups. The A5202/DT5202 is an ideal solution for scalable, low-power front-end readout in applications such as particle and nuclear physics, medical imaging, and radiation monitoring.

COMM. INTERFACES

10/100 MbE · USB 2.0 · TDLINK

SOFTWARE & LIBRARY

WEB INTERFACE · JANUS FERS CAEN · CAEN FERSlib

APPLICATIONS

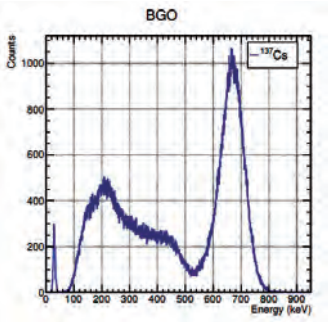
- Cosmic ray and particle detection
- Nuclear and gamma spectroscopy
- Calorimetry and high-energy physics
- Medical imaging and dosimetry

MORE INFO

A5202 DT5202

Amplitude Measurements with SiPM and ASIC (Citiroc 1A) Front-End Electronics.

Abstract - [...] In this paper, we describe a SiPM-based application with CAEN Front-End Readout System based on Citiroc 1A chip from Weeroc . Besides the use of this chip for well known single photon spectra and event counting, this paper exploits the possibility to acquire energy spectra directly from scintillators, paired with SiPM, through peak-and-hold readout. In particular, good energy resolutions have been achieved even with slow scintillators, like LYSO, CsI(Tl), and BGO, which have 40 ns, 1000 ns, and 300 ns of light decay time, respectively.[...] Several measurements have been performed using multiple radioactive γ sources and the resulting energy spectra demonstrate a resolution compatible with that found in literature [4] [5] [6] [7]. [...]



Calibrated energy spectra from 137Cs γ-radioactive source measured with BGO crystal coupled with single 6 × 6 mm2 SiPMs and acquired with the A5202 board.

See: Documentation Area - CAEN - Tools for Discovery/ AR9655 - Amplitude Measurements with SiPM and ASIC (Citiroc 1A) Front-End Electronics

A5203/DT5203

PICOTDC-BASED 64/128 CH HIGH-RESOLUTION TDC MODULE

The best achievable timing resolution in a compact form factor and optional dual-threshold discriminators.

The A5203 (and its desktop version DT5203) is a compact front-end module (~7 × 17 cm) within the CAEN FERS-5200 ecosystem, integrating the CERN picoTDC ASIC and providing 64 digital LVDS inputs (128 in the A5203B). Each channel timestamps rising and falling edges to reconstruct Time of Arrival (ToA), either as absolute time or as deltaT relative to a Tref pulse, and records Time over Threshold (ToT) for amplitude estimation and walk correction. At firmware level, a ToT filter rejects spurious low or saturated events, reducing noise and data throughput—especially valuable in high-rate environments.

Acquisition modes supported include Common Start, Common Stop, Trigger Matching, and continuous Streaming, allowing flexible operation in triggered or free-running scenarios

The TDC offers 3.125 ps LSB resolution with typical jitter around 7 ps RMS for fixed-amplitude signals, and about 20 ps RMS over a 50 dB dynamic range after walk correction via ToT .

Multiple A5203/DT5203 units can be synchronized using optical TDlink via the DT5215 concentrator (and the upcoming DT5216), enabling scalable multi-board systems with global timing alignment.

Full control and data acquisition is handled through Janus 5203, CAEN's open-source software suite for Windows and Linux, featuring both GUI and console modes for configuration, monitoring, run control, histogramming, and data export. For advanced users, the FERSlib C++ API enables development of fully customized acquisition and analysis software.

COMM. INTERFACES

10/100 MbE · USB 2.0 · TDLINK

SOFTWARE & LIBRARY

WEB INTERFACE · JANUS FERS CAEN · CAEN FERSlib

APPLICATIONS

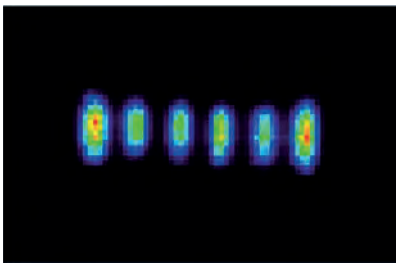
- Particle tracking
- Time-of-flight (ToF) systems
- Fast detector R&D
- Synchronized multi-channel acquisition systems

MORE INFO

A5203 DT5203

Picosecond timing measurements with the FERS-5200.

Abstract - [...] The A5203 FERS houses the recently released CERN picoTDC ASIC and provides high-resolution time measurements of Time of Arrival (ToA) and Time over Threshold (ToT). In this work we will analyze the performances of the A5203 unit: 3.125 ps LSB, ToA measurements down to ~7 ps RMS for signals of fixed amplitude over a single board, and ~20 ps RMS for input signals of variable amplitude (over a 50 dB dynamic range). The walk effect introduced by different amplitudes is corrected using the ToT. Besides walk correction, the ToT is used for signal amplitude reconstruction and background reduction. The A5203 has been used in various applications, both experimental and industrial. At the end of this work, its application in the ProVision PET scanner will be presented. Compactness, scalability and applicability to thousands of channels is required for the readout electronics.



Coronal view of a stack of 6 Na22 sources obtained during tests of the Picotech PET scanner.

See: https://pos.sissa.it/476/1203/

A5204/DT5204

RADIOROC-BASED 64 CH SIPM READOUT WITH HIGH-RESOLUTION TDC

Ideal for large SiPM arrays. Fully supports 64-channel matrices with bias and timing readout.

The A5204 (naked board) and DT5204 (desktop version) are advanced 64-channel front-end modules developed for high-performance readout of Silicon Photomultipliers (SiPMs) within the CAEN FERS-5200 ecosystem. At their core is the RADIOROC ASIC, specifically designed for fast and precise signal acquisition from SiPMs. Each channel includes a programmable preamplifier, dual-gain shaping chain, discriminator, and peak-and-hold logic, enabling both energy and time measurements. Timing is further enhanced by the integration of a 64-channel picoTDC ASIC from CERN, delivering sub-nanosecond resolution with 3.125 ps LSB.

The A5204 provides an internal programmable high-voltage generator (up to +85 V) and per-channel 8-bit DACs for fine SiPM bias adjustment, gain equalization, and temperature compensation. The fast discriminator line supports self-triggering down to 1/3 photoelectron, as well as majority and coincidence logic for trigger formation.

Data acquisition modes include spectroscopy, counting, and timing (common start/stop and streaming). Communication interfaces include USB, Ethernet, and optical TDlink, allowing the module to operate either standalone or as part of a synchronized multi-board system via the DT5215 or DT5216* concentrator.

Full control and data acquisition are provided by Janus 5204 open-source software, available in both GUI and console modes. For user-customized applications, the system is also supported by the FERSlib C++ API, enabling the development of tailored acquisition and control software.

* Coming soon

COMM. INTERFACES

10/100 M6E · USB 2.0 · TDLINK

SOFTWARE & LIBRARY

WEB INTERFACE · JANUS FERS CAEN · CAEN FERSlib

APPLICATIONS

- Precision timing and fast photon counting
- Dual-gain spectroscopy with SiPM detectors
- Scalable readout for large SiPM arrays
- Medical imaging and trigger-based acquisition

HIGHLIGHTS

- 64-channel front-end with RADIOROC + picoTDC architecture
- Dual-gain energy readout with programmable shaping for PSD
- Sub-nanosecond timing resolution (55 ps FWHM, 3.125 ps LSB)
- Internal HV generator up to +85 V with per-channel DAC trimming
- Fast self-triggering down to 1/3 photoelectron
- Multiple acquisition modes: spectroscopy, timing, counting
- Full support for trigger logic, coincidences, and majority logic
- Standalone or scalable setup with TDlink optical daisy chain
- Real-time control and visualization with Janus 5204 software (GUI/Console)
- Compact size, USB/Ethernet/TDlink interfaces, low power consumption
- For user-customized applications, the system is also supported by the FERSlib C++ API, enabling the development of tailored acquisition and control software.

MORE INFO

A5204 DT5204

COMING SOON

A5205/DT5205

PSIROC-BASED 64 CH CHARGE & TDC READOUT MODULE

Ideal for precision readout of silicon strips, GEMs, and PIN diodes in high-resolution tracking and low-charge detection systems.

The A5205 (board version) and DT5205 (desktop version) are 64-channel front-end modules of the CAEN FERS-5200 family, designed for the high-resolution readout of PIN diodes, silicon strip detectors, and GEMs. At their core is the Weeroc Psiroc ASIC, coupled with the CERN picoTDC chip, enabling precise charge and timing measurements for capacitive detectors operating at very low signal levels.

Each channel features a charge-sensitive preamplifier with programmable gain from 125 mV/pC up to 4 V/pC, followed by a shaping stage and peak detector. The input stage accepts both positive and negative polarity signals. Psiroc enables triggering down to 0.5 fC on sub-20 pF detectors, and supports dual-gain charge measurement. For input charges above a few pC, a channel-wise Time over Threshold (ToT) output is also available, providing high-rate, low-dead-time pulse amplitude estimation without the need for multiplexed ADC conversion.

Data acquisition can operate in global or per-channel mode, with individual triggers routed to the integrated picoTDC, offering sub-nanosecond timing resolution (3.125 ps LSB). Timestamp and PHA acquisition are fully supported.

The A5205/DT5205 includes synchronization and communication interfaces (USB, Ethernet, and TDlink) and is fully managed by the Janus 5205 open-source software, available for Windows® and Linux®. A complete set of dedicated accessories—cables, adapters, and remote connectors—is available to support a wide range of detector formats and experimental configurations.

COMM. INTERFACES

10/100 MbE · USB 2.0 · TDLINK

SOFTWARE & LIBRARY

WEB INTERFACE · JANUS FERS CAEN · CAEN FERSlib

APPLICATIONS

- Silicon strip and pixel detectors
- Micro-pattern gaseous detectors (GEM, Micromegas)
- PIN diode arrays for beam and dose monitoring
- High-precision tracking and timing in nuclear physics

MORE INFO

A5205 DT5205

HIGHLIGHTS

- 64-channel readout with Weeroc Psiroc ASIC
- Triggering down to 0.5 fC for sub-20 pF detectors
- Dual-gain charge measurement and ToT output
- Sub-ns timing resolution with picoTDC (3.125 ps LSB)
- Positive/negative input polarity supported
- Adjustable gain up to 4 V/pC, shaping from 20 ns to 3 µs
- Low dead time acquisition without multiplexed ADC
- Fully supported by Janus 5205 software suite

DT5215

CONCENTRATOR BOARD FOR FERS-5200

The DT5215 Concentrator Board manages synchronization and data aggregation from multiple FERS units within the CAEN acquisition ecosystem. It provides 8 optical links running the CAEN TDlink proprietary protocol, each capable of daisy-chaining up to 16 FERS boards, for a total of up to 128 modules per concentrator—corresponding to several thousand acquisition channels, depending on the configuration.

At the heart of the concentrator is an embedded Linux-based single board computer, which supervises the FERS network and collects data fragments from each unit. These fragments are transmitted directly to the host computer through high-speed communication interfaces, including USB 3.0, 1 Gb Ethernet, and 10 Gb Ethernet, supporting data rates up to 300 MB/s.

Multiple DT5215 boards can be synchronized to build scalable, distributed acquisition systems with unified timing. Synchronization can also be extended to CAEN digitizer families, enabling time-correlated acquisition across heterogeneous systems. In such cases, FERS modules and digitizers typically run under separate acquisition software, unless the user develops a custom unified solution using the available software libraries.

The DT5215 is fully supported by CAEN's Janus software for system configuration, monitoring, and control, and by the FERSlib C++ API, which allows users to develop custom acquisition and data handling applications.

COMM. INTERFACES

USB 3.0 | 1 GbE | 10 GbE

FEATURES

MULTI BOARD SYNC

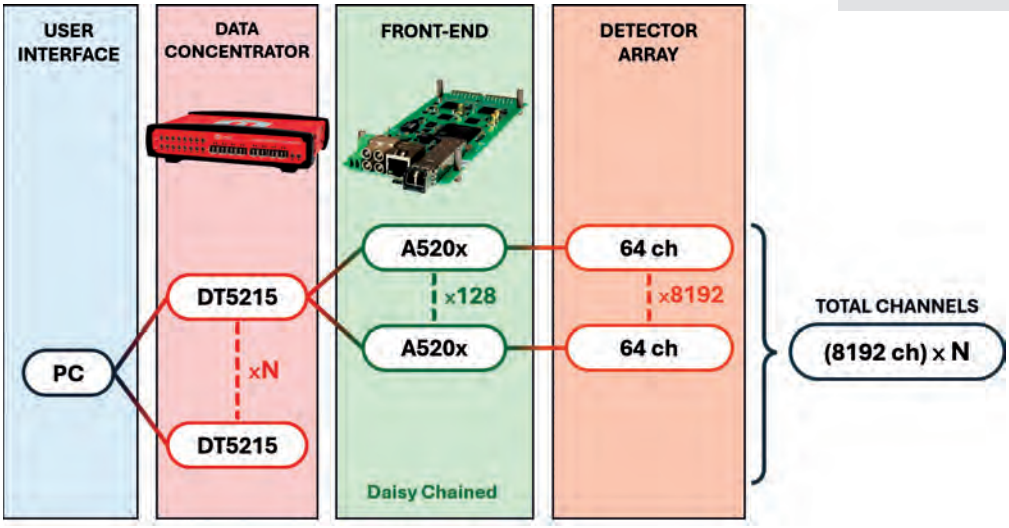
SOFTWARE & LIBRARY

WEB INTERFACE | JANUS FERS CAEN | CAEN FERSlib

HIGHLIGHTS

- Concentrator board for multiboard management in FERS-5200, the CAEN platform for the readout of large arrays of detectors (SiPM, MA-PMTs, Gas Tubes, Si detectors, ...).
- Scalability: from a single standalone FERS unit for prototyping to many thousands of channels, with simple tree network structure.
- Modularity: multiple FERS units can be distributed on large detector volume and managed by a single Concentrator board.
- 8x TDlink for event data building, processing and formatting.
- Easy-synch: one single optical link (TDlink) for data readout, slow control and boards synchronization.
- Available also in single TDlink version (DT5216): supports up to 8 FERS units in daisy chain.

MORE INFO



NOTE: using the A5203B the channel numbers are doubled

COMING SOON

DT5216

COMPACT DATA CONCENTRATOR FOR FERS-5200

Ideal for mid-scale detector setups. Manages up to 8 FERS units with synchronized readout and control.

The DT5216 is a compact Data Concentrator developed for the CAEN FERS-5200 platform, designed to manage small-to-medium scale readout systems based on front-end units such as the A5202, A5203, A5204 and A5205. It features a single TDlink optical port and supports up to 8 FERS units in daisy chain, allowing the acquisition of up to 512 channels when used with 64-channel front-end boards. TDlink handles data transfer, slow control, and timing synchronization over a single optical connection, significantly simplifying system architecture.

Communication with the host PC is provided via high-speed USB 3.0 (Type-C), ensuring fast data throughput and streamlined setup. The DT5216 is ideal for prototyping, beamline tests, and mid-scale experiments requiring synchronized, multi-board operation without the complexity of a full-scale system. Its compact size and low channel count make it a cost-effective alternative to the DT5215 concentrator, while maintaining compatibility with the entire FERS-5200 ecosystem.

Firmware is upgradable via USB, and synchronization performance is optimized through software compensation of optical delays, achieving typical clock jitter of 20 ps and fixed skew under 6.4 ns. The DT5216 offers a scalable path to future system expansion, providing the same user interface and DAQ software tools as larger FERS deployments.

COMM. INTERFACES

USB 3.0

SOFTWARE & LIBRARY

JANUS FERS CAEN

CAEN FERSlib

HIGHLIGHTS

- Compact concentrator for up to 8 FERS units via TDlink
- USB 3.0 host interface with up to 300 MB/s readout rate
- Full synchronization: data, control, and timing over one link
- Ideal for prototyping and distributed DAQ setups
- Firmware upgradeable via USB; plug-and-play operation
- Seamless integration with Janus software and DT5215-based networks

MORE INFO

NOTE: using the A5203B the channel numbers are doubled

JANUS

FERS-5200 DAQ SOFTWARE

A single DAQ software to control the FERS-5200 board family. Available in Console and GUI Mode, it allows the user to customize the DAQ, and offers an easy way to approach multi-boards and high-channel density FERS-5200 systems.

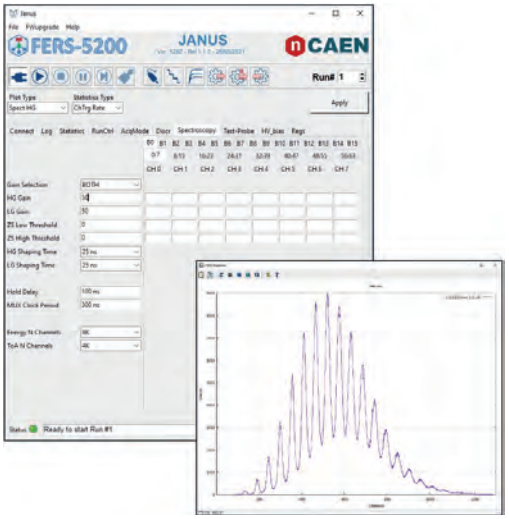
Janus is an open source software for the control and readout of FERS-5200 boards. Available in two versions (Ver. 5202, Ver. 5203), it can be used as a platform for the development of custom DAQ, tailored to the specific application. Indeed, the user can change the data treatment, the acquired statistics and the output file format.

Janus can manage up to 16 FERS units connected via Ethernet or USB directly as well as the readout of the DT5215 Concentrator Board, so that a single user interface is available for the whole system.

Janus is composed of two parts, one written in C, which is the real heart of the application, one written in Python which manages the user interface. The plots are executed through Gnuplot. All the configuration parameters are written in a textual configuration file.

It is possible to launch and use Janus in 2 different modes:

- **Console Mode**. In this case, the Python part of the software is not used. The user can edit the configuration file with any text editor and save the proper values for the desired parameters. Then, the user can launch a purely textual console window. The application writes a series of messages (which are also saved in a log file) and, during the run, prints statistics on the screen. The only graphical part is the plot, which is managed by Gnuplot.
- **GUI Mode**. In this case, the user only have to run the Python program which calls the C program and connects to it via a socket to send commands and receive messages which are then displayed in the Python GUI.



HIGHLIGHTS

- Model-dependent GUI for a quick and easy start
- Open-Source for user customization
- Management of the acquisition parameters of all connected boards
- Multi parametric Jobs and Runs with time or counts preset
- Data saving of lists in .bin, .txt format
- Statistics and Plots visualization

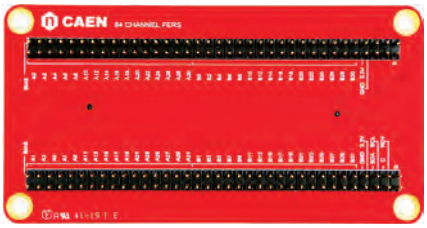
MORE INFO

MORE INFO

ACCESSORIES
FOR FERS-5200

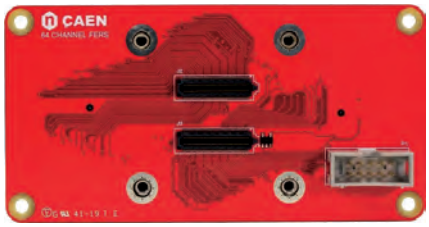
A5250

Converts 2.54 mm pitch pin headers to FERS-5200 input format, enabling direct connection of SiPMs or similar detectors to CAEN A5202 and A5204 front-end readout boards.



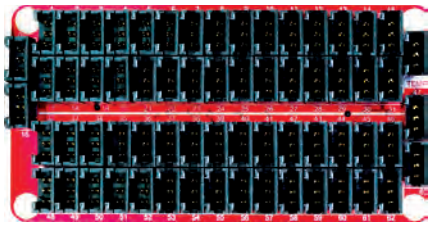
A5251

Interfaces Hamamatsu S13361-3050AE-08 SiPM matrices with A5202 and A5204 boards, providing direct signal routing to FERS-5200 inputs via Samtec-compatible high-density connectors.



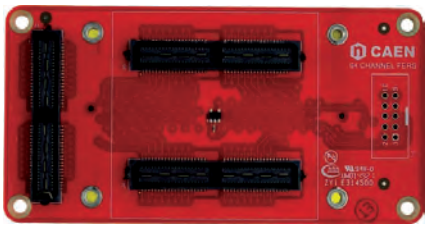
A5253

Ideal for connecting individual SiPMs to A5202 and A5204 boards via 3-pin connectors; compatible with A5261 cable for low-noise, remote signal transmission to FERS-5200 inputs.



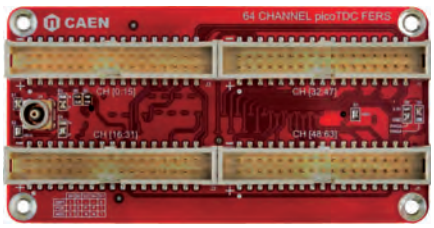
A5254

Connects OnSemi SiPM matrices (ARRAYJ/ARRAYC-60035-64P-PCB) to A5202 and A5204 boards using high-density Samtec connectors, ensuring reliable signal transfer to FERS-5200 inputs.



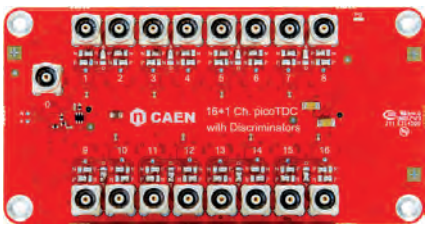
A5255

Provides direct connection of 64 LVDS differential inputs to A5203 via 2.54 mm pitch quad-row header, allowing signal routing from custom detectors to the FERS-5200 TDC system.



A5256

Provides 16+1 single-threshold or 8+1 dual-threshold edge discriminators for single-ended signals, delivering LVDS outputs to A5203 for time digitization in FERS-5200 systems.



A5260

Flat cable with 2.54 mm pitch connectors, used to place FERS boards away from front-end adapters, reducing mechanical constraints near the detector.

A5261

Shielded cable with 3-pin connectors designed to route single-ended signals to A5202/A5204 inputs via A5253 adapter, ensuring low-noise remote connection.

A5270

Fan unit for FERS boards, used when ventilation is limited or when required by system specifications to ensure proper cooling of non-boxed modules.

FERS 5200

Front-End Readout System

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