

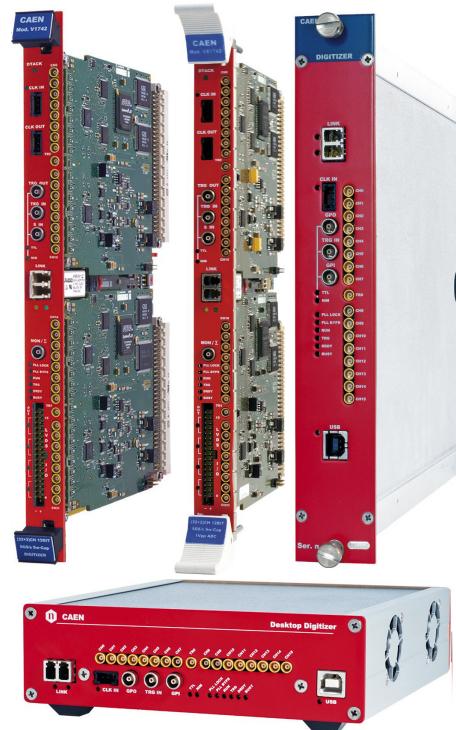


Rev. 4 - September 5<sup>th</sup>, 2025

# 742 Registers

16+1 Channel 12 bit 5 GS/s  
Switched Capacitor Digitizer

n



## Purpose of the Document



The User Manual contains the full description of the Waveform Recording firmware registers for the 742 digitizer family. The description is compliant with the firmware revision **4.30\_1.08**.

For future release compatibility, check in the firmware history file.

## Change Document Record

Date	Revision	Changes
January 26 <sup>th</sup> , 2017	00	Initial Release
February 05 <sup>th</sup> , 2020	01	Register 0x8000: updated bit[14] and bit[16]. Register 0x8100: updated bit[3], bit[11] and bit[12]. Register 0x8110: updated bit[29]. Register 0x811C: updated bit[7:6]. Register 0x8178: updated bit[3:0]. Register 0x1nA0: updated bit[7:0]. Register 0xEF04: updated bit[1] and bit[3]. Register 0xEF28: updated register description. Added register 0x81C4.
May 23 <sup>rd</sup> , 2022	02	Updated text formatting and copyrights. Register 0x1n14, 0x8014: updated register description and address (now 0x1n14, 0x8114). Register 0x1nA8,0x80A8: updated register description and bit[7:0]. Register 0x8000: updated bit[6], bit[15] and bit[17]. Register 0x8100: updated bit[3], bit[8], bit[9], bit[11] and bit[12]. Register 0x8170: updated register description.
January 31 <sup>st</sup> , 2023	03	Register 0x8000: updated bit[20] (extended trigger timestamp flag).
Sep. 5 <sup>th</sup> , 2025	04	Updated registers <b>1.15</b> , <b>1.22</b> , <b>1.23</b> . Enumerated document sections.

## Symbols, Abbreviated Terms, and Notations

ADC	Analog-to-Digital Converter
AMC	ADC & Memory Controller
DAQ	Data Acquisition
DAC	Digital-to-Analog Converter
DC	Direct Current
DPP	Digital Pulse Processing
LVDS	Low-Voltage Differential Signal
ROC	ReadOut Controller
USB	Universal Serial Bus

## Manufacturer Contacts



### CAEN S.p.A.

Via Vетраia, 11 55049 Viareggio (LU) - ITALY  
Tel. +39.0584.388.398 Fax +39.0584.388.959  
[www.caen.it](http://www.caen.it) | [info@caen.it](mailto:info@caen.it)  
©CAEN SpA – 2025

## Limitation of Responsibility

If the warnings contained in this manual are not followed, CAEN will not be responsible for damage caused by improper use of the device. The manufacturer declines all responsibility for damage resulting from failure to comply with the instructions for use of the product. The equipment must be used as described in the user manual, with particular regard to the intended use, using only accessories as specified by the manufacturer. No modification or repair can be performed.

## Disclaimer

No part of this manual may be reproduced in any form or by any means, electronic, mechanical, recording, or otherwise, without the prior written permission of CAEN SpA.

The information contained herein has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies. CAEN SpA reserves the right to modify its products specifications without giving any notice; for up to date information please visit [www.caen.it](http://www.caen.it).

## Made in Italy

We remark that all our boards have been designed and assembled in Italy. In a challenging environment where a competitive edge is often obtained at the cost of lower wages and declining working conditions, we proudly acknowledge that all those who participated in the production and distribution process of our devices were reasonably paid and worked in a safe environment (while this is true for the boards marked "MADE IN ITALY", we cannot guarantee for third-party manufacturers).



# Index

<b>Purpose of the Document</b> . . . . .	<b>2</b>
<b>Change document record</b> . . . . .	<b>2</b>
<b>Symbols, abbreviated terms and notation</b> . . . . .	<b>2</b>
<b>Manufacturer Contacts</b> . . . . .	<b>3</b>
<b>Limitation of Responsibility</b> . . . . .	<b>3</b>
<b>Disclaimer</b> . . . . .	<b>3</b>
<b>Made in Italy</b> . . . . .	<b>3</b>
<b>1 Registers and Data Format</b> . . . . .	<b>6</b>
1.1 Reset and Clear . . . . .	6
1.2 Register Address Map . . . . .	7
1.3 Event Readout Buffer . . . . .	10
1.4 Post Trigger . . . . .	11
1.5 Dummy32 . . . . .	12
1.6 Group n Channel Threshold . . . . .	13
1.7 Group n Status . . . . .	14
1.8 AMC Firmware Revision . . . . .	15
1.9 Group n Channel DC Offset . . . . .	16
1.10 DRS4 Chip Temperature . . . . .	17
1.11 Group n Channel Selection . . . . .	18
1.12 Group n Channel Trigger Mask . . . . .	19
1.13 Group n TR Trigger Threshold . . . . .	20
1.14 Group n TR DC Offset . . . . .	21
1.15 Board Configuration . . . . .	22
1.16 Custom Size . . . . .	24
1.17 Test Mode Initial Value . . . . .	25
1.18 DRS4 Sampling Frequency . . . . .	26
1.19 Acquisition Control . . . . .	27
1.20 Acquisition Status . . . . .	29
1.21 Software Trigger . . . . .	30
1.22 Global Trigger Mask . . . . .	31
1.23 Front Panel TRG-OUT (GPO) Enable Mask . . . . .	32
1.24 LVDS I/O Data . . . . .	33
1.25 Front Panel I/O Control . . . . .	34
1.26 Group Enable Mask . . . . .	36
1.27 ROC FPGA Firmware Revision . . . . .	37
1.28 Software Clock Sync . . . . .	38
1.29 Board Info . . . . .	39
1.30 Event Size . . . . .	40
1.31 Fan Speed Control . . . . .	41
1.32 Run/Start/Stop Delay . . . . .	42
1.33 Board Failure Status . . . . .	43
1.34 Front Panel LVDS I/O New Features . . . . .	44
1.35 Extended Veto Delay . . . . .	45
1.36 Readout Control . . . . .	46
1.37 Readout Status . . . . .	47
1.38 Board ID . . . . .	48

1.39 MCST Base Address and Control . . . . .	49
1.40 Relocation Address . . . . .	50
1.41 Interrupt Status/ID . . . . .	51
1.42 Interrupt Event Number . . . . .	52
1.43 Max Number of Events per BLT . . . . .	53
1.44 Scratch . . . . .	54
1.45 Software Reset . . . . .	55
1.46 Software Clear . . . . .	56
1.47 Configuration Reload . . . . .	57
1.48 Configuration ROM Checksum . . . . .	58
1.49 Configuration ROM Checksum Length BYTE 2 . . . . .	59
1.50 Configuration ROM Checksum Length BYTE 1 . . . . .	60
1.51 Configuration ROM Checksum Length BYTE 0 . . . . .	61
1.52 Configuration ROM Constant BYTE 2 . . . . .	62
1.53 Configuration ROM Constant BYTE 1 . . . . .	63
1.54 Configuration ROM Constant BYTE 0 . . . . .	64
1.55 Configuration ROM C Code . . . . .	65
1.56 Configuration ROM R Code . . . . .	66
1.57 Configuration ROM IEEE OUI BYTE 2 . . . . .	67
1.58 Configuration ROM IEEE OUI BYTE 1 . . . . .	68
1.59 Configuration ROM IEEE OUI BYTE 0 . . . . .	69
1.60 Configuration ROM Board Version . . . . .	70
1.61 Configuration ROM Board Form Factor . . . . .	71
1.62 Configuration ROM Board ID BYTE 1 . . . . .	72
1.63 Configuration ROM Board ID BYTE 0 . . . . .	73
1.64 Configuration ROM PCB Revision BYTE 3 . . . . .	74
1.65 Configuration ROM PCB Revision BYTE 2 . . . . .	75
1.66 Configuration ROM PCB Revision BYTE 1 . . . . .	76
1.67 Configuration ROM PCB Revision BYTE 0 . . . . .	77
1.68 Configuration ROM FLASH Type . . . . .	78
1.69 Configuration ROM Board Serial Number BYTE 1 . . . . .	79
1.70 Configuration ROM Board Serial Number BYTE 0 . . . . .	80
1.71 Configuration ROM VCXO Type . . . . .	81
<b>2 Technical Support . . . . .</b>	<b>82</b>

# 1 Registers and Data Format

All registers described in the User Manual are 32-bit wide. In case of VME access, **A24** and **A32** addressing mode can be used.

## 1.1 Reset and Clear

The module's registers can be set back to their default values on software reset command by writing in the Software Reset register or by system reset from backplane, in case of VME boards. In particular, the registers or buffers listed below

- Event Readout Buffer
- Buffer Occupancy
- Event Stored
- Event Size

are also be set back to their default values (registers) or emptied (buffers) by a clear issued:

- automatically by the firmware at the start of each run;
- on software command by writing in the Software Clear register;
- by hardware (VME boards only), through the LVDS interface properly configured (see the section "Front Panel LVDS I/Os" of the digitizer User Manual).

## 1.2 Register Address Map

The table below reports the complete list of registers that can be accessed by the user. The register names in the first column can be clicked to be redirected to the relevant register description. The register address is reported on the second column as a hex value. The third column indicates the allowed register access mode, where:

- R **Read only.** The register can be accessed in read only mode.
- W **Write only.** The register can be accessed in write only mode.
- R/W **Read and write.** The register can be accessed both in read and write mode.

According to the attribute reported in the fourth column, the following choices are available:

- G **Group register.** In case of 740 and 742 digitizer families, some registers manage **groups** of channels. Group registers have M instances, where M is the total number of groups. Write access can be performed in single group mode (one group at a time) or broadcast (simultaneous write access to all groups). Read command must be in single group mode. Single group access can be performed at address 0x1nXY, where n identifies the n<sup>th</sup> group, while broadcast write can be performed at the address 0x80XY. For example:
  - access to address 0x1320 to read/write register 0x1n20 for group 3 of the board. In case of 740 and 742 board, group 3 corresponds to channels from 24 to 31 (8 channels per group). The same value is applied to all channels in the same group.
  - to write the same value for all groups in the board, access to 0x8020 (broadcast write). To read the corresponding value, access to the individual address 0x1n20.
- C **Common register.** Register with this attribute has a single instance, therefore read and write access can be performed at address 0x80XY only.

Register Name	Address	Mode	Attribute
Event Readout Buffer	0x0000 - 0x0FFC	R	C
Post Trigger	0x1n14, 0x8114	R/W	G
Dummy32	0x1n24, 0x8024	R/W	G
Group n Channel Threshold	0x1n80, 0x8080	R/W	G
Group n Status	0x1n88	R	G
AMC Firmware Revision	0x1n8C	R	G
Group n Channel DC Offset	0x1n98, 0x8098	R/W	G
DRS4 Chip Temperature	0x1nA0	R	G
Group n Channel Selection	0x1nA4	R/W	G
Group n Channel Trigger Mask	0x1nA8, 0x80A8	R/W	G
Group n TR Trigger Threshold	0x1nD4, 0x80D4	R/W	G
Group n TR DC Offset	0x1nDC, 0x80DC	R/W	G
Board Configuration	0x8000, 0x8004 (BitSet), 0x8008 (BitClear)	R/W	C
Custom Size	0x8020	R/W	C
Test Mode Initial Value	0x807C	R/W	C
DRS4 Sampling Frequency	0x80D8	R/W	C
Acquisition Control	0x8100	R/W	C
Acquisition Status	0x8104	R	C
Software Trigger	0x8108	W	C
Global Trigger Mask	0x810C	R/W	C
Front Panel TRG-OUT (GPO) Enable Mask	0x8110	R/W	C
LVDS I/O Data	0x8118	R/W	C
Front Panel I/O Control	0x811C	R/W	C
Group Enable Mask	0x8120	R/W	C
ROC FPGA Firmware Revision	0x8124	R	C
Software Clock Sync	0x813C	W	C
Board Info	0x8140	R	C
Event Size	0x814C	R	C
Fan Speed Control	0x8168	R/W	C
Run/Start/Stop Delay	0x8170	R/W	C
Board Failure Status	0x8178	R	C
Front Panel LVDS I/O New Features	0x81A0	R/W	C
Extended Veto Delay	0x81C4	R/W	C
Readout Control	0xEF00	R/W	C
Readout Status	0xEF04	R	C
Board ID	0xEF08	R/W	C
MCST Base Address and Control	0xEF0C	R/W	C
Relocation Address	0xEF10	R/W	C
Interrupt Status/ID	0xEF14	R/W	C
Interrupt Event Number	0xEF18	R/W	C
Max Number of Events per BLT	0xEF1C	R/W	C
Scratch	0xEF20	R/W	C
Software Reset	0xEF24	W	C
Software Clear	0xEF28	W	C
Configuration Reload	0xEF34	W	C
Configuration ROM Checksum	0xF000	R	C
Configuration ROM Checksum Length BYTE 2	0xF004	R	C
Configuration ROM Checksum Length BYTE 1	0xF008	R	C
Configuration ROM Checksum Length BYTE 0	0xF00C	R	C
Configuration ROM Constant BYTE 2	0xF010	R	C
Configuration ROM Constant BYTE 1	0xF014	R	C
Configuration ROM Constant BYTE 0	0xF018	R	C
Configuration ROM C Code	0xF01C	R	C
Configuration ROM R Code	0xF020	R	C
Configuration ROM IEEE OUI BYTE 2	0xF024	R	C

<b>Configuration ROM IEEE OUI BYTE 1</b>	0xF028	R	C
<b>Configuration ROM IEEE OUI BYTE 0</b>	0xF02C	R	C
<b>Configuration ROM Board Version</b>	0xF030	R	C
<b>Configuration ROM Board Form Factor</b>	0xF034	R	C
<b>Configuration ROM Board ID BYTE 1</b>	0xF038	R	C
<b>Configuration ROM Board ID BYTE 0</b>	0xF03C	R	C
<b>Configuration ROM PCB Revision BYTE 3</b>	0xF040	R	C
<b>Configuration ROM PCB Revision BYTE 2</b>	0xF044	R	C
<b>Configuration ROM PCB Revision BYTE 1</b>	0xF048	R	C
<b>Configuration ROM PCB Revision BYTE 0</b>	0xF04C	R	C
<b>Configuration ROM FLASH Type</b>	0xF050	R	C
<b>Configuration ROM Board Serial Number BYTE 1</b>	0xF080	R	C
<b>Configuration ROM Board Serial Number BYTE 0</b>	0xF084	R	C
<b>Configuration ROM VCXO Type</b>	0xF088	R	C

## 1.3 Event Readout Buffer

This is the addressing space for the event readout. The event payload is made of 32-bit words; its structure is defined in the User Manual of the board.

Address	0x0000 - 0x0FFC
Mode	R
Attribute	C

Bit	Description
[31:0]	32-bit word of the event.

## 1.4 Post Trigger

The post trigger corresponds to the delay between the trigger arrival and the DRS4 chip holding phase. The value written in this register must be multiplied by 8.5 ns.

**Note:** An additional latency time should be added to the post-trigger size, which depends on the trigger source. In case of TRG-IN the latency is about 115 ns (for ROC FPGA firmware less than 4.07 the latency was 255 ns); in case of TRn the latency is about 42 ns.

**Note:** The post-trigger value must be set common to all the channels at the broadcast address 0x8114 and can be read at the same register address, or individually read per channel group at the addresses 0x1n14 (n = 0, 1, 2, 3).

Address	0x1n14, 0x8114
Mode	R/W
Attribute	G

Bit	Description
[9:0]	Post Trigger value. <b>Note:</b> For FW rev. < 0.3, the Post Trigger value is over 7 bits.
[31:10]	Reserved

## 1.5 Dummy32

Writing and reading at this register can be used for debug purposes to test the local bus.

**Note:** Since this register is common to two groups, a write access to either 0x1024 or 0x1124 leads to the same setting for group 0 and group 1, and a write access to either 0x1224 or 0x1324 leads to the same setting for group 2 and group 3.

Address 0x1n24, 0x8024  
Mode R/W  
Attribute G

Bit	Description
[31:0]	Dummy32 value (default value is 0).

## 1.6 Group n Channel Threshold

This register manages the Trigger Threshold of all channels of the board. In particular the index n (from 0 to 3) controls the group number, and bits[15:12] control the channel index (from 0 to 7) of group n. Bits[15:12] can be used in write access only. In read access, the channel index must be set through register 0x1nA4 (see Sec. 1.11).

For example, to set the Threshold value 0x100 for channel 15 (channel 7 of group 1), write 0x7100 at 0x1180. To read the Threshold value of channel 15, write 0x7 at 0x11A4, then read at 0x1180.

**Note:** this register is implemented from AMC FPGA firmware revision 0.4 on.

Address	0x1n80, 0x8080
Mode	R/W
Attribute	G

Bit	Description
[11:0]	Threshold value in LSB counts.
[15:12]	Channel index. From 0x0 to 0x7 it addresses a single channel of Group n, while 0xF addresses all channels of Group n.
[31:16]	Reserved

## 1.7 Group n Status

This register contains the status information common to all the channels of group n.

Address 0x1n88  
Mode R  
Attribute G

Bit	Description
[0]	Memory Full.
[1]	Memory Empty.
[2]	If 1, the SPI bus is busy.
[5:3]	Reserved
[6]	If 1, the DRS4 PLL of the even group is locked.
[7]	If 1, the DRS4 PLL of the odd group is locked.
[8]	If 1, the DRS4 chip is busy.
[9]	Mezzanine PCB revision. Options are: 0 = revision 0; 1 = revision equal or higher than 1.
[31:10]	Reserved

## 1.8 AMC Firmware Revision

This register contains the channel FPGA (AMC) firmware revision information.

The complete format is:

Firmware Revision = X.Y (16 lower bits)

Firmware Revision Date = Y/M/DD (16 higher bits)

**EXAMPLE 1:** revision 1.03, November 12th, 2007 is 0x7B120103.

**EXAMPLE 2:** revision 2.09, March 7th, 2016 is 0x03070209.

**Note:** the nibble code for the year makes this information to roll over each 16 years.

Address	0x1n8C
Mode	R
Attribute	G

Bit	Description
[7:0]	AMC Firmware Minor Revision Number (Y).
[15:8]	AMC Firmware Major Revision Number (X).
[31:16]	AMC Firmware Revision Date (Y/M/DD).

## 1.9 Group n Channel DC Offset

This register allows to adjust the baseline position (i.e. the 0 Volt) of the input signal on the ADC scale. The ADC scale ranges from 0 to  $2^{\text{NBit}-1}$ , where NBit is the number of bits of the on-board ADC. The DAC controlling the DC Offset has 16 bits, i.e. it goes from 0 to 65535 independently from the NBit value and the board type.

Typically a DC Offset value of 32K (DAC mid-scale) corresponds to about the ADC mid-scale. Increasing values of DC Offset make the baseline decrease. The range of the DAC is about 5% (typ.) larger than the ADC range, hence DAC settings close to 0 and 64K correspond to ADC respectively over and under range.

This register manages the DC Offset of all channels of the board. In particular the index n (from 0 to 3) controls the group number, and bits[19:16] control the channel index (from 0 to 7) of group n. Bits[19:16] can be used in write access only. In read access, the channel index must be set through register 0x1nA4 (see Sec. 1.11).

For example, to set the DC Offset value 0x6C00 for channel 15 (channel 7 of group 1), write 0x76C00 at 0x1198. To read the DC Offset value of channel 15, write 0x7 at 0x11A4, then read at 0x1198.

**WARNING:** before writing this register, it is necessary to check that bit[2] = 0 at 0x1n88 (see Sec. 1.7), otherwise the writing process will not run properly!

Address	0x1n98, 0x8098
Mode	R/W
Attribute	G

Bit	Description
[15:0]	DC Offset value in DAC LSB unit.
[19:16]	Channel index. From 0x0 to 0x7 it addresses a single channel of Group n, while 0xF addresses all channels of Group n.
[31:20]	Reserved

## 1.10 DRS4 Chip Temperature

Address 0x1nA0  
Mode R  
Attribute G

Bit	Description
[7:0]	DRS4 temperature from -64°C to 127°C. The minimum readable temperature is 0xC0 (-64°C), while the maximum readable temperature is 0x7F (127°C).
[31:8]	Reserved

## 1.11 Group n Channel Selection

This register allows the user to select the channel of group n to read registers 0x1n80 (see Sec. 1.6) and 0x1n98 (see Sec. 1.9).

For example, to read the DC Offset of channel 15 (channel 7 of group 1), write 0x7 at 0x11A4, then read at 0x1198.

Address	0x1nA4
Mode	R/W
Attribute	G

Bit	Description
[3:0]	DAC Channel index for readout, from 0x0 to 0x7.
[31:4]	Reserved

## 1.12 Group n Channel Trigger Mask

This register must be set if working in Self-Trigger mode. It allows selecting which channels of group n (8-channels group) must participate in logic OR to generate the trigger for the event acquisition. This trigger is common to the couples of adjacent groups 0-1, and 2-3 (VME form factor only). When at least one channel of group 0 or group 1 crosses the programmable threshold (register 0x1n80, see Sec. 1.6), all the enabled channels of these two groups do acquire an event simultaneously. The same in the case of group 2 and group 3, supported by the VME form factor only. The two couples of groups 0-1 and 2-3 (VME form factor only) can be considered independent.

**Note:** this register is implemented from AMC FPGA firmware revision 0.4 on.

Address 0x1nA8, 0x80A8  
 Mode R/W  
 Attribute G

Bit	Description
[7:0]	Bit m corresponds to channel m of group n. Options are: 0 = Channel does not participate in the trigger generation; 1 = Channel participates in the trigger generation.
[31:8]	Reserved

## 1.13 Group n TR Trigger Threshold

This register sets the trigger threshold of the TRn.

NOTE: Since one TRn is common to two groups, a write access to either 0x10D4 or 0x11D4 leads to the same setting for TR0 input, and a write access to either 0x12D4 or 0x13D4 leads to the same setting for TR1 input (VME only).

Few examples of possible choices of Threshold according to the input pulse are reported in the table below.

**Note:** On boards with Mezzanine PCB Rev.1 and signal on TRn higher than 2 V it is recommended to use an external attenuator.

**WARNING:** before writing this register, it is necessary to check that bit[2] = 0 at 0x1n88 (see Sec. 1.7), otherwise the writing process will not run properly!

Address	0x1nD4, 0x80D4
Mode	R/W
Attribute	G

Bit	Description
[15:0]	Threshold value for TRn
[31:16]	Reserved

## 1.14 Group n TR DC Offset

This register sets the DC Offset for the TRn.

**Note:** Since one TRn is common to two groups, a write access to either 0x10DC or 0x11DC leads to the same setting for TR0 input, and a write access to either 0x12DC or 0x13DC leads to the same setting for TR1 input (VME only).

Few examples of possible choices of DC Offset according to the input pulse are reported in the table below.

**Note:** On boards with Mezzanine PCB Rev.1 and signal on TRn higher than 2 V it is recommended to use an external attenuator.

**WARNING:** before writing this register, it is necessary to check that bit[2] = 0 at 0x1n88 (see Sec. 1.7), otherwise the writing process will not run properly!

Address	0x1nDC, 0x80DC
Mode	R/W
Attribute	G

Bit	Description
[15:0]	DC Offset in DAC LSB unit.
[31:16]	Reserved

## 1.15 Board Configuration

This register contains general settings for the board configuration.

Address 0x8000, 0x8004 (BitSet), 0x8008 (BitClear)  
 Mode R/W  
 Attribute C

Bit	Description
[2:0]	Reserved
[3]	Test Mode (default value is 0). When the test pattern is enabled, the input samples are replaced by a sawtooth test signal. Options are: 0 = Test Mode disabled; 1 = Test Mode enabled.
[4]	Reserved: must be 1.
[5]	Reserved
[6]	Trigger polarity (supported by both fast trigger on TRn and channel self-trigger). Options are: 0 = Rising Edge (Default); 1 = Falling Edge.
[7]	Reserved
[8]	Individual trigger (default value is 0): MUST BE 1. <b>Note:</b> Despite the other digitizers running Raw Waveform Firmware, the 742 series must have this bit set to 1 to work properly.
[10:9]	Reserved: must be 0
[11]	TRn Readout Enable. When this bit is 1, the signal TRn is digitized and it is present in data readout. Options are: 0 = Signal TRn Readout disabled (Default); 1 = Signal TRn Readout enabled.
[12]	TRn Trigger Enable. When this bit is 1, the TRn signal is used as fast trigger. Options are: 0 = TRn Local Trigger disabled (Default); 1 = TRn Local Trigger enabled.
[13]	Enable the acquisition in "Transparent Mode". When this bit is 1, data in the event are referred to the ADC. Refer to the User Manual for more details. Options are: 0 = Acquisition in Output Mode (Default); 1 = Acquisition in Transparent Mode. <b>Note:</b> this bit is valid from AMC FPGA firmware revision 0.04.
[14]	Reserved
[15]	Enable the signal on TRG-IN to gate/veto the acquisition (see also bit[17] of this register and bits[11:10] of register 0x811C, see Sec. 1.25). Options are: 0 = disabled (default); 1 = enabled.
[16]	Reserved
[17]	Signal on TRG-IN connector is used to gate/veto the acquisition. Enable this option through bit[15] of this register. Refer also to bits[11:10] of register 0x811C, see Sec. 1.25. Options are: 0 = gate (default); 1 = veto.
[19:18]	Reserved
[20]	Extended Group Trigger Time Tag flag (EGTTT). If enabled, the Group Trigger Time Tag information is extended to 60 bits. Referring to the event structure of the digitizer and channel groups 0-1, the MSB of the EGTTT (common to Group0 and Group1) is the 30-bit Group Trigger Time Tag header information of Group1, while the LSB is the 30-bit Group Trigger Time Tag of Group0. So for the EGTTT of Group2 and Group3 in the case of VME digitizers. Options: 0 = EGTTT disabled (default) 1 = EGTTT enabled

[21]	<p>Disable Automatic Acquisition with self-trigger mode.      This bit is used to disable the automatic acquisition from the channels when self-trigger mode is enabled.      When the board is configured in self-trigger acquisition mode, this bit should be set to "0" to allow automatic data acquisition from the two groups on the mezzanine, whenever the input signal exceeds the threshold on at least one enabled channel.      Set this bit to "1" if you want to route the self-trigger signals to the motherboard (according to the settings in bits [31:28]). This enables the use of self-trigger signals in alternative configurations, such as generating a Global acquisition trigger for the entire board (applicable only to VME boards).      Options are:      0 = automatic acquisition with self-trigger is enabled (default).      1 = automatic acquisition with self-trigger is disabled.  <b>Note:</b> the Global Trigger acquisition mode is available starting from revision firmware <b>4.30_1.08</b>.</p>
[27:22]	Reserved
[31:28]	<p>Select monitor signal from daughter board to TRG-OUT connector (set bits[17:16]=00 in register 0x811C, see Sec. <b>1.25</b>).      Options are:      0000 = no signal (default);      0001 = all fast trigger TRn;      0010 = accepted fast trigger TRn;      0011 = busy of all groups in logic OR.      0100 = when operating in self-trigger acquisition mode, this setting enables the transmission of channel over-threshold signals to the motherboard.</p>

## 1.16 Custom Size

Sets the record length, which is the number of samples (Ns) of the digitized waveform in the acquisition window.

**Note:** modifying the record length does not reduce the dead-time, since all the 1024 capacitances are read anyway for each channel.

**WARNING:** this register must not be written while the acquisition is running.

Address 0x8020  
 Mode R/W  
 Attribute C

Bit	Description
[1:0]	Custom size (default value is 00). Options are: 00 = 1024 samples/ch; 01 = 520 samples/ch; 10 = 256 samples/ch; 11 = 136 samples/ch.
[31:2]	Reserved

## 1.17 Test Mode Initial Value

Sets the initial value for the test mode (refer to bit[3] of register 0x8000, see Sec. [1.15](#)).

**Note:** This register must be read at address 0x1n7C, where n is the group index, while write access can be performed at address 0x807C only.

Address	0x807C
Mode	R/W
Attribute	C

Bit	Description
[11:0]	ADC value (default value is 0).
[31:12]	Reserved

## 1.18 DRS4 Sampling Frequency

This register sets the sampling frequency of each DRS4 chip.

**WARNING:** This register must not be written while the acquisition is running.

**Note:** This register must be read at address 0x1nD8, where n is the group index, while write access can be performed at address 0x80D8 only.

Address	0x80D8
Mode	R/W
Attribute	C

Bit	Description
[1:0]	<p>Frequency options are:            00 = 5 GS/s (default);            01 = 2.5 GS/s;            10 = 1 GS/s;            11 = 750 MS/s;</p> <p><b>Note:</b> Option 11 is valid from AMC firmware revision 1.0. x742 boards bought before the introduction of this option do not have the corrections for this frequency. Please contact CAEN support for the upgrade.</p>
[31:2]	Reserved

## 1.19 Acquisition Control

This register manages the acquisition settings.

Address 0x8100  
 Mode R/W  
 Attribute C

Bit	Description
[1:0]	Start/Stop Mode Selection (default value is 00). Options are: 00 = SW CONTROLLED. Start/stop of the run takes place on software command by setting/resetting bit[2] of this register; 01 = S-IN/GPI CONTROLLED (S-IN for VME, GPI for Desktop/NIM). Acquisition must be armed by setting bit[2] = 1, then the run can optionally START/STOP ON LEVEL or START ON EDGE according to bit[11] ( <b>Note:</b> the START ON EDGE option is implemented from ROC FPGA fw revision 4.22 on); 10 = FIRST TRIGGER CONTROLLED. If the acquisition is armed (i.e. bit[2] = 1), then the run starts on the first trigger pulse (rising edge on TRG-IN); this pulse is not used as input trigger, while actual triggers start from the second pulse. The stop of Run must be SW controlled (i.e. bit[2] = 0); 11 = LVDS CONTROLLED (VME only). It is like option 01 but using LVDS (RUN) instead of S-IN. The LVDS can be set using registers 0x811C (see Sec. 1.25) and 0x81A0 (see Sec. 1.34).
[2]	Acquisition Start/Arm (default value is 0). When bits[1:0] = 00, this bit acts as a Run Start/Stop. When bits[1:0] = 01, 10, 11, this bit arms the acquisition and the actual Start/Stop is controlled by an external signal. Options are: 0 = Acquisition STOP (if bits[1:0]=00); Acquisition DISARMED (others); 1 = Acquisition RUN (if bits[1:0]=00); Acquisition ARMED (others).
[3]	Reserved: must be 0
[5:4]	Reserved
[6]	PLL Reference Clock Source (Desktop/NIM only). Default value is 0. Options are: 0 = internal oscillator (50 MHz); 1 = external clock from front panel CLK-IN connector. <b>Note:</b> this bit is reserved in case of VME boards.
[7]	Reserved.
[8]	LVDS I/O Busy-In Enable (VME only). Default value is 0. This bit must be enabled to let the board accept the Busy signal as input on the LVDS I/Os. Options are: 0 = disabled; 1 = enabled. <b>Note:</b> this bit is supported only by VME boards and meaningful only if the LVDS new features are enabled (bit[8]=1 of register 0x811C, see Sec. 1.25), the LVDS I/O mode is set to nBusy/nVeto (register 0x81A0, see Sec. 1.34), and the LVDS I/Os are set as inputs (register 0x811C, see Sec. 1.25).
[9]	LVDS I/O Veto-In Enable (VME only). Default value is 0. This bit must be enabled to let the board accept the Veto signal as input on the LVDS I/Os. Options are: 0 = disabled; 1 = enabled. <b>Note:</b> this bit is supported only by VME boards and meaningful only if the LVDS new features are enabled (bit[8]=1 of register 0x811C, see Sec. 1.25), the LVDS I/O mode is set to nBusy/nVeto (register 0x81A0, see Sec. 1.34), and the LVDS I/Os are set as inputs (register 0x811C, see Sec. 1.25). <b>Note:</b> LVDS I/O Veto-In signal does not inhibit triggers from TRn or channels self-triggers.
[10]	Reserved.

[11]	<p>LVDS I/O RunIn Enable Mode (VME only) and START ON EDGE Enable for S-IN/GPI CONTROLLED Mode.</p> <p>- If LVDS CONTROLLED MODE is set (bit[1:0] = 0b11) and acquisition is armed (bit[2] = 1), this bit let the LVDS I/Os be set to accept a RunIn signal to control the acquisition upon two options. One is start/stop on level, where the start of the RUN is given at RunIn signal level high and the stop at RunIn signal level low. The other is start on edge, where the start of the RUN is given on the rising edge of the RunIn signal, while the Stop must be only on software command:</p> <p>0 = starts on RunIn level (default);  1 = starts on RunIn rising edge.</p> <p><b>Note:</b> this bit is meaningful only if the LVDS new features are enabled (bit[8]=1 of register 0x811C, see Sec. 1.25). Register 0x81A0 (see Sec. 1.34) must also be configured for nBusy/nVeto.</p> <p><b>Note:</b> this register is valid from ROC FPGA fw revision 4.16 on.</p> <p>- If S-IN/GPI CONTROLLED Mode is set (bit[1:0] = 0b01) and acquisition is armed (bit[2] = 1):</p> <p>0 = Start/Stop run on S-IN/GPI level (default);  1 = Start run on S-IN/GPI rising edge (stop must be by software command: bit[2] = 0).</p> <p><b>Note:</b> options bit[11] = 1 is valid from ROC FPGA fw revision 4.22 on.</p>
[12]	<p>Vetoln as veto for TRG-OUT (VME boards only). When the LVDS Vetoln signal is enabled (bit[9] = 1 in the 0x8100 register, see Sec. 1.19), this bit permits to use Vetoln to inhibit the triggers on TRG-OUT connector. The duration of the veto signal on TRG-OUT can be optionally extended by a time value set in the 0x81C4 register (see Sec. 1.35). Such function is useful in particular cases of synchronization of a multi-board system.</p> <p>Options are:</p> <p>0 = Vetoln not used (default)  1 = Vetoln used for TRG-OUT inhibit</p> <p><b>Note:</b> this bit is reserved in case of Desktop and NIM digitizers or ROC FPGA firmware rel. &lt; 4.16 .</p>
[31:13]	Reserved.

## 1.20 Acquisition Status

This register monitors a set of conditions related to the acquisition status.

Address 0x8104  
 Mode R  
 Attribute C

Bit	Description
[1:0]	Reserved.
[2]	Acquisition Status. It reflects the status of the acquisition and drives the front panel 'RUN' LED. Options are: 0 = acquisition is stopped ('RUN' is off); 1 = acquisition is running ('RUN' lits).
[3]	Event Ready. Indicates if any events are available for readout. Options are: 0 = no event is available for readout; 1 = at least one event is available for readout. <b>Note:</b> the status of this bit must be considered when managing the readout from the digitizer.
[4]	Event Full. Indicates if the board memory has reached the FULL condition (i.e. maximum number of storable events). Options are: 0 = the board is not FULL; 1 = the board is FULL.
[5]	Clock Source. Indicates the clock source status. Options are: 0 = internal (PLL uses the internal 50 MHz oscillator as reference); 1 = external (PLL uses the external clock on CLK-IN connector as reference).
[6]	Reserved.
[7]	PLL Unlock Detect. This bit flags a PLL unlock condition. Options are: 0 = PLL has had an unlock condition since the last register read access; 1 = PLL has not had any unlock condition since the last register read access. <b>Note:</b> flag can be restored to 1 via read access to register 0xEF04 (see Sec. 1.37).
[8]	Board Ready. This flag indicates if the board is ready for acquisition (PLL and ADCs are correctly synchronized). Options are: 0 = board is not ready to start the acquisition; 1 = board is ready to start the acquisition. <b>Note:</b> this bit should be checked after software reset to ensure that the board will enter immediately in run mode after the RUN mode setting; otherwise, a latency between RUN mode setting and Acquisition start might occur.
[14:9]	Reserved.
[15]	S-IN (VME boards) or GPI (DT/NIM boards) Status. Reads the logical level on S-IN (GPI) front panel connector.
[16]	TRG-IN Status. Reads the logical level on TRG-IN front panel connector.
[31:17]	Reserved.

## 1.21 Software Trigger

Writing this register causes a software trigger generation which is propagated to all the enabled channels of the board.

Address 0x8108  
Mode W  
Attribute C

Bit	Description
[31:0]	Write whatever value to generate a software trigger.

## 1.22 Global Trigger Mask

This register sets which signal can contribute to the global trigger generation.

Address 0x810C  
 Mode R/W  
 Attribute C

Bit	Description
[3:0]	<p>When the Global Trigger acquisition mode is enabled, bit n corresponds to the trigger request from group n that participates to the global trigger generation (n = 0,1 for DT, NIM; n = 0,...,3 for VME boards).</p> <p>Options are:</p> <p>0 = trigger request does not participate to the global trigger generation;    1 = trigger request participates to the global trigger generation.</p> <p><b>Note:</b> in case of DT, NIM only bits[1:0] are meaningful, while bits[3:2] are reserved.</p> <p><b>Note:</b> Global Trigger acquisition mode is available starting from revision firmware <b>4.30_1.08</b>.</p>
[29:4]	Reserved
[30]	<p>External Trigger (default value is 1). When enabled, the external trigger on TRG-IN participates to the global trigger generation in logic OR with the other enabled signals. Options are:</p> <p>0 = disabled;    1 = enabled.</p>
[31]	<p>Software Trigger (default value is 1). When enabled, the software trigger participates to the global trigger signal generation in logic OR with the other enabled signals. Options are:</p> <p>0 = disabled;    1 = enabled.</p>

## 1.23 Front Panel TRG-OUT (GPO) Enable Mask

This register sets which signal can contribute to generate the signal on the front panel TRG-OUT LEMO connector (GPO in case of DT and NIM boards).

Address	0x8110
Mode	R/W
Attribute	C

Bit	Description
[3:0]	Bit n corresponds to the signal from group n which participates to the TRG-OUT (GPO) generation. Signal can be selected through bits[31:28] of register 0x8000 (see Sec. 1.15). Options are: 0 = Signal from group n does not participate to the TRG-OUT (GPO) signal; 1 = Signal from group n participates to the TRG-OUT (GPO) signal. <b>Note:</b> In case of DT and NIM boards, only bits[1:0] are meaningful while bits[3:2] are reserved.
[7:4]	Reserved. <b>Note:</b> in case of DT and NIM boards bits[7:2] are reserved.
[9:8]	TRG-OUT (GPO) Generation Logic. The enabled input (bits[3:0]) can be combined to generate the TRG-OUT (GPO) signal. Options are: 00 = OR; 01 = AND; 10 = Reserved; 11 = Reserved.
[29:10]	Reserved
[30]	External Trigger (default value is 1). When enabled, the external trigger on TRG-IN can participate in the TRG-OUT (GPO) signal generation in logic OR with the other enabled signals. Options are: 0 = disabled; 1 = enabled.
[31]	Software Trigger (default value is 1). When enabled, the software trigger can participate in the TRG-OUT (GPO) signal generation in logic OR with the other enabled signals. Options are: 0 = disabled; 1 = enabled.

## 1.24 LVDS I/O Data

This register allows to read out the logic level of the LVDS I/Os if the LVDS pins are configured as outputs, and to set the logic level of the LVDS I/Os if the pins are configured as inputs.

**NOTE:** this register is supported by VME boards only.

Address	0x8118
Mode	R/W
Attribute	C

Bit	Description
[15:0]	<p>LVDS I/O Data (VME boards only). It is the logic level of the corresponding nth LVDS I/O to read out or write, according to its direction (0x811C, bit[5:2], see Sec. 1.25). A write operation sets the corresponding pin logic state if configured as input, while a read operation returns the logic state of the corresponding pin if configured as output.</p> <p>In case of Old LVDS I/O Features (0x811C, bit[8] = 0, , see Sec. 1.25), the general purpose I/O option must be set (0x811C, bit[7:6] = 00, , see Sec. 1.25).</p> <p>In case of New LVDS I/O Features (0x811C, bit[8] = 1, , see Sec. 1.25), REGISTER mode must be set (0000 option in the 0x81A0 register, see Sec. 1.34).</p>
[31:16]	Reserved.

## 1.25 Front Panel I/O Control

This register manages the front panel I/O connectors. Default value is 0x0000000.

Address 0x811C  
 Mode R/W  
 Attribute C

Bit	Description
[0]	LEMO I/Os Electrical Level. This bit sets the electrical level of the front panel LEMO connectors: TRG-IN, TRG-OUT (GPO in case of DT and NIM boards), S-IN (GPI in case of DT and NIM boards). Options are: 0 = NIM I/O levels; 1 = TTL I/O levels.
[1]	TRG-OUT Enable (VME boards only). Enables the TRG-OUT LEMO front panel connector. Options are: 0 = enabled (default); 1 = high impedance. <b>Note:</b> this bit is reserved in case of DT and NIM boards.
[2]	LVDS I/O [3:0] Direction (VME boards only). Sets the direction of the signals on the first 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. <b>Note:</b> this bit is reserved in case of DT and NIM boards.
[3]	LVDS I/O [7:4] Direction (VME boards only). Sets the direction of the second 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. <b>Note:</b> this bit is reserved in case of DT and NIM boards.
[4]	LVDS I/O [11:8] Direction (VME boards only). Sets the direction of the third 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. <b>Note:</b> this bit is reserved in case of DT and NIM boards.
[5]	LVDS I/O [15:12] Direction (VME boards only). Sets the direction of the fourth 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. <b>Note:</b> this bit is reserved in case of DT and NIM boards.
[7:6]	LVDS I/O Signal Configuration (VME boards only). Valid for old LVDS I/O features only (0x811C, bit[8] = 0, see Sec. 1.25). Options are: 00 = general purpose I/Os: LVDS I/Os work as register; I/O direction is configured through bit[5:2]; the logic level is read out or set in the 0x8118 register (see Sec. 1.24). 01 = programmed I/Os: direction and function of the LVDS signals are fixed (see the tabled signal pinout in the digitizer User Manual). 10 = pattern mode: LVDS signals are inputs and their value is written into the header PATTERN field of the event (see the digitizer User Manual); 11 = reserved. <b>Note:</b> these bits are reserved in case of DT and NIM boards.
[8]	LVDS I/O New Features Selection (VME boards only). Options are: 0 = LVDS old features; 1 = LVDS new features. The new features options can be configured through register 0x81A0 (see Sec. 1.34). Please, refer to the User Manual for all details. <b>Note:</b> LVDS I/O New Features option is valid from motherboard firmware revision 3.8 on. <b>Note:</b> this bit is reserved in case of DT and NIM boards.

[9]	LVDS I/Os Pattern Latch Mode (VME boards only). Options are: 0 = Pattern (i.e. 16-pin LVDS status) is latched when the (internal) global trigger is sent to channels, in consequence of an external trigger. It accounts for post-trigger settings and input latching delays; 1 = Pattern (i.e. 16-pin LVDS status) is latched when an external trigger arrives. <b>Note:</b> this bit is reserved in case of DT and NIM boards.
[10]	TRG-IN control. The board trigger logic can be synchronized either with the edge of the TRG-IN signal, or with its whole duration. <b>Note:</b> this bit must be used in conjunction with bit[11] = 0. Options are: 0 = trigger is synchronized with the edge of the TRG-IN signal; 1 = trigger is synchronized with the whole duration of the TRG-IN signal.
[11]	TRG-IN to Mezzanines (channels). Options are: 0 = TRG-IN signal is processed by the motherboard and sent to mezzanine (default). The trigger logic is then synchronized with TRG-IN; 1 = TRG-IN is directly sent to the mezzanines with no mother board processing nor delay. This option can be useful when TRG-IN is used to veto the acquisition. <b>Note:</b> if this bit is set to 1, then bit[10] is ignored.
[13:12]	Reserved.
[14]	Force TRG-OUT (GPO). This bit can force TRG-OUT (GPO in case of DT and NIM boards) test logical level if bit[15] = 1. Options are: 0 = Force TRG-OUT (GPO) to 0; 1 = Force TRG-OUT (GPO) to 1.
[15]	TRG-OUT (GPO) Mode. Options are: 0 = TRG-OUT (GPO) is an internal signal (according to bits[17:16]); 1 = TRG-OUT (GPO) is a test logic level set via bit[14].
[17:16]	TRG-OUT (GPO) Mode Selection. Options are: 00 = Trigger: TRG-OUT/GPO propagates the internal trigger sources according to register 0x8110 (see Sec. 1.23); 01 = Motherboard Probes: TRG-OUT/GPO is used to propagate signals of the motherboards according to bits[19:18]; 10 = Channel Probes: TRG-OUT/GPO is used to propagate signals of the mezzanines (Channel Signal Virtual Probe) according to bits[31:28] of register 0x8000 (see Sec. 1.15); 11 = S-IN (GPI) propagation.
[19:18]	Motherboard Virtual Probe Selection (to be propagated on TRG-OUT/GPO). Options are: 00 = RUN/delayedRUN: this is the RUN in case of ROC FPGA firmware rel. less than 4.12. This probe can be selected according to bit[20]. 01 = CLKOUT: this clock is synchronous with the sampling clock of the ADC and this option can be used to align the phase of the clocks in different boards; 10 = CLK Phase; 11 = BUSY/UNLOCK: this is the board BUSY in case of ROC FPGA firmware rel. 4.5 or lower. This probe can be selected according to bit[20].
[20]	According to bits[19:18], this bit selects the probe to be propagated on TRG-OUT. If bits[19:18] = 00, then bit[20] options are: 0 = RUN, the signal is active when the acquisition is running and it is synchronized with the start run. This option must be used to synchronize the start/stop of the acquisition through the TRG-OUT->TR-IN or TRG-OUT->S-IN (GPI) daisy chain. 1 = delayedRUN. This option can be used to debug the synchronization when the start/stop is propagated through the LVDS I/O (VME boards). If bits[19:18] = 11, then bit[20] options are: 0 = Board BUSY; 1 = PLL Lock Loss. <b>Note:</b> this bit is reserved in case of ROC FPGA firmware rel. 4.5 or lower. <b>Note:</b> this bit corresponds to BUSY/UNLOCK for ROC FPGA firmware rel. less than 4.12.
[22:21]	Pattern Configuration. Configures the information given by the 16-bit PATTERN field in the header of the event format (VME only). Options are: 00 = PATTERN: 16-bit pattern latched on the 16 LVDS signals as one trigger arrives (default); Other options are reserved.
[31:23]	Reserved.

## 1.26 Group Enable Mask

This register enables/disables selected groups to participate in the event readout.

**WARNING:** this register must not be modified while the acquisition is running.

Address 0x8120  
 Mode R/W  
 Attribute C

Bit	Description
[3:0]	<p>Group Enable Mask. Default value is 0xF. Bit n can enable/disable group n to participate in the event readout. Options are:            0: disabled;            1: enabled.</p> <p><b>Note:</b> this function concerns only bits[1:0] in case of DT and NIM boards.</p>
[31:4]	Reserved

## 1.27 ROC FPGA Firmware Revision

This register contains the motherboard FPGA (ROC) firmware revision information.

The complete format is:

Firmware Revision = X.Y (16 lower bits)

Firmware Revision Date = Y/M/DD (16 higher bits)

**EXAMPLE 1:** revision 3.08, November 12th, 2007 is 0x7B120308.

**EXAMPLE 2:** revision 4.09, March 7th, 2016 is 0x03070409.

**Note:** the nibble code for the year makes this information to roll over each 16 years.

Address	0x8124
Mode	R
Attribute	C

Bit	Description
[7:0]	ROC Firmware Minor Revision Number (Y).
[15:8]	ROC Firmware Major Revision Number (X).
[31:16]	ROC Firmware Revision Date (Y/M/DD).

## 1.28 Software Clock Sync

At power-on, a Sync command is issued by the firmware to the ADCs to synchronize all of them to the clock of the board. In the standard operating, this command is not required to be repeated by the user.

A write access to this register (any value) forces the PLL to re-align all the clock outputs with the reference clock.

**EXAMPLE:** in case of Daisy chain clock distribution among VME boards, during the initialization and configuration, the reference clocks along the Daisy chain can be unstable and a temporary loss of lock may occur in the PLLs; although the lock is automatically recovered once the reference clocks return stable, it is not guaranteed that the phase shift returns to a known state. This command allows the board to restore the correct phase shift between the CLK-IN and the internal clocks.

**Note:** this register is supported by VME boards only.

**Note:** the command must be issued starting from the first to the last board in the clock chain.

Address	0x813C
Mode	W
Attribute	C

Bit	Description
[31:0]	Write whatever value to generate a Sync command.

## 1.29 Board Info

This register contains the specific information of the board, such as the digitizer family, the channel memory size and the channel density.

Address	0x8140
Mode	R
Attribute	C

Bit	Description
[7:0]	Digitizer Family Code: 0x06 = 742 digitizer family.
[15:8]	Channel Memory Size Code. Options are: 0x01 = 128 events per channel; 0x08 = 1024 events per channel.
[23:16]	Equipped Groups Number. Options are: 0x02 = 2 groups (DT and NIM boards); 0x04 = 4 groups (VME boards). <b>Note:</b> if this number is lower than the physical group number, there could be a communication problem with some of the mezzanines.
[31:24]	Reserved.

## 1.30 Event Size

This register contains the current available event size in 32-bit words. The value is updated after a complete readout of each event.

Address 0x814C  
Mode R  
Attribute C

Bit	Description
[31:0]	Event Size (32-bit words).

## 1.31 Fan Speed Control

This register manages the on-board fan speed in order to guarantee an appropriate cooling according to the internal temperature variations.

**Note:** from revision 4 of the motherboard PCB (register 0xF04C of the Configuration ROM, see Sec. 1.67), the automatic fan speed control has been implemented, and it is supported by ROC FPGA firmware revision greater than 4.4 (register 0x8124, see Sec. 1.27).

Independently of the revision, the user can set the fan speed high by setting bit[3] = 1. Setting bit[3] = 0 will restore the automatic control for revision 4 or higher, or the low fan speed in case of revisions lower than 4.

**Note:** this register is supported by Desktop (DT) boards only.

Address	0x8168
Mode	R/W
Attribute	C

Bit	Description
[2:0]	Reserved: Must be 0.
[3]	Fan Speed Mode. Options are: 0 = slow speed or automatic speed tuning; 1 = high speed.
[5:4]	Reserved: Must be 1.
[31:6]	Reserved: Must be 0.

## 1.32 Run/Start/Stop Delay

This register sets the delay in the Start Run of the board either the command is issued by software, or by hardware through a single-ended (via S-IN/GPI or TRG-IN connectors) or differential (via LVDS I/O connector) input signal. This delay especially occurs in the daisy chain propagation of the run signal in a multi-board system. The latency, mainly due to the cable length and the board's internal circuitry, can be compensated by properly delaying the start of run for each board in the chain. The delay value to set is usually zero for the last board and rises going backwards along the chain.

Address 0x8170  
Mode R/W  
Attribute C

Bit	Description
[7:0]	Delay value in steps 34 ns.
[31:8]	Reserved.

## 1.33 Board Failure Status

This register informs on the cause of a board fail. In event of a failure, bit[26] in the second word of the event format header is set to 1 during data readout (refer to the event structure description in the User Manual of the digitizer). Reading at this register checks which kind of error occurred.

**Note:** in case of problems with the board, the user is recommended to contact CAEN for support.

Address 0x8178  
 Mode R  
 Attribute C

Bit	Description
[3:0]	Reserved.
[4]	PLL Lock Loss. Options are: 0 = no error; 1 = PLL Lock Loss occurred.
[31:5]	Reserved.

## 1.34 Front Panel LVDS I/O New Features

If the LVDS I/O new features are enabled (bit[8] = 1 of 0x811C, see Sec. 1.25), this register programs the functions of the front panel LVDS I/O 16-pin connector. It is possible to configure the LVDS I/O pins by group of four (4).

Options are:

- 1) 0000 = REGISTER, where the four LVDS I/O pins act as register (write/read according to the configured input/output option);
- 2) 0001 = TRIGGER, where each group of four LVDS I/O pins can be configured to receive an input trigger for each channel (DPP Firmware only), or to propagate out the trigger request;
- 3) 0010 = nBUSY/nVETO, where each group of four LVDS I/O pins can be configured as inputs (0 = nBusyIn, 1 = nVetoIn, 2 = nTrigger In, 3 = nRun In) or as outputs (0 = nBusy, 1 = nVeto, 2 = nTrigger Out, 3 = nRun );
- 4) 0011 = LEGACY, that is to say according to the old LVDS I/O configuration (i.e. ROC FPGA firmware revisions lower than 3.8), where the LVDS can be configured as 0 = nclear TTT, and 1 = 2 = 3 = reserved in case of input LVDS setting, while they can be configured as 0 = Busy, 1 = Data ready, 2 = Trigger, 3 = Run in case of output LVDS setting.

Please refer to the Front Panel LVDS I/Os section of the digitizer User Manual for detailed description.

**Note:** LVDS I/O new features are supported from ROC FPGA firmware revision 3.8 on.

**Note:** this register is supported by VME boards only.

Address	0x81A0
Mode	R/W
Attribute	C

Bit	Description
[3:0]	LVDS I/O pins[3:0] Configuration.
[7:4]	LVDS I/O pins[7:4] Configuration.
[11:8]	LVDS I/O pins[11:8] Configuration
[15:12]	LVDS I/O pins[15:12] Configuration.
[16]	This bit permits selecting whether the nTrigger signal, when configured as output (in nBusy/nVeto LVDS I/O mode), is a copy of the signal sent on the TRG-OUT connector or a copy of the acquisition common trigger. Options are: 0 = nTrigger output is a copy of TRG-OUT signal; 1 = nTrigger output is a copy of the acquisition common trigger. <b>Note:</b> this bit is reserved for ROC FPGA firmware revisions less than 4.9.
[31:17]	Reserved.

## 1.35 Extended Veto Delay

This register is valid for VME boards only and set the duration of the Extended VetoIn signal for trigger inhibit on TRG-OUT when bit[12]=1 of 0x8100 register (see Sec. 1.19). Such function is useful in particular cases of synchronization of a multi-board system.

**Note:** This register is valid from ROC FPGA fw revision 4.16 on.

Address 0x81C4  
Mode R/W  
Attribute C

Bit	Description
[15:0]	Extended VetoIn duration value in units of Trigger Clock (17 ns).
[31:16]	Reserved.

## 1.36 Readout Control

This register is mainly intended for VME boards, anyway some bits are applicable also for DT and NIM boards.

Address 0xEF00  
 Mode R/W  
 Attribute C

Bit	Description
[2:0]	VME Interrupt Level (VME boards only). Options are: 0 = VME interrupts are disabled; 1,...,7 = sets the VME interrupt level. <b>Note:</b> these bits are reserved in case of DT and NIM boards.
[3]	Optical Link Interrupt Enable. Options are: 0 = Optical Link interrupts are disabled; 1 = Optical Link interrupts are enabled.
[4]	VME Bus Error / Event Aligned Readout Enable (VME boards only). Options are: 0 = VME Bus Error / Event Aligned Readout disabled (the module sends a DTACK signal until the CPU inquires the module); 1 = VME Bus Error / Event Aligned Readout enabled (the module is enabled either to generate a Bus Error to finish a block transfer or during the empty buffer readout in D32). <b>Note:</b> this bit is reserved (must be 1) in case of DT and NIM boards.
[5]	VME Align64 Mode (VME boards only). Options are: 0 = 64-bit aligned readout mode disabled; 1 = 64-bit aligned readout mode enabled. <b>Note:</b> this bit is reserved (must be 0) in case of DT and NIM boards.
[6]	VME Base Address Relocation (VME boards only). Options are: 0 = Address Relocation disabled (VME Base Address is set by the on-board rotary switches); 1 = Address Relocation enabled (VME Base Address is set by register 0xEF0C, see Sec. 1.39). <b>Note:</b> this bit is reserved (must be 0) in case of DT and NIM boards.
[7]	Interrupt Release mode (VME boards only). Options are: 0 = Release On Register Access (RORA): this is the default mode, where interrupts are removed by disabling them either by setting VME Interrupt Level to 0 (VME Interrupts) or by setting Optical Link Interrupt Enable to 0; 1 = Release On Acknowledge (ROAK). Interrupts are automatically disabled at the end of a VME interrupt acknowledge cycle (INTACK cycle). <b>Note:</b> ROAK mode is supported only for VME interrupts. ROAK mode is not supported on interrupts generated over Optical Link. <b>Note:</b> this bit is reserved (must be 0) in case of DT and NIM boards.
[8]	Extended Block Transfer Enable (VME boards only). Selects the memory interval allocated for block transfers. Options are: 0 = Extended Block Transfer Space is disabled, and the block transfer region is a 4kB in the 0x0000 - 0x0FFC interval; 1 = Extended Block Transfer Space is enabled, and the block transfer is a 16 MB in the 0x00000000 - 0xFFFFFFFFC interval. <b>Note:</b> in Extended mode, the board VME Base Address is only set via the on-board [31:28] rotary switches or bits[31:28] of register 0xEF10 (see Sec. 1.40). <b>Note:</b> this register is reserved in case of DT and NIM boards.
[31:9]	Reserved.

## 1.37 Readout Status

This register contains information related to the readout.

Address 0xEF04  
 Mode R  
 Attribute C

Bit	Description
[0]	Event Ready. Indicates if there are events stored ready for readout. Options are: 0 = no data ready; 1 = event ready.
[1]	Reserved.
[2]	Bus Error (VME boards) / Slave-Terminated (DT/NIM boards) Flag. Options are: 0 = no Bus Error occurred (VME boards) or no terminated transfer (DT/NIM boards); 1 = a Bus Error occurred (VME boards) or one transfer has been terminated by the digitizer in consequence of an unsupported register access or block transfer prematurely terminated in event aligned readout (DT/NIM). <b>Note:</b> this bit is reset after register readout at 0xEF04.
[3]	VME FIFO Flag. Options are: 0 = VME FIFO not empty; 1 = VME FIFO is empty.
[31:4]	Reserved.

## 1.38 Board ID

The meaning of this register depends on which VME crate it is inserted in.

In case of VME64X crate versions, this register can be accessed in read mode only and it contains the GEO address of the module picked from the backplane connectors; when CBLT is performed, the GEO address will be contained in the Board ID field of the Event header (see the User Manual for further details).

In case of other crate versions, this register can be accessed both in read and write mode, and it allows to write the correct GEO address (default setting = 0) of the module before CBLT operation. GEO address will be contained in the Board ID field of the Event header (see the User Manual for further details).

**Note:** this register is supported by VME boards only.

Address	0xEF08
Mode	R/W
Attribute	C

Bit	Description
[4:0]	GEO Address (VME boards only).
[31:5]	Reserved.

## 1.39 MCST Base Address and Control

This register configures the board for the VME Multicast Cycles.

**Note:** this register is supported by VME boards only.

Address	0xEF0C
Mode	R/W
Attribute	C

Bit	Description
[7:0]	These bits contain the most significant bits of the MCST/CBLT address of the module set via VME, that is the address used in MCST/CBLT operations.
[9:8]	Board Position in Daisy chain. Options are: 00 = board disabled; 01 = last board; 10 = first board; 11 = intermediate board.
[31:10]	Reserved.

## 1.40 Relocation Address

If address relocation is enabled through register 0xEF00 (bit[6] = 1, see Sec. 1.36), this register sets the VME Base Address of the module.

**Note:** this register is supported by VME boards only.

Address	0xEF10
Mode	R/W
Attribute	C

Bit	Description
[15:0]	These bits contain the A31...A16 bits of the address of the module. If bit[6] = 1 of 0xEF00 (see Sec. 1.36), they set the VME Base Address of the module.
[31:16]	Reserved.

## 1.41 Interrupt Status/ID

This register contains the STATUS/ID that the module places on the VME data bus during the Interrupt Acknowledge cycle.

**Note:** this register is supported by VME boards only.

Address	0xEF14
Mode	R/W
Attribute	C

Bit	Description
[31:0]	STATUS/ID (VME boards only).

## 1.42 Interrupt Event Number

This register sets the number of events that causes an interrupt request. If interrupts are enabled, the module generates a request whenever it has stored in memory a Number of Events > INTERRUPT EVENT NUMBER.

Address 0xEF18  
Mode R/W  
Attribute C

Bit	Description
[9:0]	INTERRUPT EVENT NUMBER.
[31:10]	Reserved.

## 1.43 Max Number of Events per BLT

This register sets the maximum number of complete events which has to be transferred for each block transfer (via VME BLT/CBLT cycles, or block readout through USB or Optical Link).

Address 0xEF1C  
Mode R/W  
Attribute C

Bit	Description
[9:0]	MAX NUM EVENT PER BLT.
[31:10]	Reserved.

## 1.44 Scratch

This register can be used to write/read words for test purposes.

Address            0xEF20  
Mode              R/W  
Attribute         C

Bit	Description
[31:0]	SCRATCH.

## 1.45 Software Reset

All the digitizer registers can be set back to their default values on software reset command by writing any value at this register, or by system reset from backplane in case of VME boards.

Address            0xEF24  
Mode              W  
Attribute        C

Bit	Description
[31:0]	Whatever value written at this location issues a software reset. All registers are set to their default values (actual settings are lost).

## 1.46 Software Clear

All the digitizer internal memories are cleared:

- automatically by the firmware at the start of each run;
- on software command by writing at this register;
- by hardware (VME boards only) through the LVDS interface properly configured.

A clear command does not change the registers actual value, except for resetting the following registers:

- Event Stored;
- Event Size;
- Channel / Group n Buffer Occupancy.

This register resets also the trigger time stamp.

Address            0xEF28  
Mode              W  
Attribute         C

Bit	Description
[31:0]	Whatever value written at this location generates a software clear.

## 1.47 Configuration Reload

A write access of any value at this location causes a software reset, a reload of Configuration ROM parameters and a PLL reconfiguration.

Address	0xEF34
Mode	W
Attribute	C

Bit	Description
[31:0]	Write whatever value to perform a software reset, a reload of Configuration ROM parameters and a PLL reconfiguration.

## 1.48 Configuration ROM Checksum

This register contains information on 8-bit checksum of Configuration ROM space.

Address 0xF000  
Mode R  
Attribute C

Bit	Description
[7:0]	Checksum.
[31:8]	Reserved.

## 1.49 Configuration ROM Checksum Length BYTE 2

This register contains information on the third byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address 0xF004  
Mode R  
Attribute C

Bit	Description
[7:0]	Checksum Length: bits[23:16].
[31:8]	Reserved.

## 1.50 Configuration ROM Checksum Length BYTE 1

This register contains information on the second byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address 0xF008  
Mode R  
Attribute C

Bit	Description
[7:0]	Checksum Length: bits[15:8].
[31:8]	Reserved.

## 1.51 Configuration ROM Checksum Length BYTE 0

This register contains information on the first byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address 0xF00C  
Mode R  
Attribute C

Bit	Description
[7:0]	Checksum Length: bits[7:0].
[31:8]	Reserved.

## 1.52 Configuration ROM Constant BYTE 2

This register contains the third byte of the 3-byte constant.

Address 0xF010  
Mode R  
Attribute C

Bit	Description
[7:0]	Constant: bits[23:16] = 0x83.
[31:8]	Reserved.

## 1.53 Configuration ROM Constant BYTE 1

This register contains the second byte of the 3-byte constant.

Address 0xF014  
Mode R  
Attribute C

Bit	Description
[7:0]	Constant: bits[15:8] = 0x84.
[31:8]	Reserved.

## 1.54 Configuration ROM Constant BYTE 0

This register contains the first byte of the 3-byte constant.

Address 0xF018  
Mode R  
Attribute C

Bit	Description
[7:0]	Constant: bits[7:0] = 0x01.
[31:8]	Reserved.

## 1.55 Configuration ROM C Code

This register contains the ASCII C character code (identifies this as CR space).

Address 0xF01C  
Mode R  
Attribute C

Bit	Description
[7:0]	ASCII 'C' Character Code.
[31:8]	Reserved.

## 1.56 Configuration ROM R Code

This register contains the ASCII R character code (identifies this as CR space).

Address 0xF020  
Mode R  
Attribute C

Bit	Description
[7:0]	ASCII 'R' Character Code.
[31:8]	Reserved.

## 1.57 Configuration ROM IEEE OUI BYTE 2

This register contains information on the third byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Address 0xF024  
Mode R  
Attribute C

Bit	Description
[7:0]	IEEE OUI: bits[23:16].
[31:8]	Reserved.

## 1.58 Configuration ROM IEEE OUI BYTE 1

This register contains information on the second byte of the 3-byte IEEE Organizational Unique Identifier (OUI).

Address 0xF028  
Mode R  
Attribute C

Bit	Description
[7:0]	IEEE OUI: bits[15:8].
[31:8]	Reserved.

## 1.59 Configuration ROM IEEE OUI BYTE 0

This register contains information on the first byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Address 0xF02C  
Mode R  
Attribute C

Bit	Description
[7:0]	IEEE OUI: bits[7:0].
[31:8]	Reserved.

## 1.60 Configuration ROM Board Version

This register contains the board version information.

Address 0xF030  
Mode R  
Attribute C

Bit	Description
[7:0]	Board Version Code. Options are: 0x70 = V1742/VX1742/DT5742/N6742; 0x71 = V1742B/VX1742B/DT5742B/N6742B.
[31:8]	Reserved.

## 1.61 Configuration ROM Board Form Factor

This register contains the information of the board form factor.

Address 0xF034  
Mode R  
Attribute C

Bit	Description
[7:0]	Board Form Factor CAEN Code. Options are: 0x00 = VME64; 0x01 = VME64X; 0x02 = Desktop; 0x03 = NIM.
[31:8]	Reserved.

## 1.62 Configuration ROM Board ID BYTE 1

This register contains the MSB of the 2-byte board identifier.

Address 0xF038  
Mode R  
Attribute C

Bit	Description
[7:0]	Board Number ID: bits[15:8].
[31:8]	Reserved.

## 1.63 Configuration ROM Board ID BYTE 0

This register contains the LSB information of the 2-byte board identifier.

Address 0xF03C  
Mode R  
Attribute C

Bit	Description
[7:0]	Board Number ID: bits[7:0].
[31:8]	Reserved.

## 1.64 Configuration ROM PCB Revision BYTE 3

This register contains information on the fourth byte of the 4-byte hardware revision.

Address 0xF040  
Mode R  
Attribute C

Bit	Description
[7:0]	PCB Revision: bits[31:24].
[31:8]	Reserved.

## 1.65 Configuration ROM PCB Revision BYTE 2

This register contains information on the third byte of the 4-byte hardware revision.

Address 0xF044  
Mode R  
Attribute C

Bit	Description
[7:0]	PCB Revision: bits[23:16].
[31:8]	Reserved.

## 1.66 Configuration ROM PCB Revision BYTE 1

This register contains information on the second byte of the 4-byte hardware revision.

Address 0xF048  
Mode R  
Attribute C

Bit	Description
[7:0]	PCB Revision: bits[15:8].
[31:8]	Reserved.

## 1.67 Configuration ROM PCB Revision BYTE 0

This register contains information on the first byte of the 4-byte hardware revision.

Address 0xF04C  
Mode R  
Attribute C

Bit	Description
[7:0]	PCB Revision: bits[7:0].
[31:8]	Reserved.

## 1.68 Configuration ROM FLASH Type

This register contains information on which FLASH type (storing the FPGA firmware) is present on- board.

Address 0xF050  
Mode R  
Attribute C

Bit	Description
[7:0]	FLASH Type. Options are: 0x00 = 8 Mb FLASH; 0x01 = 32 Mb FLASH.
[31:8]	Reserved.

## 1.69 Configuration ROM Board Serial Number BYTE 1

This register contains information on the MSB of the board serial number.

Address 0xF080  
Mode R  
Attribute C

Bit	Description
[7:0]	Board Serial Number: bits[15:8].
[31:8]	Reserved.

## 1.70 Configuration ROM Board Serial Number BYTE 0

This register contains information on the LSB of the board serial number.

Address 0xF084  
Mode R  
Attribute C

Bit	Description
[7:0]	Board Serial Number: bits[7:0].
[31:8]	Reserved.

## 1.71 Configuration ROM VCXO Type

This register contains information on which type of VCXO is present on-board.

Address 0xF088  
Mode R  
Attribute C

Bit	Description
[31:0]	VCXO Type Code. Options for VME Digitizers are: 0 = AD9510 with 1 GHz; 1 = AD9510 with 500 MHz (not programmable); 2 = AD9510 with 500 MHz (programmable). Options for Desktop/NIM Digitizers are: Reserved (value = 0).

## 2 Technical Support

To contact CAEN specialists for requests on the software, hardware, and board return and repair, it is necessary a MyCAEN+ account on [www.caen.it](http://www.caen.it):

<https://www.caen.it/support-services/getting-started-with-mycaen-portal/>

All the instructions for use the Support platform are in the document:



A paper copy of the document is delivered with CAEN boards.

The document is downloadable for free in PDF digital format at:

[https://www.caen.it/wp-content/uploads/2022/11/Safety\\_information\\_Product\\_support\\_W.pdf](https://www.caen.it/wp-content/uploads/2022/11/Safety_information_Product_support_W.pdf)



**CAEN S.p.A.**  
Via Vetraia 11  
55049 - Viareggio  
Italy  
Phone +39 0584 388 398  
Fax +39 0584 388 959  
[info@caen.it](mailto:info@caen.it)  
[www.caen.it](http://www.caen.it)



**CAEN GmbH**  
Eckehardweg 10  
42653 - Solingen  
Germany  
Phone +49 212 254 40 77  
Fax +49 212 254 40 79  
[info@caen-de.com](mailto:info@caen-de.com)  
[www.caen-de.com](http://www.caen-de.com)

**CAEN Technologies, Inc.**  
1 Edgewater Street - Suite 101  
Staten Island, NY 10305  
USA  
Phone: +1 (718) 981-0401  
Fax: +1 (718) 556-9185  
[info@caentechnologies.com](mailto:info@caentechnologies.com)  
[www.caentechnologies.com](http://www.caentechnologies.com)

**CAENspa INDIA Private Limited**  
B205, BLDG42, B Wing,  
Azad Nagar Sangam CHS,  
Mhada Layout, Azad Nagar, Andheri (W)  
Mumbai, Mumbai City,  
Maharashtra, India, 400053  
[info@caen-india.in](mailto:info@caen-india.in)  
[www.caen-india.in](http://www.caen-india.in)



Copyright ©CAEN SpA. All rights reserved. Information in this publication supersedes all earlier versions. Specifications subject to change without notice.