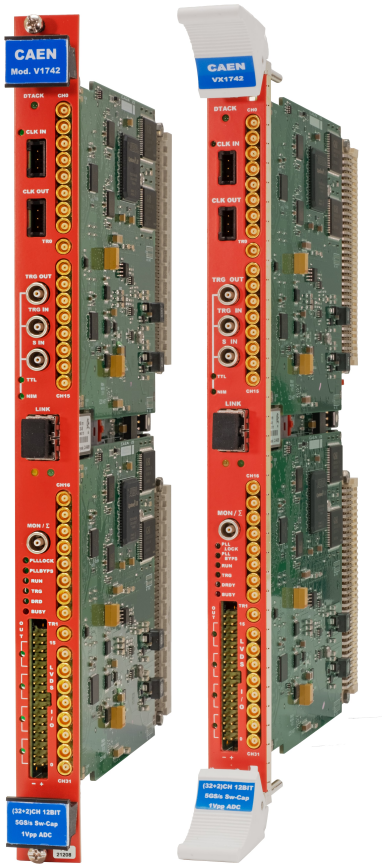
Rev. 12 - September 5th, 2025

V1742/VX1742

16+1 Channel 12 bit 5 GS/s Switched Capacitor Digitizer



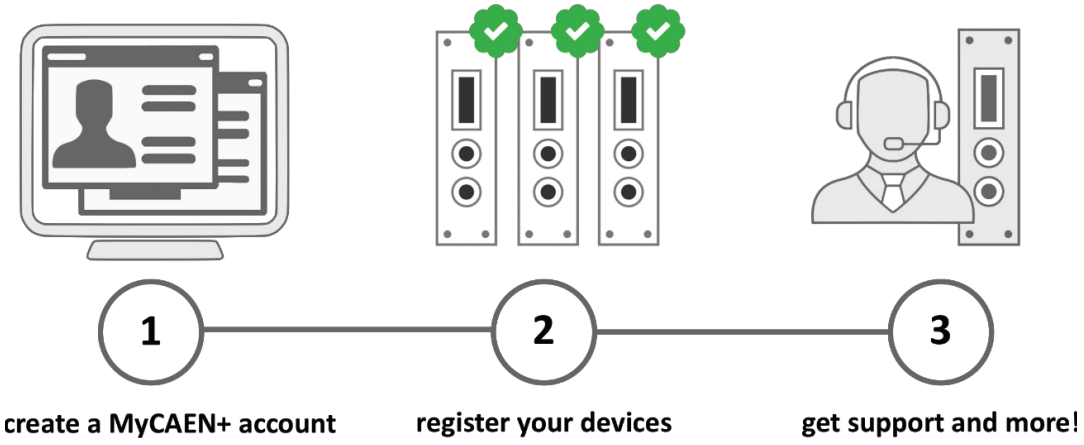
CAEN
Tools for Discovery

User Manual
UM4279

Register your device

Register your device to your **MyCAEN+** account and get access to our customer services, such as notification for new firmware or software upgrade, tracking service procedures or open a ticket for assistance. **MyCAEN+** accounts have a dedicated support service for their registered products. A set of basic information can be shared with the operator, speeding up the troubleshooting process and improving the efficiency of the support interactions.

MyCAEN+ dashboard is designed to offer you a direct access to all our after sales services. Registration is totally free, to create an account go to https://www.caen.it/become-mycaenplus-user and fill the registration form with your data.



https://www.caen.it/become-mycaenplus-user/

Purpose of the Document

This document contains the full hardware description of the V1742 and VX1742 CAEN digitizers and their principle of operating as **Waveform Recording Digitizer** (basing on the hereafter called *"waveform recording firmware"*). The reference firmware revision is: **4.30_1.08**.
For higher releases compatibility, check in the firmware revision history files. For any reference to registers in this user manual, please refer to document [RD1] at the digitizer web page.

Change Document Record

Date	Revision	Changes
-	00-06	N/A
Jan. 27th, 2017	07	Revised text layout. Improved text description to make it clearer.
Feb. 5th, 2020	08	Updated Sections: **8.2**, **9.5**, **9.13.3**, **9.11**, **13.3**. Reviewed Sections: **9.15**, **9.16**, **10.1**. Added Sections: **9.17**.
Apr. 4th, 2022	09	Updated text formatting and copyrights. Added **Safety Notices**, **Chap. 5**, **Chap. 7**, **Chap. 14**, **Chap. 15**, **Chap. 16**, Updated **Chap. 1** (**Tab. 1.1**), **Chap. 3**, **Chap. 4**, **Chap. 8**, **Chap. 9** (**Sec. 9.7.3**, **Sec. 9.8.2**, **Sec. 9.9.3**, **Sec. 9.9.4**, **Sec. 9.13**, **Sec. 9.16**), **Chap. 10**, **Chap. 12**.
January 31st, 2023	10	Added the extended 60-bit Trigger Timestamp specifications in **Chap. 3** and the description in **Sec. 9.8.2**.
June 21st, 2023	11	Added information about the input range customization at 2 V_{pp} in **Chap. 1**, **Chap. 3**, **Chap. 8**, and **Chap. 9**.
September 5th, 2025	12	Reviewed End page. Replaced references to CAENUpgrader with CAENToolbox. Updated **Safety Notices**, Chap. **1**, Tab **1.1**, Chap. **3**, Chap. **6**, Chap. **7**, Sec. **9.8.2**, Sec. **9.11**, Sec. **9.16**, Chap. **10**, Chap. **11**, Sec. **13.3**. Added Sec. **9.9.5.1**, Sec. **11.1**.

Symbols, Abbreviated Terms, and Notations

ADC	Analog-to-Digital Converter
AMC	ADC & Memory Controller
CML	Current-Mode Logic
DAQ	Data Acquisition
DAC	Digital-to-Analog Converter
DC	Direct Current
DRS4	Domino Ring Sampler 4
ECL	Emitter Coupled Logic
FPGA	Field-Programmable Gate Array
GPI	General Purpose Input
GPO	General Purpose Output
LVDS	Low-Voltage Differential Signal
LVPECL	Low-Voltage Positive Emitter Coupled Logic
NIM	Nuclear Instrumentation Module
PECL	Positive Emitter Coupled Logic
PLL	Phase-Locked Loop
ROC	ReadOut Controller
SW	SoftWare
TTL	Transistor-Transistor Logic
TTT	Trigger Time Tag
USB	Universal Serial Bus

Reference Documents

[RD1] UM5698 - 742 Registers Description

[RD2] UM11111 – CAEN Toolbox User Manual

[RD3] Precautions for Handling, Storage and Installation

[RD4] UM1935 - CAENDigitizer User & Reference Manual

[RD5] UM2091 - CAEN WaveDump User Manual

[RD6] UM7715 - CAENVMELib User & Reference Manual

[RD7] UM1934 - CAENComm User & Reference Manual

[RD8] GD5695 - 742 Quick Start Guide

[RD9] AN2086 - Synchronization of CAEN Digitizers in Multiple Board Acquisition Systems

[RD10] UM10551 A5818 Technical Information Manual

[RD11] UM7685 - V3718 & VX3718 User & Reference Manual

[RD12] UM8305 - V4718 & VX4718 User & Reference Manual

[RD13] DS7799 - A4818 Adapter Data Sheet

All CAEN documents can be downloaded at:
https://www.caen.it/support-services/documentation-area/ **(login required)**

Manufacturer Contacts

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www.caen.it | info@caen.it

Limitation of Responsibility

If the warnings contained in this manual are not followed, CAEN will not be responsible for damage caused by improper use of the device. The manufacturer declines all responsibility for damage resulting from failure to comply with the instructions for use of the product. The equipment must be used as described in the user manual, with particular regard to the intended use, using only accessories as specified by the manufacturer. No modification or repair can be performed.

Disclaimer

No part of this manual may be reproduced in any form or by any means, electronic, mechanical, recording, or otherwise, without the prior written permission of CAEN SpA.

The information contained herein has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies. CAEN SpA reserves the right to modify its products specifications without giving any notice; for up to date information please visit www.caen.it.

Made in Italy

We remark that all our boards have been designed and assembled in Italy. In a challenging environment where a competitive edge is often obtained at the cost of lower wages and declining working conditions, we proudly acknowledge that all those who participated in the production and distribution process of our devices were reasonably paid and worked in a safe environment (while this is true for the boards marked ”MADE IN ITALY”, we cannot guarantee for third-party manufactures).

Index

List of Figures

List of Tables

Safety Notices

N.B. Read carefully the "Precautions for Handling, Storage and Installation document provided with the product before starting any operation.

The following HAZARD SYMBOLS may be reported on the unit:

	Caution, refer to product manual
	Caution, risk of electrical shock
	Protective conductor terminal
	Earth (Ground) Terminal
	Alternating Current
	Three-Phase Alternating Current

The following symbol may be reported in the present manual:

	General warning statement

The symbol could be accompanied by the following terms:

- **DANGER**: indicates a hazardous situation which, if not avoided, will result in serious injury or death.
- **WARNING**: indicates a hazardous situation which, if not avoided, could result in death or serious injury.
- **CAUTION**: indicates a situation or condition which, if not avoided, could cause physical injury or damage the product and / or the surrounding environment.

GENERAL NOTICES:

CAUTION: To avoid potential hazards

USE THE PRODUCT ONLY AS SPECIFIED.
ONLY QUALIFIED PERSONNEL SHOULD PERFORM SERVICE PROCEDURES

CAUTION: Avoid Electric Overload

TO AVOID ELECTRIC SHOCK OR FIRE HAZARD, DO NOT POWER A LOAD OUTSIDE OF ITS SPECIFIED RANGE

CAUTION: Avoid Electric Shock

TO AVOID INJURY OR LOSS OF LIFE, DO NOT CONNECT OR DISCONNECT CABLES WHILE THEY ARE CONNECTED TO A VOLTAGE SOURCE

CAUTION: Do Not Operate without Covers

TO AVOID ELECTRIC SHOCK OR FIRE HAZARD, DO NOT OPERATE THIS PRODUCT WITH COVERS OR PANELS REMOVED

CAUTION: Do Not Operate in Wet/Damp Conditions

TO AVOID ELECTRIC SHOCK, DO NOT OPERATE THIS PRODUCT IN WET OR DAMP CONDITIONS

CAUTION: Do Not Operate in an Explosive Atmosphere

TO AVOID INJURY OR FIRE HAZARD, DO NOT OPERATE THIS PRODUCT IN AN EXPLOSIVE ATMOSPHERE

THIS DEVICE SHOULD BE INSTALLED AND USED BY SKILLED TECHNICIAN ONLY OR UNDER HIS SUPERVISION

DO NOT OPERATE WITH SUSPECTED FAILURES.
IF YOU SUSPECT THIS PRODUCT TO BE DAMAGED, PLEASE CONTACT THE TECHNICAL SUPPORT

See Chap. **17** for the Technical Support contacts.

VME NOTICES:

CAUTION: This product needs proper cooling.

USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEATING MAY DEGRADE THE MODULE PERFORMANCES

V1742 DIGITIZERS CANNOT BE OPERATED WITH CAEN CRATES VME8001, VME8002, VME8004, AND VME8004A. OVERHEAT MAY DAMAGE THE MODULE

CAUTION: This product needs proper handling.

THE VME DIGITIZER DOES NOT SUPPORT LIVE INSERTION (HOT-SWAP)
REMOVE OR INSERT THE BOARD WHEN THE CRATE IS POWERED OFF

ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE

1 Introduction

The Mod. V1742/VX1742 is a 1-unit wide VME 6U 32+2 Channel 12 bit 5 GS/s Switched Capacitor Digitizer based on the Switched Capacitor Array DRS4 (Domino Ring Sampler 4) chip[1].

The default input dynamic range is 1 V_{pp} (DC coupled) on single-ended MCX coaxial connectors with programmable DC Offset ($\pm$ 1 V range, controlled by a 16-bit DAC on each channel). The customization at 2 V_{pp} of input range is available by ordering option.

The analog input signal is continuously sampled by the 1024 capacitive cells of the DRS4 in a circular way, at a frequency that is software selectable amongst 5 GHz, 2.5 GHz, 1GHz, and 750 MHz.

The analog to digital conversion is not simultaneous with the chip sampling phase, and it starts as soon as the trigger condition is met. When the trigger stops the DRS4 chip sampling (holding phase), the analog memory buffer is frozen, and the cell content is made available to the 12 bit ADC for the digital conversion. The digital memory allows the subsequent events to be stored, even if the readout is not yet started. Moreover, since the digital memory buffers work like FIFOs, the readout activity from VME or Optical Link does not affect write operations of subsequent events.

The chip functioning has two major consequences:

1. there is an unavoidable dead-time when the DRS4 chip stops its acquisition and the ADC converts the capacitances (110 µs in case only the analog inputs are digitized, 181 µs when also TRn are digitized).
2. the acquisition window is fixed to 1024 samples, that in case of 5 GHz corresponds to a maximum of about 200 ns. Refer to Sec. **9.2**.

Moreover, the trigger processing introduces a latency between the trigger arrival and the DRS4 holding phase that varies according to the trigger source. The user must consider it when choosing the proper trigger source for its setup and the type of signal. Four possible trigger sources are available:

1. *Software Trigger*, common to all enabled groups, mainly intended for debug purposes. Refer to Sec. **9.9.1**.
2. *External Trigger*, trigger on TRG-IN connector, common to all enabled groups. The external trigger latency makes this mode difficult to use at 5 GHz, while all other frequencies can be used with no problem. Refer to Sec. **9.9.2**.
3. *Fast (Low Latency) Local Trigger*, trigger on TR0 and TR1 connectors, common to couples of 8-channels groups. This mode is called “Fast” or “Low Latency” since the trigger latency is reduced with respect to the external trigger. This trigger mode is convenient for high precision timing measurements, since the TRn can be digitized and reported in the output data to be used as time reference. Refer to Sec. **9.9.3**.
4. *Self-trigger*, common to couples of 8-channels groups or to all channels of the board (*Global Trigger* mode). For each group is possible to select combinations of channels (logic OR) that provide a trigger whenever the input crosses the threshold. This *Self-trigger* mode cannot be used at 5 GHz due to the high trigger latency. Similarly, *Global trigger* mode introduces an additional latency, making it not recommended also at 2.5 GHz. Refer to Sec. **9.9.4** for additional details.

The module features the front panel CLK IN/CLK OUT connectors and an internal PLL for clock synthesis from internal/external references. V1742 supports multi-board synchronization allowing all DRS4s to be synchronized with a common clock source and ensuring Trigger Time Stamps alignment. Once synchronized, all data will be aligned and coherent across multiple V1742 boards.

By ordering options (see **Tab. 1.1**), the module is available with digital memory sizes of 128 event/ch or 1024 event/ch.

[1] Designed at Paul Scherrer Institute (PSI). Detailed documentation of the DRS4 chip is available at http://drs.web.psi.ch/

The VME interface of the module is VME64X compliant, and the data readout can be performed in several data transfer modes: BLT32, MBLT64 (up to 70 MB/s of transfer rate using CAEN Bridge), CBLT32/64, 2eVME, 2eSST (up to 200 MB/s of transfer rate). The built-in daisy chainable Optical Link, implementing CONET proprietary protocol, is able to transfer data at 80 MB/s, thus it is possible to connect up to 8 boards to a single A4818 Adapter, or up to 32 to a single A5818 Controller (4-link version, see **Tab. 1.1**).

Board Models	Description
V1742	32+2 Ch. 12 bit 5 GS/s Switched-Capacitor Digitizer: 128 events/ch (1kS/events), EP3C16, SE
V1742B	32+2 Ch. 12 bit 5 GS/s Switched-Capacitor Digitizer: 1024 events/ch (1kS/events), EP3C16, SE
VX1742	32+2 Ch. 12 bit 5 GS/s Switched-Capacitor Digitizer: 128 events/ch (1kS/events), EP3C16, SE
VX1742B	32+2 Ch. 12 bit 5 GS/s Switched-Capacitor Digitizer: 1024 events/ch (1kS/events), EP3C16, SE
Personalizations	**Description**
VPERS1742	x742 Customization with 2 V_{pp} Input Range
Related Products	**Description**
A4818	A4818 – USB-3.0 to Optical Link
A5818	A5818 - PCIe 4 Optical Link, Gen. 3
V3718	V3718 – VME to USB2/CONET Bridge
VX3718	VX3718 – VME to USB2/CONET Bridge
V4718	V4718 – VME to USB 3.0/Ethernet/CONET Bridge
VX4718	VX4718 – VME to USB 3.0/Ethernet/CONET Bridge
VME8004B	VME8004B - 2U 4 Slot VME64 Mini Crate
VME8004X	VME8004X - 2U 4 Slot VME64X Mini Crate
VME8008B	VME8008B - 4U 8 Slot VME64 Mini Crate
VME8008X	VME8008X - 4U 8 Slot VME64X Mini Crate
VME8010	VME8010 - 7U 21 Slot VME64 Low Cost Crate
VME8011	VME8011 - 7U 21 Slot VME64 Low Cost Crate, pluggable power supply
VME8100	VME8100 - 8U 21 Slot VME64/64X Enhanced Crate Series
VME8200	VME8200 - 9U 21 Slot VME64X Enhanced Crate series
µ-Crate	µ-Crate - Desktop single-slot VME64X Crate
NV8020A	NV8020A - U CRATE VME/NIM 8 slot VME64 365W, 5 slot NIM 150W
Accessories	**Description**
A316	A316 - Cable assembly 2.54mm 2-pin header female - 5 cm
A317	A317 - Cable assembly for Clock distribution 3-pin AMPMODU IV female terminations - 18 cm
A317L	A317L - Cable assembly for Clock distribution 3-pin AMPMODU IV female terminations - 25 cm
DT4700	Clock Generator and FAN-OUT
A318	Adapter for Clock signal FISCHER S101A004 male to 3-pin AMPMODU IV female - 10 cm
A654	Cable assembly LEMO 00 male to MCX male – 1 m
A654 KIT4	4 Cable assembly LEMO 00 male to MCX male - 1 m
A654 KIT8	8 Cable assembly LEMO 00 male to MCX male - 1 m
A659	Cable assembly BNC male to MCX male – 1 m
A659 KIT4	4 MCX TO BNC Cable Adapter
A659 KIT8	8 MCX TO BNC Cable Adapter
A952	A952 - Cable assembly 2.54mm 34 pin female to 2.54mm 34 pin female - 50 cm
A953	A953 - Cable assembly 2.54mm 34 pin female to two 2.54mm 34 pin female - 50 cm
A954	A954 - Cable assembly 2.54mm 34 pin female to two 2.54mm 16 pin female - 50 cm
AI2740	Optical Fibre 40 m simplex
AI2730	Optical Fibre 30 m simplex
AI2720	Optical Fibre 20 m simplex
AI2705	Optical Fibre 5 m simplex
AI2703	Optical Fibre 30 cm simplex

AY2730	Optical Fibre 30 m duplex
AY2720	Optical Fibre 20 m duplex
AY2705	Optical Fibre 5 m duplex (Rohs compliant)

Tab. 1.1: Table of models and related items

2 Block Diagram

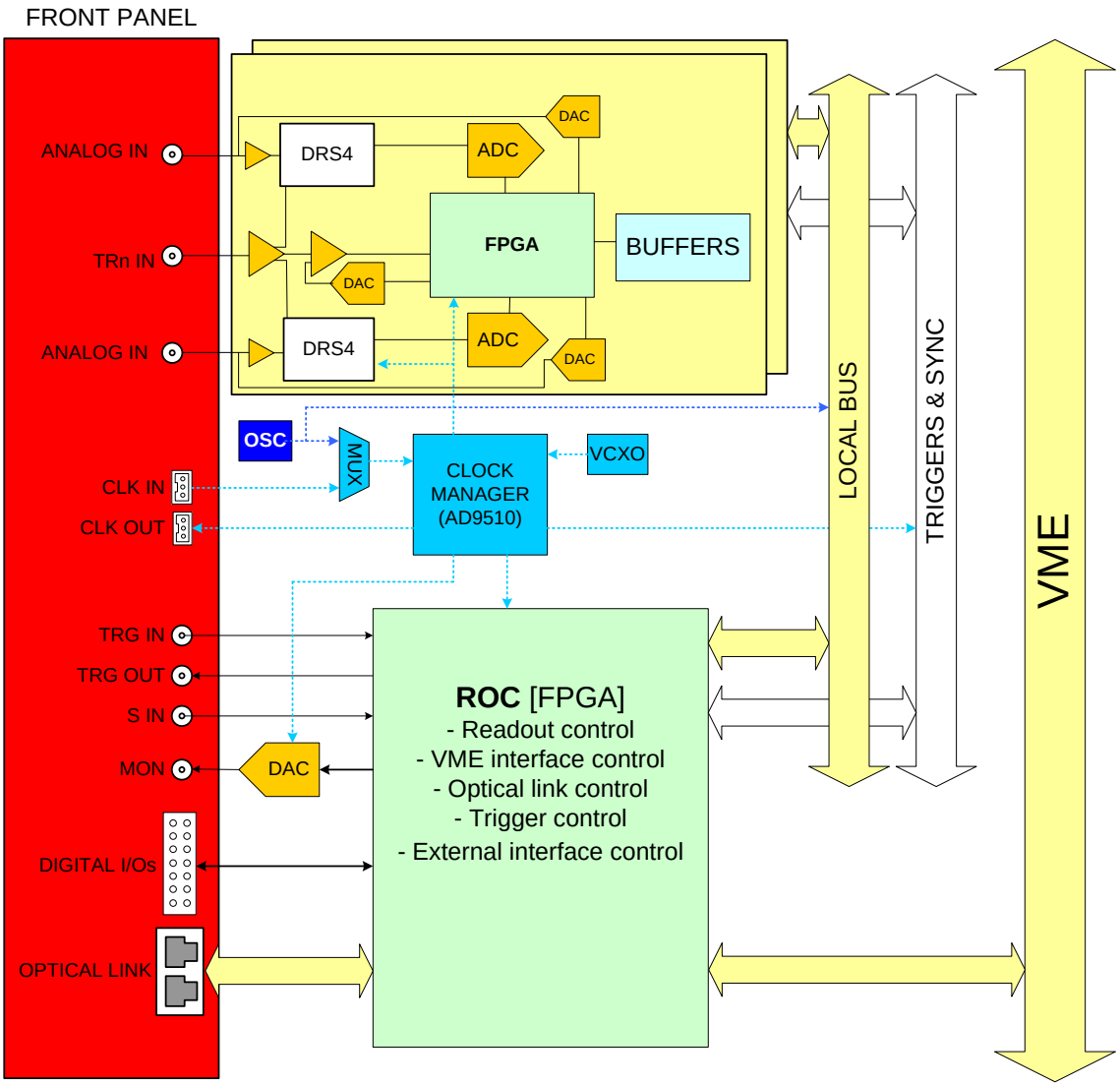


Fig. 2.1: Block Diagram

3 Technical Specifications

ANALOG INPUTS	**Number of Channels** 32 channels 2 special channels (TR0, TR1) Single ended **Full Scale Range (FSR)** 1 V_{pp} (default) 2 V_{pp} (by customization) **Absolute Max Analog Input Voltage (for any DAC Offset)** @1V_{pp} = 3 V_{pp} (with V_{rail} max +3V or -3V) @2V_{pp} = 6 V_{pp} (with V_{rail} max +6V or -6V)	**Impedance** Z_{in} = 50 Ω **DC Offset** Programmable 16-bit DAC for DC offset adjustment on each channel. Range: ± 1 V	**Connector** MCX **Bandwidth** 500 MHz
DIGITAL CONVERSION	**Resolution** 12 bits **Switched Capacitor Array** Domino Ring Sampler chip (DRS4), 8+1 channels with 1024 storage cells each	**Sampling Rate** 5 GS/s - 2.5 GS/s - 1 GS/s - 0.75 GS/s SW selectable, simultaneously on each channel	**Dead Time (A/D Conversion)** 110 µs, analog inputs only 181 µs, digitizing TR0 and TR1
FPGA	Altera Cyclone EP3C16 (one FPGA manages 16+1 channels)		
TRIGGER	**Trigger Source** - *Fast* (Low Latency) *trigger*: Programmable threshold on TR0 and TR1 (each TRn signal drives two 8-ch groups) - *Self-trigger*: Logic OR combination of channels over/under threshold (each channel self-trigger drives two 8-ch groups, or all 8-ch groups in case of *Global trigger* mode) - *External-trigger*: Common trigger by TRG-IN connector - *Software-trigger*: Common trigger by software command		**Trigger Propagation** TRG-OUT programmable digital output **Trigger Time Stamp** 30-bit counter (extendable to 60-bit by sw) 8.5 ns resolution 9 s range Timer reset by S-IN
ACQUISITION MEMORY	128 events/ch or 1024 events/ch (1024 S/event) Multi-event Buffer Independent read and write access; programmable event size and pre/post-trigger		
ADC CLOCK GENERATION	Clock source: internal/external. On-board programmable PLL provides generation of the main board clocks from internal (50 MHz local Oscillator) or external (front panel CLK-IN connector) reference		

DIGITAL I/O	**CLK-IN (AMP Modu II)** AC coupled differential input clock LVDS, ECL, PECL, LVPECL, CML (single ended NIM/TTL available by A318 adapter) accuracy < 100 ppm requested **CLK-OUT (AMP Modu II)** DC coupled differential LVDS clock output locked at ADC sampling clock	**TRG-IN (LEMO)** External trigger digital input NIM/TTL Signal Width > 17 ns Z_{in} = 50 Ω **TRG-OUT (LEMO)** Trigger digital output NIM/TTL Z_{in} = 50 Ω	**S-IN (LEMO)** SYNC/START front panel digital input NIM/TTL Signal Width > 17 ns Z_{in} = 50 Ω **LVDS I/O** 16 general purpose LVDS I/O controlled by the FPGA: Busy, Data Ready, Memory full, Individual Trig-Out and other functions can be programmed. An Input Pattern from the LVDS I/O can be associated to each trigger as an event marker
SYNCHRONIZATION	**Clock Propagation** *Daisy chain*: through CLK-IN/CLK-OUT connectors *One-to-many*: clock distribution from an external clock source to CLK-IN connector Clock Cable delay compensation	**Acquisition Synchronization** Sync, Start/Stop through digital I/Os (S-IN or TRG-IN input / TRG-OUT output) **Trigger Time Stamps Aligment** By S-IN input connector **Data Aligment** Busy/Veto management through digital I/Os (TRG-OUT/TRG-IN) or LVDS I/Os	
COMMUNICATION INTERFACES	**Optical Link** CAEN CONET proprietary protocol Up to 80 MB/s transfer rate Daisy-chain capability	**VME** VME 64X compliant Data transfer mode: BLT32, MBLT64 (70 MB/s by CAEN Bridge), CBLT32/64, 2eVME, 2eSST (200 MB/s)	
FIRMWARE	**Waveform Recording Firmware** Free firmware for waveform recording	**Upgrades** Supported via VMEbus/Optical Link	
SOFTWARE	**Readout SW** *WaveDump* readout software with C source files and VS project for developers (Windows® , Linux®)	**Libraries and Tools** General purpose C libraries with readout demos (Windows® , Linux® , and LabVIEW™ support) and configuration tools	
MECHANICAL	**Form Factor** 1-unit wide VME64/VME64X boards	**Weight** 520 g	**Dimension** 6U x 160 mm
ENVIRONMENTAL	**Environment:** Indoor use **Operating Temperature:** 0°C to +40°C **Storage Temperature:** –10°C to +60°C **Operating Humidity:** 10% to 90% RH non condensing **Storage Humidity:** 5% to 90% RH non condensing **Altitude:** < 2000m **Pollution Degree:** 2 **Overvoltage Category:** II **EMC Environment:** Commercial and light industrial **IP Degree:** IPX0 Enclosure, not for wet location		
REGULATORY COMPLIANCE	**EMC** CE 2014/30/EU Electromagnetic compatibility Directive	**Safety** CE 2014/35/EU Low Voltage Directive	
POWER REQUIREMENTS	5.5 A @ +5V 85 mA @ +12V		

Tab. 3.1: Specification table

4 Packaging and Compliancy

The V1742/VX1742 digitizer modules are available in 1-unit wide VME64/VME64X boards, EMC compliant.

The devices are inspected by CAEN before the shipment, and they are guaranteed to leave the factory free of mechanical or electrical defects.

The content of the delivered package standardly consists of the part list shown in the table below (**Tab. 4.1**).

	Part	Description	Qt
	V1742/VX1742	32+2 Channel 12 bit 5 GS/s Switched Capacitor Digitizer	x1
	Documentation	UM4279 - V1742/VX1742 User Manual	-

Tab. 4.1: Delivered kit content

CAUTION: to manage the product, consult the operating instructions provided.

When receiving the unit, the user is strictly recommended to:

- Inspect containers for damage during shipment. Report any damage to the freight carrier for possible insurance claims.
- Check that all the components received match those listed on the enclosed packing list as in **Tab. 4.1** . (CAEN cannot accept responsibility for missing items unless any discrepancy is promptly notified.)
- Open shipping containers; be careful not to damage contents.
- Inspect contents and report any damage. The inspection should confirm that there is no exterior damage to the unit such as broken knobs or connectors and that the front panel is not scratched or cracked. Keep all packing material until the inspection has been completed.
- If damage is detected, file a claim with carrier immediately and notify CAEN service (see Chap. **17**).
- If equipment must be returned, carefully repack equipment in the original shipping container with original packing materials, if possible. Please contact CAEN service.
- If equipment is not installed when unpacked, place equipment in original shipping container and store in a safe place until ready to install.

DO NOT SUBJECT THE ITEM TO UNDUE SHOCK OF VIBRATIONS

DO NOT BUMP, DROP OR SLIDE SHIPPING CONTAINERS

DO NOT LEAVE ITEMS OR SHIPPING CONTAINERS UNSUPERVISED IN AREAS WHERE UNTRAINED PERSONNEL MAY MISHANDLE THE ITEMS

USE ONLY ACCESSORIES WICH MEET THE MANUFACTURER SPECIFICATIONS

For a correct and safe use of the module, refer to Chap. **6** and **7**.

5 PID (Product Identifier)

PID is the CAEN product identifier, an incremental number greater than 10000 that is unique for each product[1]. The PID is on a label affixed to the product (Fig. 5.2) and it is even stored in an on-board non-volatile memory readable at bits [7:0] of registers 0xF080 or 0xF084 **[RD1]**. The PID information is also available through CAENToolbox Software (for more details refer to **[RD2]**).

Note: The serial number is still valid to identify older boards, where the PID label is not present.

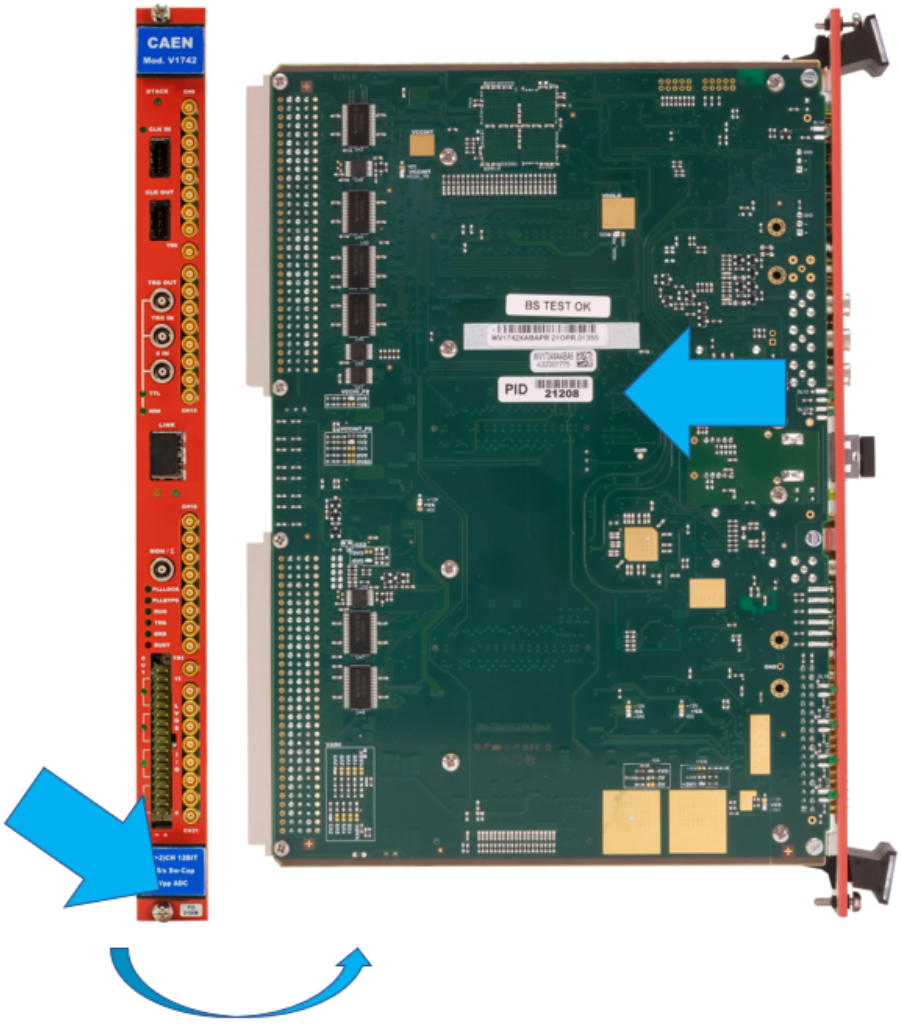


Fig. 5.1: PID location on V1742 (the number in the picture is purely indicative)

[1]The PID substitutes the serial number previously identifying the boards.

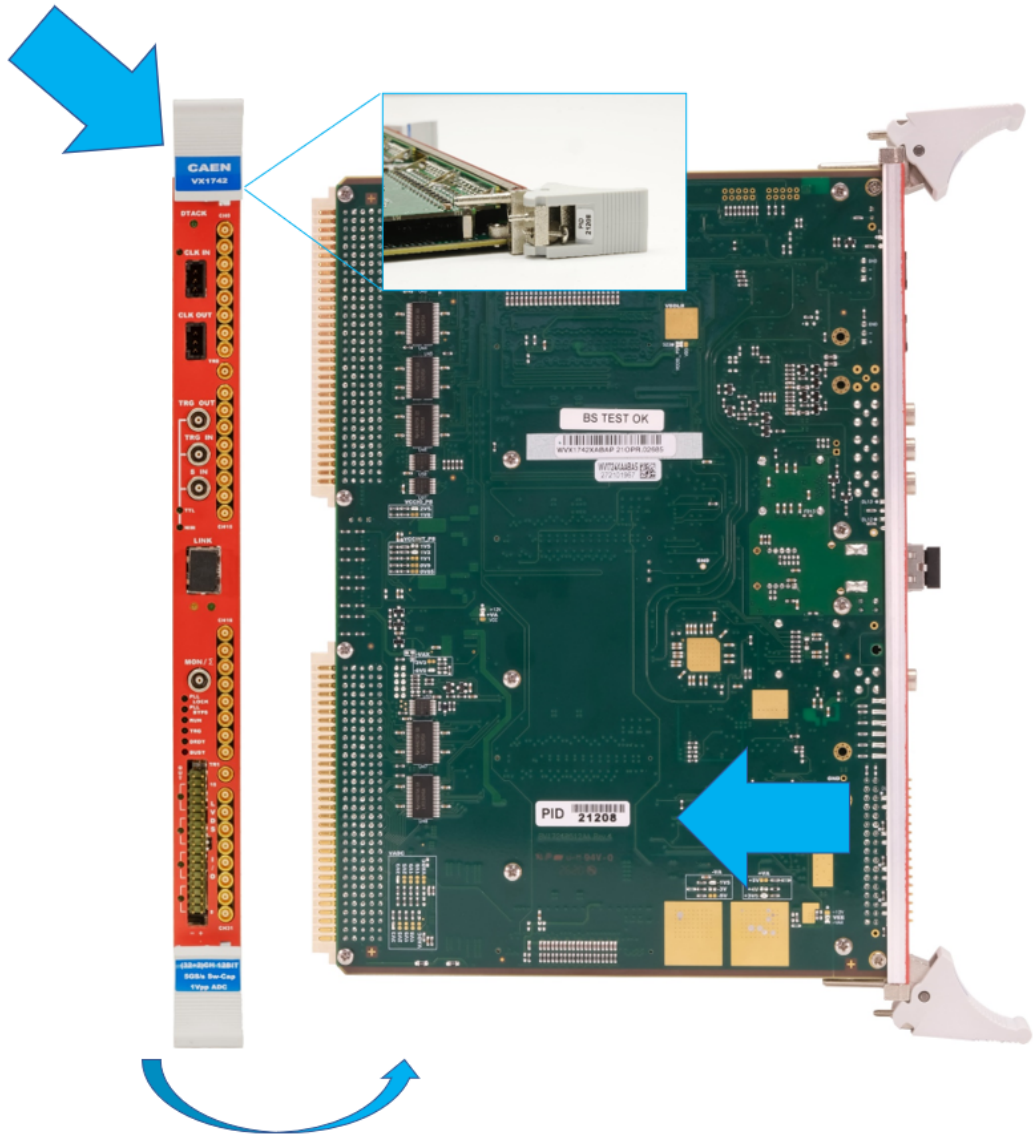


Fig. 5.2: PID location on VX1742 (the number in the picture is purely indicative)

6 Power Requirements

The table below resumes the V1742/VX1742 power consumptions per relevant power supply voltage.

MODULE	SUPPLY VOLTAGE	
	+5 V	+12 V
V1742/VX1742	5.5 A	85 mA
V1742B/VX1742B	5.5 A	85 mA

Tab. 6.1: Power requirements table

Note: The declared values are measured in standard operating conditions. In general, they could be subject to slight changes due to the firmware type, the firmware version, and the operating mode.

Note: The reported power requirements may be different depending on the motherboard revision numbers, which could be read at 0xF04C register. Please, contact CAEN for old power consumption specifications.

7 Cooling Management

The V1742/VX1742 Digitizers can operate in the temperature range 0° ÷ +40°C **[RD3]**.

The VME models must be operated in ventilated crates as recommended in the **Safety Notices**.

EXTERNAL FANS MUST BE USED WHEN THE BOARD IS INSTALLED IN A SETUP WITH POOR AIR FLOW

V1742 DIGITIZERS CANNOT BE OPERATED WITH CAEN CRATES VME8001, VME8002, VME8004, AND VME8004A. OVERHEAT MAY DAMAGE THE MODULE

The User must take care to provide a proper cooling to the board with external fan if the board is used in an enclosure or if the board is installed in a setup with poor air flow.
Excessive temperature will, in first instance, reduce the performance and the quality of the measurements and can also damage the board.

If the board is stored in cold environment, please check for water condensation before power on.

7.1 Cleaning Air Vents

CAEN recommends to occasionally clean the air vents on all vented sides of the board or crate, if present. Lint, dust, and other foreign matter can block the vents and limit the airflow. Be sure to power off the board and disconnect it from the power by physically detach the power chord before cleaning the air vents and follow the general cleaning safety precautions.

IT IS UNDER THE RESPONSIBILITY OF THE CUSTOMER A NON-COMPLIANT USE OF THE PRODUCT

8 Panels Description

V1742 and VX1742 present the same front panel structure.

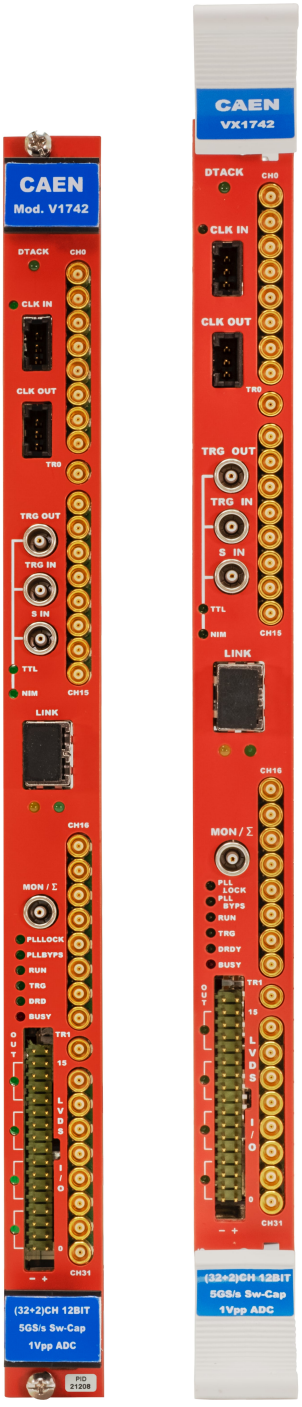


Fig. 8.1: Front panels view: V1742 on the left, VX1742 on the right

8.1 Front Panel

ANALOG INPUT

DESCRIPTION
Analog input connectors.

FUNCTION
CH[i] (i = 0 to 31) receives signals from the detector.
TR[i] (i = 0 to 1) receives the fast (low latency) trigger, that can possibly be digitized.

ELECTRICAL SPECS
Input dynamics:

- 1 V_{pp} (deafult) or 2 V_{pp}(by customization) for CH0-CH31;
- 2 V_{pp} for TR0 and TR1 (PCB Rev $\geq$ 1);
- 3 V_{pp} for TR0 and TR1 (PCB Rev = 0)

Input impedance (Z_{in}): 50 Ω.
Absolute max analog input voltage (for any DAC offset in the single-ended configuration):

- 3 V_{pp} (with Vrail max +3 V or -3 V) for 1V_{pp} FSR
- 6 V_{pp} (with Vrail max +6 V or -6 V) for 2V_{pp} FSR

MECHANICAL SPECS
Series: MCX connectors.
Type: CS 85MCX-50-0-16 (jack/female).
Manufacturer: SUHNER
Suggested plug/male: MCX-50-2-16.
Suggested cable: RG174 type.

CLOCK INPUT/CLOCK OUTPUT

DESCRIPTION
Input and output clock connectors.

FUNCTION
CLK-IN accepts an external reference clock.
CLK-OUT propagates the clock externally.
CLK-IN and CLK-OUT can be used to daisy chain the clock in multi-board synchronization (A317 distribution cable available: see **Tab. 1.1**)

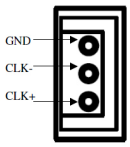
ELECTRICAL SPECS
Signal Level:
differential LVDS, ECL, PECL, LVPECL, CML.
Single-ended-to-differential A318 cable adapter available for CLK-IN (see **Tab. 1.1**).
Coupling:

- AC (CLK-IN);
- DC (CLK-OUT).

Z_{diff}: 100 Ω.
Accuracy < 100 ppm.

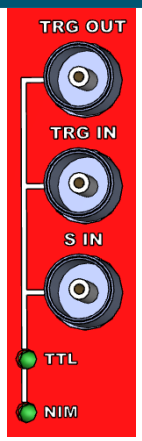
MECHANICAL SPECS
Series: AMPMODU connectors.
Type: 3-102203-4 (3-pin).
Manufacturer: AMP Inc.

PINOUT



CLK-IN LED (GREEN): indicates that the external clock is enabled.

TRIGGER INPUT/TRIGGER OUTPUT/SYNC INPUT



DESCRIPTION
General purpose digital I/O connectors.

FUNCTION

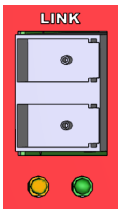
- TRG-OUT: optionally provides out:
  - probes from the mezzanines;
  - S-IN signal.
  - OR of the over-threshold signals from enabled channels
- TRG-IN: external trigger input.
- S-IN: SYNC/START/STOP configurable input as reset of the time stamp (**Sec. 9.13.3**) or as acquisition start/stop (**Sec. 9.8.1**).

ELECTRICAL SPECS
Signal Level: single-ended NIM/TTL, SW selectable.
TRG-IN/S-IN input Signal Width:
> 17 ns (2 Trigger Clocks).
TRG-IN/S-IN input impedance (Z_{in}): 50 Ω
TRG-OUT requires 50 Ω termination.

MECHANICAL SPECS
Series: 101 A 004 connectors.
Type: DLP 101 A 004-28.
Manufacturer: FISCHER.
Alternatively:
Type: EPL 00 250 NTN.
Manufacturer: LEMO.

TTL (GREEN), NIM (GREEN): indicates the standard TTL or NIM set for TRG-OUT, TRG-IN, and S-IN.

OPTICAL LINK PORT



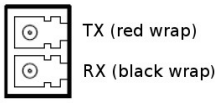
DESCRIPTION
Optical link port.

FUNCTION
Data readout and flow control through optical link. Daisy chainable. Compliant with optical fibers 50/125 µm OM2 and OM3 (back-compliant with 62.5/125 µm OM1) featuring LC connectors on both sides.

ELECTRICAL SPECS
Transfer rate: up to 80 MB/s.

MECHANICAL SPECS
Series: SFF Transceivers.
Type: FTLF8519F-2KNL (LC connectors).
Manufacturer: FINISAR.

PINOUT



LINK LEDs (GREEN/YELOW): right LED (GREEN) indicates the network presence, while left LED (YELLOW) indicates the data transfer activity

ANALOG MONITOR

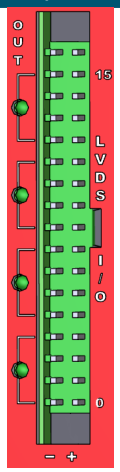
DESCRIPTION
Analog Monitor LEMO connector

FUNCTION
(not used)

DIAGNOSTIC LEDs

DTACK (GREEN): indicates there is a VME read/write access to the board;
PLL LOCK (GREEN): indicates the PLL is locked to the reference clock;
PLL BYPS (GREEN): *not used*;
RUN (GREEN): indicates the acquisition is running (data taking);
TRG (GREEN): indicates the trigger is accepted;
DRDY (GREEN): indicates the event/data is present in the Output Buffer;
BUSY (RED): indicates the board is either in Dead Time condition during the analog-to-digital conversion or that all the buffers are full for at least one channel.

LVDS I/O CONNECTOR



DESCRIPTION
General purpose 16-pin LVDS I/O connector.

FUNCTION
Programmable general purpose LVDS I/O signals organized in 4 independent signal groups: 0÷3; 4÷7; 8÷11; 12÷15.
In/Out direction is software controlled.
Different selectable modes (see **Sec. 9.11**):

- Register
- Trigger
- nBusy/nVeto
- Legacy

ELECTRICAL SPECS
Level: differential LVDS
Z_{diff}: 100 Ω

MECHANICAL SPECS
Series : TE - AMPMODU Mod II Series
Type: 5-826634-0 (lead spacing: 2.54 mm; row pitch: 2.54 mm)
Manufacturer: AMP Inc.

LVDS I/O LEDs (GREEN): Each LED close to a 4-pin group lights on if the pins are set as outputs.

IDENTIFICATION LABELS

On top and bottom of insertion/extraction handle:

- Manufacturer
- Model name
- Brief ADC features

On the bottom (V1742) or on the HANDLE (VX1742):

- Product Identifier (PID)

Note: For older boards, a 4-digit Serial Number (S/N) is reported on a little serigraph on the bottom of the VME board's front panel.

8.2 Internal Components

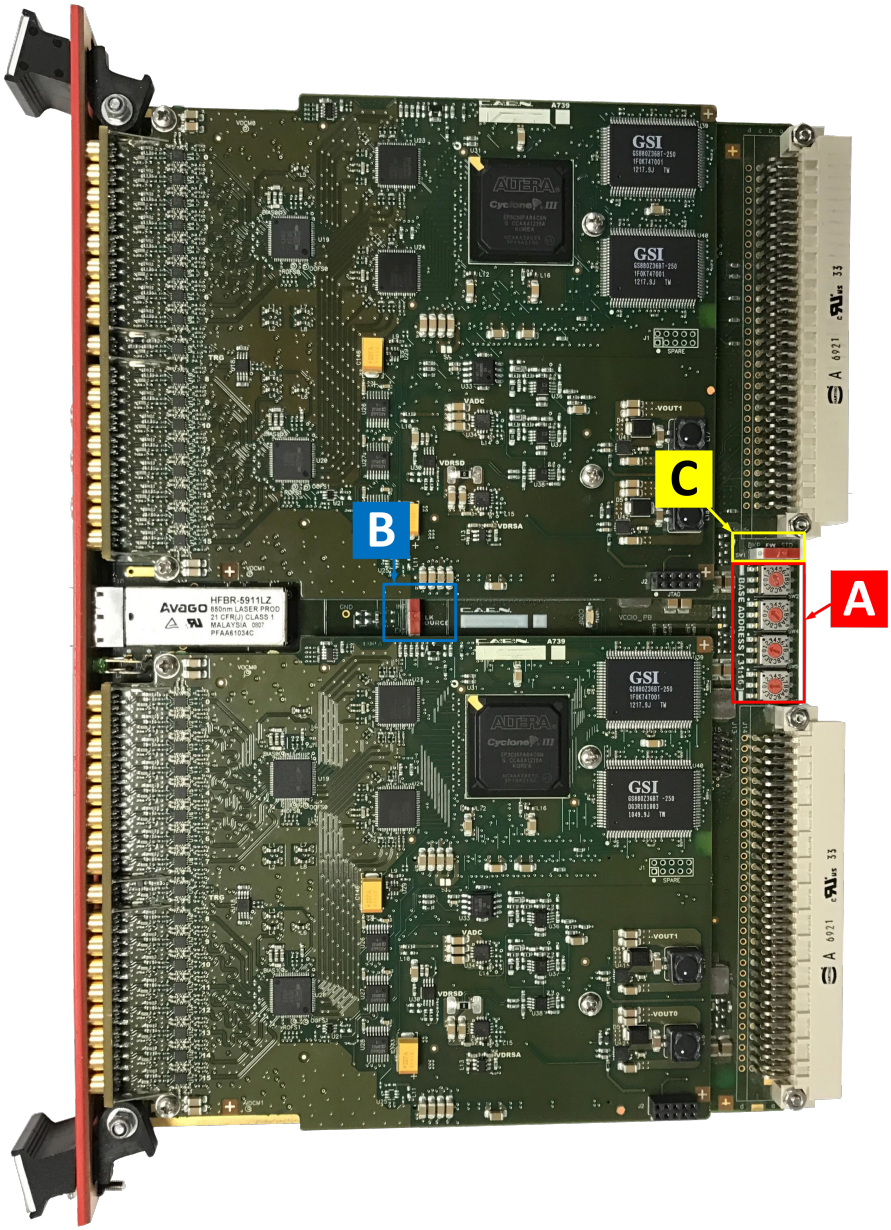


Fig. 8.2: Rotary and dip switches location

A	**SW3, 4, 5, 6**: **"Base Address [31:16]"**	**Type**: Rotary Switches	**Function**: Set the VME Base Address of the module
B	**SW2**: **"CLOCK SOURCE" INT/EXT**	**Type**: Dip Switch	**Function**: Selects the clock source (External or Internal)
C	**SW7**: **"FW" BKP/STD**	**Type**: Dip Switch	**Function**: Selects between the "Standard" (STD) and the "Backup" (BKP) FLASH page as the first to be read at power-on to load the FW on the FPGAs (default position is STD); see Sec. **13.1**

9 Functional Description

9.1 Analog Input Stage

The default input dynamic is 1 V_{pp} on the single-ended MCX coaxial connectors (Z_{in} = 50 Ω). In order to preserve the full dynamic range according to the polarity of the input signal (bipolar, positive unipolar, negative unipolar), it is possible to add a DC offset by means of a 16-bit DAC, which is up to ± 1 V DC. The input bandwidth ranges from DC to 500 MHz (with 2^{nd} order linear phase anti-aliasing low-pass filter).
A customization with input range of 2 V_{pp} is available, with unchanged values for input impedance and bandwidth, and DC Offset range.

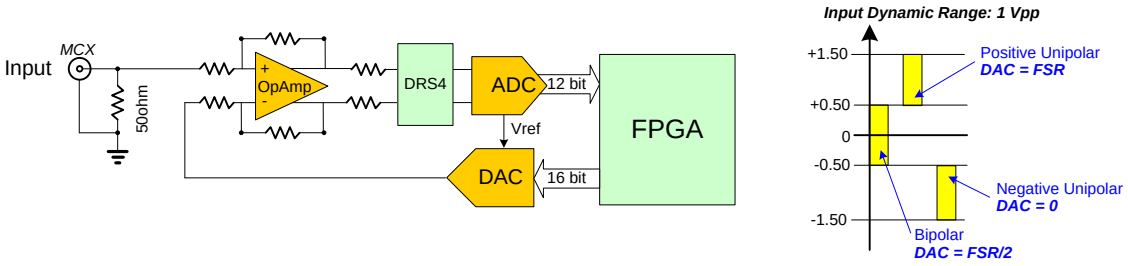


Fig. 9.1: Analog input diagram

9.1.1 DC Offset Setting

The DC Offset can optionally be set as common for a 8-channel group of the digitizer, or as individual for the 8 channels inside a group. In both cases, this can be done either by a direct write at 0x1n98 register addresses (or 0x8098 for common setting) **[RD1]**, or by library function (CAENDigitizerLib -> SetChannelDCOffset) **[RD4]**, or in the WaveDump readout software **[RD5]**.

9.1.2 Additional Input

An additional channel is available on the TRn connector. The TRn can act as a fast trigger (refer to Sec. **9.3** and **9.9.3**) and it can also be digitized and saved into memory. The TRn appears as the ninth channel of each group in the final readout. The TRn input dynamics is 2 V_{pp} for Mezzanine PCB revision ≥ 1, and 3 V_{pp} for Mezzanine PCB revision = 0[1]. The input dynamics is then attenuated by a factor of 2 (3 in the latter case) to make it compliant with the 1 V_{pp} dynamics of the other channels. The 16-bit DAC then allows the user to adjust the DC Offset making the TRn suitable for positive and negative unipolar signals. The DC Offset of the TRn input can be set either by writing at register address 0x1nDC **[RD1]**, or by library function (CAENDigitizerLib -> SetGroupFastTriggerDCOffset) **[RD4]**, or in the readout software **[RD5]**.

[1] To check the PCB revision number, read bit[9] of register 0x1n88 **[RD1]**

9.2 Domino Ring Sampling

The analog input signals are continuously sampled by the DRS4 (Domino Ring Sampler) chip[2] which consists of an on-chip inverter chain (domino wave circuit) generating a maximum of 5 GS/s sampling frequency; 2.5 GS/s, 1 GS/s, and 750 MS/s frequencies can be also programmed. The board has one chip per group, and each chip consists of 1024 capacitor cells per channel, which perform the analog sampling of the input (high frequency analog sampling). The record length of the acquisition is constrained by the cell number, and it is fixed to 1024 samples. Options 512, 256, and 136 can be selected by software to reduce the amount of data to be transferred, but all the 1024 cells are converted anyway (no dead-time reduction).

The DRS4 chip continuously samples the input in a circular way (samples are overwritten) until a trigger signal stops its acquisition (holding phase). Then the cells release their capacitances at a readout frequency controlled by the FPGA (Output Mode).

The analog samples are digitized by the 12-bit ADC at a frequency of 29.296 MHz (low frequency digital sampling). The ADC output is stored by the FPGA into the Digital Memory Buffer and data is then available for readout (for the data format refer to Sec. **9.8.2**).

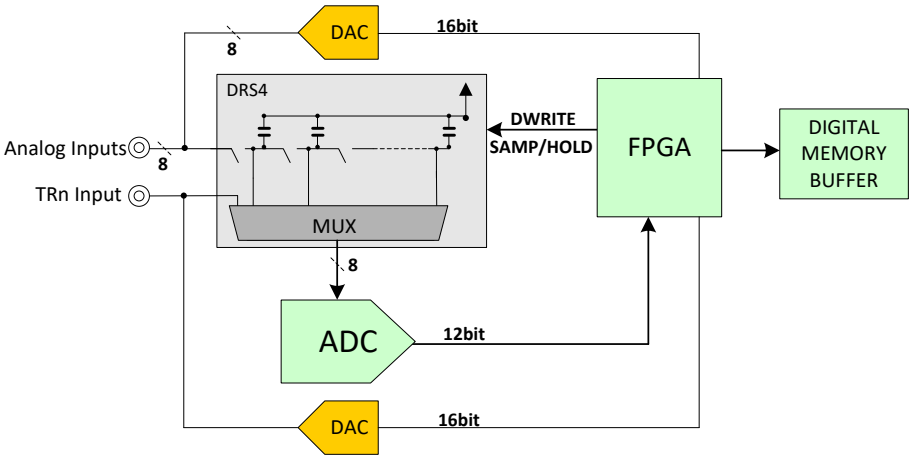


Fig. 9.2: Input Diagram

The single TRn is split into the two DRS4 chips (see also Sec. **9.3**). Delay lines are equal in the two paths, anyway small differences in the digitized samples are possible due to differences in the chips and in the ADCs. When the digitization of the TRn is enabled, there is a double conversion that increases the dead-time from 110 µs, when only the inputs are converted, to 181 µs when also the TRn are converted.

[2] Detailed documentation of the DRS4 is available at http://drs.web.psi.ch/

9.3 TR0 and TR1 Inputs

The module features two fast trigger inputs TR0 and TR1 with extended level amplitude (NIM/LVTTL compliant); TR0 is common to group 0 (ch[7..0]) and group 1 (ch[15..8]), TR1 to group 2 (ch[23..16]) and group 3 (ch[31..24]). TRn signal can be used as external trigger (see Sec. **9.9**). Moreover, they can be also sampled into the DRS4s analog memory buffers for applications where high resolution timing and time analysis with a common reference signal (like a trigger or system clock) is required; this is achieved by setting bit[11]=1 at 0x8000 **[RD1]**.

> **IMPORTANT**: The TRn input is attenuated by a factor of 2 (PCB revision ≥ 1), or 3 (PCB revision 0) to make it compliant with the 1 V_{pp} dynamics of the DRS4 chip. For signals higher than 2 V_{pp} (3 V_{pp}) it is recommended to use an external attenuator.

To properly handle bipolar signals and also unipolar positive or negative signal, a 16-bit DAC allows the user to add a DC offset to TRn; offset value can be programmed via register 0x1nDC.

When the TRn signals are used as triggers they are processed by an internal comparator, whose threshold can be programmed via register 0x1nD4: when the TRn crosses the threshold, the FPGA stops the DRS4 acquisition and controls the sample digitalization. Examples of TRn DC Offset and Threshold are reported in Sec. **9.9.3**

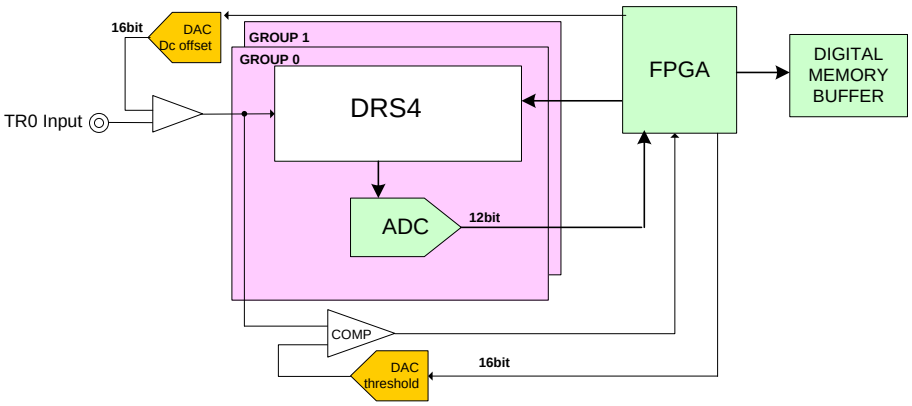


Fig. 9.3: TR0 logic block diagram

9.4 Clock Distribution

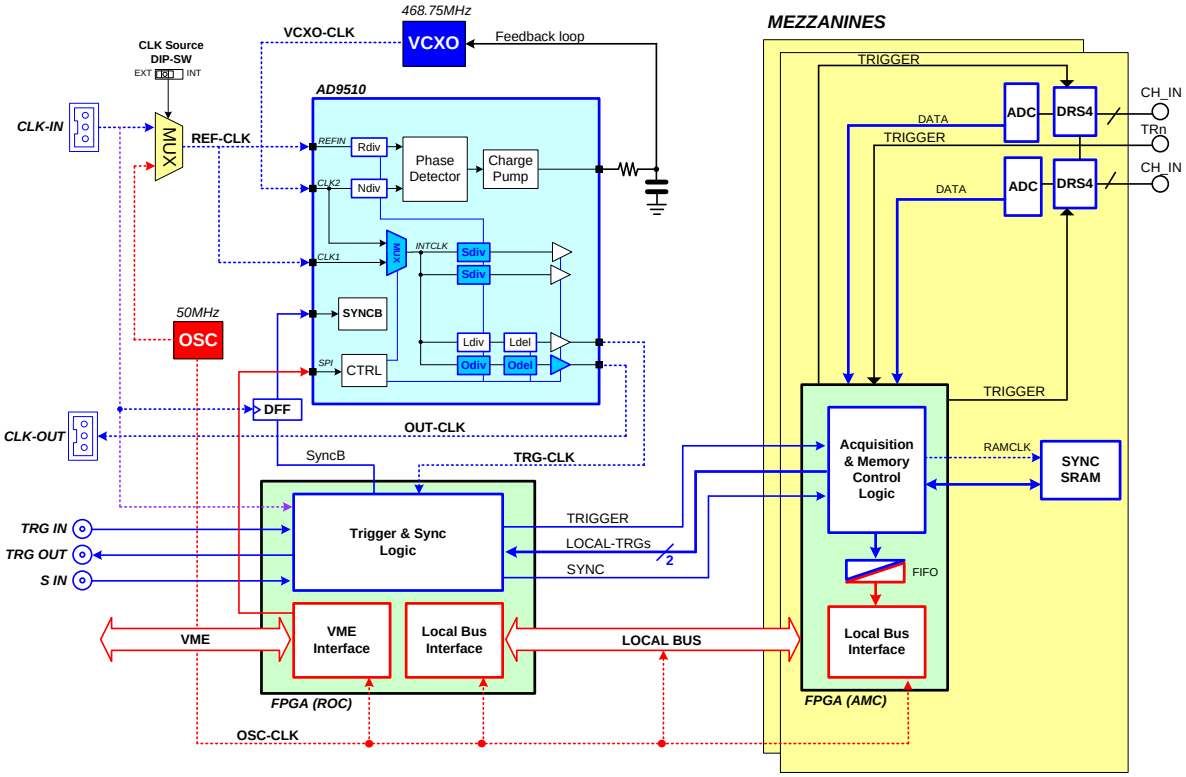


Fig. 9.4: Clock distribution diagram

The clock distribution of the module takes place on two domains: OSC-CLK and REF-CLK.

OSC-CLK is a fixed 50-MHz clock provided by a local oscillator which handles both VME and Local Bus (communication between motherboard and mezzanine boards; see red traces in the above figure).

REF-CLK handles ADC sampling, trigger logic, acquisition logic (samples storage into RAM, buffer freezing on trigger) through a clock chain. REF-CLK can be either an external (via front panel signal on CLK-IN connector) or an internal (via local oscillator) source. In the latter case, OSC-CLK and REF-CLK will be synchronous (the operating mode remains the same anyway).

REF-CLK clock source selection can be done by setting SW2 on-board switch (see Sec. **8.2**):

- INT mode (default) means that REF-CLK is the 50 MHz of the local oscillator (REF-CLK = OSC-CLK);
- EXT mode means that REF-CLK is the external frequency fed on CLK-IN connector.

CLK-IN signal must be differential (LVDS, ECL, PECL, LVPECL, CML) with a jitter lower than 100 ppm. CAEN provides the A318 cable to adapt single-ended signals coming from an external clock unit into the differential CLK-IN connector.

The board mounts a phase-locked-loop (PLL) and clock distribution device, AD9510. It receives the REF-CLK (internal 50 MHz by default) and generates the sampling clock for ADCs and the mezzanine FPGA (SAMPCLK0 and SAMPCLK1), as well as the trigger logic synchronization clock (TRG-CLK) and the output clock (CLK-OUT).

Refer to the AD9510 datasheet for more details:
https://www.analog.com/media/en/technical-documentation/data-sheets/AD9510.pdf
(in case the active link above does not work, copy and paste it on the internet browser)

9.5 PLL Mode

As introduced in Sec. **9.4**, the source of the REF-CLK signal (see **Fig. 9.4**) can be external on CLK-IN front panel connector or internal from the 50 MHz local oscillator. Selecting the REF-CLK source internal or external can be performed by acting on the on-board dip switch SW2 (see Sec. **8.2**). Selecting the external clock source, the CLK-IN front panel LED must be on (see Sec. **8.1**).

The following options are allowed:

1. 50 MHz internal clock source – This is the standard operating mode, where the default AD9510 configuration does not require to be changed: OSC-CLK = REF-CLK.

Note: The ClkOut frequency is a submultiple of the VCXO frequency. With a 50 MHz internal or external clock source, the ClkOut presents a frequency of 58.594 MHz.

2. 50 MHz external clock source – This external frequency does not require any change of the AD9510 configuration: CLK-IN = REF-CLK.

Note: It is not advisable to connect in FAN-IN an external clock source of 50 MHz to multiple boards. With this configuration, the boards will be PLL locked, but not synchronized, resulting in possible data misalignment.

3. 58.594 MHz external clock source – In this case, the user is required to program the AD9510 dividers to lock the VCXO to REF-CLK: CLK-IN = REF-CLK.
   Please contact CAEN to receive the PLL programming file (Chap. **17**).
4. External clock source different from 58.594 MHz – In this case, the AD9510 dividers must be reprogrammed to lock the VCXO to REF-CLK: CLK-IN = REF-CLK.
   In principle, the allowed external frequencies are submultiples of the VCXO frequency (468.75 MHz).
   Please contact CAEN indicating the required reference clock frequency to check the feasibility and receive the PLL programming file (Chap. **17**).

If the digitizer is locked, the PLL-LOCK front panel LED must be on (see Sec. **8.1**).

Note: the user can configure the clock parameters, generate the PLL programming file and load it on the board by using the CAEN Toolbox software (see **11**).

9.6 Output Clock

The AD9510 output can be available on the front panel CLK-OUT connector (see Chap. **8**). This option is particularly used in case of multi-board synchronization to propagate the clock reference source in Daisy Chain between boards using the A317 clock distributor cable (see **1.1**). (see Sec. **9.10**).

This option can be enabled by the user while configuring the PLL programming file in the CAEN Toolbox software (see **11**).

9.7 Data Correction

The DRS4 chip needs data corrections due to the unavoidable differences in the chip construction process. The corrections are managed at software level, while the firmware on-board retrieves the raw data. There are three available corrections:

1. **Cell Index Offset correction**, which compensates the signal offset for the differences in cell amplitudes;
2. **Sample Index Offset correction**, which corrects the signal offset for a noise over the last 30 samples;
3. **Time correction**, which compensates the differences of the delay line of the chips.

The default correction tables are provided by CAEN in the memory flash of the board. WaveDump software **[RD5]** (and the underlying CAENDigitizer library **[RD4]**) then can retrieve the tables and make the appropriate corrections.

The user can leave the software automatically apply all the corrections, or decide which correction applies to which group through the CORRECTION_LEVEL function of WaveDump.

If the user wants to apply its own corrections, he/she can use the CAENDigitizer function GetCorrectionTable **[RD4]** to retrieve the default correction files from the board and modify them with his/her own values.

The list of CAENDigitizer functions to be used on-line are:

- **LoadDRS4CorrectionData**, loads the correction parameters stored on board. The correction parameters to load depend on the operating sampling frequency.
- **DecodeEvent**, decode the event and apply the correction to data if LoadDRS4CorrectionData has been previously called.
- **Enable/Disable DRS4Correction**, enables/disables the data correction in the x742 series. When enabled, the data correction through the DecodeEvent function only applies if LoadDRS4CorrectionData has been previously called, otherwise the DecodeEvent runs the same, but data will be provided out not compensated.
- **GetCorrectionTables**, reads the correction tables from the x742 digitizer flash memory, related to the selected sampling frequency, and fills in a structure with the read values. In this way, the stored correction table become available for the user.

Finally, it is also possible to save the raw data and apply the corrections off-line. An example code is available in the CAENDigitizer library. To access the code, download and install the CAENDigitizer library (the prior installation of CAENVMELib **[RD6]** and CAENComm library **[RD7]** are required) and include the examples in the installation. Then access to the subfolder called ”x742_DataCorrection”:

C:/Program Files/CAEN/Digitizers/Library/Samples/x742_DataCorrection

Here the list of CAENDigitizer functions **[RD4]** to be used off-line:

- **LoadCorrectionTables**, loads the correction tables stored onto the board into a user defined structure.
- **ApplyDataCorrection**, applies the desired correction data (configured through a mask) to the raw data acquired by the user.
- **GetNumEvents**, gets the current number of events stored in the acquisition buffer.
- **GetEventPtr**, retrieves the event pointer of a specified event in the acquisition buffer.
- **X742_DecodeEvent**, decodes a specified event stored in the acquisition buffer writing data in Evt memory.

9.7.1 Cell Index Offset Correction

The analog capacitors of the DRS4 chip might have small differences between each other due to the construction processes. According to the cell index where the stop acquisition arrives, the same input signal can be reconstructed in different ways. For this reason, it is required a cell amplitude calibration to compensate for the amplitude differences in the capacitors. The correction adjusts the baseline of the input (i.e. its offset).

Taking into account the internal noise of each channel, **Fig. 9.5** shows the sampled waveform on the left and the noise distribution histogram on the right, measured as the occurrence of the ADC counts. Plots are made before the correction. **Fig. 9.6** shows the same quantities after the correction. As expected, the noise in **Fig. 9.6** is flatter with no patterns, and its distribution has a smaller RMS.

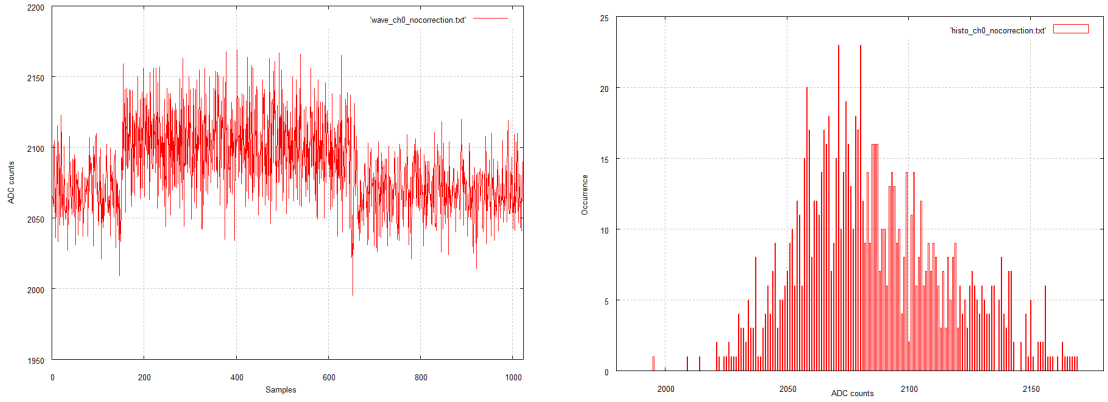


Fig. 9.5: Sampled waveform (left) and noise histogram (right) before cell index offset correction

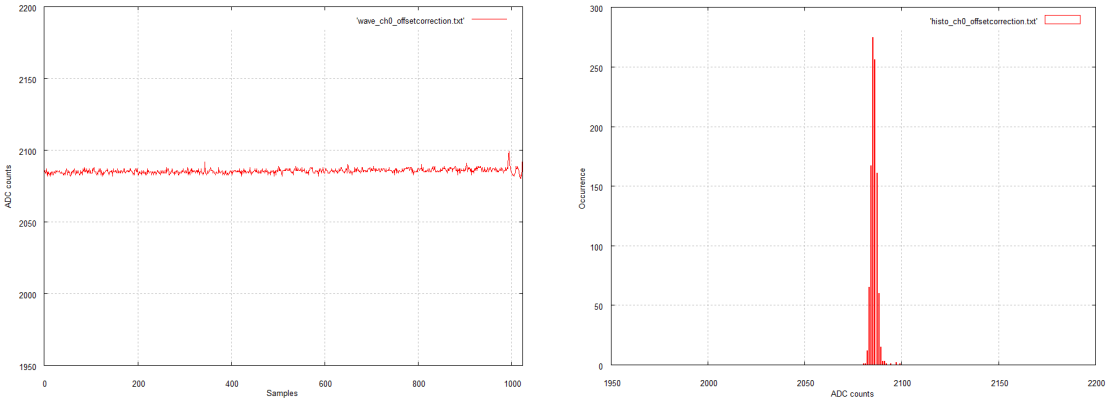


Fig. 9.6: Sampled waveform (left) and noise histogram (right) after cell index offset correction

9.7.2 Sample Index Offset Correction

From **Fig. 9.6** it is possible to see a fixed pattern over the last about 30 samples of the waveform. Therefore, it is required to perform an additional calibration, called ”Sample Index”, that corrects for the latest samples.

Fig. 9.7 shows the result on the baseline after the correction, where the pattern on the latest samples has been corrected.

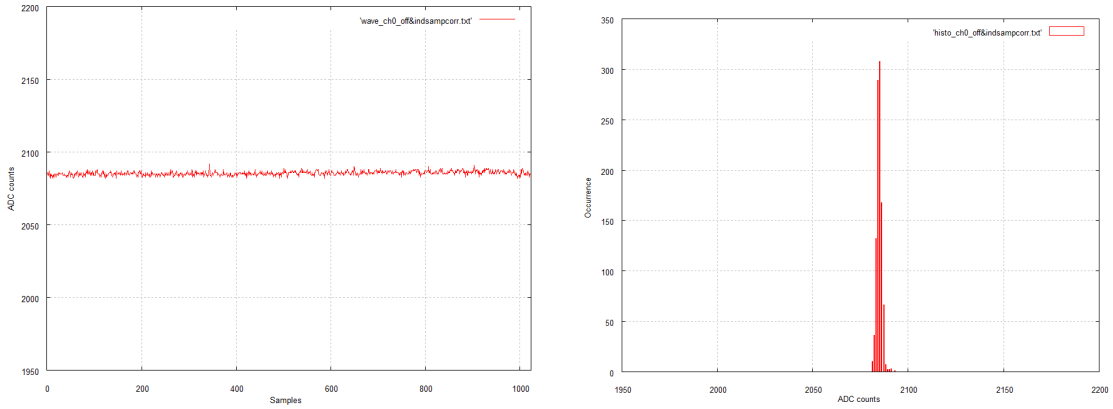


Fig. 9.7: Sampled waveform (left) and noise histogram (right) after sample index offset correction

9.7.3 Time Correction

The sampling sequence is handled by multiple DRS4 (one for each group of 8 channels) through 1024 physical delay lines each; the unavoidable construction differences between such delay lines and among the different DRS4 chips must be compensated through a time calibration.
The time corrections provided by CAEN are made by means of a very precise external clock sampled by the TRn channel, i.e. by the DRS4 chip of Group 0 (GR0) and by the DRS4 chip of Group 1 (GR1) (see for example **Fig. 9.8**), and analogously TR1 for Group 2 (GR2), and Group 3 (GR3). The correction is made by supposing that the ideal sampling frequency is 200 ps (@ 5 GSps) and measuring how far is the voltage from the ideal voltage value at 200 ps.

Note: The time correction is an indirect measurement, the final information provided by the chip is a voltage, not a time.

All the contributions from the cells are summed in Integral Non-Linearity (INL) plots and the resulting trend is quite a sinusoidal shape for all chips (see **Fig. 9.10**). The final corrections are made by sampling thousands of times the square pulse and correcting at every cycle the cells by reporting the expected value of the voltage.

As mentioned, this method is an indirect method, and the final result can suffer from many contributions, like the intrinsic jitter of the pulse generator, the uncertainty of the edge shape of the pulse, the point where it is sampled, the approximation of the voltage value, etc. The sum of these factors gives a non-zero residual, as shown in **Fig. 9.11**. Due to the above factors, each board will show a different residual contribution.

Fig. 9.8 and **Fig. 9.9** show the fast trigger signal (TR0) sampled by the DRS4 chip related to GR0 and GR1, before and after the time correction respectively [3]. High discrepancies can be seen before the correction, while the differences after the correction are extremely reduced.

The corresponding INL plots are reported in **Fig. 9.10** and **Fig. 9.11** before and after the correction respectively. As expected, the INL shows a better agreement after the correction, with a reduction factor higher than x10 of the maximum time delay among cells. As mentioned, each board could have a different INL residual curve, anyway this general trend is expected for all boards.

[3] The figures, representing a single measurement performed on an individual module, have been chosen among others to highlight the efficiency of the time correction. Values could be different for each board.

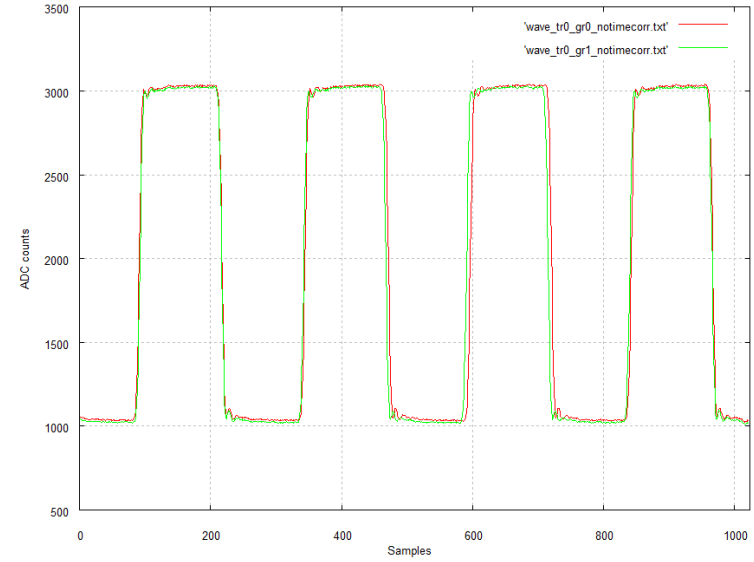


Fig. 9.8: Sampled TR0 signal in DRS4 chip for GR0 and GR1 before time correction

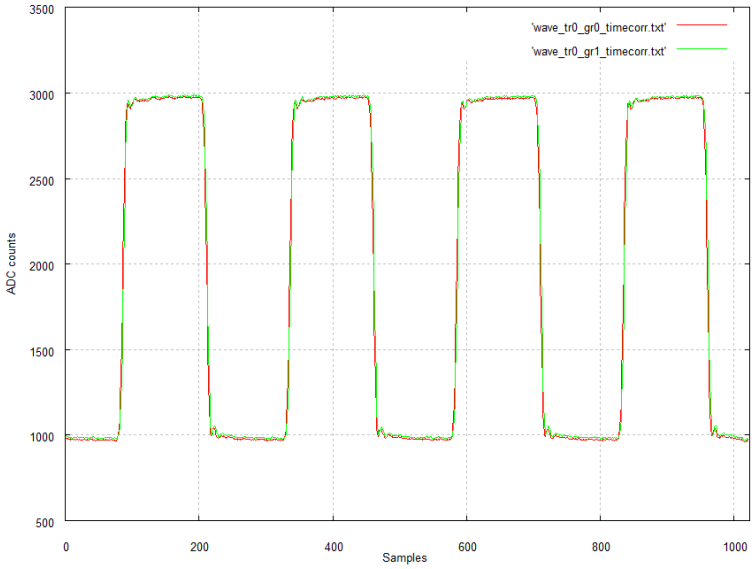


Fig. 9.9: Sampled TR0 signal in DRS4 chips for GR0 and GR1 after time correction

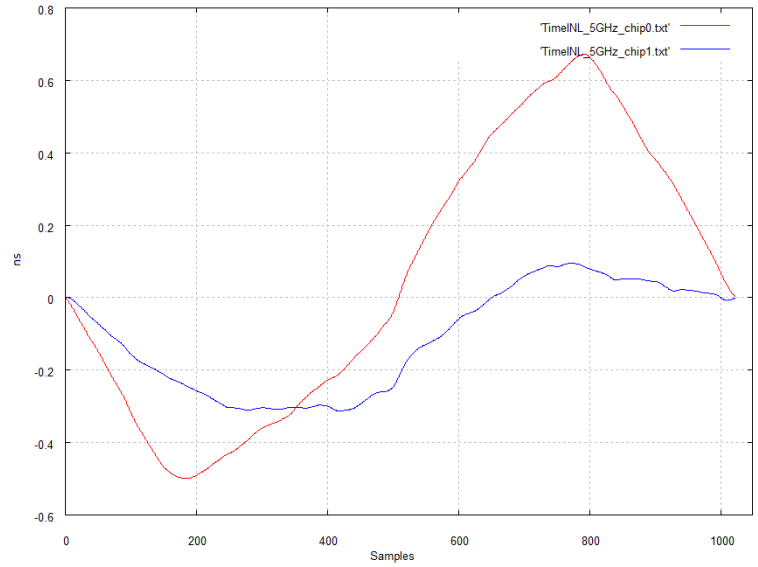


Fig. 9.10: INL time profile of DRS4 chips for GR0 and GR1 before time correction

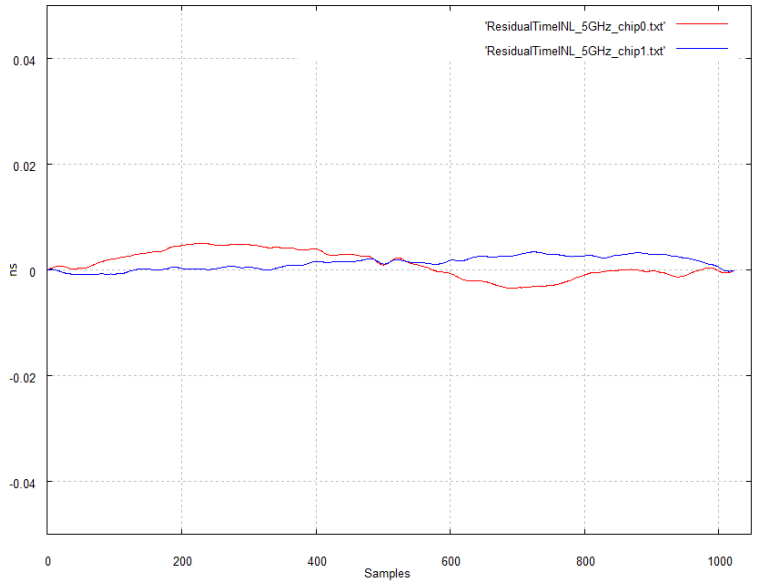


Fig. 9.11: INL time profile of DRS4 chips for GR0 and GR1 after time correction

9.8 Acquisition Modes

9.8.1 Acquisition Run/Stop

The acquisition can be started and stopped in different ways, according to bit[2:0] of 0x8100 register:

- SW CONTROLLED (bits[1:0] = 00): Start and Stop take place by software command. Bit[2] = 0 means stopped, while bit[2] = 1 means running.
- S-IN CONTROLLED (bits[1:0] = 01): acquisition is armed by setting bit[2] = 1, then two options are selectable through bit[11]:
  - START/STOP ON LEVEL - If bit[11] = 0, then acquisition starts when the S-IN signal is high and stops when it is low; if bit[2] = 0 (disarmed), the acquisition is always off.
  - START ON EDGE - If bit[11] = 1, then acquisition starts on the rising edge of the S-IN signal and must be stopped by software command (bit[2] = 0).
- FIRST TRIGGER CONTROLLED (bits[1:0] = 10): bit[2] = 1 arms the acquisition and the Start is issued on the first trigger pulse (rising edge) on the TRG-IN connector. This pulse is not used as a trigger; actual triggers start from the second pulse on TRG-IN. The Stop acquisition must be SW controlled (bit[2] is reset). For debugging purposes, the Start of the acquisition can be given also by Software Trigger.
- LVDS I/Os CONTROLLED: this mode acts like the S-IN CONTROLLED (bits[1:0] = 01), but using the configurable features of the signals on the LVDS I/Os connector (see Sec. **9.11**).

9.8.2 Event Structure

The event can be read out via VMEbus or Optical Link; data format is 32-bit long word (see **Fig. 9.12**).

An event is structured as:

- **Header** (four 32-bit words)
- **Data** (variable size and format)

The Header is composed by four words, namely:

- **TOTAL EVENT SIZE** (bit[27:0] of 1^{st} header word) is the total size of the event, i.e. the number of 32-bit long words to be read;
- **BOARD ID** (bit[31:27] of 2^{nd} header word) is the GEO address, meaningful for VME64X modules;
- **BOARD FAIL FLAG** (bit[26] of 2^{nd} header word), implemented from ROC FPGA firmware revision 4.5 on (reserved otherwise), is set to "1" in consequence of a hardware problem (e.g. PLL unlocking or over-temperature condition). The user can collect more information about the failure by reading at 0x8178 register address and contact CAEN Support Service if necessary (see Chap. **17**);
- **PATTERN** (bit[23:8] 2^{nd} header word) is the 16-bit PATTERN latched on the LVDS I/Os as the trigger arrives (VME boards only).
- **GROUP MASK** (bit[3:0] of the 2^{nd} header word) is the mask of the groups participating in the event (e.g. GROUP 0 and GROUP 3 participating → Group Mask = 1001). This information must be used by the software to retrieve to which groups the samples belong.
- **EVENT COUNTER** (bit[23:0] of 3^{rd} header word) is the trigger counter;
- **EVENT TIME TAG** (4^{th} header word) is a 31-bit counter for the event time tag (bit[30:0]) plus the overflow bit (bit[31]) indicating that the timestamp counter has overflowed at least once; the counter is reset when the acquisition starts or by an external signal (see Sec. **9.13.3**) and it is incremented at each trigger clock hit.

IMPORTANT NOTE: this time tag corresponds to the time when the event is created in the digitizer memory (so related to the readout), while is not related to the time when the event occurred at the group (i.e. channel) level, so it does not correspond to any physical quantity. **The physical time of arrival of the pulse can be read in the GROUP TRIGGER TIME TAG**.

After the header, the data from the enabled groups is reported consecutively. The group data format for group 0 is reported in **Fig. 9.13**.

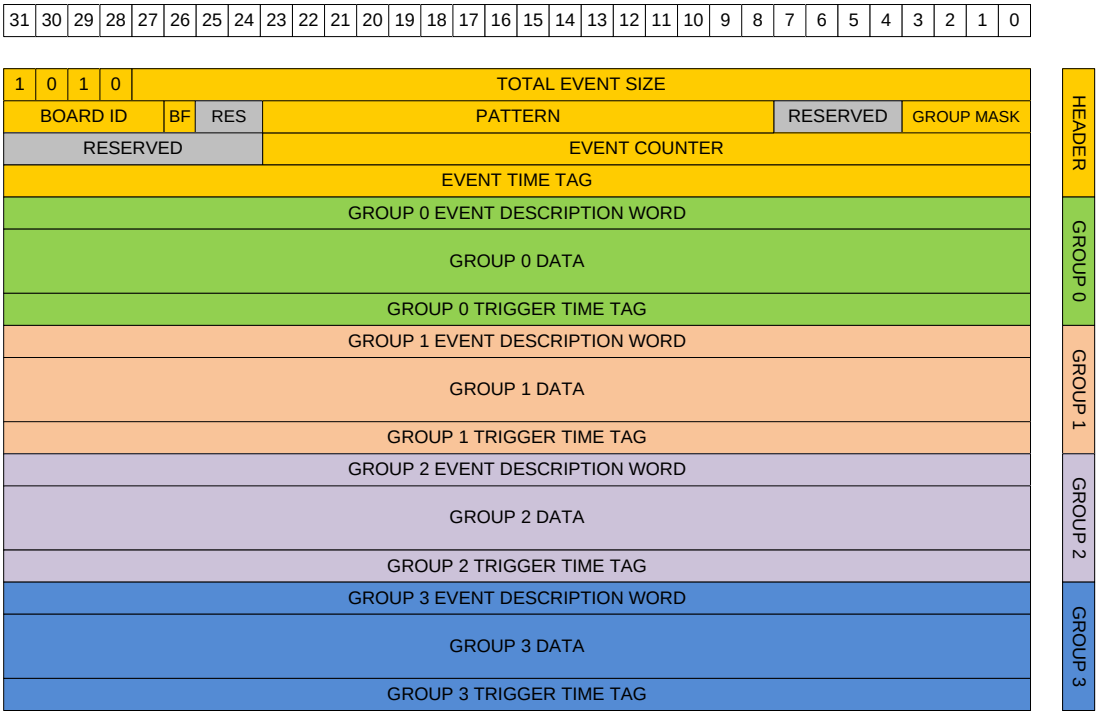


Fig. 9.12: Event Format

Each group is composed by 8 channels (GROUP 0 = CHANNEL 0 – 7, GROUP 1 = CHANNEL 8 – 15, etc.) and by the special channel TRn: such signal is common to two groups; it can be used as Local Trigger or "digitized" and stored with the data for high resolution timing analysis between the ADC channels and the TRn itself (refer to Sec. **9.3**).

Note: TR0 (TR1) is split into the two DRS4 chips of the mezzanine and follows two different path (two different ADCs and two memory buffers). This might imply that the digitized samples of TRn might have small differences from one group to the other.

TR0 can trigger both GROUP 0 and GROUP 1 and it is stored in both group data (referring to **Fig. 9.13** the label $TR0_0$ indicates that the TR0 is saved into GROUP 0).

In the **Group Event Description** word (yellow row in **Fig. 9.13**) the following fields are shown:

- **START INDEX CELL** (Bits[29:20]) is the index cell of the DRS4 chip, corresponding to the first sample of the event;
- **FREQ** (Bit[17:16]) is the sampling frequency of the DRS4 chip, whose options are:
  - 00 = 5 GS/s;
  - 01 = 2.5 GS/s;
  - 10 = 1 GS/s;

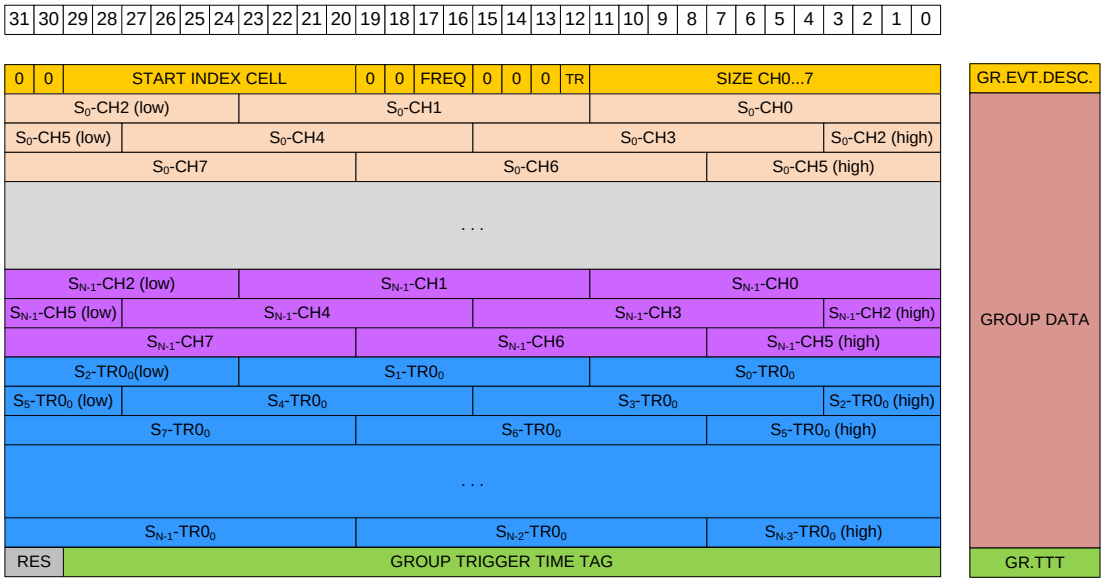


Fig. 9.13: Group Data Format

  - 11 = 750 MS/s.

- **TR** (Bit[12]) flag indicates whether the TRn has been digitized and it is available in the readout. Options are:
  - 0 = TRn signal not present in the readout;
  - 1 = TRn signal present in the readout.

- **SIZE CH0...7** (Bit[11:0]) is the number of words to be read for the CH0...7 samples. Considering that each channel has 1024 samples, and that one sample is written in three words, “SIZE CH0...7” is 0xC00.

The **GROUP DATA** corresponds to the waveform samples, where each sample is reported from the lowest channel index to the highest.

If the readout of TRn is disabled, data related to such channel (light blue in **Fig. 9.13**) are not present in the event; if readout of TRn is enabled, data size related to such channel is Size TRn = (SIZE CH0...7)/8. The

GROUP TRIGGER TIME TAG records the Trigger arrival time into a 30-bit number (steps of 8.5 ns). This is the physical trigger information of the event.
From revision number **1.06** of the mezzanine firmware (AMC FPGA), the option to extend the Group Trigger Time Tag on 60 bits is available (same 8.5ns resolution). The Extended Group Trigger Time Tag (EGTTT) must be enabled by bit[20] of register 0x8000 **[RD1]**. Then, the 60-bit value for GROUP 0-1 is given by (GROUP 1 TRIGGER TIME TAG) & (GROUP 0 TRIGGER TIME TAG), while the extended timestamp value for GROUP 2-3 is given by (GROUP 3 TRIGGER TIME TAG) & (GROUP 2 TRIGGER TIME TAG).

Note: Enabling only GROUP 0and/or GROUP 2, the timestamp actually remains at 30 bits even if the EGTTT is set. Instead, enabling only GROUP 1and/or GROUP 3, the EGTTT must not be set, as the resulting timestamp is inconsistent.

9.9 Trigger Management

Once a trigger condition is met, the DRS4 chip stops its sampling phase and the analog capacitances are converted (holding phase) by a 12-bit ADC. There are four possible trigger sources:

- **Software Trigger** (common to all enabled groups). The trigger is issued through a software write on the relevant FPGA register. This mode is mainly used for debugging purposes.
- **External Trigger** (trigger on TRG-IN connector, common to all enabled groups). The TRG-IN connector accepts NIM and TTL input logic, which can be programmed via software. More details are in Sec. **9.9.2**.
- **Fast (Low Latency) Local Trigger** (trigger on TR0 and TR1 connectors, common to couples of groups[4]). This mode is called "Fast" or "Low Latency" since the latency from the trigger arrival and the DRS4 stop acquisition is significantly reduced with respect to the External Trigger mode. See Sec. **9.9.3**.
- **Self-trigger** (common to couples of groups[5] or to all groups[6]), the acquisition is controlled by combinations in logic OR of the channel self-triggers. See Sec. **9.9.4**.

During the analog to digital conversion process, the board cannot handle other triggers. The corresponding dead-time is equal to 110 µs when only the inputs are digitized, and 181 µs when also the TRn are digitized.

Fig. 9.14 shows the block diagram of the 742 trigger management.

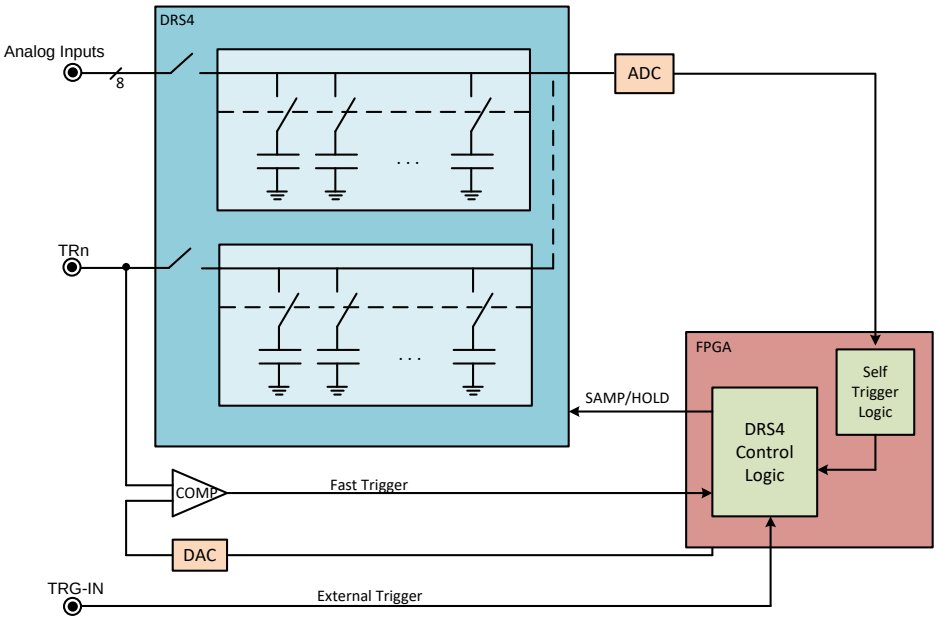


Fig. 9.14: Block diagram of Trigger management

[4] TR0 manages the acquisition of group 0 and group 1, while TR1 manages the acquisition of group 2 and group 3 (VME form factor only).

[5] The self-trigger of the channels belonging to group 0 and group 1 manages the acquisition of group 0 and group 1 simultaneously, while the self-trigger of the channels belonging to group 2 and group 3 (VME form factor only) controls the acquisition of group 2 and group 3 simultaneously. The two couples of groups (gr0/gr1, and gr2/gr3) can be considered independent.

[6] In *Global trigger* mode, the self-trigger signals from the enabled channels are sent to the motherboard, which then generates a global trigger for the entire board.

9.9.1 Software Trigger

Software triggers are internally produced via a software command (write access at 0x8108 register address) through VMEbus or Optical Link.

9.9.2 External Trigger

A TTL or NIM external signal can be provided in the front panel TRG-IN connector (configurable at 0x811C register address).

The TRG-IN signal is first processed by the mother board with a clock of about 58 MHz, and sent to the DRS4 to stop its acquisition with a latency of about 115 ns and a jitter of about 17 ns[7]. The latency of the external trigger makes this mode difficult to use at 5 GHz, where the maximum acquisition window is about 200 ns (1024 samples of 200 ps).

9.9.3 Fast ("Low Latency") Trigger

The trigger signal is fed into TR0 and TR1 connectors, and it is common to couples of groups[8]. The TRn connector accepts signals with maximum amplitude of 2 V_{pp} in case of Mezzanine PCB revision ≥ 1 (3 V_{pp} in case of Mezzanine PCB revision = 0)[9].

> **IMPORTANT**: The TRn input is attenuated by a factor of 2 (PCB revision ≥ 1), or 3 (PCB revision 0) to make it compliant with the 1 V_{pp} dynamics of the DRS4 chip. For signals higher than 2 V_{pp} (3 V_{pp}) it is recommended to use an external attenuator.

This mode is called "Fast" or "Low Latency" since the latency from the trigger arrival and the DRS4 holding phase is reduced to about 42 ns with a jitter of about 8.5 ns. The signal on TRn is sent to a comparator with programmable threshold (no mother-board processing) whose output is sampled at about 117 MHz (twice the external trigger processing). When the TRn signal crosses the threshold, the acquisition of the DRS4 chip is stopped and the digitalization process starts.
This trigger mode is convenient for high precision timing measurements, since the TRn can be digitized as the other analog inputs and reported in the output data as channel number 8 of each group. The trigger can therefore be used as a time reference for the input. The DRS4 sampling period becomes the time jitter of the trigger with respect to an input of the same group, which can reach 200 ps in case of sampling at 5 GHz. The resolution in a time of flight measurement reaches up to 50 ps in case of signals and TRn in the same TRn group, and 100 ps for signals and TRn in different groups.

Note: TR0 (TR1) is split into the two DRS4 of the mezzanine and follows two different path (two different ADCs and two memory buffers). This might imply that the digitized samples of TRn might have small differences from one group to the other.

TRn acting as input signal can manage several types of signal polarities (bi-polar, negative, and positive), thanks to the possibility to modify the DC Offset (i.e. the baseline position, or 0-Volt) and Trigger Threshold of the TRn itself. From **Fig. 9.3**, a fast analog comparator is available in the board to identify when the TRn crosses the threshold and to generate a trigger when the Low Latency trigger mode is enabled. The comparator has two inputs, one for TRn plus its DC Offset, the other for the Threshold. Both DC Offset and Threshold come from two 16-bit DACs, and their corresponding registers (addresses 0x1nDC (Bit[15:0]) and 0x1nD4 (Bit[15:0]), respectively **[RD1]**) must be written as 16-bit numbers.

[7] The TRG-IN latency has been reduced to 115 ns from ROC firmware revision 4.07, while for firmware revisions less than 4.07 the latency was 255 ns with a jitter of about 34 ns.
[8] TR0 manages the acquisition of group 0 and group 1, while TR1 manages the acquisition of group 2 and group 3.
[9] To check the PCB revision number, read bit[9] of 0x1n88 register **[RD1]**

Due to the real design complexity of the TRn input stage needed to fit its multiple functions (the schemes in this document are simplified), there is not a simple formula for setting the desired trigger Threshold value (even in mV) for different values of the DC Offset. For this reason, CAEN provides ready-to-use information: **Tab. 9.1** and **9.2** report the DC Offset and trigger Threshold values (hexadecimal / decimal) for typical signals that can be fed into the TRn connector, where the Threshold values are set at half of the signal height. This information can be used directly to set the involved registers **[RD1]** or the software parameters **[RD5][RD4]**. A practical example of setting the TR0 triggering mode in the CAEN WaveDump software is described in **[RD8]**.

Mezzanine PCB Rev. $\geq$ 1	
ECL signal on TRn	TRn DC Offset = 0x55A0 / 21920 TRn Threshold = 0x6666 / 26214
NIM signal on TRn	TRn DC Offset = 0x8000 / 32768 TRn Threshold = 0x51C6 / 20934
Negative signal on TRn: V = 0 ÷ -400mV	TRn DC Offset = 0x8000 / 32768 TRn Threshold = 0x5C16 / 23574
Negative signal on TRn: V = 0 ÷ -200mV	TRn DC Offset = 0x8000 / 32768 TRn Threshold = 0x613E / 24894
Bipolar signal on TRn	TRn DC Offset = 0x8000 / 32768 TRn Threshold = 0x6666 / 26214
TTL on TRn or Positive signal on TRn: V = 0 ÷ ≥ 2V	TRn DC Offset = 0xA800 / 43008 TRn Threshold = 0x6666 / 26214
Positive on TRn: V = 0 ÷ 2V	TRn DC Offset = 0x91A7 / 37287 TRn Threshold = 0x6666 / 26214

Tab. 9.1: Examples of DC Offset and Trigger Threshold (in hexadecimal / decimal) for typical signals on TRn connector. Values are valid for mezzanine PCB revision ≥ 1.

Mezzanine PCB Rev. 0	
NIM signal on TRn	TRn DC Offset = 0x1000 / 4096 TRn Threshold = 0x717D / 29053
Negative signal on TRn: V = 0 ÷ -400mV	TRn DC Offset = 0x1000 / 4096 TRn Threshold = 0x6E72 / 28274
Bipolar signal on TRn	TRn DC Offset = 0x1000 / 4096 TRn Threshold = 0x6C80 / 27776
Positive on TRn: V = 0 ÷ 2V	TRn DC Offset = 0x4000 / 16384 TRn Threshold = 0x7158 / 29016

Tab. 9.2: Examples of DC Offset and Trigger Threshold (in hexadecimal / decimal) for typical signals on TRn connector. Values are valid for mezzanine PCB revision 0.

For example, consider the case of a **NIM signal** (0, -800 mV), assuming to set the DC Offset at mid-scale and the Threshold at half of the amplitude of the TRn signal.

Considering the 16-bit DAC of the comparator, in order to set the 0-Volt of the TRn at mid-scale, the DC Offset parameter must be set to **0x8000** (i.e. the decimal value of **32768** = $(2^{16} - 1)/2$) on the 0x1nDC (Bit[15:0]) register. When the TRn is digitized by the 12-bit ADC (@ 5 GS/s like the other analog channels of the digitizer), the 16-bit DC Offset of TR0 is scaled into the 12-bit range of the ADC and a factor of 16 must be considered, so that the 32768 value should ideally turn into around 2048 ADC counts.
Concerning the Trigger Threshold, the half of the amplitude of the TRn signal corresponds to -400 mV with respect to the pulse 0-Volt.

The user must first consider that mid-scale of the ADC dynamics (that is 1 V in the [0:2] V range) corresponds to write 0x6666 in the Trigger Threshold DAC, that is (1 V/2.5 V)$\times 2^{16}$, where 2.5 V is the input dynamic of the fast comparator. For example, this is also the value written in **Tab. 9.1** and **9.2** for the bipolar signal.

With respect to the mid-scale value, moving the threshold by 1 mV implies setting a value of, ideally, 13.2 in the DAC. In order to set the threshold at -400 mV, the following calculation must be done: 400 $\times$ 13.2 = 5280, which corresponds to 0x14A0. The last step is to subtract from the mid-scale value the desired threshold value, in our example: 0x6666-0x14A0 = **0x51C6** (i.e. the decimal value of **20934**) is the Trigger Threshold to be set in the 0x1nD4 (Bit[15:0]) register.

9.9.4 Self-Trigger

The self-trigger mode is available on 742 series from AMC firmware revision 0.4. In self-trigger mode each channel can self-trigger on its own input – leading edge discrimination – and logic OR combinations of the self-triggers enable the groups to acquire at the same time. In particular, the self-trigger of the channels belonging to group 0 and group 1 manages the acquisition of group 0 and group 1 simultaneously, while the self-trigger of the channels belonging to group 2 and group 3 (VME form factor only) controls the acquisition of group 2 and group 3 simultaneously. The two couples of groups (gr0/gr1, and gr2/gr3) can be considered independent.

Starting from revision **4.30_1.08**, the self trigger signals from the enabled channels can be used to generate a global trigger for the entire board.

The DRS4 chip has two operating modes: “Transparent” and “Output”. In Transparent mode (see **Fig. 9.15**), the input pulse is both sampled by the DRS4 capacitors (analog sampling) at high frequency, and made available at the output for the ADC digital sampling at a smaller rate, about 30 MHz. In transparent mode, the output stage is not a pure differential, since it has an offset and it is attenuated with respect to the signal correctly shaped. Transparent mode is the standard operating mode of the DRS4 chip, which continuously samples the input.

In Output mode (see **Fig. 9.16**), the input is no longer sampled and the capacitors hold the acquired samples and send them one at a time to the ADC at a frequency controlled by the FPGA (readout frequency). The Output mode starts when a trigger condition is met (see **Fig. 9.14**). Samples in Output mode are those available in the readout for the user and they are correctly shaped.

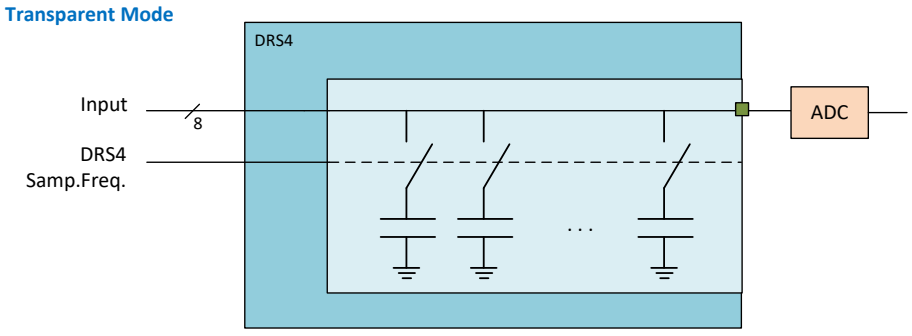


Fig. 9.15: Diagram showing the “Transparent Mode” functioning. The analog input is both sampled by the DRS4 capacitors (analog sampling) and made available at the output for the ADC digital sampling at a smaller rate. The output stage is distorted with respect to the Output mode.

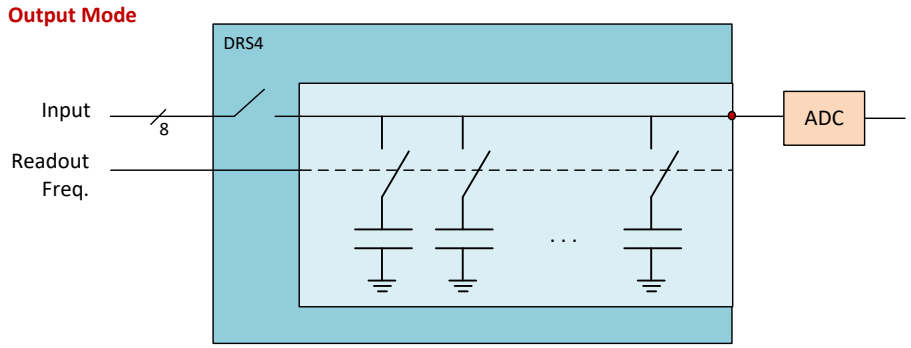


Fig. 9.16: Diagram showing the "Output Mode" functioning. the input is no longer sampled and the capacitors hold the acquired samples and send them one at a time to the ADC at a frequency controlled by the FPGA (readout frequency). The output stage is correctly differential.

Since the Self-Trigger Logic inside the FPGA reads data from the ADC while the DRS4 chip works in Transparent mode, the Trigger Threshold has to be referred to the values read in Transparent mode itself, rather to the values reported in Output mode.

To correctly set the threshold value, it is first required to make an acquisition in Transparent mode to visualize the waveform as sampled by the ADC.

Considering that the ADC frequency is about 30 MHz, it is important that the input can be sampled by the ADC itself. In particular, the pulse width should be greater than 30 ns, and the input frequency should be high enough to visualize some pulses.

IMPORTANT: In *Self-trigger* mode, the procedure of reading from the ADC and processing data by the FPGA introduces a latency of about 320 ns (with a jitter of 17 ns) before the DRS4 holding phase. This mode is therefore not compliant with the DRS4 frequency = 5 GHz, but it can be useful when the board works at 2.5 GS/s, 1 GS/s, or 750 MS/s.
In *Global trigger* mode, an additional latency of about 100 ns is introduced, making this mode not compliant with the DRS4 frequency = 5 GHz and 2.5 GHz, but it can be used when the board works at 1 GS/s, or 750 MS/s.

9.9.5 How to work with Self-Trigger

To work with the channel self-trigger feature, the board must be configured appropriately according to the following steps.

- Set the DC Offset of each channel (at least those which are required to acquire) to ensure that the entire input signal is within the input dynamics of the board. To verify this, it is suggested to make acquisitions in the standard mode ("Output Mode") using the SW trigger.
- Set the board to perform the acquisition in "Transparent Mode" (set bit[13] = 1 of 0x8000 register).
- Make acquisitions in "Transparent Mode" using the SW trigger. *No corrections are made in Transparent mode*. For each channel of interest, check the value of the signal in this acquisition mode and choose the threshold for triggering.
- Set the threshold value for each channel of interest via 0x1n80 register, where n is the group index.
- Enable the channels of interest to generate a Channel Trigger via 0x1nA8 register.
- Set the board to perform the acquisition in "Output Mode" (set back bit[13] = 0 of 0x8000 register).

The board is so ready to acquire data when triggers are generated by the channels.

Refer also to **[RD8]** for a practical example and **[RD1]** for the registers description.

9.9.5.1 Channel Self-Trigger to generate a Global Trigger for the entire board

Starting from revision **4.30_1.08**, self-trigger signals from enabled channels can be used to generate a global trigger for the entire board. Specifically, over-threshold signals from the selected groups are sent to the motherboard, where a logical OR is performed among them to generate a global trigger distributed to all groups.

To enable this trigger mode, after activating the self-trigger on the desired channels (see Sec. **9.9.5**), follow these three additional steps:

- set bit [21]=1 of register 0x8000: this disables automatic acquisition from channel with the self-trigger mode enabled.
- set bits[31:28]=0100 of register 0x8000: this routes ”over-threshold” signals to the motherboard.
- set the bits [4:0] of register 0x810C, according to the setup: where each bit represents a group (bit 0 is referred to group 0, bit[1] to group1 and so on...). This setting determines which groups are allowed to generate the global trigger.

Refer also to **[RD8]** for a practical example and **[RD1]** for the registers description.

9.10 Multi-board Synchronization

When multi-board systems are involved in an experiment, it is necessary to synchronize different boards. In this way, the user can acquire from N boards with Y channels each, like if they were just one board with (N x Y) channels.

While all the channels of the same board are simultaneously sampled at the same clock frequency by design, the main issue in the synchronization of a multi-board system is to have both the same ADC sampling clock and the same time reference for all boards. Clock synchronization is made through input/output daisy chain connections among the digitizers. One board must be chosen to be the “master” board, that works upon its internal 50-MHz oscillator, while a specific reference clock (58.594 MHz) is propagated through each other board in the chain, called ”slave”. A programmable phase shift can adjust possible delays in the clock propagation. This allows the boards to have both the same ADC sampling clock and the same time reference. Having the same time reference means that the acquisition starts/stops at the same time and that the time stamps of different boards are aligned to the same absolute time.

The user must then take care of the proper run and trigger propagation to all boards. When operating at high rates, it could be required to inhibit the acquisition for all boards while the state of one board or more is busy due to a memory full.

The steps to be performed to synchronize two or more V1742 are the following:

1. **Clock synchronization**.
   a Choose one “master” board and connect its CLK-OUT to the CLK-IN connector of the first “slave” board. The ”CLOCK SOURCE” dip switch (see Sec. **8.2**) of the master board must be set to INT (internal).
   Connect the CLK-OUT of the first slave board to the CLK-IN of the second slave board, and so for the other slaves. The ”CLOCK SOURCE” dip switch of the slave boards must b e set to EXTERNAL.
   CAEN can provide A317 cables for the clock distribution.
   b Program the PLL of the master board to work with its internal 50-MHz oscillator and to provide a reference clock at 58.594 MHz on CLK-OUT connector.
   Program the PLL of the slave boards to receive the 58.594-MHz clock on CLK-IN and to provide it on CLK-OUT.
   Contact CAEN to receive the PLL programming files (Chap. **17**).
   c Configure the boards to provide the clock on TRG-OUT and check the clock delay between the boards on a digital oscilloscope; then program again the slaves to compensate for the delay.
   Report to CAEN the delay values to receive the PLL programming files (Chap. **17**).
   NOTE: in case of fast trigger on TRn it is not required to achieve high precision in the clock alignment, since the time reference is defined by the common TRn (see next point)
2. **Fast Trigger**. To achieve high time precision in the measurement, it is recommended to use the ”one to many” mode for the Fast trigger using the TRn connector (see Sec. **9.9.3**) and to digitize and save it in the data: the TRn acts as a common reference time for the channels. To ensure a precise time alignment, make sure that a common trigger is split in all the TRn by using cables of the same length.
   NOTE: Use the Group Trigger Time Tag as time reference of the trigger (see Sec. **9.8.2**), while the Event Trigger Time Tag is the time when the event is composed by the FPGA.
3. **Run propagation**. The start of the run is made via software and it is propagated from the master board to the slaves through either TRG-OUT/S-IN daisy chain, or through the LVDS I/Os.
   a TRG-OUT/S-IN daisy chain:
      i Connect the TRG-OUT of the master to the S-IN of the slave, and so on.
      ii Program the TRG-OUT to be synchronized with the start run (bit[17:16] and bit[19:18] of register 0x811C).
      iii Program the acquisition to be controlled by S-IN (bit[2:0] of register 0x8100).
   b LVDS I/O daisy chain:
      i Connect the LVDS Output of the master to the LVDS Input of the slave, and so on.
      ii Program the LVDS I/O as nRUN option of the nBUSY/nVETO mode (see Sec. **9.11.3**).

iii Program the acquisition to be controlled by the LVDS I/O (bit[2:0] of register 0x8100).

The delay in the run propagation can be compensated via software.

4. **Busy management**. The acquisition of all boards should be inhibited when at least one board is busy to avoid that one board acquires while the others are busy. The system busy (logic OR of the busy of all boards) can be propagated out on the TRG-OUT connector of the last board through the following steps:
   a Propagate the busy from the master to the slaves through the LVDS I/O connectors (refer to registers 0x811C, 0x81A0, and 0x8110).
   b Program the TRG-OUT connector of the last slave to propagate out the OR of the busy (busy from its groups and busy from the LVDS) through register 0x811C.

   The TRG-OUT signal than can be used to directly veto the TRn source before it is fed into the board (recommended option), or it can be propagated to the TRG-IN connector of all boards. In the latter case the steps are as follows:
   a Use an external FAN IN/FAN OUT board to split the TRG-OUT signal.
   b Feed the fan-out output to the TRG-IN connector of all boards of the chain.
   c Program the veto from TRG-IN (refer to registers 0x8000 and 0x811C).

A detailed guide to multi-board synchronization can be found in **[RD9]**. Though it doesn't apply specifically to V1742 modules, it represents a valid reference to approach CAEN multi-board synchronization concepts and architecture. Please contact CAEN for clarifications and support (see Chap. **17**).

9.11 Front Panel LVDS I/Os

The V1742 and VX1742 are provided with 16 general purpose programmable LVDS I/O signals. From the ROC FPGA firmware revision 3.8 on, a more flexible configuration management has been introduced, which allows these signals to be programmed in terms of direction (INPUT/OUTPUT) and function by groups of 4.

ROC FPGA FIRMWARE REVISIONS < 3.8:

In case of ROC FPGA firmware revisions < 3.8, the signals on the LVDS I/O pins are fixed (see the pinout in **Tab. 9.3**).

Nr.	Direction	Description
0	out	GROUP 0 Trigger Request
1	out	GROUP 1 Trigger Request
2	out	GROUP 2 Trigger Request
3	out	GROUP 3 Trigger Request
4 - 7	-	not used
8	out	Memory Full
9	out	Event Data Ready
10	out	Channels Trigger
11	out	RUN Status
12	in	Trigger Time Tag Reset (active low)
13	in	Memory Clear (active low)
14	-	Reserved
15	-	Reserved

Tab. 9.3: Functional description of the LVDS I/O signals for ROC FPGA firmware revisions < 3.8

ROC FPGA FIRMWARE REVISIONS $\geq$ 3.8:

THE USER MUST SET BIT[8] = 1 AT 0x811C IN ORDER TO ENABLE THE NEW LVDS I/Os CONFIGURATION MODES.

FOR THOSE USERS WHOSE SOFTWARE BASES ON THE OLD LVDS I/Os CONFIGURATION MANAGEMENT, THE WAVEFORM RECORDING FIRMWARE OF V1742 MAKES ALSO AVAILABLE THE OLD CONFIGURATIONS (bit[8] = 0 and bit[7:6] = 01 at 0x811C).
SINCE THIS COULD BE NO LONGER GUARANTEED IN THE FUTURE, THE USER IS RECOMMENDED TO TAKE THE NEW CONFIGURATION MANAGEMENT AS REFERENCE!

Configure the LVDS I/O signals as inputs or outputs by groups of 4 involves bit [5:2] at 0x811C register address:

Bit[2] acts on LVDS I/O[3:0]

Bit[3] acts on LVDS I/O[7:4]

Bit[4] acts on LVDS I/O[11:8]

Bit[5] acts on LVDS I/O[15:12]

Setting the bit to ”0” enables the relevant signals in the group as INPUT, while setting it to ”1” enables them as OUTPUT.

Programming the function by groups of 4 LVDS I/O signals, involves bit[15:0] at 0x81A0 register address:

- Mode 0 (bits[n+3:n] = 0000): REGISTER
- Mode 1 (bits[n+3:n] = 0001): TRIGGER
- Mode 2 (bits[n+3:n] = 0010): nBUSY/nVETO
- Mode 3 (bits[n+3:n] = 0011): LEGACY

where n = 0, 4, 8, 12.

Note: Whatever option is set, the LVDS I/Os are always latched with the trigger and the relevant status of the 16 signals is always written into the header Pattern field (see Sec. **9.8.2**). The user can then choose to read out it or not.

GROUP / FUNCTION	REGISTER	TRIGGER	nBUSY/nVETO	LEGACY
LVDS IN [15:12]	Reg[15:12]	*Not used*	15: nRunIn 14: reserved 13: nVetoIn 12: nBusyIn	15: reserved 14: reserved 13: reserved 12: nClear_TTT
LVDS IN [11:8]	Reg[11:8]	*Not used*	11: nRunIn 10: reserved 9: nVetoIn 8: nBusyIn	11: reserved 10: reserved 9: reserved 8: nClear_TTT
LVDS IN [7:4]	Reg[7:4]	*Not used*	7: nRunIn 6: reserved 5: nVetoIn 4: nBusyIn	7: reserved 6: reserved 5: reserved 4: nClear_TTT
LVDS IN [3:0]	Reg[3:0]	*Not used*	3: nRunIn 2: reserved 1: nVetoIn 0: nBusyIn	3: reserved 2: reserved 1: reserved 0: nClear_TTT

Tab. 9.4: Functional description of the LVDS I/O signals when configured as INPUT

GROUP / FUNCTION	REGISTER	TRIGGER	nBUSY/nVETO	LEGACY
LVDS OUT [15:12]	Reg[15:12]	*Not used*	15: nRun 14: nTrigger 13: nVeto 12: nBusy	15: Run 14: Trigger 13: DataReady 12: Busy
LVDS OUT [11:8]	Reg[11:8]	TrigOut_Gr[3:0]	11: nRun 10: nTrigger 9: nVeto 8: nBusy	11: Run 10: Trigger 9: DataReady 8: Busy
LVDS OUT [7:4]	Reg[7:4]	*Not used*	7: nRun 6: nTrigger 5: nVeto 4: nBusy	7: Run 6: Trigger 5: DataReady 4: Busy
LVDS OUT [3:0]	Reg[3:0]	TrigOut_Gr[3:0]	3: nRun 2: nTrigger 3: nVeto 0: nBusy	3: Run 2: Trigger 1: DataReady 0: Busy

Tab. 9.5: Functional description of the LVDS I/O signals when configured as OUTPUT

9.11.1 Mode 0: REGISTER

Direction is INPUT: the logic level of the LVDS I/O signals can be read at 0x8118 register address.

Direction is OUTPUT: the logic level of the LVDS I/O signals can be written at 0x8118 register address.

9.11.2 Mode 1: TRIGGER

Direction is INPUT: Not available.

Direction is OUTPUT: TrigOut_Gr[3:0] are the signals from the 8-channel groups Gr0 (CH0:CH7), Gr1 (CH8:CH15), Gr2 (CH16:CH23), and Gr3 (CH24:CH31). They can be the TR fast local triggers (all TR or the accepted TR) or the busy signals (refer to 0x8000 and 0x811C registers).

9.11.3 Mode 2: nBUSY/nVETO

nBusy Signal

nBusyIn (INPUT) is an active low signal which, if enabled, is used to generate the nBusy signal (OUTPUT) as below.

The Busy signal (fed out on LVDS I/Os or TRG-OUT LEMO connector) is:

Full OR Dead_Time OR (LVDS_BusyIn AND BusyIn_enable)

where

- Full condition due to the saturation of the channels' memory.
- Dead_Time condition due to the analog-to-digital conversion;
- LVDS_BusyIn is available in nBUSY/nVETO configuration (see **Tab. 9.5**);
- BusyIn_enable is set at register address 0x8100, bit[8].

nVETO Signal

Direction is INPUT: nVETOIn is an active low signal which, if enabled (register address 0x8100, bit[9] = 1), is used to veto the generation of the common trigger propagated to the channels for the event acquisition.

Direction is OUTPUT: the nVETO signal is the copy of nVETOIn.

nTrigger Signal

Direction is INPUT: reserved.

Direction is OUTPUT: nTrigger signal is the copy of the trigger signal propagated to the TRG-OUT LEMO connector or copy of the acquisition common trigger. This is selected by bit[16] of the 0x81A0 register.

nRun Signal

Direction is INPUT: nRunIn is an active low signal which can be used as Start for the digitizer (register address 0x8100, bits[1:0] = 11). It is possible to program the Start on the level or on the edge of the nRunIn signal (register address 0x8100, bit[11]).

Direction is OUTPUT: nRun signal is the inverse of the internal Run of the board.

9.11.4 Mode 3: LEGACY

Legacy Mode has been introduced in order the LVDS connector (properly programmed) to be able to feature the same I/O signals available in the ROC FPGA firmware revisions lower than 3.8.

nClear_TTT Signal

Direction is INPUT: It is the Trigger Time Tag (TTT) reset, like in the old configuration.

Direction is OUTPUT: not used.

Busy Signal

Direction is INPUT: not used.

Direction is OUTPUT: the Busy signal is active high and it is exactly the inverse of the nBusy signal (see Sec. **9.11.3**).

DataReady Signal

Direction is INPUT: not used.

Directin is OUTPUT: The DataReady is an active high signal indicating that the board has data available for readout (the same as the DataReady front panel LED does).

Trigger Signal

Direction is INPUT: not used.

Direction is OUTPUT: the active high Trigger signal is the copy of the acquisition trigger (common trigger) sent from the motherboard to the mezzanines (it is neither the signal provided out on the TRG-OUT LEMO connector nor the inverse of the signal sent to the LVDS connector).

Run Signal

Direction is INPUT: not used.

Direction is OUTPUT: The Run signal is active high and represents the inverse of the nRun signal (see Sec. **9.11.3**).

Note: The Memory Clear is not implemented in the LEGACY LVDS configuration mode.

9.12 Test Pattern Generator

The FPGA can emulate the ADC and write into memory a saw tooth signal for test purposes. It can be enabled via Group Configuration register.

The following figure shows the test waveforms for even and odd groups respectively.

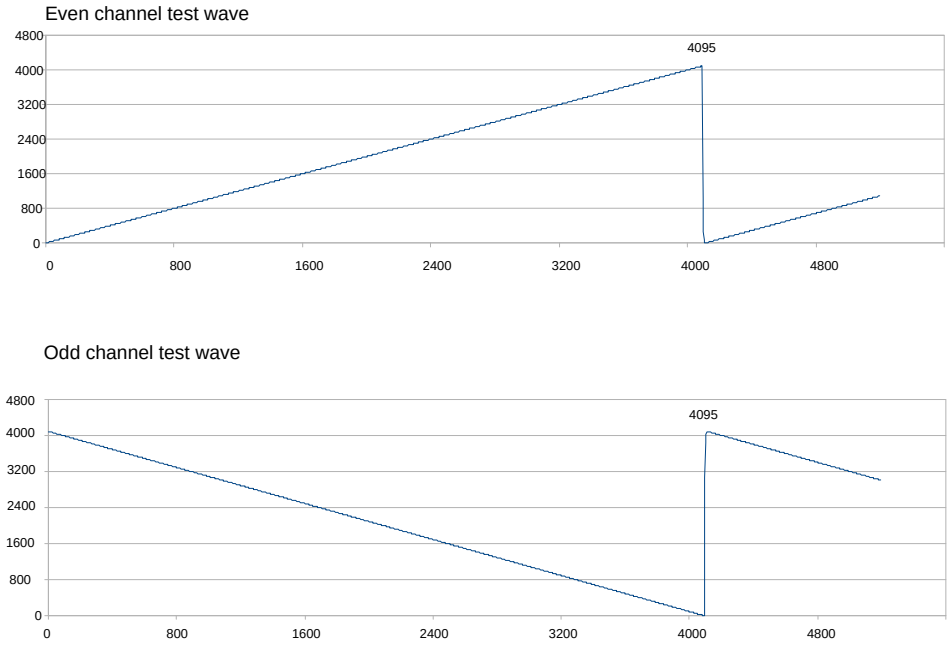


Fig. 9.17: FPGA test waveform

Since an event is made up of up to 1024 samples, the test event samples only a “portion” of the saw tooth; the start point of the sampling can be programmed via Initial Test Wave Value register; for example if this register is set to 0x0FF then the channels in the even groups sample the ramp between 255 and 1278; the channels in the odd groups instead sample the complementary value, therefore between 3840 and 2817.

9.13 Reset, Clear and Default Configuration

9.13.1 Global Reset

A global reset is performed at power-on of the module or can be issued via software by write access at 0xEF24 register address. By a global reset, the data from the Output Buffer are cleared, the event counters are reset and so all the board FPGAs which turn back to their default configuration. All counters are initialized to their initial state and all detected error conditions are cleared.

9.13.2 Memory Reset

The memory reset clears the data off the Output Buffer.
It can be issued by write access at 0xEF28 register address (whatever 32-bit value can be written) or by hardware. In this second case (VME only), the user must switch to the LVDS old features, by setting bit[8]=0 of register address 0x811C, and send the memory clear signal to the LVDS pin 13 (see **Tab. 9.3**).

9.13.3 Timer Reset

The timer reset initializes the time tag counters (Event Time Tag and Group Trigger Time Tag).
The timer reset can be issued either via software by a software clear command at 0xEF28 register address, or via hardware by sending a pulse to the front panel Trigger Time Tag Reset input of LVDS I/Os (see Sec. **9.11**), or to the S-IN input (leading edge sensitive). In case the S-IN connector needs to be used to reset the trigger time stamps, no configuration or access to registers is necessary. The user only has to transmit a NIM or TTL signal to the input, depending on the software selected logic level for the S-IN connector. The time stamps reset occurs at every leading edge of the logic signal sent to the S-IN connector.

9.14 VMEBus Interface

The module is provided with a fully compliant VME64/VME64X interface, whose main features are:

- EUROCARD 9U Format
- J1/P1 and J2/P2 with either 160 pins (5 rows) or 96 (3 rows) connectors
- A24, A32 and CR-CSR address modes
- D32, BLT/MBLT, 2eVME, 2eSST data modes
- MCST write capability
- CBLT data transfers
- RORA interrupter
- Configuration ROM

9.14.1 Addressing Capabilities

- Base address: the module works in A24/A32 mode The Base Address of the module is selected through four rotary switches (see **Fig. 8.2**), then it is validated only with either a power-on cycle or a system reset (see Sec. **9.13.1**).

ADDRESS MODE	ADDRESS RANGE	NOTES
A24	[0x000000:0xFF0000]	SW3 and SW4 ignored

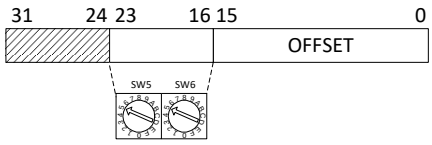


Fig. 9.18: A24 addressing

ADDRESS MODE	ADDRESS RANGE	NOTES
A32	[0x00000000:0xFFFF0000]	

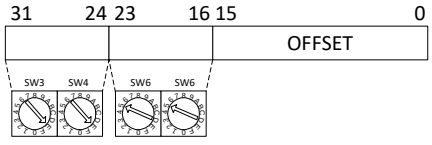


Fig. 9.19: A32 addressing

- CR/CSR address: the addressing is based on the slot number taken from the relevant backplane lines. The recognised Address Modifier for this cycle is 2F. *This feature is implemented only on versions with 160-pin connectors.*

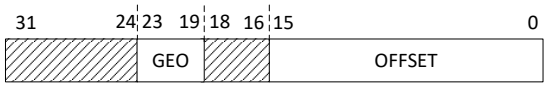


Fig. 9.20: CR/CSR addressing

9.14.2 Address Relocation

By bit[15:0] at register address 0xEF10, it is possible to set the board Base Address via software (valid values ≠ 0). Such register allows to overwrite the rotary switches settings; its setting is enabled via bit[6] at 0xEF00 register address.

The used addresses are:

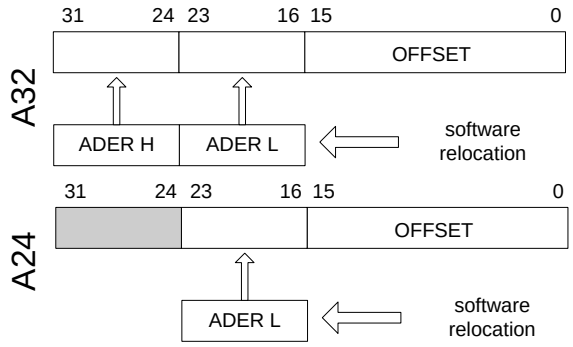


Fig. 9.21: Software relocation of base address

9.15 Data Transfer Capabilities and Events Readout

Once it is written in the memory, the event becomes available for the readout via VMEbus or Optical Link. According to the board model (**Tab. 1.1**), up to 128 or 1024 events per channel (1024 samples per event) can be stored in the digitizer digital memory.

The events are read out sequentially and completely, starting from the Header of the first available event, followed by the samples of the enabled groups as reported in **Fig. 9.12**. It is not possible to read out an event partially.

The size of the event (EVENT SIZE) is configurable and depends on register addresses 0x8020 **[RD1]**, as well as on the number of enabled groups. Reducing the event size does not reduce the digitizer dead time.

The board supports D32 single data readout, Block Transfer BLT32, MBLT64, CBLT32/64, 2eVME and 2eSST cycles. Theoretical maximum transfer rate is up to 70 MB/s with MBLT64 (using CAEN Bridge), up to 200 MB/s with 2eSST. Up to 80 MB/s can be achieved by direct optical link.

9.15.1 Block Transfer D32/D64, 2eVME and 2eSST

The Block Transfer readout mode allows to read N complete events sequentially, where N is set at register address 0xEF1C, or by using the SetMaxNumEventsBLT function of the CAENDigitizer library **[RD4]**.

When developing programs, the readout process can be implemented on different basis:

- Using Interrupts: as soon as the programmed number of events is available for readout, the board. sends an interrupt to the PC over the optical communication link (not supported by USB and A4818).
- Using Polling (interrupts disabled): by performing periodic read accesses to a specific register of the board it is possible to know the number of events present in the board and perform a BLT read of the specific size to read them out.
- Using Continuous Read (interrupts disabled): continuous data read of the maximum allowed size (e.g. total memory size) is performed by the software without polling the board. The actual size of the block read is determined by the board that terminates the BLT access at the end of the data, according to the configuration of 0xEF1C register address, or the SetMaxNumEventsBLT library function mentioned above. If the board is empty, the BLT access is immediately terminated and the “Read Block” function will return 0 bytes (it is the ReadData function in the CAENDigitizer Library).

Whatever the method from above, it is suggested to ask the board for the maximum of the events per block being set. Furthermore, the greater this maximum, the greater the readout efficiency, despite of a greater memory allocation required on the host station side that is actually not a real drawback, considering the features of the personal computers available on the market.

The event is configurable as indicated in the introduction of the paragraph, namely:

[Event Size] = [8*(Buffer Size)] + [16 bytes]

Then, it is necessary to perform as many cycles as required in order to readout the programmed number of events.

It is suggested to enable BERR signal during BLT32 cycles, in order to end the cycle avoiding filler readout. The last BLT32 cycle will not be completed, it will be ended by BERR after the #N event in memory is transferred (see example in the figure below).

Since some 64-bit CPU cut off the last 32- bit word of a transferred block, if the number of words composing such block is odd, it is necessary to add a dummy word (which has then to be removed via software) in order

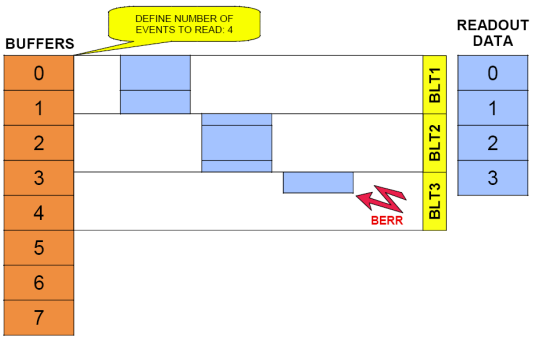


Fig. 9.22: Example of BLT readout

to avoid data loss. This can be achieved by setting the ALIGN64 bit (bit[5]) at 0xEF00 register address .

MBLT64 cycle is similar to the BLT32 cycle, except that the address and data lines are multiplexed to form 64 bit address and data buses.

The 2eVME allows to achieve higher transfer rates thanks to the requirement of only two edges of the two control signals (DS and DTACK) to complete a data cycle.

9.15.2 Chained Block Transfer D32/D64

The board allows to readout events from more daisy chained boards (Chained Block Transfer mode).

The technique which handles the CBLT is based on the passing of a token between the boards; it is necessary to verify that the used VME crate supports such cycles.

Several contiguous boards, in order to be Daisy chained, must be configured as “first”, “intermediate” or “last” via 0xEF0C register address. A common Base Address is then defined via the same register; when a BLT cycle is executed at the address CBLT_Base + 0x0000 ÷ 0x0FFC, the “first” board starts to transfer its data, driving DTACK properly; once the transfer is completed, the token is passed to the second board via the IACKIN-IACKOUT lines of the crate, and so on until the “last” board, which completes the data transfer and asserts BERR (which has to be enabled): the Master then ends the cycle and the slave boards are rearmed for a new acquisition. If the size of the BLT cycle is smaller than the events size, the board which has the token waits for another BLT cycle to begin (from the point where the previous cycle has ended).

9.15.3 Single D32 Transfer

This mode allows the user to read out a word at a time, from the header (4 words) of the first available event, followed by all the words until the end of the event, then the second event is transferred. The exact sequence of the transferred words is shown in Sec. **9.8.2**.

After the 1st word is transferred, It is suggested to check the EVENT SIZE information and then do as many cycles as necessary (actually EVENT SIZE -1) in order to read the event completely.

9.16 Optical Link Access

The digitizer houses an interface for optical link communication which uses optical fiber cables as physical transmission line, with a maximum transfer data rate of 80 MB/s.

CONET is the proprietary serial protocol designed by CAEN to enable optical link communication between digitizers (acting as CONET slaves) and the host PC. This communication needs CONET master such as the A5818 controllers, or the A4818 adapter.

CONET2 is the latest protocol version, implemented at the firmware level on digitizers and controllers, that improves the data transfer rate efficiency by 50% compared to the earlier CONET1 version.

Note: CONET1 and CONET2 protocol versions are incompatible; communication will fail in any optical chain containing both CONET1 and CONET2 boards.

To update your system from CONET1 to CONET2, it is recommended to follow the instructions provided by CAEN in the dedicated Application Note **[CONETMigration]**.

The optical link interface has Daisy-chain capability. Therefore, it is possible to connect up to eight digitizers to a single Optical Link Controller by using the A4818 adapter, while up to thirty- two digitizers with the A5818 PCIe card. Detailed information can be found at the relevant controller web page on CAEN website.

The parameters for read/write accesses via Optical Link are the same used by VME cycles (Address Modifier, Base Address, data Width, etc); wrong parameter settings cause Bus Error.

Setting bit[3] at register address 0xEF00 enables the module to broadcast an interrupt request on the Optical Link; the enabled Optical Link Controllers propagate the interrupt on the PCI bus when a request from the Optical Link is sensed. Interrupts can also be managed at the CAENDigitizer library level **[RD4]**.

Note: The CONET protocol implemented in the A4818 adapter from USB-3.0 to Optical Link does not support the interrupts.

VME and Optical Link accesses take place on independent paths and are handled by board internal controller, with VME having higher priority; anyway it is better to avoid accessing the board via VME and Optical Link simultaneously.

9.17 Trigger Rate

Introducing the trigger rate, it is worth remarking those features which are typical of the 742 digitizer family:

- The channels can only be enabled by 8-channel groups, not individually; each group counts on a 128-event or a 1024-event memory, depending on the board model (see **Tab. 1.1**); each event is composed by a number or samples of the digitized wave which are configurable as fixed values: 1024, 520, 256, or 136 samples.
- Due to the particular architecture of the analog-to-digital conversion based on switched-capacitors, there is a dead-time of 110 µs (if the TR fast local trigger is not digitized) or 181 µs (if TR is digitized).

The dead-time forces a ”peak” trigger rate, $\text{TRG-RATE}_{\text{peak}}$, which is:

$\text{TRG-RATE}_{\text{peak}} = \frac{1}{110}$ MHz $\simeq$ 9.09 kHz if TR is not digitized;

$\text{TRG-RATE}_{\text{peak}} = \frac{1}{181}$ MHz $\simeq$ 5.525 kHz if TR is digitized.

The dead-time represents the minimum time distance between a trigger event and the next one which makes the latter to be sensed and processed by the board. This means that a trigger occurring less than 110 µs after the last one in one case and less than 181 µs in the other will not be sensed, and the relevant event is lost (i.e. not stored in the digital memory and so not available for readout).

The ”peak” trigger rate is sustainable and valid only for the first 128 events (or 1024, in case of bigger size memory), then the reference becomes the ”average” trigger rate. Among the other things, the ”average” trigger rate is linked to the readout and represents the average data flow supported by the board without entering the memory full condition.

The ”average” trigger rate can only be computed theoretically, as it relies on the maximum transfer rate declared for the communication link being used, which is theoretical as well (i.e. guaranteed only under optimal conditions).

The board supports an Optical and a VME communication interface whose transfer rate specifications are:

- 80 MB/s for the Optical Link;
- 70 MB/s for the VME Link.

Basically, the ”average” trigger rate depends on multiple factors like the number of enabled channels, the size of the acquired wave, as well as the acquisition mode, and the readout software. The optimization of the code plays a critical role in the capability of getting the ”average” trigger rate the closer to its theoretical value. In this view, applying offline all the required corrections (see Sec. **9.7**) can help. Even data saving is a significant point, but it is of course an essential function of the software.

9.17.1 "Average" Trigger Rate Calculation

The "average" trigger rate can be computed by the following formula:

$$\frac{\text{TRANSFER\_RATE}}{\text{EVENT\_SIZE}} \tag{9.1}$$

where:

TRANSFER_RATE is the maximum theoretical declared for the specific communication link;
EVENT_SIZE is computed upon the event data format (refer to Sec. **9.8.2**).

For a single event of a x742 digitizer, the EVENT_SIZE is made of:

- 16 bytes from the HEADER field;
- 8 bytes per enabled channel group (i.e. the sum of EVENT DESCRIPTION field and GROUP EVENT TIME TAG field);
- $3 \cdot N_S \cdot 4$ bytes (N_S is the number of acquired samples; 1 sample is over 3 words that is to say 24 bytes).

In case the TRn digitization is enabled, an additional factor of $\frac{3 \cdot N_S}{8} \cdot 4$ bytes must be considered.

The resulting EVENT_SIZE is finally:

$$\text{EVENT\_SIZE} = 16 + N_G \cdot \left[8 + 3 \cdot N_S \cdot 4 + \left(\frac{3 \cdot N_S}{8} \cdot 4 \right) \right] \text{Byte} \tag{9.2}$$

where N_G is the number of enabled channel groups.

The values of the theoretical "average" trigger rate, computed upon the formulas given above, are reported in the following tables for N_S = 1024 samples.

N_G	TRn Not Digitized	TRn Digitized
1	6.813 kHz	6.058 kHz
2	3.409 kHz	3.030 kHz
3	2.273 kHz	2.021 kHz
4	1.705 kHz	1.516 kHz

Tab. 9.6: Theoretical "average" trigger rate values for the Optical Link

N_G	TRn Not Digitized	TRn Digitized
1	5.962 kHz	5.300 kHz
2	2.983 kHz	2.652 kHz
3	1.989 kHz	1.768 kHz
4	1.492 kHz	1.326 kHz

Tab. 9.7: Theoretical "average" trigger rate values for the VME Link

10 Drivers & Libraries

10.1 Drivers

To interface with the board, CAEN provides Windows® and Linux® drivers for the different types of the supported physical communication links:

- **CONET Optical Link**, managed by the CAEN controllers A5818 PCIe card. The driver installation packages is available on CAEN website in the "Software/Firmware" tab at the A5818 page (**login required**).

Note: For the installation of the Optical Link driver, refer to the User Manual of the specific card **[RD10]**.

- **USB 2.0 link**, managed by CAEN (USB-to-VME) Bridges V3718. The driver installation packages is downloadable for free on CAEN website at the V3718 page (**login required**).
- **USB 3.0 link**, managed by the V4718 USB-to-VME Bridge and by the A4818 (USB3-to-CONET) Adapter. The driver installation packages are downloadable for free on CAEN website at the V4718 and A4818 page respectively (**login required**). The driver for the V4718 has to be installed for Linux users only.

Note: To install the USB Link driver, follow the instructions inside the ReadMe file included in the packet or refer to the V3718, V4718 User Manuals **[RD11][RD12]** or A4818 adapter Data Sheet **[RD13]**.

10.2 Libraries

CAEN libraries are a set of middleware software required by CAEN software tools for a correct functioning. These libraries, including also demo and example programs, represent a powerful base for users who want to develop customized applications for the digitizer control (communication, configuration, readout, etc.):

- **CAENDigitizer [RD4]** is a library of C functions specifically designed for the Digitizer families and supports both waveform recording and DPP firmware. The CAENDigitizer library is based on the CAENComm which, in turn, is based on CAENVMELib. For this reason, **the CAENVMELib and CAENComm libraries must be already installed on the host PC before installing the CAENDigitizer**.
- **CAENComm** library **[RD7]** manages the communication at low level (read and write access). The purpose of this library is to implement a common interface to the higher software layers, masking the details of the physical channel and its protocol, thus making the libraries and applications that rely on the CAENComm independent from the physical layer. **The CAENComm requires the CAENVMELib library (access to the VME bus), even in the cases where the VME is not used**.

Installation packages are available for free download on CAEN web site (*www.caen.it*) at each library page (**login required**).

WHEN TO INSTALL CAEN LIBRARIES:

WINDOWS® and LINUX® compliant customized software. The user must install the required libraries apart.

LINUX® compliant non-stand alone CAEN software. The user must install the required libraries apart to run the software.

CAENComm (and so the CAENDigitizer) supports the following communication channels (**Fig. 10.1**):

PC → USB3 → A4818 → CONET → V1742/VX1742
PC → USB → V3718/VX3718 → VMEbus → V1742/VX1742
PC → USB3 → V4718/VX4718 → VMEbus → V1742/VX1742
PC → USB3 → A4818 → CONET → V3718/VX3718 → VMEbus → V1742/VX1742
PC → USB3 → A4818 → CONET → V4718/VX4718 → VMEbus → V1742/VX1742
PC → PCIe → A5818 → CONET → V1742/VX1742
PC → PCIe → A5818 → CONET → V3718/VX3718 → VMEbus → V1742/VX1742
PC → PCIe → A5818 → CONET → V4718/VX4718 → VMEbus → V1742/VX1742
PC → ETHERNET → V4718/VX4718 → VMEbus → V1742/VX1742

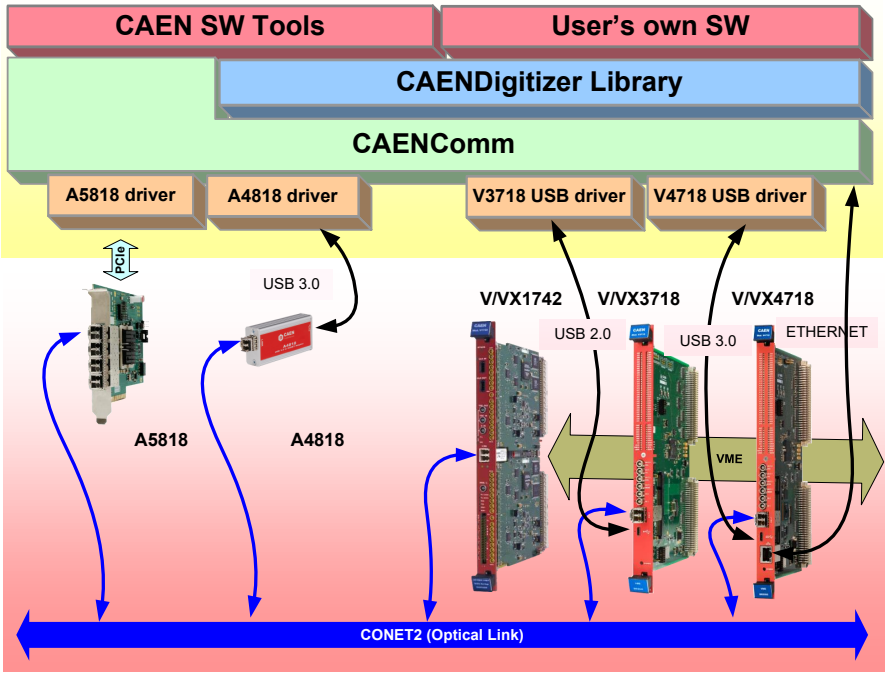


Fig. 10.1: Drivers and software layers (the obsolete bridge models are not shown in the figure)

11 Software Tools

CAEN provides software tools to interface the 742 digitizer family, which are available for free download on CAEN web site (*www.caen.it*) in the software and firmware product pages (**login required).**

11.1 CAEN Toolbox

CAEN Toolbox is the comprehensive software suite designed for CAEN Front-End boards.

With V1742, CAEN Toolbox simplifies various tasks into a few easy steps, including:

- Uploading different FPGA firmware versions to the digitizer
- Reading the firmware release of the digitizer
- Managing firmware licenses, particularly for DPP firmware
- Upgrading the internal PLL
- Obtaining the Board Info file, useful for support
- Managing the reboot of the FPGA firmware from either the Backup or the Standard FLASH page
- Debugging your setup using the Manual Controller

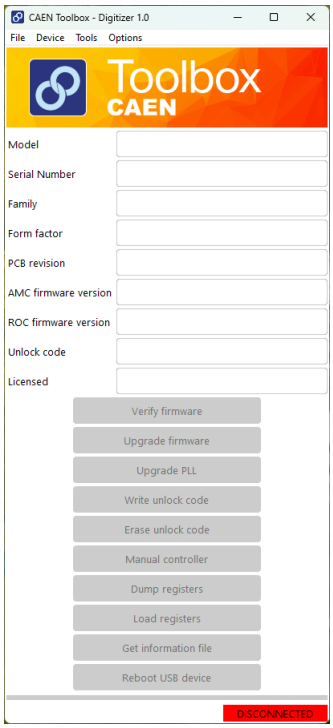


Fig. 11.1: CAEN Toolbox Graphical User Interface

Related to V1742/VX1742 , CAEN Toolbox is based on the CAENComm library (see Sec. **10.2**). The software is compatible with both Windows® and Linux® platforms, operating as a standalone application on each available version. For installation instructions and a detailed description of its features, refer to the CAEN Toolbox documentation **[RD2]**. Both the documentation and software packages can be downloaded directly from the dedicated webpage on the CAEN website (**login required**).

11.2 CAENComm Demo

CAENComm Demo is a simple program developed in C/C++ source code and provided both with Java™ and LabVIEW™ GUI interface. The demo mainly allows the user for a full board configuration at low level by direct read/write access to the registers, and may be used as a debug instrument.

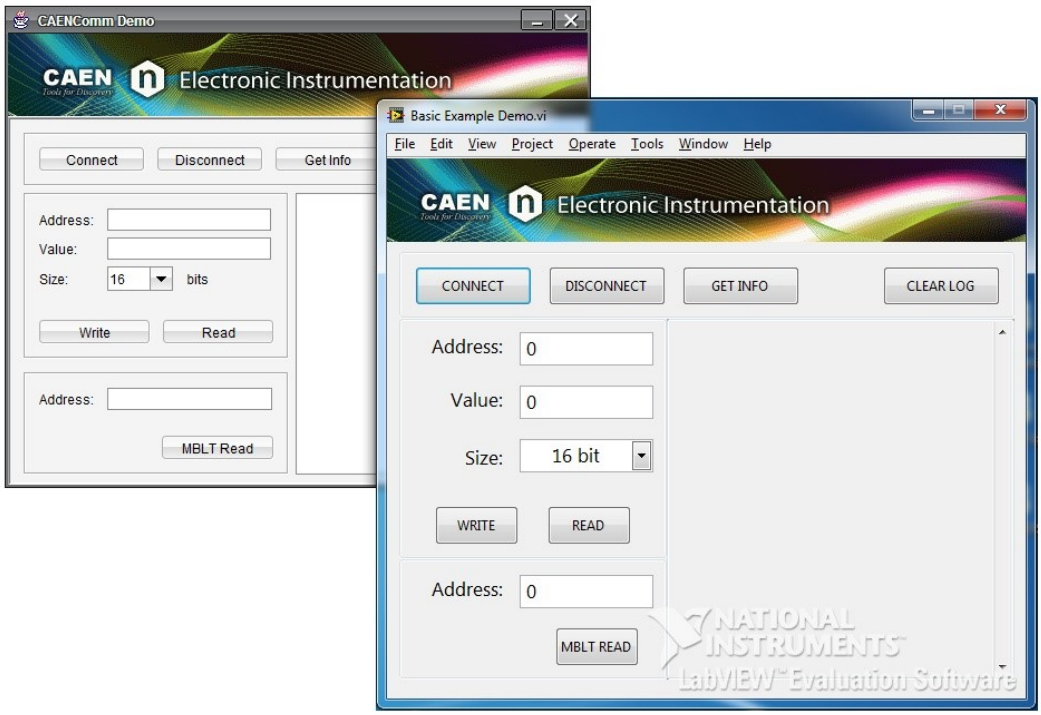


Fig. 11.2: CAENComm Demo Java™ and LabVIEW™ graphical interface

CAENComm Demo is based on the CAENComm library (see Sec. **10.2**) and it is included in the installation package of the library. Th software is available only for Windows®platform.

The software installation package and the documentation **[RD7]** can be downloaded from the CAEN website (**login required**).

11.3 CAEN WaveDump

WaveDump is a basic console application, with no graphics, supporting only CAEN digitizers running the waveform recording firmware. It allows the user to program a single board (according to a text configuration file containing a list of parameters and instructions), to start/stop the acquisition, read the data, display the readout and trigger rate, apply some post-processing (e.g. FFT and amplitude histogram), save data to a file and also plot the waveforms using Gnuplot third-party graphing utility (*www.gnuplot.info*).

WaveDump is a very helpful example of C code demonstrating the use of libraries and methods for an efficient readout and data analysis. Thanks to the included source files and the VS project, starting with this demo is strongly recommended to all those users willing to write the software on their own.

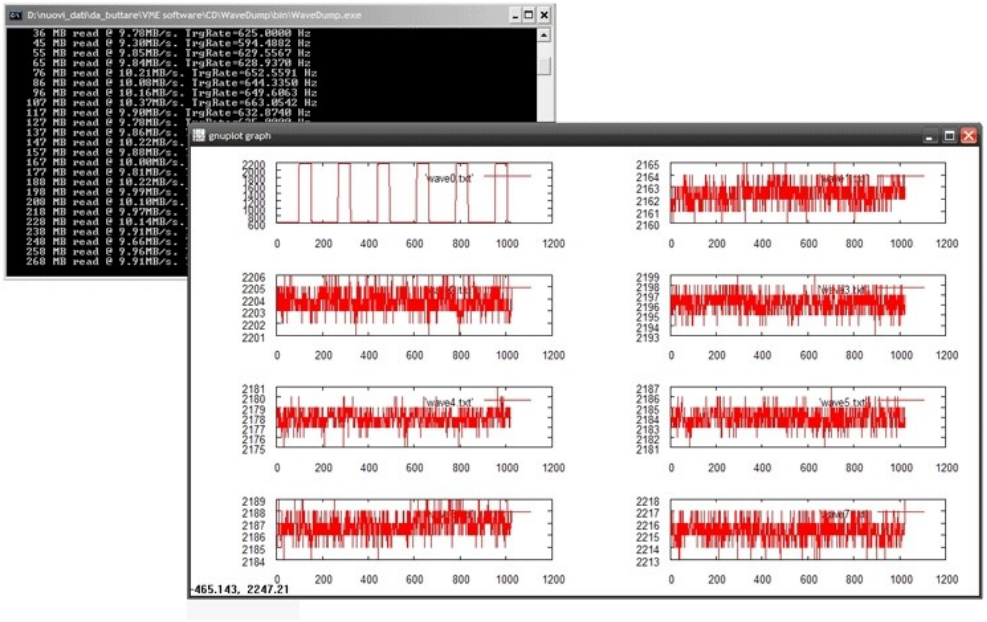


Fig. 11.3: CAEN WaveDump

CAEN WaveDump relies on the CAENDigitizer library (see Sec. **10.2**) and it can run on Windows®and Linux® platforms. Windows®versions of WaveDump are stand-alone (all required libraries are present within the software package), while the Linux®versions need the required libraries to be previously installed by the user. Moreover Linux®users are required to install the third-party Gnuplot.

The installation packages, the software User Manual **[RD5]** and a guide for getting started with it **[RD8]** can be downloaded from CAEN website (**login required**).

12 HW Installation

To power on the board, perform the following steps:

- Insert the Digitizer into the crate:
  - The V1742 fits into 6U VME crates.
  - VX1742 versions require VME64X compliant crates.
- Power up the crate.

ONLY QUALIFIED PERSONNEL SHOULD PERFORM INSTALLATION OPERATIONS

DO NOT INSTALL THE EQUIPMENT IN A SETUP WHERE IT IS DIFFICULT TO ACCESS THE BACK PANEL FOR DISCONNECTING THE DEVICE

IT IS RECOMMENDED THAT THE SWITCH OR CIRCUIT-BREAKER IS NEAR THE EQUIPMENT

THE SAFETY OF ANY SYSTEM THAT INCORPORATES THE DEVICE IS UNDER THE RESPONSIBILITY OF THE ASSEMBLER OF THE SYSTEM

12.1 Power-on Status

Power-on takes few seconds during which the front panel LEDs may flash.

At power-on, the module is in the following status:

- The Output Buffer is cleared;
- Registers are set to their default configuration;
- Only NIM and PLL LOCK LEDs must stay on (see **Fig. 12.1**).

Fig. 12.1: Front panel LEDs status at power-on

13 Firmware and Upgrades

The board hosts one FPGA on the mainboard and one FPGA on the mezzanine (i.e. one FPGA manages 16+1 channels). The channel FPGAs firmware is identical. A unique file is provided that will update all the FPGAs at the same time.

ROC FPGA MAINBOARD FPGA (Readout Controller + Communication Interface):

FPGA Altera Cyclone EP1C20.

AMC FPGA MEZZANINE FPGA (ADC readout/Memory Controller):

FPGA Altera Cyclone EP3C16

The firmware is stored onto the on-board FLASH memory. Two copies of the firmware are stored in two different pages of the FLASH, referred to as Standard (STD) and Backup (BKP). In case of waveform recording firmware, the board is delivered equipped with the same firmware version on both pages.

At power-on, a microcontroller reads the FLASH memory and programs the module automatically loading the first working firmware copy, that is the STD one by default in normal operating.

The on-board dedicated SW7 dip switch (see Sec. **8.2**) allows to select the first FLASH page to be read at power-on (STD by default).

It is possible to upgrade the board firmware via VMEbus or Optical Link by writing the FLASH with the CAENToolbox software (see Chap. **11**).

IT IS STRONGLY SUGGESTED TO OPERATE THE DIGITIZER UPON THE STD COPY OF THE FIRMWARE. UPGRADES ARE SO RECOMMENDED ONLY ON THE STD PAGE OF THE FLASH. THE BKP COPY IS TO BE INTENDED ONLY FOR RECOVERY USAGE. IF BOTH PAGES RESULT CORRUPTED, THE USER WILL NO LONGER BE ABLE TO UPLOAD THE FIRMWARE VIA VMEbus OR OPTICAL LINK AGAIN AND THE BOARD NEEDS TO BE SENT TO CAEN FOR REPAIR!

13.1 Firmware Updates

Firmware updates are available for download on CAEN web site (*www.caen.it*) at the digitizer page (**login required**). The waveform recording is free firmware and updates are free downloadable.

13.2 Firmware File Description

The programming file is a CFA file (CAEN Firmware Archive). It is an archiving file format that aggregates all the programming files of the same firmware kind which are compatible with the same digitizer family.

The name of the CFA file follows a general convention:

- *<DIGITIZER>*_rev_X.Y_W.Z.CFA for the waveform recording firmware

where:
<DIGITIZER> are all the boards that can be updated by the CFA file;

options are:

- x742 (includes x742, x742B module versions);
  where x = DT5 for desktop, x = N6 for NIM, x = V1/VX1 for VME64/VME64x format;

X.Y is the major/minor revision number of the ROC FPGA;

W.Z is the major/minor revision number of the AMC FPGA.

13.3 Troubleshooting

In case of upgrade failure (e.g. STD FLASH page is corrupted), the user can try to reboot the board: after a power cycle, the system programs the board automatically from the alternative FLASH page (e.g. BKP FLASH page), if this is not corrupted as well (see Sec. **12.1**). The user can so perform a further upgrade attempt on the STD page to restore the firmware copy.

BECAUSE OF AN UPGRADE FAILURE, THE SW7 DIP SWITCH POSITION MAY NOT CORRESPOND TO THE FLASH PAGE FIRMWARE COPY LOADED ON THE BOARD FPGAs

Note: old versions of the digitizer motherboard have a slightly different FLASH management and the firmware selection switch is SW7. To obtain information about the FLASH type of the digitizer, the user can download the BoardInfoFile (text file) through the "Get information file" tab in CAEN Toolbox software (see. Chap. **11**) and check the value of the FLASH_TYPE parameter: FLASH_TYPE=0 indicates an older version. Alternatively, the user can use CAENComm software or the "Manual Controller" available in CAEN Toolbox to directly access register 0xF050 and check the status of bit[7:0]. If so, it means that, at power on, the microcontroller loads exactly the firmware copy from the FLASH page.

When a failure occurs during the upgrade of the STD page of the FLASH, which compromises the communication with the V1742/VX1742 the user can perform the following recovering procedure as first attempt:

- force the board to reboot loading the copy of the firmware stored on the BKP page of the FLASH. For this purpose, power off the crate, switch the dedicated SW7 switch to BKP position and power on the crate;
- use CAEN Toolbox to read the firmware revision (in this case the one of the BKP copy). If this succeeds, it is so possible to communicate again with the board;
- use CAEN Toolbox to load the proper firmware file on the STD page, then power off the crate, switch SW7 back to STD position and power on the crate.

If neither of the procedures here described succeeds, it is recommended to send the board back to CAEN in repair (see Chap. **17**).

14 Instructions for Cleaning

The equipment may be cleaned with isopropyl alcohol or deionized water and air dried. Clean the exterior of the product only.
Do not apply cleaner directly to the items or allow liquids to enter or spill on the product.

14.1 Cleaning the Touchscreen

To clean the touchscreen (if present), wipe the screen with a towelette designed for cleaning monitors or with a clean cloth moistened with water.
Do not use sprays or aerosols directly on the screen; the liquid may seep into the housing and damage a component. Never use solvents or flammable liquids on the screen.

14.2 Cleaning the Air Vents

It is recommended to occasionally clean the air vents (if present) on all vented sides of the board. Lint, dust, and other foreign matter can block the vents and limit the airflow. Be sure to unplug the board before cleaning the air vents and follow the general cleaning safety precautions.

14.3 General Cleaning Safety Precautions

CAEN recommends cleaning the device using the following precautions:

- Never use solvents or flammable solutions to clean the board.
- Never immerse any parts in water or cleaning solutions; apply any liquids to a clean cloth and then use the cloth on the component.
- Always unplug the board when cleaning with liquids or damp cloths.
- Always unplug the board before cleaning the air vents.
- Wear safety glasses equipped with side shields when cleaning the board.

15 Device Decommissioning

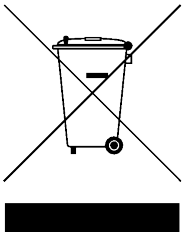
After its intended service, it is recommended to perform the following actions:

- Detach all the signal/input/output cable
- Wrap the device in its protective packaging
- Insert the device in its packaging (if present)

THE DEVICE SHALL BE STORED ONLY AT THE ENVIRONMENT CONDITIONS SPECIFIED IN THE MANUAL, OTHERWISE PERFORMANCES AND SAFETY WILL NOT BE GUARANTEED

16 Disposal

The disposal of the equipment must be managed in accordance with Directive 2012/19 / EU on waste electrical and electronic equipment (WEEE).



The crossed bin symbol indicates that the device shall not be disposed with regular residual waste.

17 Technical Support

To contact CAEN specialists for requests on the software, hardware, and board return and repair, it is necessary a MyCAEN+ account on www.caen.it:

https://www.caen.it/support-services/getting-started-with-mycaen-portal/

All the instructions for use the Support platform are in the document:

A paper copy of the document is delivered with CAEN boards.
The document is downloadable for free in PDF digital format at:

https://www.caen.it/wp-content/uploads/2022/11/Safety_information_Product_support_W.pdf

User Manual V1742/VX1742

32+2 Channel 12 bit 5 GS/s Switched Capacitor Digitizer

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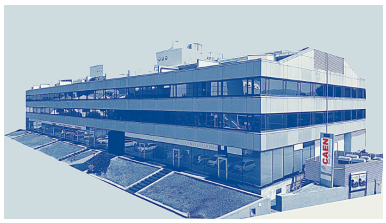

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