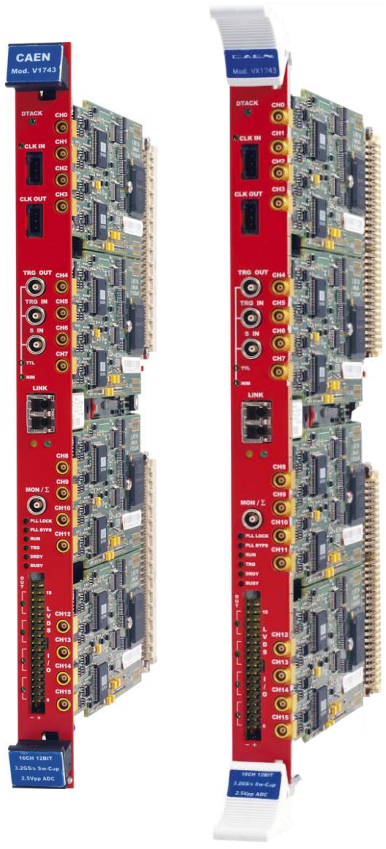
Rev. 5 - May 26th, 2025

V1743 & VX1743

16/8-channel 14-bit 500/250 MS/s Waveform Digitizer



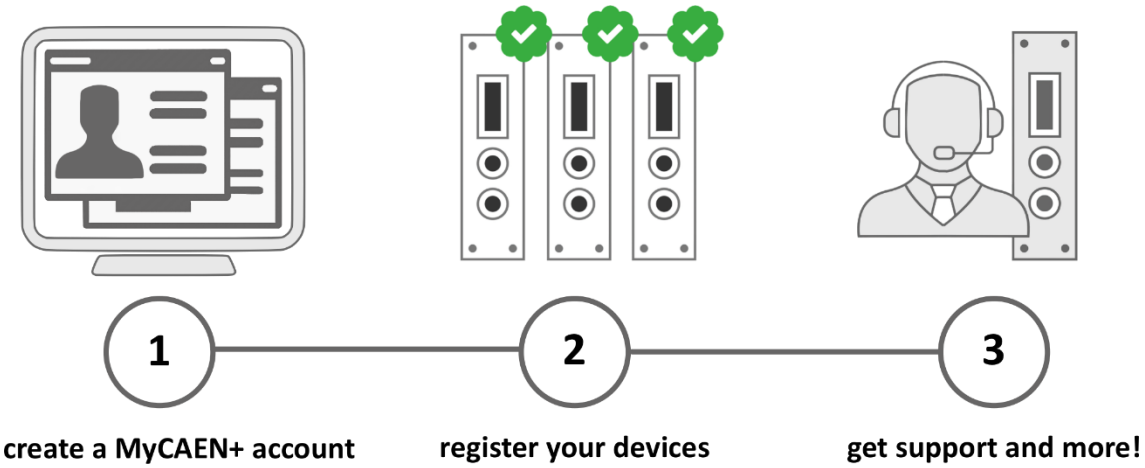
CAEN
Tools for Discovery

User Manual
UM2750

Register your device

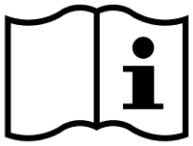
Register your device to your **MyCAEN+** account and get access to our customer services, such as notification for new firmware or software upgrade, tracking service procedures or open a ticket for assistance. **MyCAEN+** accounts have a dedicated support service for their registered products. A set of basic information can be shared with the operator, speeding up the troubleshooting process and improving the efficiency of the support interactions.

MyCAEN+ dashboard is designed to offer you a direct access to all our after sales services. Registration is totally free, to create an account go to https://www.caen.it/become-mycaenplus-user **and fill the registration form with your data.**



https://www.caen.it/become-mycaenplus-user/

Purpose of this Manual



This User Manual contains the hardware description of the V1743 and VX1743 Digitizers and their principle of operating referred to the firmware revision number **4.29_2.24**.
For higher firmware revisions, look at the Release Notes file of the firmware.

Change Document Record

Date	Revision	Changes
March 6th, 2015	00	Initial release
March 29th, 2016	01	Fully revised. Added Sections: **Digital Memory Buffer**, **BUSY Front Panel LED**, **Majority Level**, **Veto for the Trigger Rate Counter**, **Timer Reset**, **Troubleshooting**.
July 17th, 2017	02	Removed the explicit board registers information according to CAEN new policy.
November 20th, 2020	03	Updated **Chap. 3** and **Sec. Data Correction**
March 31st, 2022	04	Fully revised. Major updates: Sec. **Safety Notices**, Chap. **3**, Chap **18**, removed "Coming Soon" from Sec. **Multi-board Synchronization**, fixed the group data format in **Fig. 10.8**, removed Sec. Firmware Upgrades. Added Chap. **5**, Chap. **8**, Chap **15**, Chap. **16**, Chap. **17**, Sec**. Buffer Occupancy Mode**, Sec. **Firmware U**. Updated Sec. **Acquisition Modes** **Acquisition** Run/Stop, Sec. **Test Pattern** , Sec. **Hit Rate Monitor**, Sec. **Trigger Coincidence Level**, Sec. **TRG-IN as Gate**, Sec. **WaveDemo_x743**.
May 26th, 2025	05	Replaced CAENUpgrader with CAEN Toolbox references within the document. Updated **Tab. 1.1**. Added Sec. **10.7**. Updated Sec. **10.10.3.1**, Sec. **10.12.4**, Sec. **10.19.3**, Sec. **10.22**, Chap. **11**, Chap. **12**, Sec. **14.2**, Sec. **14.3**, Chap. **18**.

Symbols, Abbreviated Terms, and Notations

DLL	Delay Line Loop
INL	Integral Non-Linearity
LVDS	Low Voltage Digital Signal
PLL	Phase-Locked Loop
TDC	Time to Digital Converter
USB	Universal Serial Bus

Reference Documents

[RD1] UM11111 – CAEN Toolbox User Manual

[RD2] Precautions for Handling, Storage and Installation

[RD3] UM1935 - CAENDigitizer User & Reference Manual

[RD4] UM1934 - CAENComm User & Reference Manual

[RD5] UM2754 - WaveCatcher User Manual

[RD6] UM8789 – CAENWaveDemo_x743 User Manual

[RD7] UM10551 - A5818 User Manual.

[RD8] UM7685 - V3718 & VX3718 User & Reference Manual

[RD9] UM8305 - V4718 & VX4718 User & Reference Manual

[RD10] DS7799 - A4818 Adapter Data Sheet

[RD11] AN2472 - CONET1 to CONET2 Migration

All CAEN documents can be downloaded at:

https://www.caen.it/support-services/documentation-area/ (**login required**)

Manufacturer Contact

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Limitation of Responsibility

If the warnings contained in this manual are not followed, CAEN will not be responsible for damage caused by improper use of the device. The manufacturer declines all responsibility for damage resulting from failure to comply with the instructions for use of the product. The equipment must be used as described in the user manual, with particular regard to the intended use, using only accessories as specified by the manufacturer. No modification or repair can be performed.

Disclaimer

The information contained herein has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies. CAEN spa reserves the right to modify its products specifications without giving any notice; for up to date information please visit www.caen.it.

Made in Italy

We remark that all our boards have been designed and assembled in Italy. In a challenging environment where a competitive edge is often obtained at the cost of lower wages and declining working conditions, we proudly acknowledge that all those who participated in the production and distribution process of our devices were reasonably paid and worked in a safe environment (this is true for the boards marked "MADE IN ITALY", while we cannot guarantee for third-party manufactures).

Index

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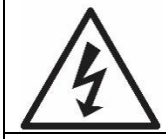
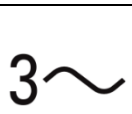
Safety Notices

N.B. Read carefully the "Precautions for Handling, Storage and Installation" document provided with the product before starting any operation.

The following HAZARD SYMBOLS may be reported on the unit:

	Caution, refer to product manual
	Caution, risk of electrical shock
	Protective conductor terminal
	Earth (Ground) Terminal
	Alternating Current
	Three-Phase Alternating Current

The following symbol may be reported in the present manual:

	General warning statement

The symbol could be followed by the following terms:

- **DANGER**: indicates a hazardous situation which, if not avoided, will result in serious injury or death.
- **WARNING**: indicates a hazardous situation which, if not avoided, could result in death or serious injury.
- **CAUTION**: indicates a situation or condition that, if not avoided, could cause physical injury, or damage the product and / or its environment.

CAUTION: Avoid potential hazards.

USE THE PRODUCT ONLY AS SPECIFIED.

ONLY QUALIFIED PERSONNEL SHOULD PERFORM SERVICE PROCEDURES

CAUTION: Avoid electric overload.

TO AVOID ELECTRIC SHOCK OR FIRE HAZARD, DO NOT POWER A LOAD OUTSIDE OF ITS SPECIFIED RANGE

CAUTION: Avoid electric shock.

TO AVOID INJURY OR LOSS OF LIFE, DO NOT CONNECT OR DISCONNECT CABLES WHILE THEY ARE CONNECTED TO A VOLTAGE SOURCE

CAUTION: Do not operate without covers.

TO AVOID ELECTRIC SHOCK OR FIRE HAZARD, DO NOT OPERATE THIS PRODUCT WITH COVERS OR PANELS REMOVED

CAUTION: Do not operate in wet/damp conditions

TO AVOID ELECTRIC SHOCK, DO NOT OPERATE THIS PRODUCT IN WET OR DAMP CONDITIONS

CAUTION: Do not operate in an explosive atmosphere.

TO AVOID INJURY OR FIRE HAZARD, DO NOT OPERATE THIS PRODUCT IN AN EXPLOSIVE ATMOSPHERE

CAUTION: Do not operate with suspected Failures.

IF YOU SUSPECT THIS PRODUCT TO BE DAMAGED, PLEASE CONTACT TECHNICAL SUPPORT

THIS DEVICE SHOULD BE INSTALLED AND USED BY SKILLED TECHNICIAN ONLY OR UNDER HIS SUPERVISION

CAUTION: This product needs proper cooling.

USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEATING MAY DEGRADE THE MODULE PERFORMANCES

V1743/VX1743 CANNOT BE OPERATED WITH CAEN CRATES VME8001, VME8002, VME8004, AND VME8004A. OVERHEAT MAY DAMAGE THE MODULE

CAUTION: this product needs proper handling.

THE VME DIGITIZER DOES NOT SUPPORT LIVE INSERTION (HOT SWAP)

REMOVE OR INSERT THE BOARD WHEN THE VME CRATE IS POWERD OFF

ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE

1 Introduction

The Mod. V1743 is a 1-unit wide VME 6U module housing a 16-channel 12-bit 3.2 GS/s Switched Capacitor Digitizer section, issued from the collaboration with CEA/IRFU & CNRS/IN2P3/LAL and based on the SAMLONG chip.

The input range is 2.5 V_{pp} (DC coupled) on single ended MCX coaxial connectors. The DC offset is adjustable in the ±1.25 V range via a 16-bit DAC on each channel (see Sec. **10.1**).

Considering the sampling frequency and the number of bits, it is well suited for very fast signals like those coming from fast scintillators coupled to PMTs, Silicon Photomultipliers, APD, Diamond detectors and others.

The analog input signals are continuously sampled inside the SAMLONG chips in a circular analog memory buffer (1024 cells) at the default sampling frequency of 3.2 GS/s (312.5 ps of sampling period); frequencies of 1.6 GS/s, 0.8 and 0.4 GS/s are also selectable by software. As a trigger signal arrives, all analog memory buffers are frozen and subsequently digitized with a resolution of 12 bits into a digital memory buffer with independent read and write access. Up to 7 full events per channel (1 event = 1024 * 12 bits) can be stored consecutively.

Each input channel is equipped with a discriminator with a 16-bit programmable threshold, which generates trigger requests. Requests from all channels are processed by the board to generate a common trigger causing all the channels to acquire an event simultaneously. The common board trigger can also be provided externally by software command, or by the front panel TRG-IN input, or by any combination of the channel discriminators and/or the TRG-IN.

During analog to digital conversion process, the V1743 cannot handle other triggers, thus generating a dead time (maximum 125 µs, decreasing proportionally with the configurable recording depth).

Each input channel is equipped with an individual hit rate monitor based on its own discriminator and on two counters giving the number of hits which cross the programmed discriminator threshold (also during the dead-time) and the time elapsed with a 1-MHz clock (see Sec. **10.18**). This permits among others measuring the hit rate with respect to the signal amplitude.

Each input channel is equipped with a digital programmable charge integrator which permits a high-rate measurement in charge mode (see Sec. **10.10.2**).

Each pair of channels is equipped with a 40-bit TDC (counter) tagging the trigger with the clock delivered to the SAMLONG chips (200 MHz down to 25 MHz depending on the selected sampling frequency).

V1743 houses a fixed amplitude pulser on each analog input, which permits an easy complete functionality test and the use of the module in reflectometer mode (see Sec. **10.17**).

The module features the front panel CLK IN/CLK OUT connectors and an internal PLL for clock synthesis from internal/external references. The V1743 supports multi-board synchronization, allowing all SAMLONG chips to be synchronized with a common clock source and ensuring Trigger Time Stamps alignment. Once synchronized, all data will be aligned and coherent across multiple V1743 boards.

A FPGA-controlled 16 general purpose LVDS I/O connector provides programmed functions (e.g. Trigger Time Tag reset, Run Status, Memory Clear, etc.). An Input Pattern (external signal) can be provided on the LVDS I/Os to be latched to each trigger as an event marker (see Sec. **10.15**).

An analog output (front panel MON/Σ connector) from the internal 12-bit 100MHz DAC, controlled by the FPGA, is programmed to provide a signal whose amplitude is proportional to the number of over-threshold channels or a DC voltage level increasing proportionally with the number of buffers of the digital memory being filled with events (see Sec. **10.16**).

The VME interface of the module is VME64X compliant, and the data readout can be performed in several data transfer modes: BLT32, MBLT64 (up to 70 MB/s of transfer rate using CAEN Bridge), CBLT32/64, 2eVME, 2eSST (up to 200 MB/s of transfer rate). The Optical Link interface implements CONET proprietary protocol and it is able to transfer data at 80 MB/s to a CONET slave. Thanks to Daisy chain capability, it is possible to connect up to 8 boards over a single optical link (with A5818 Controller or A4818 Adapter) for a total of 32 boards in the case of the 4-link A5818 Controller.

CAEN provides the drivers for each supported communication link, the WaveCatcher readout software, and a set of libraries and demos to manage the x743 boards and develop customized software (see Chap. **11** and Chap. **12**).

Board Models	Description
V1743	16 Ch. 12 bit 3.2GS/s Switched-Capacitor Digitizer: 7 events/ch (1kS/event), EP3C16, SE, VME64 Digitizer
VX1743	16 Ch. 12 bit 3.2GS/s Switched-Capacitor Digitizer: 7 events/ch (1kS/event), EP3C16, SE, VME64X Digitizer
Related Products	**Description**
A2818	PCI 1-Link Optical Controller **OBSOLETE**
A3818A	PCIe 1-Link Optical Controller **OBSOLETE**
A3818B	PCIe 2-Link Optical Controller **OBSOLETE**
A3818C	PCIe 4-Link Optical Controller **OBSOLETE**
A4818	USB-3.0 to Optical Link Adapter
A5818	PCI Express Gen 3 CONET2 Controller
V3718	VME to USB2/CONET Bridge, VME64
VX3718	VME to USB2/CONET Bridge, VME64X
V4718	VME to USB 3.0/Ethernet/CONET Bridge, VME64
VX4718	VME to USB 3.0/Ethernet/CONET Bridge, VME64X
VME8004B	VME8004B VME8004B - 2U 4 Slot VME64 Mini Crate
VME8004X	VME8004X VME8004X - 2U 4 Slot VME64X Mini Crate
VME8008B	VME8008B VME8008B - 4U 8 Slot VME64 Mini Crate
VME8008X	VME8008X VME8008X - 4U 8 Slot VME64X Mini Crate
VME8010	VME8010 VME8010 - 7U 21 Slot VME64 Low Cost Crate
VME8011	VME8011 VME8011 - 7U 21 Slot VME64 Low Cost Crate, pluggable power supply
VME8100	VME8100 VME8100 - 8U 21 Slot VME64/64X Enhanced Crate Series
VME8200	VME8200 VME8200 - 9U 21 Slot VME64X Enhanced Crate series
µ-Crate	µ-Crate µ-Crate - Desktop single-slot VME64X Crate
Accessories	**Description**
A316	Cable assembly for LVDS distribution 2.54mm 2-pin header female terminations, 5 cm
A317	Cable assembly for clock distribution 3-pin AMPMODU IV female terminations, 18 cm
A317L	Cable assembly for clock distribution 3-pin AMPMODU IV female terminations, 25 cm
A318	Adapter for Clock signal FISCHER S101A004 male to 3-pin AMPMODU IV female, 10 cm
DT4700	Clock Generation board, desktop
A654	Cable assembly LEMO 00 male to MCX male, 1 m
A654 KIT4	KIT = 4x Cable assembly LEMO 00 male to MCX male, 1 m
A654 KIT8	KIT = 8x Cable assembly LEMO 00 male to MCX male, 1 m
A659	Cable assembly BNC male to MCX male, 1 m
A659 KIT4	KIT = 4x Cable assembly BNC male to MCX male, 1 m
A659 KIT8	KIT = 8x Cable assembly BNC male to MCX male, 1 m
A952	Cable assembly 2.54mm 34 pin female to 2.54mm 34 pin female, 50 cm
A953	Cable assembly 2.54mm 34 pin female to two 2.54mm 34 pin female, 50 cm
A954	Cable assembly 2.54mm 34 pin female to two 2.54mm 16 pin female, 50 cm
AI2740	Optical Fibre 40 m simplex
AI2730	Optical Fibre 30 m simplex
AI2720	Optical Fibre 20 m simplex
AI2705	Optical Fibre 5 m simplex
AI2703	Optical Fibre 30 cm simplex
AY2730	Optical Fibre 30 m duplex
AY2720	Optical Fibre 20 m duplex
AY2705	Optical Fibre 5 m duplex

Tab. 1.1: Table of models and related items

2 Block Diagram

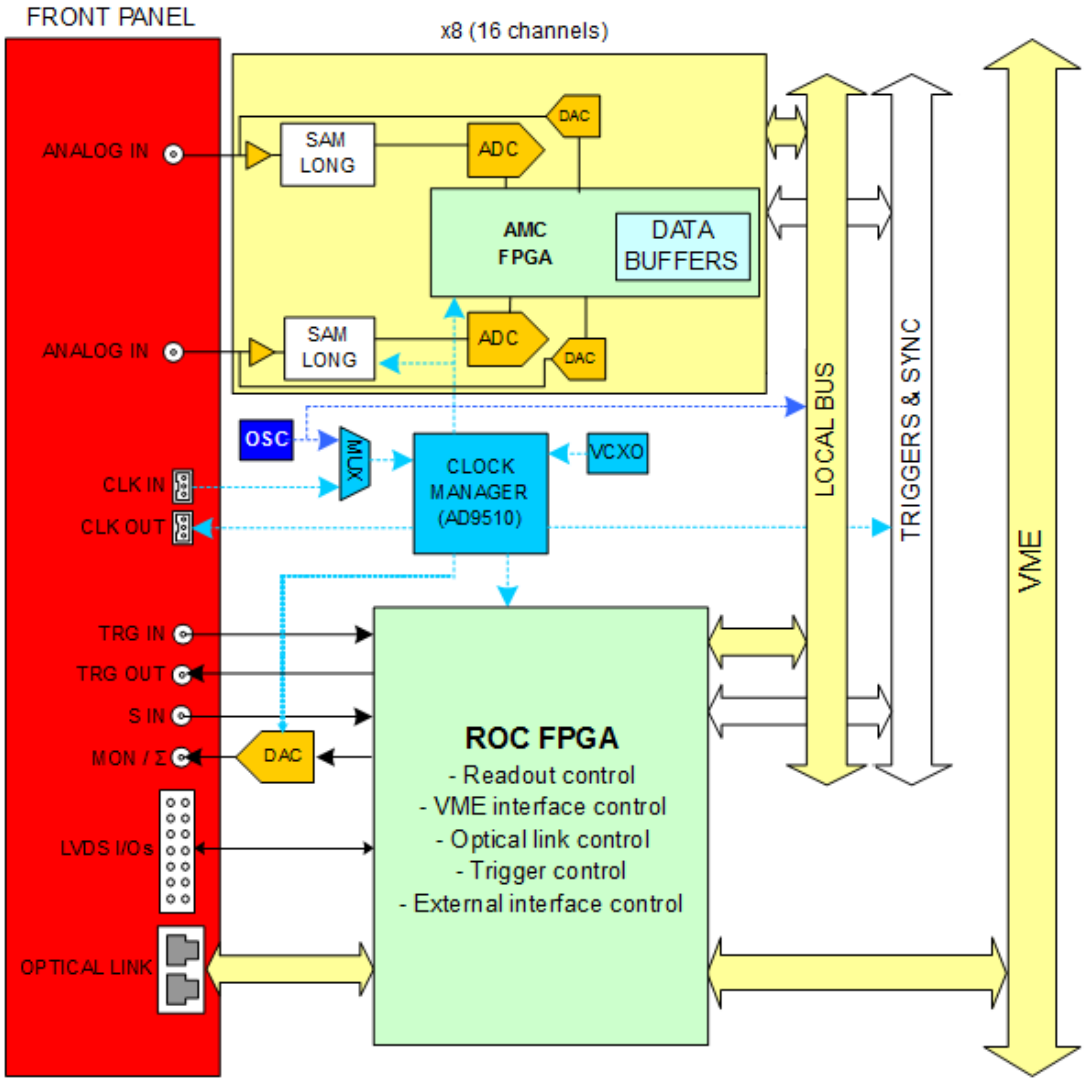


Fig. 2.1: Block Diagram

3 Technical Specifications

GENERAL	**Form Factor** 1-unit wide, 6U VME64 (V1743) and VME64X (VX1743)	**Dimensions** 6U x 160 mm	**Weight** 535 g
ANALOG INPUTS	**Channels** 16 channels Single ended **Impedance (Z_{in})** 50 Ω **Absolute max analog input voltage** ±3.5 V	**Connector** MCX **Full Scale Range (FSR)** 2.5 V_{pp} DC coupled	**Bandwidth** 500 MHz **DC Offset** Programmable 16-bit DAC for DC offset adjustment on each channel. Range: ±1.25 V
TEST FUNCTION	One pulser per channel with programmable 16-bit pattern (fixed amplitude)		
DIGITAL CONVERSION	**Resolution** 12 bits **Switched Capacitor Array** SAMLONG Fast Analog Memory chip, 2 channels with 1024 storage cells/ch 320 ns minimum recorded time/event	**Sampling Rate** 3.2 GS/S - 1.6 GS/s - 0.8 GS/s - 0.4 GS/s SW selectable, simultaneously on each channel	**Dead-Time (Event A/D Conversion)** 125 µs (max. @ 1024 samples) decreasing proportionally with the depth recording (configurable record length)
CHANNEL FPGA	Altera Cyclone EP3C16 (one FPGA serves 4 channels)		
TRIGGER	**Trigger Source** - *Self-trigger*: channel over/under threshold (based on analog discriminator on each channel with DAC adjusted threshold) for Common trigger generation - *External-trigger*: common trigger by TRG-IN connector - *Software-trigger*: common trigger by software command	**Trigger Propagation** TRG-OUT programmable digital output **Trigger Time Stamp** 40-bit counter, 5-ns resolution, 83-min range Timer reset by S-IN connector **Trigger Threshold** Programmable 16-bit DAC output per channel (±1.25V)	
ACQUISITION MEMORY	7 full event/ch @ 1024 S/event Multi-event Buffer Independent read and write access; programmable event size and post-trigger		
TIMING RESOLUTION	< 8 ps RMS (5 ps RMS typical) @ 3.2GS/s Obtained at thermal regime, after INL time calibration and with dual-pulse timing measurement by pulse generator **Test conditions:** periodic input pulses with 1V Amplitude, 1kHz Frequency, rise time of 0.8/1.6/2.5 ns; the resolution does not change significantly when varying the delay Δt between the two pulses **Note:** it is recommended to provide proper cooling to improve the resolution performances		
NOISE LEVEL	0.75 mV RMS		
ADC CLOCK GENERATION	Clock source: internal/external. On-board programmable PLL provides generation of the main board clocks from an internal (50 MHz loc. oscillator) or external (front panel CLK-IN connector) reference		
DIGITAL I/O	**CLK-IN (AMP Modu II)** AC coupled differential input clock: LVDS, ECL, PECL, LVPECL, CML (single ended NIM/TTL available by A318 adapter) Z_{diff}: 100 Ω Accuracy < 100 ppm **CLK-OUT (AMP Modu II)** DC coupled differential LVDS clock output locked at ADC sampling clock Z_{diff}: 100 Ω	**TRG-IN (LEMO)** External trigger digital input: NIM/TTL Signal width > 10 ns Z_{in} = 50 Ω **TRG-OUT (LEMO)** Trigger digital output: NIM/TTL R_t = 50 Ω (external)	**S-IN (LEMO)** SYNC/START front panel digital input: NIM/TTL Signal width > 10 ns Z_{in} = 50 Ω **LVDS I/O** 16 general purpose LVDS I/O controlled by the FPGA: Busy, Data Ready, Memory full, Memory Clear, TTT reset and other functions can be programmed. An Input Pattern from the LVDS I/O can be associated to each trigger as an event marker
ANALOG MONITOR OUTPUT	12-bit / 100MHz DAC FPGA-controlled; operating modes: - Majority signal output (default): proportional to the number of the over-threshold channels (in steps of 125 mV) - Memory occupancy signal output: DC voltage level increasing in fixed steps of 0.976 mV (amplifiable) with the memory filling with events		
SYNCHRONIZATION	**Clock Propagation** *Daisy chain*: through CLK-IN/CLK-OUT connectors. *One-to-many:* clock distribution from an	**Acquisition Synchronization** Sync, Start/Stop through LVDS I/Os (S-IN or TRG-OUT input / TRG-OUT output)	

	external clock source to CLK-IN connector. Clock Cable delay compensation		**Trigger Time Stamps Aligment** By S-IN input connector **Data Alignment** Busy/Veto through LVDS I/Os
COMMUNICATION INTERFACES	**Optical Link** CAEN CONET proprietary protocol Up to 80 MB/s transfer rate Daisy-chain: maximum 8 ADC modules connectable to the A4818 Adapter; 32 ADC modules to a A5818 Controller (8 per link)		**VME** VME 64X compliant Data transfer mode: BLT32, MBLT64 (70 MB/s by CAEN Bridge), CBLT32/64, 2eVME, 2eSST (200 MB/s)
FIRMWARE	**Normal Mode (default)** Waveform recording **Charge Mode (sw selectable)** Input pulse high-rate charge integration		**Upgrades** Supported via VMEbus/Optical Link
SOFTWARE	**Readout SW** *WaveCatcher* (Windows® only) *WaveDemo_x743* (Windows®, Linux®) including C source files and VS project.		**Libraries and Tools** General purpose C libraries (Windows®, Linux®) Configuration tools
ENVIRONMENTAL	**Environment:** Indoor use **Operating Temperature:** 0◦C to +40◦C **Storage Temperature:** –10◦C to +60◦C **Operating Humidity:** 10% to 90% RH non condensing **Storage Humidity:** 5% to 90% RH non condensing **Altitude:** < 2000m **Pollution Degree:** 2 **Overvoltage Category:** II **EMC Environment:** Commercial and light industrial **IP Degree:** IPX0 Enclosure, not for wet location		
REGULATORY COMPLIANCE	**EMC** CE 2014/30/EU Electromagnetic Compatibility Directive		**Safety** CE 2014/35/EU Low Voltage Directive
POWER REQUIREMENTS	@ +5V 4 A (max.)	@ +12 V 625 mA	@ -12V *not used*

Tab. 3.1: Specifications table

4 Packaging and Compliancy

The V1743/VX1743 digitizer modules are available in 1-unit wide VME64/VME64X boards, EMC compliant.

The device is inspected by CAEN before the shipment, and they are guaranteed to leave the factory free of mechanical or electrical defects.

The content of the delivered package standardly consists of the part list shown in the table below (**Tab. 4.1**).

	Part	Description	Qt
	V1743/VX1743	16 Channel 12 bit 3.2 GS/s Digitizer	x1
	Documentation	UM2750 – V1743 & VX1643 User Manual	-

Tab. 4.1: Delivered kit content

CAUTION: to manage the product, consult the operating instructions provided.

When receiving the unit, the user is strictly recommended to:

- Inspect containers for damage during shipment. Report any damage to the freight carrier for possible insurance claims.
- Check that all the components received match those listed on the enclosed packing list as in **Tab. 4.1**. (CAEN cannot accept responsibility for missing items unless we are notified promptly of any discrepancies.)
- Open shipping containers; be careful not to damage contents.
- Inspect contents and report any damage. The inspection should confirm that there is no exterior damage to the unit such as broken knobs or connectors and that the front panel and display face are not scratched or cracked. Keep all packing material until the inspection has been completed.
- If damage is detected, file a claim with carrier immediately and notify CAEN service (see Chap. **18**).
- If equipment must be returned for any reason, carefully repack equipment in the original shipping container with original packing materials if possible. Please, contact CAEN service (see Chap. **18**).
- If equipment must not be installed soon after unpacking, place it in the original shipping container and store in a safe place until ready to install

DO NOT SUBJECT THE ITEM TO UNDUE SHOCK OF VIBRATIONS

DO NOT BUMP, DROP OR SLIDE SHIPPING CONTAINERS

DO NOT LEAVE ITEMS OR SHIPPING CONTAINERS UNSUPERVISED IN AREAS WHERE UNTRAINED PERSONNEL MAY MISHANDLE THE ITEMS

USE ONLY ACCESSORIES WICH MEET THE MANUFACTURER SPECIFICATIONS

For the correct and safe use of the module, refer to Chap. **6** and Chap. **7**.

5 PID (Product Identifier)

PID is the CAEN product identifier, an incremental number greater than 10000 that is unique for each product. The PID is on a label affixed to the product (**Fig. 5.1**) and it is even stored in an on-board non-volatile memory, readable by CAENDigitizer library function**[RD3]** or through CAENToolbox Software**[RD1]**.

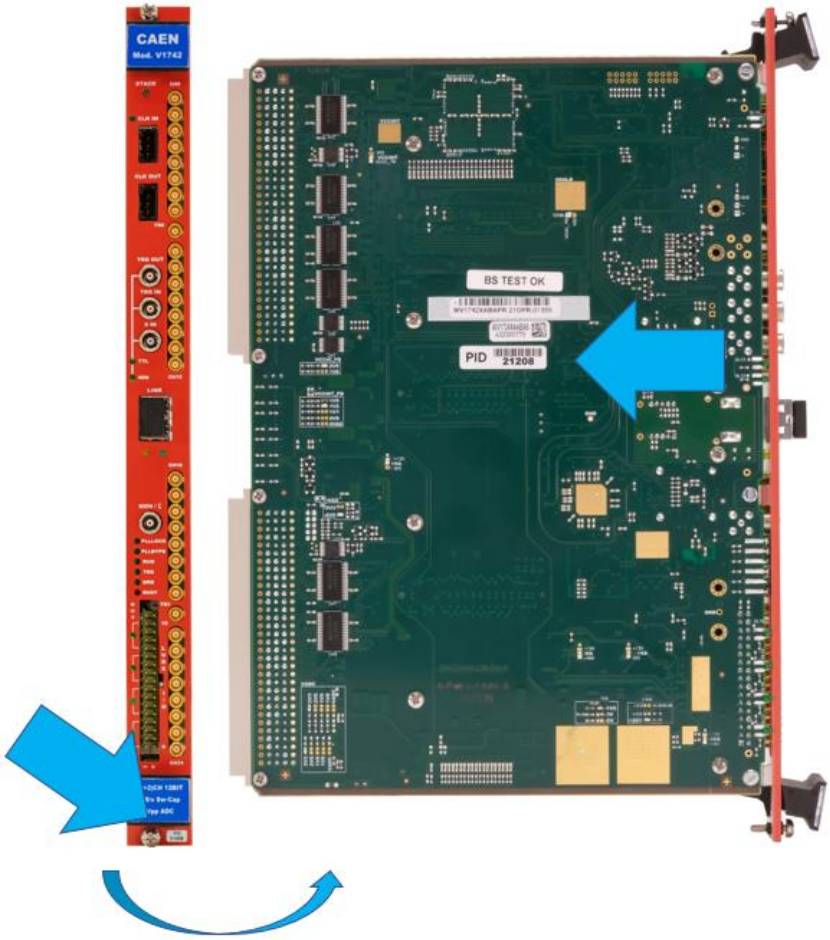


Fig. 5.1:PID location on V1743/VX1743 (the module and number in the picture are purely indicative)

6 Power Requirements

The table below resumes the V1743/VX1743 power consumptions per relevant power supply voltage.

MODULE	SUPPLY VOLTAGE		
	+5 V	+12 V	-12 V
V1743/VX1743	5 A (max.)	625 mA (max.)	*Not used*

Tab. 6.1: Power requirements table

7 Cooling Management

The V1743/VX1743 Digitizers can operate in the external temperature range of 0° ÷ +40°C **[RD2]**.

The VME models must be operated in ventilated crates as recommended in the **Safety Notices**.

EXTERNAL FANS MUST BE USED WHEN THE BOARD IS INSTALLED IN A SETUP WITH POOR AIR FLOW

V1743 DIGITIZERS CANNOT BE OPERATED WITH CAEN CRATES VME8001, VME8002, VME8004, AND VME8004A. OVERHEAT MAY DAMAGE THE MODULE

The User must take care to provide a proper cooling to the board with external fan if the board is used in an enclosure or if the board is installed into a setup with poor air flow.

Excessive temperature will, in first instance, reduce the performance and the quality of the measurements and can also damage the board.

If the board is stored in cold environment, please check for water condensation before power on.

The board has not been tested for radiation hardness. High energy particles can be source of errors and can damage the FPGA. If used in strong proton or neutron beams, arrange proper shielding or remote the sensors with a custom cable.

7.1 Cleaning Air Vents

CAEN recommends to occasionally clean the air vents on all vented sides of the board or crate, if present.

Lint, dust, and other foreign matter can block the vents and limit the airflow. Be sure to power off the board and disconnect it from the power by physically detach the power chord before cleaning the air vents and follow the general cleaning safety precautions.

IT IS UNDER THE RESPONSIBILITY OF THE CUSTOMER A NON-COMPLIANT USE OF THE PRODUCT

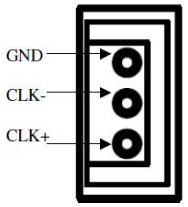
8 Panels Description

V1743 and VX1743 present the same front panel structure.

Fig. 8.1: Front panel view

8.1 Front Panel

CHx		
	**DESCRIPTION** Analog input connector **FUNCTION** CH[i] (i = 0 to 15) receives signals from the detector **ELECTRICAL SPECS** Input dynamic: 2.5 V_{pp} Input impedance (Z_{in}): 50 Ω Abs. max. analog input voltage: ±3.5 V	**MECHANICAL SPECS** Series: MCX connectors Type: CS 85MCX-50-0-16 (jack/female) Manufacturer: SUHNER Suggested plug/male: MCX-50-2-16 Suggested cable: RG174 type

CLK IN / CLK OUT		
	**DESCRIPTION** Input and output clock connectors **FUNCTION** CLK-IN accepts an external reference clock CLK-OUT propagates the clock externally CLK-IN and CLK-OUT can be used to daisy chain clock in multi-board synchronization (A317 cable available: see **Tab. 1.1**) **ELECTRICAL SPECS** Signal Level: differential LVDS, ECL, PECL, LVPECL, CML. Single-ended-to-differential A318 cable available for CLK-IN (see **Tab. 1.1**) Coupling: AC (CLK-IN); DC (CLK-OUT) Z_{diff}: 100 Ω Accuracy < 100 ppm	**MECHANICAL SPECS** Series: AMPMODU connectors Type: 3-102203-4 (3-pin) Manufacturer: AMP Inc. **PINOUT** 

CLK IN LED (GREEN): indicates the external clock is enabled.

TRG IN / TRG OUT / S IN

DESCRIPTION

General purpose digital I/O connectors

FUNCTION

- TRG-OUT provides out the OR of the following trigger sources:
  - software trigger (default)
  - external trigger
  - ORed trigger requests from the enabled channel couples

See also Sec. **10.13**

- TRG-IN is the external trigger input
- S-IN: SYNC/START/STOP input configurable as reset of the time stamp (Sec. **10.19.3**) or as acquisition start/stop (Sec. **10.10**)

ELECTRICAL SPECS

Signal level: single-ended NIM/TTL, sw selectable

TRG-IN/S-IN input impedance (Z_{in}): 50 Ω

TRG-OUT requires 50 Ω termination

MECHANICAL SPECS

Series: 101 A 004 connectors

Type: DLP 101 A 004-28

Manufacturer: FISCHER

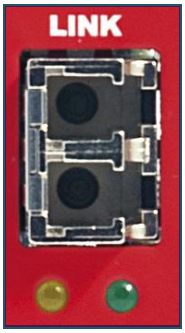
Alternatively:

Type: EPL 00 250 NTN

Manufacturer: LEMO

TTL (GREEN), NIM (GREEN): indicates the standard TTL or NIM is set for TRG-OUT, TRG-IN, and S-IN.

LINK



DESCRIPTION

Optical link port

FUNCTION

Data readout and flow control through optical link. Daisy chainable. Compliant with optical fibers 50/125 µm OM2 and OM3 (back compliant with 62.5/125 µm OM1) featuring LC connectors on both sides

ELECTRICAL SPECS

Transfer rate: up to 80 MB/s

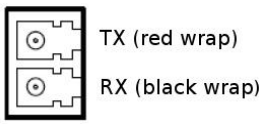
MECHANICAL SPECS

Series: SFF Transceivers

Type: FTLF8519F-2KNL (LC connectors)

Manufacturer: FINISAR

PINOUT



LINK LEDs (GREEN/YELLOW): LED on the right (GREEN) indicates the network presence, while LED on the left (YELLOW) signals the data transfer activity.

MON / Σ

DESCRIPTION

Analog Monitor programmable output connector.

FUNCTION

Single-ended output, software configurable in:

- Trigger Majority mode (default)
- Memory Occupancy Monitor Mode

See Sec. **10.16**.

ELECTRICAL SPECS

12-bit, 100MHz DAC output
$1V_{pp}$ on R_t=50 Ω

MECHANICAL SPECS

Series: 101 A 004 connectors

Type: DLP 101 A 004-28

Manufacturer: FISCHER

Alternatively:

Type: EPL 00 250 NTN

Manufacturer: LEMO

DIAGNOSTIC LEDs

DTACK (GREEN): indicates there is a VME read/write access to the board

PLL LOCK (GREEN): indicates the PLL is locked to the reference clock

PLL BYPS (GREEN): *not used*

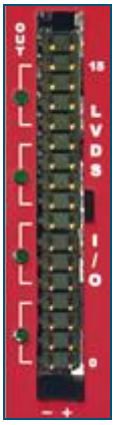
RUN (GREEN): indicates the acquisition is running (data taking)

TRG (GREEN): indicates the trigger is accepted

DRDY (GREEN): indicates the event/data is present in the Output Buffer

BUSY (RED): indicates the board is either in dead-time condition during the analog-to-digital conversion or that all the buffers are full for at least one channel

LVDS I/O



DESCRIPTION

General purpose 16-pin LVDS I/O connector

FUNCTION

Detailed in Sec. **10.15**

ELECTRICAL SPECS

Signal Level: differential LVDS

Z_{diff}: 100 Ω

MECHANICAL SPECS

Series: TE - AMPMODU Mod II Series

Type: 5-826634-0

Lead spacing: 2.54mm

Row pitch: 2.54mm

Manufacturer: AMP Inc.

LVDS I/O LEDs (GREEN): Each LED close to a 4-pin group lights on if the pins are set as outputs.

IDENTIFICATION LABELS	
	On top and bottom of insertion/extraction handle: • Manufacturer • Model name • Brief ADC features
	On the bottom (V1743) or on the handle (VX1743): • Product Identifier (PID) **Note:** For older boards, a 4-digit Serial Number (S/N) is reported on a little serigraph on the bottom of the VME board front panel.

9 Internal Components

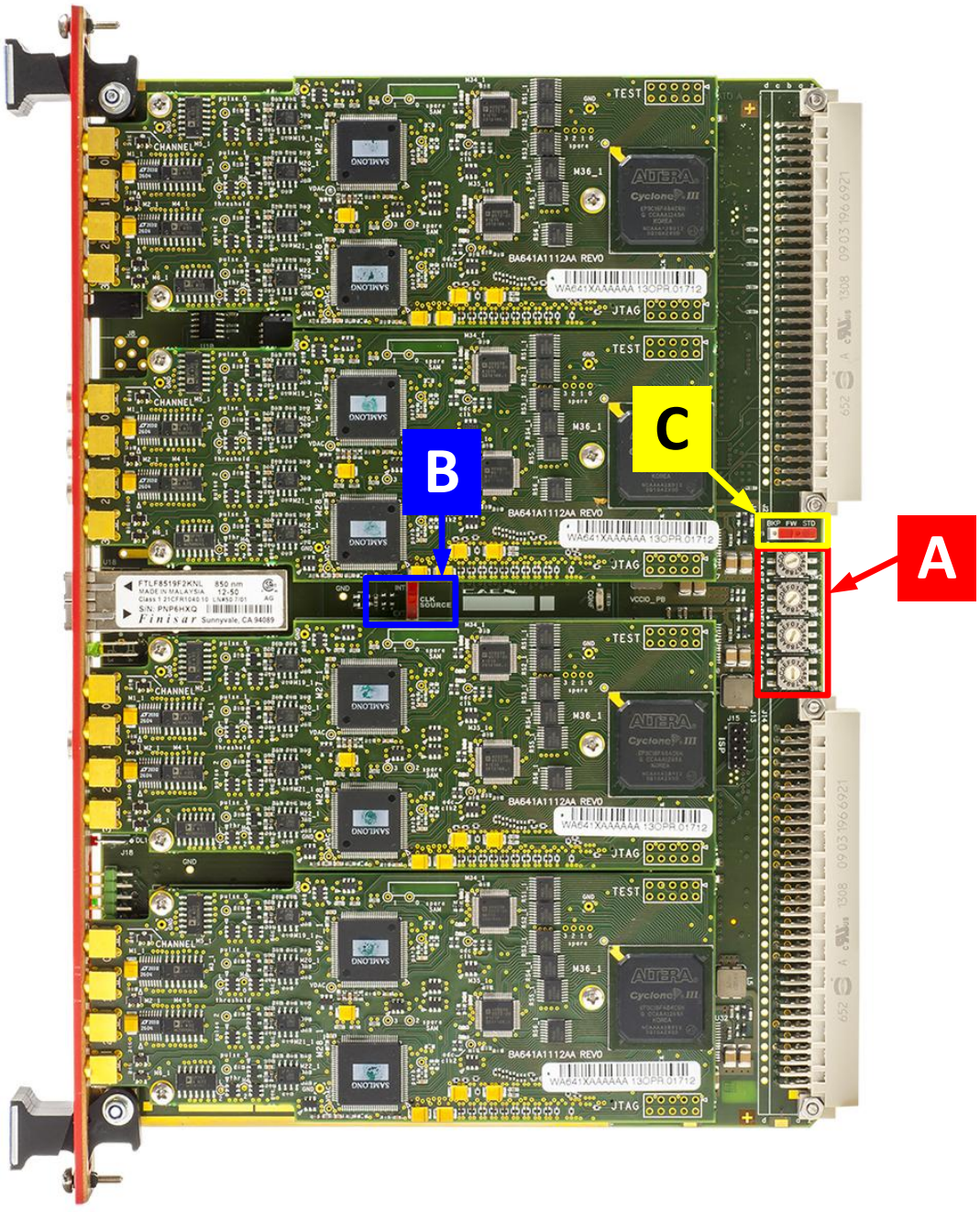


Fig. 9.1: Rotary and dip switches location

A	**SW3, 4, 5, 6:** **"Base Address [31:16]"**	**Type:** Rotary Switches	**Function:** Set the VME Base Address of the module
B	**SW2:** **"CLOCK SOURCE" INT/EXT**	**Type:** Dip Switch	**Function:** Selects the clock source (External or Internal)
C	**SW7:** **"FW" BKP/STD**	**Type:** Dip Switch	**Function:** Selects between the "Standard" (STD) and the "Backup" (BKP) FLASH page as the first to be read at power-on to load the FW on the FPGAs (default position: STD). See Chap. **14**.

10 Functional Description

10.1 Analog Input Stage

The input dynamic is 2.5 V_{pp} on the single ended MCX coaxial connectors (Z_{in} = 50 Ω). To preserve the full dynamic range according to the polarity of the input signal (bipolar, positive unipolar, negative unipolar), it is possible to add a DC offset by means of a 16-bit DAC, which is up to a ±1.25 V DC. The input bandwidth ranges from DC to 500 MHz (with 2nd order linear phase anti-aliasing low pass filter).

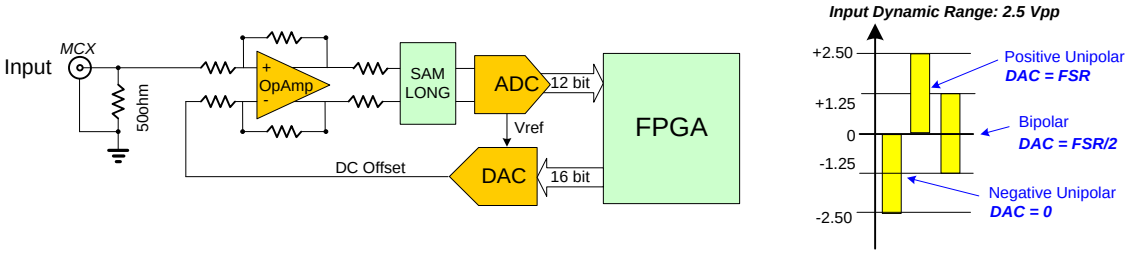


Fig. 10.1: Analog Input Diagram

The DC offset can be managed individually per each channel by WaveCatcher software**[RD5]** or through the *Set/GetChannelDCOffset()* functions of the CAENDigitizer library**[RD3]**.

10.2 Sampling in the Analog Memory

The analog input signals from each pair of channels are continuously sampled into one SAMLONG chip, which consists of a matrix of Delay Line Loops (DLLs) generating a 3.2 GS/s sampling frequency from an input clock of 200 MHz; 1.6 GS/s, 0.8 and 0.4 GS/s frequencies can be also programmed (see Sec. **10.6**).

Signals produced by the DLLs simultaneously open write switches in both sampling channels, where the differential input signals are sampled (1024 sampling capacitance cells per channel).

After being started by the so-called "Run" signal (corresponding to the WRITE signal on **Fig. 10.2**) going high, the DLLs run continuously in a circular fashion (after reaching the end of the matrix, samples are over written) until decoupled from the write switches when the Run signal goes down. This actually takes place after the arrival of a trigger signal synchronously delayed by the so-called post-trigger delay (managed by the *SetSAMPostTriggerSize()* function of the CAENDigitizer library**[RD3]**), which finally provokes the freezing of the currently stored signal in the sampling capacitance cells.

Subsequently, the cells are multiplexed into the 12-bit ADCs whose output are stored by the FPGA into the Digital Memory Buffer and made ready for readout in the shape of events data.

A 16-bit DAC allows to add up a ±1.25 V DC offset to preserve the full dynamic range also in the extreme case of unipolar positive or negative input signals (see Sec. **10.1**).

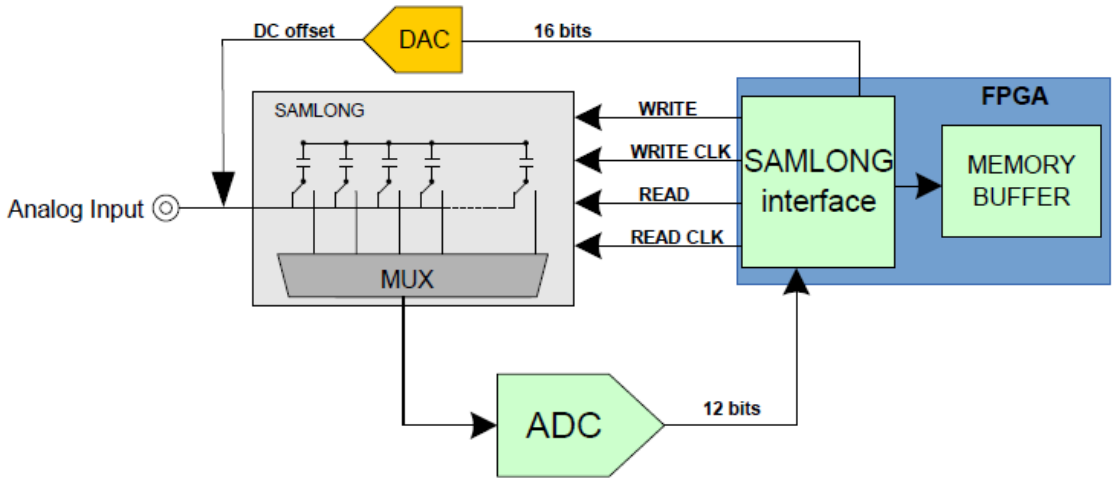


Fig. 10.2: Input Diagram

Detailed documentation of the SAMLONG chip is available at:

http://electronique.lal.in2p3.fr/echanges/USBWaveCatcher/Documentation/Boards&Chips/doc_SAMLONG_rev1.pdf

(in case the active link above does not work, copy and paste it on the internet browser)

10.3 Digital Memory Buffer

Each pair of input channels shares a SRAM memory in the channel FPGA (see **Fig. 2.1**) that is organized into buffers whose number depends on the event size. This Digital Memory can consecutively store up to 7 full events per channel (1 full event = 1024 samples). It is possible to configure the board to read less than 1024 samples per event, so extending the number of events consecutively storable in the Digital Memory. This option is managed by the *SetRecordLength()* function of the CAENDigitizer library**[RD3]** and by WaveCatcher software**[RD5]**.

10.4 Clock Distribution

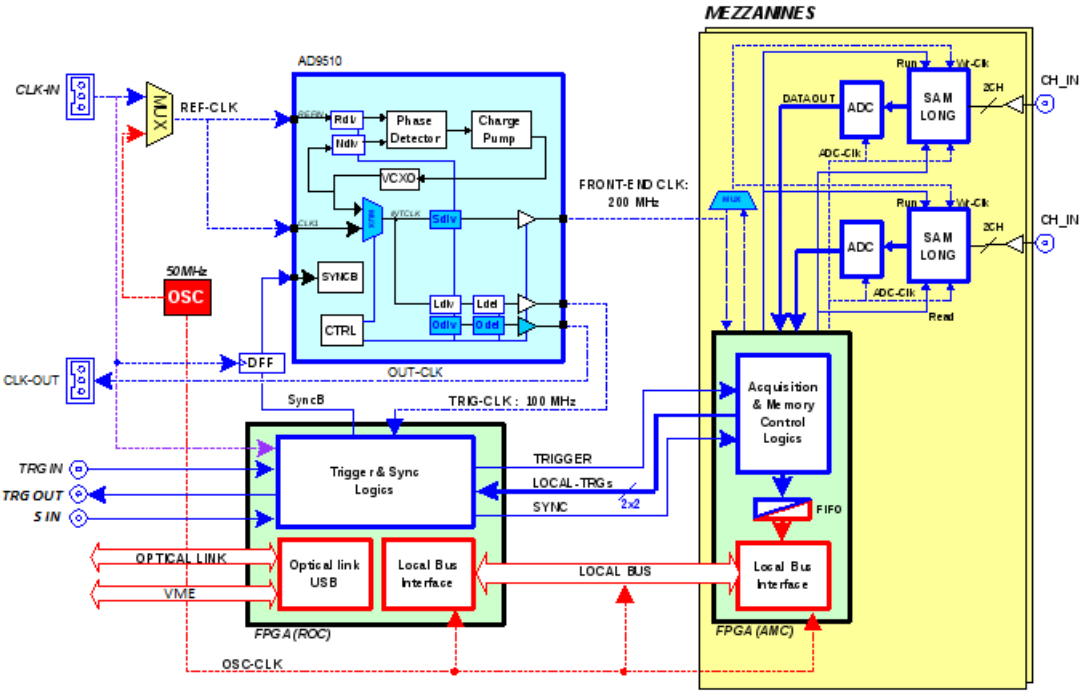


Fig. 10.3: Clock Distribution Diagram

The clock distribution of the module takes place on two domains: OSC-CLK and REF-CLK.

OSC-CLK is a fixed 50-MHz clock coming from a local oscillator which handles VMEbus, Optical Link and Local Bus, that takes care of the communication between motherboard and mezzanines (see red traces in **Fig. 10.3**).

REF-CLK handles ADC sampling, trigger logic, and acquisition logic (samples storage into RAM, buffer freezing on trigger) through a clock chain. REF-CLK can be either an external source (via front panel signal on CLK-IN connector) or an internal one (via local oscillator). In the latter case, OSC-CLK and REF-CLK will be synchronous (the operating mode remains the same).

REF-CLK clock source selection can be done by on-board dip switch (see Chap. **9**) between:

- INT mode (default) means that REF-CLK is the 50 MHz frequency of the local oscillator (REF-CLK = OSC-CLK)
- EXT mode means that REF-CLK is the external frequency fed on CLK-IN connector

The external CLK-IN signal must be differential (LVDS, ECL, PECL, LVPECL, CML) with accuracy lower than 100 ppm.

The board mounts a phase-locked-loop (PLL) and clock distribution device, AD9510. It receives the REF-CLK and processes it to generate the 200-MHz clock signals delivered directly to SAMLONG chips (WRITE_CLK in **Fig. 10.2**, Wr_Clk in **Fig. 10.3**) and to the mezzanine FPGA. The latter will divide it to produce a 10 MHz clock used both for the readout of the SAMLONG chips (READ_CLK on **Fig. 10.2**) and for driving the ADC conversion (ADC_Clk on **Fig. 10.3**). The AD9510 device also provides a 100 MHz clock to the trigger logics.

Refer to the AD9510 datasheet for more details:

https://www.analog.com/media/en/technical-documentation/data-sheets/AD9510.pdf

(in case the active link above does not work, copy and paste it on the internet browser)

When running with the reduced sampling frequencies (see Sec. **10.6**), the 200 MHz clock is divided inside the mezzanine FPGA before being sent to the SAMLONG chips via the clock multiplexer as shown in **Fig. 10.3**.

10.5 PLL Mode

As introduced in Sec. **10.4**, the source of the REF-CLK signal (see **Fig. 10.2**) can be external on CLK-IN front panel connector or internal from the 50MHz local oscillator (default option). Selecting the REF-CLK source internal or external can be performed by acting on the on-board dip switch SW2 (see Chap. **9**). Selecting the external clock source, the front panel CLK-IN LED must be on (see Sec. **8.1**).

The following options are allowed:

1. 50 MHz internal clock source – This is the standard operating mode: AD9510 dividers do not require to be reprogrammed (the digitizer works in the AD9510 default configuration). Onboard clock source selection switch SW2 is set to INT. OSC-CLK = REF-CLK.
2. 50 MHz external clock source – In this case, the clock source is generated externally; AD9510 dividers do not need to be reprogrammed, as the external frequency is the same as the default one. Onboard clock source selection switch SW2 must be set to EXT. CLK-IN = OSC-CLK = REF-CLK.
3. External clock frequency different from 50 MHz – The clock source is externally provided as in point 2. In this case, AD9510 dividers must be reprogrammed to lock the VCXO to the new REF-CLK and still provide the nominal sampling frequency. Onboard clock source selection switch SW2 must be set to EXT. CLK-IN = REF-CLK≠ OSC-CLK.

Whichever the PLL mode is set, the PLL-LOCK front panel LED must be on if the digitizer is locked.

Note: Users can configure the clock parameters, generate the PLL programming file and load it on the board by using the CAEN Toolbox software**[RD1]**

10.6 Changing the Sampling Frequency

The sampling frequency of the SAMLONG chips can be programmed by software through WaveCatcher or the *SetSAMSamplingFrequency()* library function**[RD5][RD3]**.

The admitted values are:

3.2 GS/s (default)

1.6 GS/s

0.8 GS/s

0.4 GS/s

10.7 Trigger Clock

The Trigger logic works at 100 MHz, that is ½ FRONT-END CLCK (see **Fig. 10.3**).

10.8 Output Clock

The AD9510 output can be available on the front panel CLK-OUT connector (see **Fig. 10.3**). This option is particularly used in case of multi-board synchronization to propagate the clock reference source in Daisy chain, Users can enable this option while configuring custom PLL programming file in CAEN Toolbox software**[RD1]**.

10.9 Data Correction

To compensate for unavoidable construction differences among the SAMLONG chips, the digitizer requires different types of data corrections. Each digitizer is factory calibrated during the production test and the correction parameters are stored on an on-board non-volatile memory. The corrections are not applied at FPGA level but must be implemented runtime/offline at software level by the User. Software and libraries provided by CAEN (see Chap. **12**) automatically read the correction parameters from the on-board memory and apply them to the raw data provided by the digitizer.

The different data correction types are:

- **Line Offset Correction:** this correction permits reducing the baseline noise down to ~ 0.95 mV RMS. With this sole calibration performed, waveform data is already directly usable with a dynamic range of 11.5 bits and a sampling time precision of around 20 ps RMS. The factory stored correction parameters cannot be modified by the user.
- **Individual Pedestal Correction:** this correction permits reducing the baseline noise down to around 0.75 mV RMS, thus increasing the dynamic range to 11.7 bits. The factory stored correction parameters can be modified by the user.
- **Time INL Correction:** this correction compensates for the fixed time dispersion along the sampling matrix allowing the eventual sampling time precision to scale down to around 5 ps RMS. The factory stored correction parameters cannot be modified; the user can only enable or disable the correction in the software**[RD5]**.
- **Trigger Threshold DAC Offset Correction:** this correction is necessary to obtain the best precision for small signals on the trigger threshold for the channel input discriminator. The factory stored correction parameters cannot be modified by the user.

10.9.1 Individual Pedestal Correction

This is the only data correction for which the User can modify the factory stored parameters. It is recommended to perform this correction once the setup is ready.

After the Line Offset correction, there is still a small residual individual offset distribution remaining on the baseline that is removed by applying the individual pedestal correction.

Fig. 10.4 and **Fig. 10.5** show the waveform before and after this residual pedestal correction.

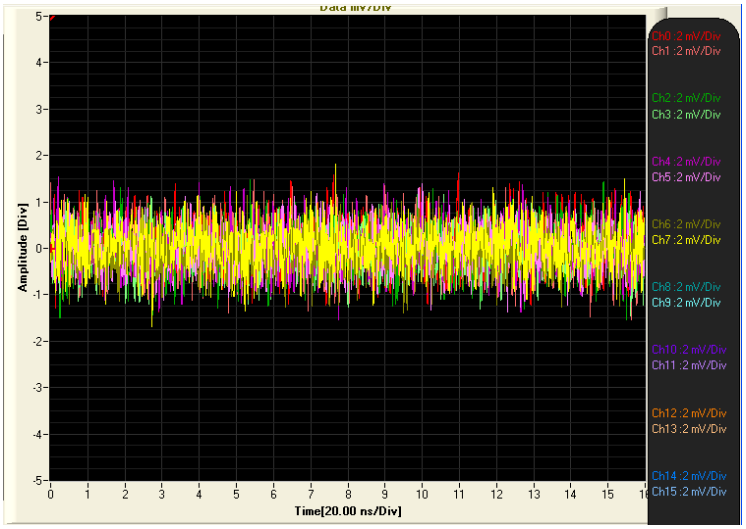


Fig. 10.4: Sampled waveform before individual pedestal correction

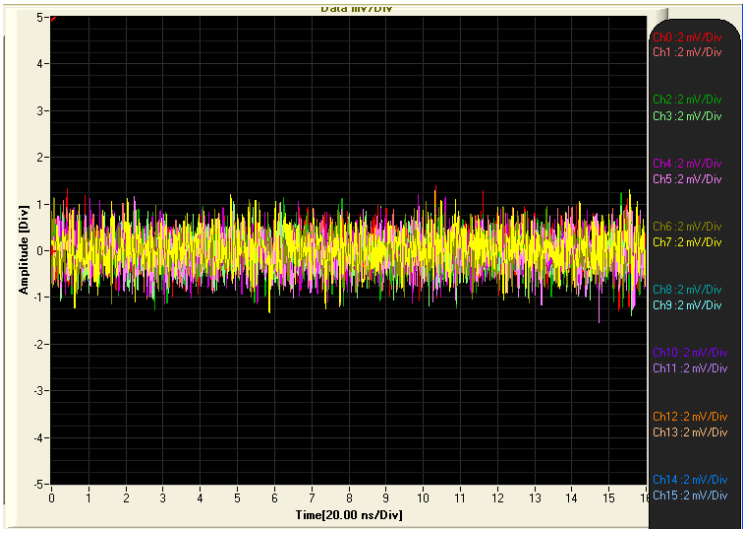


Fig. 10.5: Sampled waveform after individual pedestal correction

Users can perform the individual pedestal correction by WaveCatcher software in the following conditions**[RD5]**:

- All the board channels must be disconnected.

- Calibration must be done after the board is at its thermal regime.

- Calibration must be repeated each time the temperature conditions vary significantly.

10.10 Acquisition Modes

10.10.1 Acquisition Run/Stop

The acquisition can be started and stopped in different ways:

- SW CONTROLLED (default): Start and Stop take place by software command (configurable by the *Set/GetAcquisitionMode()*, *SWStartAcquisition()* and *SWStopAcquisition()* library functions of the CAENDigitizer library**[RD3]**, WaveCatcher**[RD5]** and WaveDemo_x743 software**[RD6]**).

- S-IN CONTROLLED: Start is issued as the S-IN signal is set high and the Stop occurs when S-IN is set low (configurable by the *Set/GetAcquisitionMode()*, *SWStartAcquisition()* and *SWStopAcquisition()* functions of the CAENDigitizer library**[RD3]**).

- FIRST TRIGGER CONTROLLED: The first TTL/NIM pulse arriving at the TRG-IN connector (leading edge) is used to start the acquisition, while next arriving pulses are sensed as triggers for event taking. The Stop acquisition must be SW controlled (configurable by the *Set/GetAcquisitionMode()*, *SWStartAcquisition()* and *SWStopAcquisition()* functions of the CAENDigitizer library**[RD3]**).

- LVDS I/O CONTROLLED: This mode can be used to propagate the start acquisition in a multi-board system; special pins of the LVDS I/O connector are configured for Run input / Run output function (see Sec. **10.15**). Start is issued as the Run signal is set high and the Stop occurs when Run is set low (configurable by WaveCatcher**[RD5]** and WaveDemo_x743 software**[RD6]**).

10.10.2 Running in Charge Mode

The V1743 features an embedded Charge Mode which permits using the FPGA to calculate the charge comprised within a predefined part of each event. As the calculation is performed by the firmware, the acquisition rate can raise up to 7 kHz for full events (depending on the signal input rate). The system will start the summation at a predefined cell value (REF_CELL_FOR_CHARGE). It will last until a total number N (CHARGE_LENGTH) of cells have been summed. Then the result will be stored in a dedicated FIFO (CHARGE_FIFO) together with the physical position of the column where REF_CELL_FOR_CHARGE is located, in order to allow the concerned cells to have their pedestal corrected if necessary. The storage into the FIFO might optionally be filtered by a programmable threshold set on the charge result (CHARGE_THRESHOLD).

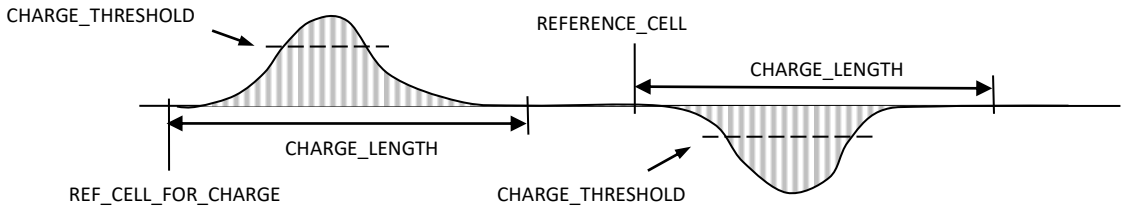


Fig. 10.6: Parameters used for the charge measurement mode

Fig. 10.6 describes the meaning of the different parameters quoted here above, for the integration of both positive and negative signal.

These operations are performed in parallel and independently on all channels. The event is readout only when the charge FIFOs will get full (they contain 256 events). To this end, the board front-end is automatically restarted as long as this does not happen.

As the number of words might be different in both channels in specific trigger modes, the charge and cell position will get forced to zero when the corresponding read FIFO is empty.

Charge mode is managed by WaveCatcher software**[RD5]** and dedicated functions are available in the CAENDigitizer library**[RD3]**.

10.10.3 Event Structure

The event can be read out via VMEbus or Optical Link in 32-bit long word data format (see **Fig. 10.7**).

An event is structured in:

- **Header** (four 32-bit words)
- **Data** (variable size and format)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HEADER	1	0	1	0	TOTAL EVENT SIZE (LWORDS)																											
	BOARD ID					BF	RES.	1	PATTERN															GROUP MASK							
	RESERVED										EVENT COUNTER																			
	EVENT TIME TAG																													
GROUP 0	GROUP HEADER								GROUP 0 CHANNEL DATA first word																					
	GROUP 0 information								GROUP 0 CHANNEL DATA																					
	GROUP TRAILER								GROUP 0 CHANNEL DATA last word																					
GROUP 1	GROUP HEADER								GROUP 1 CHANNEL DATA first word																					
	GROUP 1 information								GROUP 1 CHANNEL DATA																					
	GROUP TRAILER								GROUP 1 CHANNEL DATA last word																					
GROUP 2	GROUP HEADER								GROUP 2 CHANNEL DATA first word																					
	GROUP 2 information								GROUP 2 CHANNEL DATA																					
	BLOCK TRAILER								GROUP 2 CHANNEL DATA last word																					
. . .	. . .								. . .																					
GROUP 7	GROUP HEADER								GROUP 7 CHANNEL DATA first word																					
	GROUP 7 information								GROUP 7 CHANNEL DATA																					
	GROUP TRAILER								GROUP 7 CHANNEL DATA last word																					

Fig. 10.7: Event Format

Note: A group is composed by 2 adjacent analog channels (GROUP 0 = channels 0 - 1, GROUP 1 = channels 2 - 3, GROUP 2 = channels 4 - 5, …, GROUP 7 = channels 14 - 15) managed by the same SAMLONG chip.

10.10.3.1 Header

The **Header** consists in 4 words carrying the following information:

- **TOTAL EVENT SIZE** (Bit[27:0] of 1st header word) is the total size of the event, including the header, which means the number of 32-bit long words to be read;

Note: Total event size takes also includes extra words present in the GROUP structure, but they are not of interest to users. Each extra word, which occurs every 17 words, is in fact discarded by the CAENDigitizer library when decoding the event in the *DecodeEvent()* function**[RD3]**.

- **BOARD ID** (Bit[31:27] of 2nd header word) is the GEO address, meaningful for VME64X modules only;
- **BOARD FAIL FLAG** (Bit[26] of 2nd header word), implemented from ROC FPGA firmware revision 4.5 on (reserved otherwise), is set to "1" in consequence of a hardware problem (e.g. PLL unlocking). The user is then recommended to contact CAEN (see Chap. **18**).
- **EVENT MODE** (Bit[24] of 2nd header word) identifies the event format; in case of 743 digitizer family, it **must be set to "1"**;

Note: this bit is set to "0" by default in the firmware; WaveCatcher and WaveDemo_x743 software automatically sets it to "1" during the board initialization, but users must set it manually when developing a customized software.

- **PATTERN** (Bit[23:8] of 2nd header word) is the 16-bit pattern latched on the LVDS I/Os as the trigger arrives;
- **GROUP MASK** (Bit[7:0] of 2nd header word) is the mask of the groups participating in the event (e.g. GROUP 0 and GROUP 1 participating → GROUP MASK = 0011). This information must be used by the software to retrieve to which groups the samples belong (the first event contains the samples from the group with the lowest number);
- **EVENT COUNTER** (Bit[21:0] of 3rd header word) is the trigger counter;
- **EVENT TIME TAG** (4th header word) is made by bit[30:0] used as counter for the trigger timestamp and bit[31] that is the roll-over flag. By design, the flag sets constantly to "1" after the first roll-over event. The counter is reset when the acquisition starts or by an external signal (see Sec. **10.19.3**) and incremented on each trigger clock hit (10 ns @100MHz).
  IMPORTANT NOTE: This time tag corresponds to the time when the event is created in the digitizer memory (so, it is related to the readout), while not to the time the event occurred at the group (i.e. channel) level, so it does not correspond to any physical quantity. The physical time of arrival of the pulse is the 40-bit counter of TDC field in the data format (see Fig. 10.8).

10.10.3.2 Data

Data are the stored information from each enabled group; data from masked groups are not read. The part of an event related to each group presents the format described in **Fig. 10.8** (example based on GROUP 0).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GROUP HEADER = 0xAA								*RESERVED*												*RESERVED*											
HIT_COUNTER CH0 LSB								ADC DATA CHANNEL 1 SAMPLE 0												ADC DATA CHANNEL 0 SAMPLE 0											
HIT_COUNTER CH0 MSB								ADC DATA CHANNEL 1 SAMPLE 1												ADC DATA CHANNEL 0 SAMPLE 1											
TIME_COUNTER CH0 LSB								ADC DATA CHANNEL 1 SAMPLE 2												ADC DATA CHANNEL 0 SAMPLE 2											
TIME_COUNTER CH0 MSB								ADC DATA CHANNEL 1 SAMPLE 3												ADC DATA CHANNEL 0 SAMPLE 3											
HIT_COUNTER CH1 LSB								ADC DATA CHANNEL 1 SAMPLE 4												ADC DATA CHANNEL 0 SAMPLE 4											
HIT_COUNTER CH1 MSB								ADC DATA CHANNEL 1 SAMPLE 5												ADC DATA CHANNEL 0 SAMPLE 5											
TIME_COUNTER CH1 LSB								ADC DATA CHANNEL 1 SAMPLE 6												ADC DATA CHANNEL 0 SAMPLE 6											
TIME_COUNTER CH1 MSB								ADC DATA CHANNEL 1 SAMPLE 7												ADC DATA CHANNEL 0 SAMPLE 7											
SAMPLING_FREQUENCY								ADC DATA CHANNEL 1 SAMPLE 8												ADC DATA CHANNEL 0 SAMPLE 8											
EVENT_ID								ADC DATA CHANNEL 1 SAMPLE 9												ADC DATA CHANNEL 0 SAMPLE 9											
RESERVED								ADC DATA CHANNEL 1 SAMPLE 10												ADC DATA CHANNEL 0 SAMPLE 10											
FCR LSB								ADC DATA CHANNEL 1 SAMPLE 11												ADC DATA CHANNEL 0 SAMPLE 11											
FCR MSB								ADC DATA CHANNEL 1 SAMPLE 12												ADC DATA CHANNEL 0 SAMPLE 12											
TDC Byte 0 (LSB)								ADC DATA CHANNEL 1 SAMPLE 13												ADC DATA CHANNEL 0 SAMPLE 13											
TDC Byte 1								ADC DATA CHANNEL 1 SAMPLE 14												ADC DATA CHANNEL 0 SAMPLE 14											
TDC Byte 2								ADC DATA CHANNEL 1 SAMPLE 15												ADC DATA CHANNEL 0 SAMPLE 15											
TDC Byte 3								*RESERVED*												*RESERVED*											
TDC Byte 4 (MSB)								ADC DATA CHANNEL 1 SAMPLE 16												ADC DATA CHANNEL 0 SAMPLE 16											
DUMMY								ADC DATA CHANNEL 1 SAMPLE 17												ADC DATA CHANNEL 0 SAMPLE 17											
DUMMY …								ADC DATA …												ADC DATA …											
GROUP TRAILER = 0x55								ADC DATA CHANNEL 1 SAMPLE N-1												ADC DATA CHANNEL 0 SAMPLE N-1											

Fig. 10.8: Group Data Format

In the group data described above, the number of words directly corresponds to the number of columns read in the SAMLONG chips multiplied by 16 (fixed number of lines). Bits 0 to 23 always correspond to digitized event data. Both channels are grouped inside the same word. Bits 24 to 31 are used for header, trailer, and event information.

- For each channel, **HIT_COUNTER** and **TIME_COUNTER** are 16-bit counters used to calculate the hit rate linked to the activity on the channel since the last event. HIT_COUNTER counts the number of times the input discriminator has be toggling since the last event, whereas TIME_COUNTER counts the time in units of 1 µs. The first counter saturating blocks the other. Taking care of memorizing this information long enough in the software, this measurement can range from 0.1 Hz to > ~400 MHz (see Sec. **10.18**).
- **SAMPLING_FREQUENCY** = it is common to all channels and coded on 2 bits as follows:

  00 => 3.2 GS/s

  01 => 1.6 GS/s

  10 => 0.8 GS/s

  11 => 0.4 GS/s

- **EVENT_ID** = it corresponds to the 8 lower significant bits of the event number since the beginning of the run.
- **FCR** = it is the address of the First Cell Read in the SAMLONG chip for the current event. It is coded on 10 bits (which corresponds to the 1024 cells).
- **TDC** = it is the value of the individual channel counter and is coded over 40 bits. This is the Trigger Time Tag reference. The corresponding counter runs with the SAMLONG clock, thus covering a maximum of 1h30 at 200 MHz. It is reset when the acquisition starts or by an external signal (see Sec. **10.19.3**).

In case of charge readout mode (see Sec. **10.10.2**), the part of an event related to each group presents the format as in **Fig. 10.9** (example of GROUP 0):

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	REF CELL COLUMN						1	CHARGE CHANNEL 0 EVENT 1																							
0	0	REF CELL COLUMN						1	CHARGE CHANNEL 1 EVENT 1																							
0	0	REF CELL COLUMN						1	CHARGE CHANNEL 0 EVENT 2																							
0	0	REF CELL COLUMN						1	CHARGE CHANNEL 1 EVENT 2																							
-	-	…						-	…																						
0	0	REF CELL COLUMN						1	CHARGE CHANNEL 0 EVENT 256																							
0	0	REF CELL COLUMN						1	CHARGE CHANNEL 1 EVENT 256																							

Fig. 10.9: Group Data Format in Charge Mode

In the group data described above, the number of words (512) corresponds to twice the charge FIFO depth per channel (256 words). Charge data is coded in two's complement over 23 bits and expressed in pC. **REF CELL COLUMN** corresponds to the number of the physical column where the charge calculation started inside the SAMLONG chip (0 to 63). It is necessary for optional software correction purpose.

Note: The firmware saves the waveforms in the memory of the digitizer with a granularity of n (i.e. in groups of n samples). This way of writing the waveforms in memory allows for a potential ΔT between the instant when the trigger physically arrives and when it is sensed by the digitizer. The resulting effect is a jitter in the acquisition window between one event and the next. This jitter can be observed by graphing the waveforms of the enabled channels using an acquisition software. The channels may jitter together between one event and the next, but not among themselves.

10.11 Acquisition Synchronization

As introduced in Sec. **10.3**, each pair of input channels shares a SRAM memory in the channel FPGA (see **Fig. 2.1**) that is organized into a variable number of buffers, according to the programmable event size. Up to 7 full events per channel, that is to say 7 kS/ch (1 event = 1024 samples or 1024 * 12 bits) can be consecutively stored. When the trigger occurs, the acquisition takes place as described in Sec. **10.2**.

When the Digital Memory Buffer is filled, the board is considered FULL: no trigger is accepted and the acquisition stops. As soon as at least one buffer is readout, the board exits the FULL condition and acquisition restarts. In case of Multi-Boards synchronization, the LVDS I/Os can be software programmed to propagate the Busy signal in FULL condition and the Veto signal to guarantee the data alignment especially at high rates (managed by WaveCatcher**[RD5]** and WaveDemo_x743 software**[RD6]**).

10.11.1 BUSY Front Panel LED

The BUSY red LED on the digitizer front panel lits when at least one of the following conditions is reached:

- The board is not available to accept the triggers because of the conversion dead-time (SAMLONG)
- At least one of the memories is full (i.e. board FULL)

10.12 Trigger Management

All the channels of the board share the same trigger (common trigger), so they acquire an event simultaneously and in the same way (a determined number of samples according to the programmable acquisition window and position with respect to the trigger defined by the programmable post-trigger).

Different trigger sources can participate in the common trigger generation:

- **Software trigger**, produced via a software command
- **External trigger**, received via the front panel TRG-IN connector
- **Self-trigger**, generated by the individual discriminator with programmable threshold that is placed on each analog channel; each couple of adjacent channels generates a single trigger request upon its self-trigger signals; the trigger requests from all the couples are then logically combined to generate the common trigger
- **Coincidence**, where the common trigger is generated after validation upon the coincidence condition, either on the channel couple or a combination of enabled couples
- **Programmable majority**, where the common trigger is generated after validation upon the majority condition of the trigger requests from the enabled channel couples
- **TRG-IN as Gate**, where only the common triggers generated within the TRG-IN signal gate are accepted

As a common trigger is issued, the analog buffers (SAMLONG chips) related to that trigger are frozen, then digitized by the 12-bit ADCs, finally stored into the digital memory buffer and so available for readout (see Sec. **10.2**).

The analog-to-digital conversion is affected by a dead-time as module cannot handle other triggers during the process. This dead-time depends on the number of samples to be digitized (13 µs + ($N_{samples}$ / 16) * 1.75 µs). The V1743 features a maximum dead-time of 125 µs (@1024-sample recording).

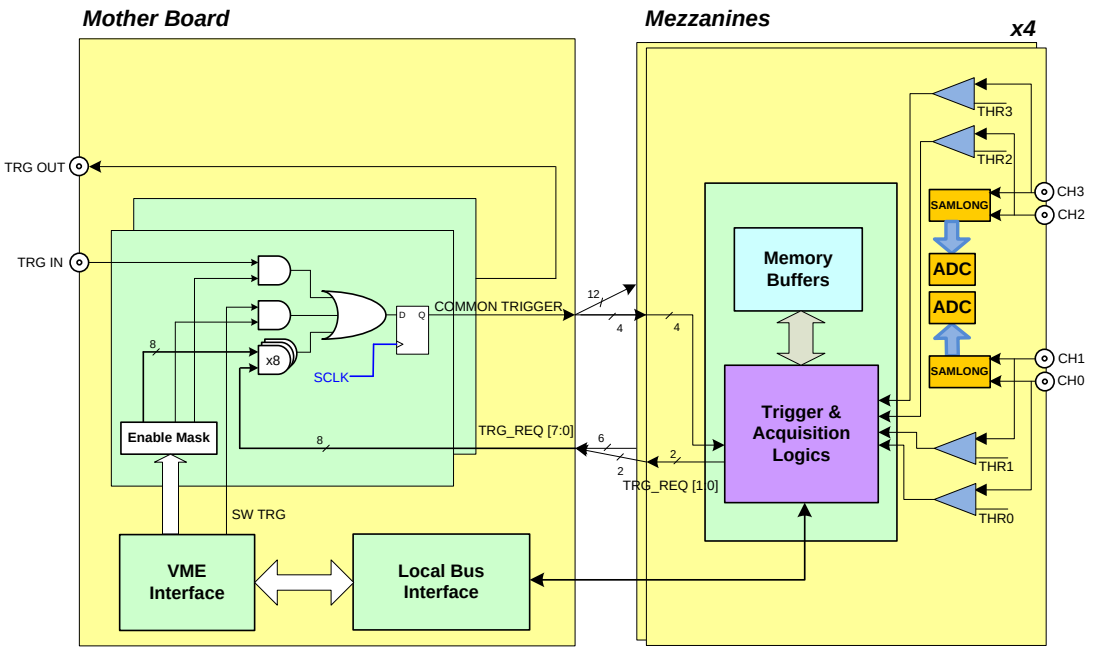


Fig. 10.10: Trigger management block diagram

10.12.1 Software Trigger

Software triggers are internally generated via a software command over VMEbus or Optical Link (through the WaveCatcher software**[RD5]** or the *SendSWTrigger()* function of the CAENDigitizer library**[RD3]**).

10.12.2 External Trigger

A TTL or NIM external signal can be provided in the front panel TRG-IN connector (configurable through the WaveCatcher software**[RD5]** or the *Set/GetExtTriggerInput()* function of the CAENDigitizer library**[RD3]**). The external trigger is synchronized with the internal 100 MHz trigger clock.

10.12.3 Self-Trigger

The V1743 is equipped with a discriminator with a 16-bit programmable threshold on each channel, which permits generating a self-trigger signal when the digitized input pulse exceeds the threshold value. The self-triggers of each couple of adjacent channels are then processed to provide out a single trigger request. The trigger requests are propagated to the central trigger logic to produce the board common trigger, which is finally distributed back to all channels causing the event acquisition (see **Fig. 10.10**). Self-trigger generation, trigger request, and common trigger logic are schematized in **Fig. 10.11**.

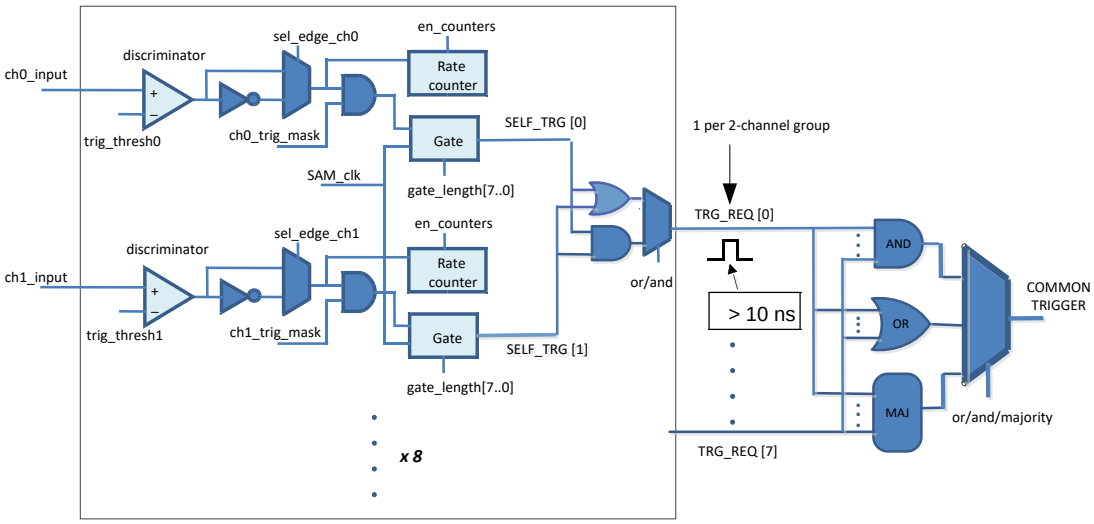


Fig. 10.11: Self-trigger generation, trigger request and common trigger logic

Tab. 10.1 shows the CAENDigitizer library functions involved in the self-trigger management**[RD3]**.

Signal/Function	Reference Library Function
Trig_thresh0/1	*SetChannelTriggerThreshold()*
sel_edge_ch0	*SetTriggerPolarity()*
ch0/ch1_trig_mask	*SetChannelSelfTrigger()*
gate_length[7..0]	*SetChannelPairTriggerLogic()*
or/and	*SetChannelPairTriggerLogic()*
or/and/majority	*SetTriggerLogic()*

Tab. 10.1: Map of available library functions for the self-trigger management

The *SetChannelPairTriggerLogic()* function programs the FPGA in order the self-trigger to be a pulse of configurable width (see **Fig. 10.12**).

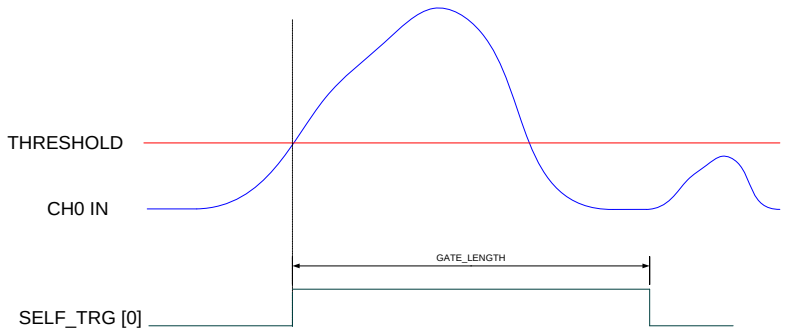


Fig. 10.12: Self-trigger generation

The *SetChannelPairTriggerLogic()* function programs the FPGA in order the trigger request for a couple of adjacent channels to be the AND or OR of the relevant self-trigger signals (see **Fig. 10.11**).

The *SetTriggerLogic()* function programs the FPGA in order the common trigger can be the OR, the AND or the Majority of the enabled trigger requests (see **Fig. 10.11**).

Firmware Default Conditions: by default, the FPGA is programmed as follows:

- All channels are disabled to generate trigger requests, while the external trigger and software trigger are enabled
- Each trigger request is the OR of two pulses whose width is fixed by default depending on the board operating frequency: 15 ns (@3.2 GS/s); 20 ns (@1.6 GS/s); 30 ns (@0.8 GS/s); 50 ns (@0.4 GS/s)
- The common trigger is generated as the OR of the enabled trigger requests

10.12.4 Trigger Coincidence Level

Coincidences between channels can be programmed thanks to the channel pair trigger logic at the mezzanine level and the global trigger logic at the motherboard level, as introduced in Sec. **10.12.3**.

Coincidence logic is managed by the CAENDigitizer library**[RD3]** and WaveCatcher software**[RD5]**.

Example: Making coincidence between two adjacent channels, CH0 and CH1:

- Enable the self-trigger only for Channel 0 and Channel 1 through the *SetChannelSelfTrigger()* function
- Program the AND logic at the mezzanine level through the *SetChannelPairTriggerLogic()* function and select the coincidence window as the value of *gate_length* (see **Tab. 10.1**)
- Program the OR logic on the motherboard through the *SetTriggerLogic()* function

Example: Making coincidence between channels belonging to different couples, CH0 and CH5:

- Enable the self-trigger only for Channel 0 and Channel 5 through the *SetChannelSelfTrigger()* function
- On the mezzanine level, program the OR logic, for the two couples including CH0 and CH5, through the *SetTriggerLogic()* function
- On the motherboard level, program the AND logic through the *SetTriggerLogic()*

Note: By design, the global trigger logic can manage only four signals (one per couple of adjacent channels), so only one channel per couple can participate in a coincidence method at the motherboard level. For example, it is not possible to set a coincidence between CH0, CH1, and CH7, because only one between CH0 and CH1 can participate.

10.12.5 Majority Level

According to the scheme in **Fig. 10.11**, it is possible to configure the board for the common trigger to be the result of the majority operation among the trigger requests coming from the channel couples. This option and the majority level are configurable through the *SetTriggerLogic()* function of CAENDigitizer library**[RD3]** or by the WaveCatcher software**[RD5]**.

The majority level can be set in the range:

[0 : (number of couples -1)]

where majority level = 0 means that the common trigger is issued when at least the trigger request from one couple arrives.

10.12.6 TRG-IN as Gate

It is possible to configure TRG-IN as a gate for trigger anti-veto function. The common acquisition trigger is then issued upon the AND between the external signal on TRG-IN and the other trigger sources but the software trigger (i.e. the software trigger cannot participate in the Trigger as Gate mode). This function is configurable only by WaveCatcher software**[RD5]**.

10.13 Trigger Distribution

As described in Sec. **10.12**, the OR of all the enabled trigger sources (only software trigger and external trigger by firmware default setting), synchronized with the internal clock, becomes the common trigger of the board and is fed in parallel to all channels, which consequently provokes the capture of an event.

A Trigger Out signal is also generated on the relevant front panel TRG-OUT connector (NIM or TTL) for the common trigger signal external propagation. Trigger Out logic is described in **Fig. 10.13**, where only the software trigger is propagated out by firmware default (red path).

Reference functions of the CAENDigitizer library**[RD3]**:

- *SetSWTriggerMode()*
- *SetExtTriggerInputMode()*
- *SetChannelSelfTrigger()*

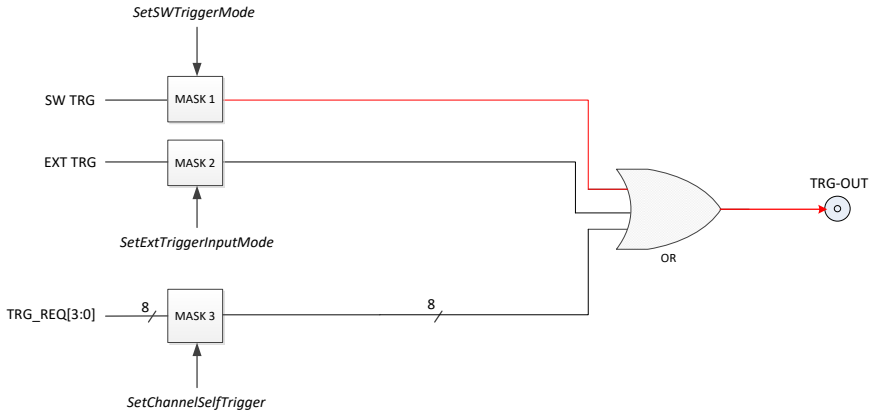


Fig. 10.13: Trigger configuration of TRG-OUT front panel connector

10.14 Multi-board Synchronization Overview

When multi-board systems are involved in an experiment, it is necessary to synchronize different boards. In the end, users can acquire from N boards with Y channels each, like if they were just one board with N · Y channels.

While all the channels of the same board are simultaneously sampled at the same clock frequency by design, the main issue in the synchronization of a multi-board system is have the same clock for all the boards, that is achieved by propagating the sampling clock from board to board. This is made through CLK-IN/CLK-OUT daisy chain connections among the digitizers. One board must be chosen to be the clock “master” that propagates its own clock to the others called “slaves”. A programmable phase shift can adjust possible delays in the clock propagation. To have the same time reference for the timestamp of all boards, the Run signal for the Start/Stop Acquisition is propagated in daisy chain through the LVDS I/Os and so for the Busy/Veto signal which guarantees the data alignment especially when operating at high rates.

The synchronization architecture of the V1743 digitizers needs an external logic for the Trigger as shown in the picture below.

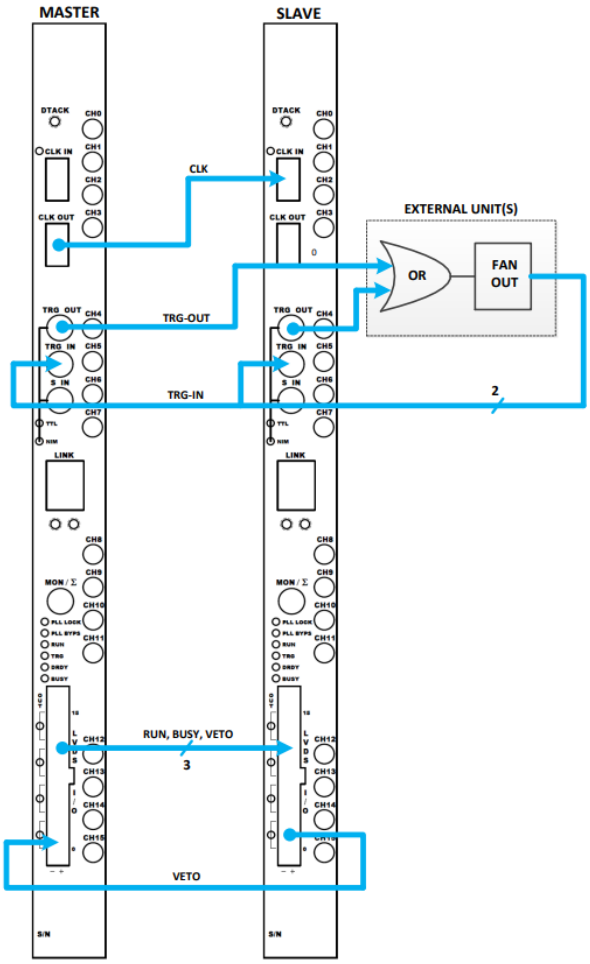


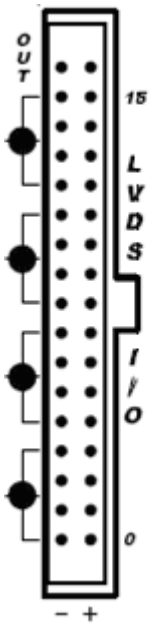
Fig. 10.14: Simplified synchronization scheme of two V1743 digitizers

CAEN provides the WaveDemo_743 program to demonstrate the synchronization, together with a step-by-step guide describing concepts and procedure**[RD6]**. Also, WaveCatcher software can manage the suggested synchronization setup**[RD5]**.

10.15 Front Panel LVDS I/Os

The VME digitizer is provided with FPGA-controlled 16-pin general purpose LVDS I/O connector (see **Chap. 7**).

The signal pinout is described in **Tab. 10.2**.



Nr.	Direction	Funtcion	Description
0	out	TRG_REQ[0]	The overthreshold information from the relevant couple of channels
1	out	TRG_REQ[1]	
2	out	TRG_REQ[2]	
3	out	TRG_REQ[3]	
4	out	TRG_REQ[4]	
5	out	TRG_REQ[5]	
6	out	TRG_REQ[6]	
7	out	TRG_REQ[7]	
8	out	Memory Full	The board Full flag
9	out	Event Data Ready	The board Event Data Ready flag
10	out	Channels Trigger	The OR of the "new event to be read" signals of each channel
11	out	Run Status	The board Run flag
12	in	Trigger Time Tag Reset (active low)	The reset of the trigger time tag counters (Event Time Tag and TDC as in Sec. **10.19.3**)
13	in	Memory Clear (active low)	The clear of all the channel memories
14	-	*reserved*	*N.A.*
15	-	*reserved*	*N.A.*

Tab. 10.2: Front panel LVDS I/O pinout

Note: WaveCatcher and WaveDemo_x743 software are able to set the special configuration of the LVDS I/O as Busy/Veto requested in case of multi-board synchronization **[RD5][RD6]**.

10.16 Analog Monitor

V1743 houses a 12-bit, 100MHz DAC with 0÷1V dynamics on a 50Ω load, whose input is controlled by the ROC FPGA and the signal output (driving 50 Ω) is available on the MON/Σ output connector (see **Fig. 2.1** and Chap. **7**). MON output of more boards can be summed by an external Linear Fan In.

The DAC control logic implements two possible functions, following described.

10.16.1 Trigger Majority Mode (default)

It is possible to generate a Majority signal with the DAC: it is a voltage signal whose amplitude is proportional to the number of triggering couples (i.e. those couples of adjacent channels, configured for self-triggering as in the logic of **Fig. 10.11**); 1 step = 125 mV. This information can be exploited, via an external discriminator, to produce a common trigger signal when the number of triggering couples has exceeded a particular threshold.

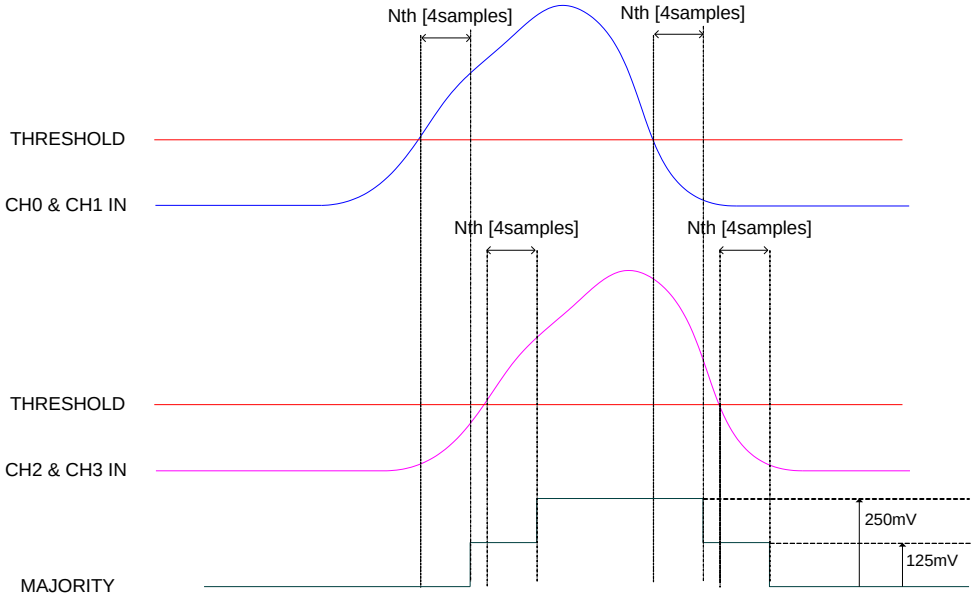


Fig. 10.15: Example of majority logic based on 2 channel couples with self-trigger logic on AND

10.16.2 Buffer Occupancy Mode

In this mode, MON output connector provides a voltage value increasing, proportionally, with the number of buffers filled with events, in fixed steps of 0.976 mV, given by:

$$\frac{V_{max}}{1024}$$

where $V_{max} \approx 1$ V. The maximum number of buffers depends on the programmed size of the event (see Sec. **10.3**).

Example: at the maximum event size of 1024 samples (i.e. 7 buffers), the maximum Buffer Occupancy output voltage level is given by (0.976 · 7) mV.

It is actually a test method for the readout efficiency: in fact, if the average event readout throughput is as fast as trigger rate, then MON out value remains constant; otherwise, if MON out value grows in time, this means that readout rate is slower than trigger rate.

Starting from revision 4.9 of the ROC FPGA firmware, it is possible to apply a digital gain to the fixed step, particularly when the memory is organized in a small number of buffers. The gain can be set between 1 (default no-gain setting) and 1024 as powers of two.

The overall Buffer Occupancy mode is managed by the WaveCatcher software**[RD5]**.

10.17 Test Pattern Pulser

Each input channel is equipped with an individual pulser. The pulse amplitude is fixed (~0.7 V with no cable plugged, half this value otherwise), while the pattern can be programmed.

The pulse pattern is a 16-bit word of the SAMLOGN main clock (200 MHz) that will be sent every 3.5 µs. This permits an easy testing of the board functionality, as well as it gives the possibility to use the board as a reflectometer. As this pulse pattern is produced from an autonomous clock source, trigger can be set on the discriminators.

Example 1: setting the 16-bit word = "1", the generated pattern si a pulse of a time duration of 1 clock period (5 ns @ 3.2 GS/s).

Example 2: setting the 16-bit word ="AAAA", the generated pattern is the 101010101010 series, where each "1" is a 5-ns pulse.

Example 3: setting the 16-bit word ="C755", the generated pattern is the 1100011101010101 series (see **Fig. 10.16**).

Pulses are sent following the binary format, where the LSB is sent for first.

Pulser function is fully managed by WaveCacther software**[RD5]** or through the *Enable / DisableSAMPulseGen()* and *SendSAMPulse()* functions of the CAENDigitizer library**[RD3]**.

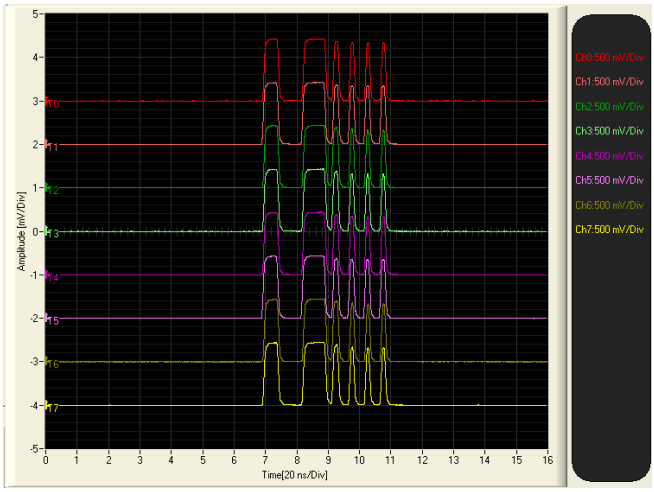


Fig. 10.16: FPGA Test Pulse with 0xC755 pattern

Each channel can make use of his pulser as a reflectometer. An example of this application is shown in **Fig. 10.17**, where a 40-ns wide square pulse produced internally is sent to a 1-meter open cable connected to the board.

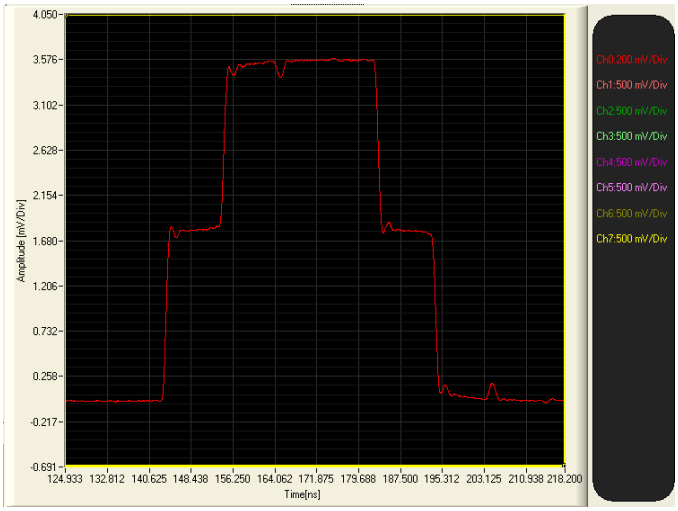


Fig. 10.17: FPGA Test Pulse in reflectometer mode

10.18 Hit Rate Monitor

Each input channel is equipped with an individual hit rate monitor. Each hit counter is based on two 16-bit counters, TRIG_COUNT and TIME_COUNT, used to calculate the "hit rate" related to the channel activity from the last event (**Fig. 10.18**).

TRIG_COUNT counts the number of threshold crossings of the discriminator from the last event, while TIME_COUNT counts the time elapsed with a 1-MHz clock (i.e. units of 1 µs). These counters are reset and restarted after each read access. Their content is stored into the event data (see Sec. **10.10.3**). As soon as any of them saturates, both are frozen, and thus their values are always valid. If the counters information is memorized long enough in the software along events, rate measurement can work from as low as ~0.1 Hz up to ~400 MHz.

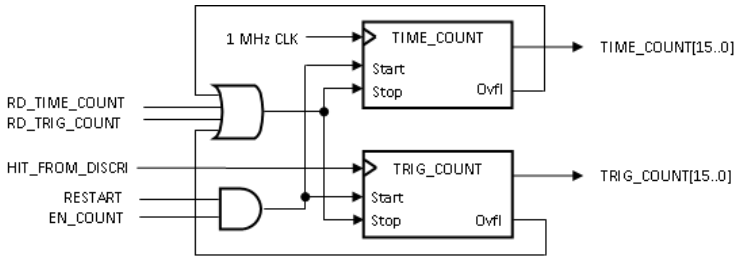


Fig. 10.18: Principle of the Hit Rate Monitor

10.18.1 Veto for the Trigger Rate Counter

It is possible to configure the board to inhibit the trigger counting within an adjustable time window after the digitization starts. This option can be used to reject unwanted after-pulses and is configurable through the *SetSAMTriggerCountVetoParam()* function of CAENDigitizer library**[RD3]** and WaveCatcher software**[RD5]**.

10.19 Reset, Clear, and Default Configuration

10.19.1 Global Reset

Global reset is performed at power-on of the module or can be issued via software by the *Reset()* function of CAENDigitizer library**[RD3]**. It allows to clear the data off the Output Buffer, the event counter, and performs a FPGAs global reset which restores the FPGAs to the default configuration. All counters are initialized to their initial state and all detected error conditions are cleared.

10.19.2 Memory Reset

The memory reset clears the data off the Output Buffer.

Memory reset can be issued by the *ClearData()* function of CAENDigitizer library**[RD3]**. It is also possible to forward a memory clear by sending a pulse to the front panel dedicated Memory Clear input of the LVDS I/O connector (see **Tab. 10.2**).

10.19.3 Timer Reset

The timer reset initializes the time tag counters, EVENT TIME TAG and TDC (see Sec. **10.10.3**).

The timer reset can be optionally issued:

- Via software, by the *ClearData()* function of CAENDigitizer library**[RD3]**
- Via hardware with no need of any firmware configuration:
  - by sending a differential pulse to the front panel Trigger Time Tag Reset input of the LVDS I/O connector (see **Tab. 10.2**)
  - by sending single-ended signal (TTL/NIM) to S-IN input; the time stamps reset occurs at every leading edge of the logic signal sent to the S-IN connector

10.20 VMEBus Interface

The module is provided with a fully compliant VME64/VME64X interface, whose main features are:

- EUROCARD 9U Format
- J1/P1 and J2/P2 with either 160 pins (5 rows) or 96 (3 rows) connectors
- A24, A32 and CR-CSR address modes
- D32, BLT/MBLT, 2eVME, 2eSST data modes
- MCST write capability
- CBLT data transfers
- RORA interrupter
- Configuration ROM

10.20.1 Addressing Capabilities

- Base address: the module works in A24/A32 mode The Base Address of the module is selected through four rotary switches (see **Fig. 9.1**), then it is validated only with either a Power-ON cycle or a System Reset (see Sec. **10.19.1**).

ADDRESS MODE	ADDRESS RANGE	NOTES
A24	[0x000000:0xFF0000]	SW3 and SW4 ignored

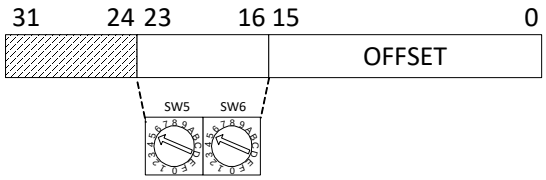


Fig. 10.19: A24 addressing

ADDRESS MODE	ADDRESS RANGE	NOTES
A32	[0x00000000:0xFFFF0000]	-

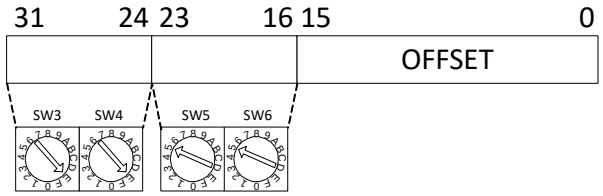


Fig. 10.20: A32 addressing

- CR/CSR address: the addressing is based on the slot number taken from the relevant backplane lines. The recognised Address Modifier for this cycle is 2F. *This feature is implemented only on versions with 160-pin connectors.*

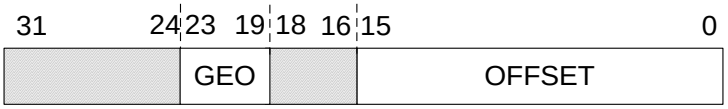


Fig. 10.21: CR/CSR addressing

10.20.2 Address Relocation

It is possible to set via software the board Base Address (valid values ≠ 0) by register access (contact CAEN as in Chap. **18**). This configuration overwrites the rotary switches settings.

The used addresses are:

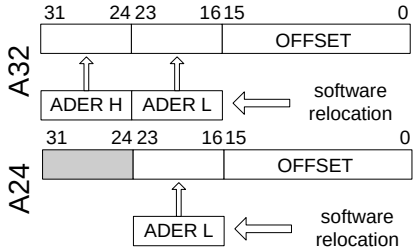


Fig. 10.22: Software relocation of base address

10.21 Data Transfer Capabilities and Events Readout

Once it is written in the memory, the event becomes available for the readout via VMEbus or Optical Link (see Sec. **10.3**).

Although the channel digital memories are SRAMs, addresses are taken from a FIFO. Therefore, data are read from the memories sequentially, according to the selected Readout Logic, from a memory space mapped on 4 Kb (0x0000÷0x0FFC).

The events are readout sequentially and completely, starting from the Header of the first available event, followed by the Trigger Time Tag, the Event Counter and all the samples of the group channels (from 0 to 1). Once an event is completed, the relevant memory buffer becomes free and ready to be written again (old data are lost). After the last word in an event, the first word (Header) of the subsequent event is readout. It is not possible to readout an event partially.

The board supports D32 single data readout, Block Transfer BLT32 and MBLT64, 2eVME and 2eSST cycles. Theoretical maximum transfer rate is up to 70 MB/s with MBLT64 (using CAEN bridge), up to 200 MB/s with 2eSST, while up to 80 MB/s can be achieved by direct optical link.

10.21.1 Block Transfer D32/D64, 2eVME

The Block Transfer readout mode allows to read N complete events sequentially, where N is set by using the *MaxNumEventsBLT()* function of CAENDigitizer library**[RD3]**.

When developing programs, the readout process can be implemented on different basis:

- Using **Interrupts**: as soon as the programmed number of events is available for readout, the board sends an interrupt to the PC over the optical communication link (not supported by USB).
- Using **Polling** (interrupts disabled): by performing periodic read accesses to a specific register of the board (contact CAEN for details), it is possible to know the number of events present in the board and perform a BLT read of the specific size to read them out.
- Using **Continuous Read** (interrupts disabled): continuous data read of the maximum allowed size (e.g. total memory size) is performed by the software without polling the board. The actual size of the block read is determined by the board that terminates the BLT access at the end of the data, according to the configuration of the *SetMaxNumEventsBLT()* library function mentioned above. If the board is empty, the BLT access is immediately terminated and the "Read Block" function will return 0 bytes (it is the *ReadData()* function in the CAENDigitizer Library**[RD3]**).

Whatever the method from above, it is suggested to ask the board for the maximum of the events per block being set. Furthermore, the greater this maximum, the greater the readout efficiency, despite of a greater memory allocation required on the host station side that is actually not a real drawback, considering the features of the personal computers available on the market.

The event is configurable as indicated in the introduction of the paragraph, namely:

[Event Size] = [8*(Buffer Size)] + [16 bytes]

Then, it is necessary to perform as many cycles as required to readout the programmed number of events.

It is suggested to enable BERR signal during BLT32 cycles to end the cycle avoiding filler readout. The last BLT32 cycle will not be completed, it will be ended by BERR after the #N event in memory is transferred (see **Fig. 10.23**).

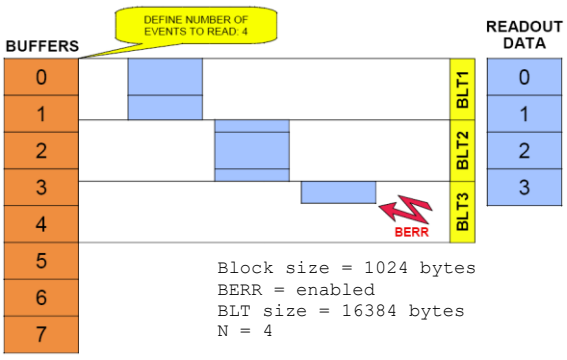


Fig. 10.23: Example of BLT readout

Since some 64-bit CPU cut off the last 32- bit word of a transferred block, if the number of words composing such block is odd, it is necessary to add a dummy word (which has then to be removed via software) to avoid data loss. This can be achieved by register setting (contact CAEN as in Chap. **18**).

MBLT64 cycle is similar to the BLT32 cycle, except that the address and data lines are multiplexed to form 64-bit address and data buses.

The 2eVME allows to achieve higher transfer rates thanks to the requirement of only two edges of the two control signals (DS and DTACK) to complete a data cycle.

10.21.2 Chained Block Transfer D32/D64

The board allows reading out the events from more Daisy-chained boards (Chained Block Transfer mode).

CBLT technique bases on a token which is passed between the boards; it is then necessary to verify that the used VME crate supports such cycles.

To Daisy chain several contiguous boards, they must set as “first”, “intermediate” or “last” by configuring a FPGA register (contact CAEN for details). A common Base Address is then defined via the same register; when a BLT cycle is executed at the address CBLT_Base + 0x0000 ÷ 0x0FFC, the “first” board starts to transfer its data, driving DTACK properly; once the transfer is completed, the token is passed to the second board via the IACKIN-IACKOUT lines of the crate, and so on until the “last” board, which completes the data transfer and asserts BERR (which has to be enabled): the Master then ends the cycle and the slave boards are rearmed for a new acquisition.

If the size of the BLT cycle is smaller than the events size, the board which has the token waits for another BLT cycle to begin (from the point where the previous cycle has ended).

10.21.3 Single D32 Transfer

This mode allows reading out one word at a time, starting from the Header (4 words) of the first available event, followed by all the words until the end of the event; the second event is then transferred. The exact sequence of the transferred words is shown in Sec. **10.10.3**.

After the 1st word is transferred, it is suggested to check the TOTAL EVENT SIZE information and then do as many cycles as necessary (that is TOTAL EVENT SIZE -1) to read the event completely.

10.22 Optical Link Access

The digitizer houses an interface for optical link communication which uses optical fiber cables as physical transmission line, with a maximum transfer data rate of 80 MB/s.

CONET is the proprietary serial protocol designed by CAEN to enable optical link communication between digitizers (acting as CONET slaves) and the host PC. This communication needs CONET master like A5818 controller or the A4818 adapter which replaced the obsolete A2818 and A3818 controllers.

CONET2 is the latest protocol version, implemented at the firmware level on digitizers and controllers, that improves the data transfer rate efficiency by 50% compared to the earlier CONET1 version.

Note: CONET1 is incompatible with CONET2 and viceversa; communication will fail in any optical chain containing both CONET1 and CONET2 boards.

Note: CONET1 is not implemented in any firmware revision of A5818 controller and A4818 adapter, so they only work upon CONET2 protocol version.

To update old systems from CONET1 to CONET2, CAEN recommend following the procedure described in the dedicated Application Note**[RD11]**.

The optical link interface has Daisy-chain capability. It is so possible to connect up to eight digitizer modules over a single optical link of the A4818, while up to thirty- two to the 4-link A5818 PCIe controller (8 modules per link).

The parameters for read/write accesses via Optical Link are the same used by VME cycles (Address Modifier, Base Address, data Width, etc); wrong parameter settings cause Bus Error.

Setting bit[3] at register address 0xEF00 enables the module to broadcast an interrupt request on the Optical Link; the enabled Optical Link Controllers propagate the interrupt on the PCI bus when a request from the Optical Link is sensed. Interrupts can also be managed at the CAENDigitizer library level**[RD3]**.

11 Drivers & Libraries

11.1 Drivers

To interface with the board, CAEN provides the drivers for the supported physical communication

channels and compliant with Windows® and Linux® OS:

- **CONET Optical Link**, managed by CAEN controllers like the A5818. The driver installation packages are available for free on CAEN website in the "Software" tab at the controller webpage (**login required**).

Note: For the installation of the Optical Link driver, refer to the controller User Manual**[RD7]**.

- **USB 2.0 Link**, managed by CAEN (USB-to-VME) Bridges like the V3718. The driver installation packages are downloadable for free on CAEN website in the "Software" tab at the bridge web page (**login required**).
- **USB 3.0 link**, managed by the V4718 USB-to-VME Bridge and by the A4818 (USB3-to-CONET) Adapter. The driver installation packages are downloadable for free on CAEN website in the "Software" tab at the V4718 and A4818 page respectively (**login required**). The driver for the V4718 must be installed for Linux users only

Note: To install the USB Link drivers, follow the instructions inside the ReadMe file included in the packet or refer to the V3718, V4718 User Manuals **[RD8][RD9]**or A4818 adapter Data Sheet **[RD10]**.

11.2 Libraries

CAEN libraries are a set of middleware software required by CAEN software tools for a correct functioning. These libraries, including also demo and example programs, represent a powerful base for users who want to develop customized applications for the digitizer control (communication, configuration, readout, etc.):

- **CAENDigitizer[RD3]** is a library of C functions designed specifically for the Digitizer families running both waveform recording and DPP firmware. The CAENDigitizer library is based on the CAENComm library which, in turn, is based on CAENVMELib library. For this reason, **the CAENVMELib and CAENComm libraries must be already installed on the host PC before installing the CAENDigitizer**.
- **CAENComm** library **[RD4]** manages the communication at low level (read and write access). The purpose of the library is to implement a common interface to the higher software layers, masking the details of the physical channel and its protocol, thus making the libraries and applications that rely on the CAENComm independent from the physical layer. **The CAENComm requires the CAENVMELib library (access to the VME bus)**, even in the case that the VME is not used

Installation packages are available for free download on CAEN web site in the "Software" tab at the relevant library page (**login required**).

WHEN TO INSTALL CAEN LIBRARIES:

WINDOWS® and LINUX® compliant customized software. The user must install the required libraries apart.

LINUX® compliant non-stand-alone CAEN software. The user must install the required libraries apart to run the software.

CAENComm (and so the CAENDigitizer) supports the following communication channels (**Fig. 11.1**):

PC → USB3 → A4818 → CONET → V1743/VX1743

PC → USB → V3718/VX3718 → VMEbus → V1743/VX1743

PC → USB3 → V4718/VX4718 → VMEbus → V1743/VX1743

PC → USB → V1718/VX1718 (**Obsolete**) → VMEbus → V1743/VX1743

PC → USB3 → A4818 → CONET → V3718/VX3718 → VMEbus → V1743/VX1743

PC → USB3 → A4818 → CONET → V4718/VX4718 → VMEbus → V1742/VX1743

PC → PCI/PCIe → A5818 → CONET → V1743/VX1743

PC → PCI/PCIe → A2818/A3818 (**Obsolete**) → CONET → V1743/VX1743

PC → PCI/PCIe → A2818/A3818 (**Obsolete**) → CONET → V3718/VX3718 → VMEbus → V1743/VX1743

PC → PCI/PCIe → A2818/A3818 (**Obsolete**) → CONET → V4718/VX4718 → VMEbus → V1743/VX1743

PC → PCI/PCIe → A2818/A3818 (**Obsolete**) → CONET → V2718/VX2718 (**Obsolete**) → VMEbus → V1743/VX1742

PC → ETHERNET → V4718/VX4718 → VMEbus → V1743/VX1743

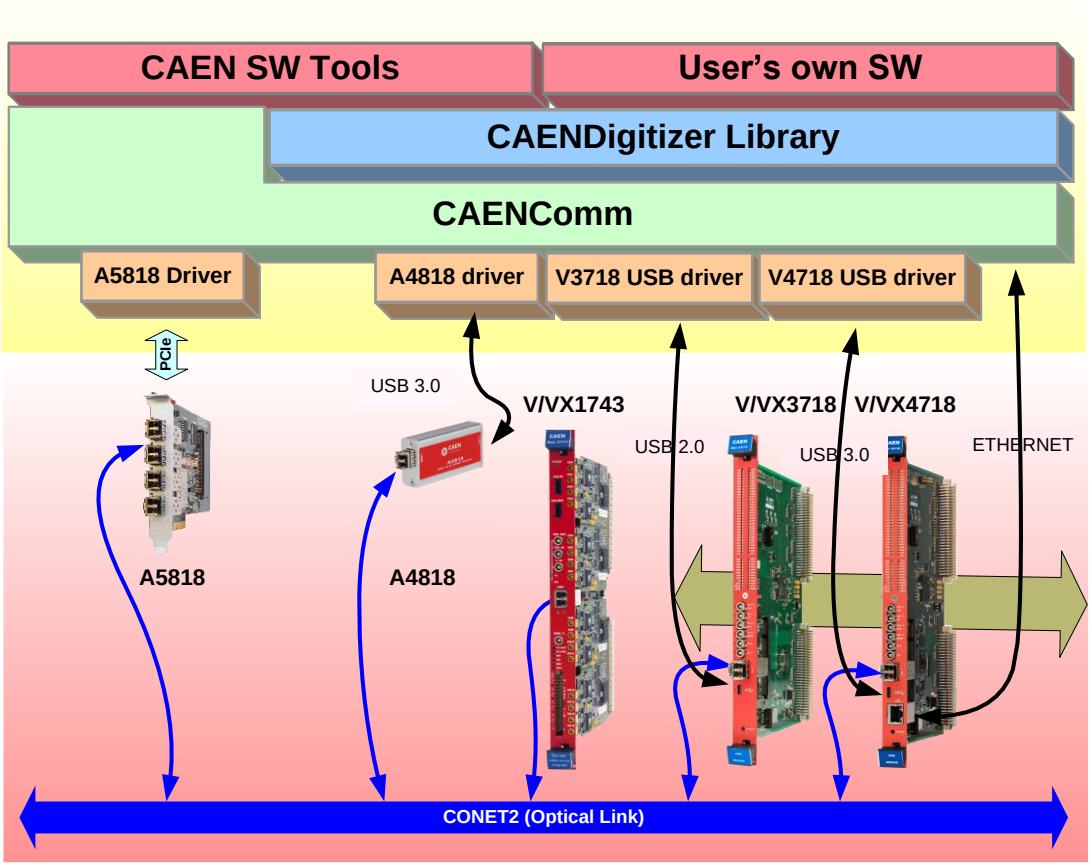


Fig. 11.1: Drivers and software layers

12 Software Tools

CAEN provides software tools to interface with the 743 digitizer family. Installation packages and user documentation are available for free download on CAEN website at the relevant software page (**login required**).

12.1 CAEN Toolbox

CAEN Toolbox is the comprehensive software suite designed for CAEN Front-End boards.

With V1743, CAEN Toolbox simplifies various tasks into a few easy steps, including:

- Uploading different FPGA firmware versions to the digitizer
- Reading the firmware release of the digitizer
- Managing firmware licenses, particularly for DPP firmware
- Upgrading the internal PLL
- Obtaining the Board Info file, useful for support
- Managing the reboot of the FPGA firmware from either the Backup or the Standard FLASH page
- Debugging your setup using the Manual Controller

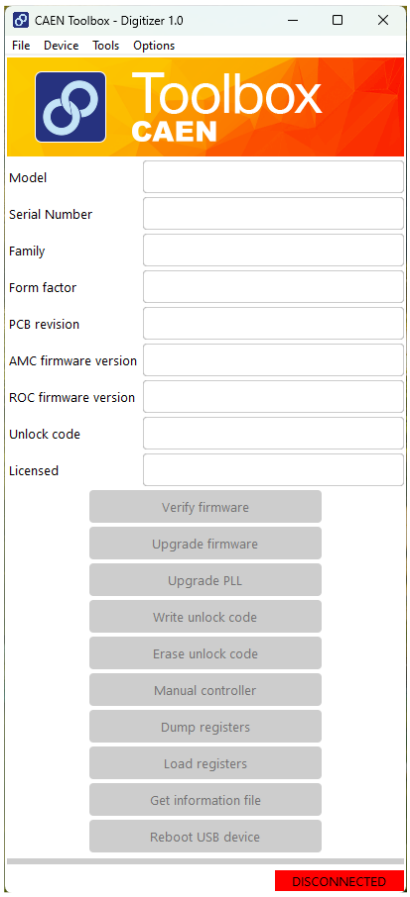


Fig. 12.1: CAEN Toolbox Graphical User Interface

CAEN Toolbox is based on the CAENComm library (see Sec. **11.2**). The software is compatible with both Windows® and Linux® platforms, operating as a standalone application on each available version. For installation instructions and a detailed description of its features, refer to the user documentation**[RD1]**.

12.2 CAENComm Demo

CAENComm Demo is a simple program developed in C/C++ source code and provided both with Java™ and LabVIEW™ GUI interfaces. The demo mainly allows for a full board configuration at low-level by direct read/write access to the registers and may be used as a debug instrument.

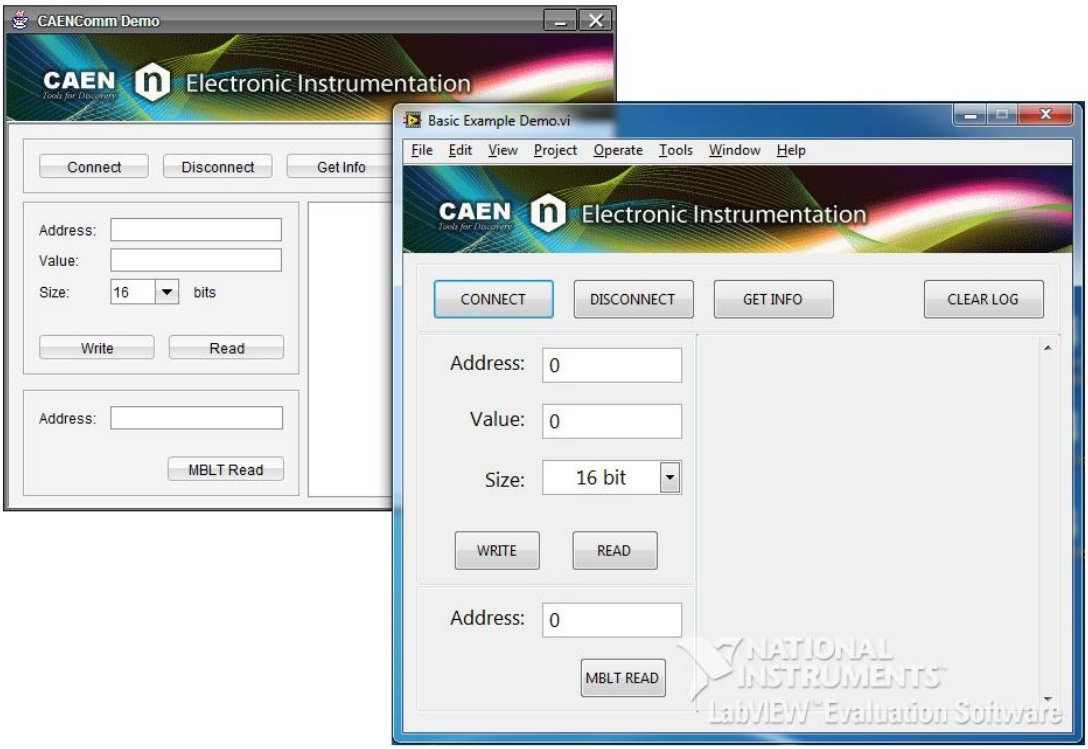


Fig. 12.2: CAENComm Demo Java™ and LabVIEW™ graphical interface

CAENComm Demo is based on the CAENComm library (see Sec. **11.2**) and included in the installation package of the library (Windows® platforms only).

For installation instructions and a detailed description of its features, refer to the user documentation **[RD4]**.

12.3 WaveDemo_x743

The CAENWaveDemo_x743 is a C-based console application for the specific support of the x743 CAEN digitizer basing on a configuration text file.

This software can control multiple digitizers and, particularly, it can be used as a demonstrator of the synchronization of the V1743/ VX1743 digitizers**[RD6]**.

Specifically, CAENWaveDemo_x743 can perform the following operations:

- Connect one or more digitizers through a physical communication interface (USB, Optical Link or VME)
- Program the digitizer according to parameters written in a configuration file (text file)
- Perform SAMLONG chips calibration
- Start and stop the acquisition (run on/off)
- Configure the Trigger mode (software, external or on the channels)
- Read the event data and display the acquisition statistics
- Perform some simple data analysis (post-processing) such as the histograms of energy and time of the events
- Save the waveforms to ASCII or binary output files, as well as the histograms and the run information
- Plot and process the acquired waveform
- Manage the configuration and acquisition of multiple boards in synchronized mode

Besides being a ready-to-use software, CAEN WaveDemo_x743 packet includes C source files to let the users customize the code for personalized solutions.

WaveDemo_x743 runs on Windows® and Linux® platforms. Additional third-party Gnuplot graphical tool must be installed only in case of Linux OS.

The software relies on the CAENVMELib, CAENComm and CAENDigitizer libraries (see Sec. **11.2**)

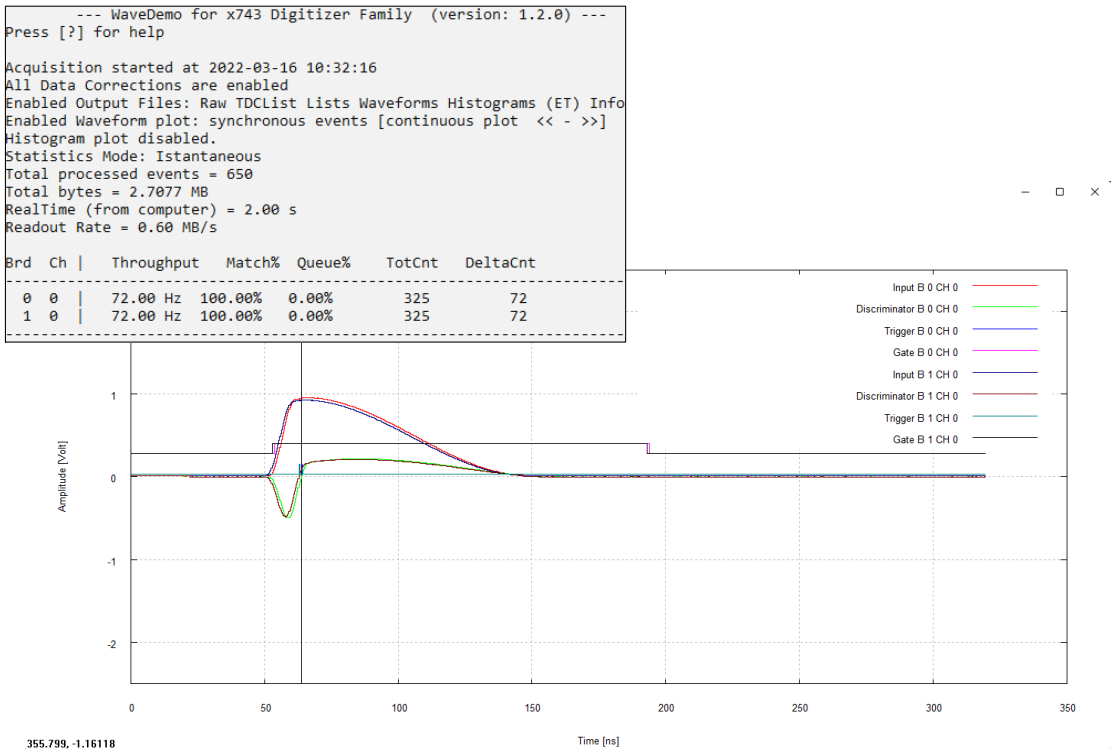


Fig. 12.3: WaveDemo_x743 software

For installation instructions and a detailed description of its features, refer to the user documentation **[RD6]**.

12.4 WaveCatcher

WaveCatcher is LabWindows/CVI application made by CNRS/IN2P3/LAL and capable to fully control the x743 digitizer. It is also possible to manage a multi-board synchronized system particularly made by V1743 boards.

The software features a graphical user-friendly interface which permits to take benefit of all the hardware functions: sampling frequency, trigger modes, waveforms and charge data acquisition, channel pulses, synchronization, and so on.

Different tools are available for on-line measurements and histograms plot: graphical cursors, noise level, raw hit rates, charge amplitude and time measurements, time distance histograms between channels (fixed threshold and digital CFD methods), charge histograms, FFT, and others.

All acquired data and computed measurements can be saved to files for further replay or off-line analysis.

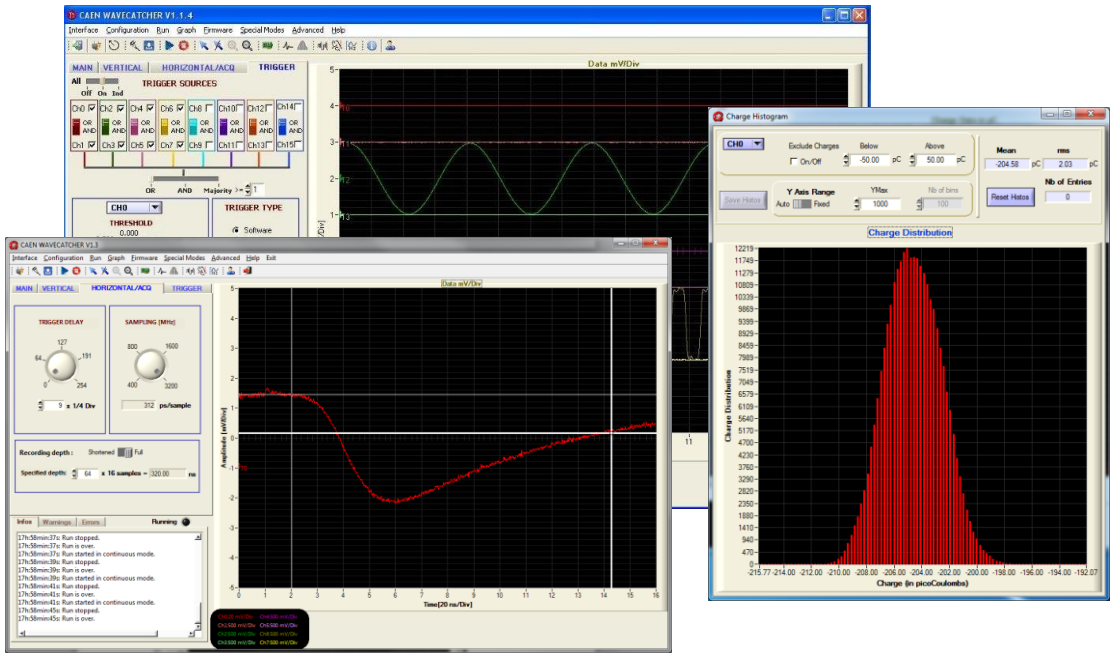


Fig. 12.4: WaveCatcher software

WaveCatcher runs on Windows® platforms only. Users must also install the required third-party NI LabWindowsTM/CVI Run-Time Engine, version 2009 or higher.

The software relies on the CAENVMELib, CAENComm and CAENDigitizer libraries (see Sec. **11.2**).

Note: WaveCatcher for Windows® is stand-alone. Users need to install only the driver for the communication link, while the DLLs of the required libraries are installed by the software locally.

For installation instructions and a detailed description of its features, refer to the user documentation **[RD5].**

13 HW Installation

To power on the board, perform the following steps:

1. Insert the Digitizer into the crate:
   - The V1743 fits into 6U VME crates
   - VX1743 versions require VME64X compliant crates
2. Power up the crate

ONLY QUALIFIED PERSONNEL SHOULD PERFORM INSTALLATION OPERATIONS

DO NOT INSTALL THE EQUIPMENT IN A SETUP WHERE IT IS DIFFICULT TO ACCESS THE BACK PANEL FOR DISCONNECTING THE DEVICE

IT IS RECOMMENDED THAT THE SWITCH OR CIRCUIT-BREAKER IS NEAR THE EQUIPMENT

THE SAFETY OF ANY SYSTEM THAT INCORPORATES THE DEVICE IS UNDER THE RESPONSIBILITY OF THE ASSEMBLER OF THE SYSTEM

13.1 Power-on Status

Power-on takes few seconds during which the front panel LEDs may flash.

At power-on, the module is in the following status:

- The Output Buffer is cleared
- Registers are set to their default configuration
- After power-on, only the NIM and PLL LOCK LEDs must lit (see **Fig. 13.1**).

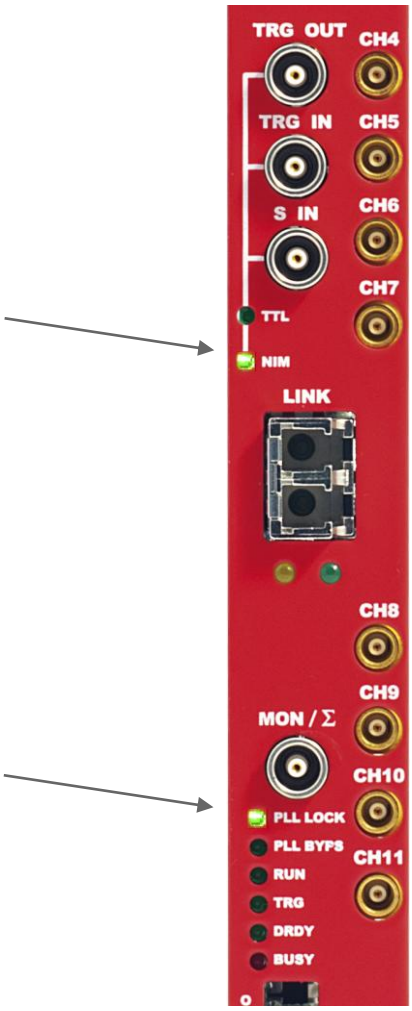


Fig. 13.1: Front panel LEDs status at power-on

14 Firmware and Upgrades

The board hosts one FPGA on the mainboard and one FPGA on each mezzanine (i.e. one FPGA manages 4 channels). The channel FPGAs firmware is identical. A unique file is provided, that updates all the mezzanine FPGAs and the mainboard FPGA at the same time.

ROC FPGA MAINBOARD FPGA (Readout Controller + Communication interface):

FPGA Altera Cyclone EP1C20

AMC FPGA MEZZANINE FPGA (ADC readout/Memory Controller):

FPGA Altera Cyclone EP3C16

The firmware is stored onto the on-board FLASH memory. Two copies of the firmware are stored in two different pages of the FLASH, referred to as Standard (STD) and Backup (BKP). The board is usually factory equipped with the same firmware version on both pages.

At power-on, a microcontroller reads the FLASH memory and programs the module by automatically loading the first working firmware copy (i.e. the STD one by default).

The on-board dedicated SW7 dip switch, which is set to STD by default, selects which FLASH page to be read for first at power-on (see Chap. **9**).

It is possible to upgrade the FPGA firmware (ROC and AMC) via VMEbus or Optical Link by writing the FLASH with the CAEN Toolbox software (see Chap. **12**).

IT IS STRONGLY SUGGESTED TO OPERATE THE DIGITIZER UPON THE STD COPY OF THE FIRMWARE. UPGRADES ARE SO RECOMMENDED ONLY ON THE STD PAGE OF THE FLASH. THE BKP COPY IS TO BE INTENDED ONLY FOR RECOVERY USAGE. IF BOTH PAGES RESULT CORRUPTED, THE USER WILL NO LONGER BE ABLE TO UPLOAD THE FIRMWARE VIA VMEbus OR OPTICAL LINK AGAIN AND THE BOARD NEEDS TO BE SENT TO CAEN IN REPAIR!

14.1 Firmware Updates

Firmware updates are available for free download on CAEN website in the Siftware/Firmware tab at the digitizer page (**login required**).

14.2 Firmware File Description

The firmware update is a CFA file (CAEN Firmware Archive) that aggregates all the programming files of the same firmware type supported by the specific digitizer family.

The CFA file name of the 743 Digitizer family follows this general scheme:

x743_rev_X.Y_W.Z.CFA

where:

- x743 are all the boards that can be updated by the CFA file.

  Options are:

  - DT5743
  - N6743
  - V1743
  - VX1743
- X.Y are the major (X) and minor (Y) revision numbers of the mainboard FPGA
- W.Z are the major (W) and minor (Z) revision numbers of the mezzanine FPGA

14.3 Troubleshooting

In the case of an upgrade failure (e.g. STD page is corrupted), users can try to reboot the board: after a power cycle, the system automatically programs the board from the alternative FLASH page (e.g. BKP FLASH page), if this is not corrupted as well (see **Fig. 13.1**). It is then possible to perform a further firmware upgrade to restore the corrupted page.

BECAUSE OF AN UPGRADE FAILURE, THE SW7 DIP SWITCH POSITION MAY NOT CORRESPOND TO THE FLASH PAGE FIRMWARE COPY LOADED ON THE BOARD FPGAs

OLD FLASH MEMORIES

The STD and BKP firmware copy management by the onboard microcontroller is different in the case of old versions of the digitizer mainboard, characterized by mounting a smaller FLASH memory size:

THE SW7 DIP SWITCH POSITION CORRESPONDS TO THE FLASH PAGE FIRMWARE COPY LOADED ON THE BOARD FPGAs

Size information can optionally be retrieved from the board by:

- reading at the 0xF050 register by using, for example, the CAENComm demo sample**[RD4]**: ”0” means small size
- checking the value of the FLASH_TYPE parameter saved into the board info file that is generated by the Get Information File function in CAEN Toolbox**[RD1]:** FLASH TYPE = “0” means small size

Supposing the STD page corruption occurred, the following recovery procedure can be performed:

- Force the board to reboot by loading the copy of the firmware stored on the BKP page of the FLASH: power off the crate, move the SW7 switch to BKP position and power on the crate
- Use CAEN Toolbox to read the firmware revision (that is the one of the BKP page of the FLASH); in case of success, it is so possible to communicate again with the board
- Use CAEN Toolbox to load a compliant CFA firmware file on the STD page, then power off the crate, move the SW7 switch back to STD position, and power on the crate to make the new firmware loaded on the FPGA
- If the LED status is compliant to **Fig. 13.1**, then the board is operative again

If none of these steps helps, then it is recommended to contact CAEN Technical Support (see Chap. **18**).

15 Instructions for Cleaning

The equipment may be cleaned with isopropyl alcohol or deionized water and air dried. Clean the exterior of the product only.

Do not apply cleaner directly to the items or allow liquids to enter or spill on the product.

15.1 Cleaning the Air Vents

It is recommended to occasionally clean the air vents (if present) on all vented sides of the board. Lint, dust, and other foreign matter can block the vents and limit the airflow. Be sure to unplug the board before cleaning the air vents and follow the general cleaning safety precautions.

15.2 General Cleaning Safety Precautions

CAEN recommends cleaning the device using the following precautions:

- Never use solvents or flammable solutions to clean the board.
- Never immerse any parts in water or cleaning solutions; apply any liquids to a clean cloth and then use the cloth on the component.
- Always unplug the board when cleaning with liquids or damp cloths.
- Always unplug the board before cleaning the air vents.
- Wear safety glasses equipped with side shields when cleaning the board.

16 Device Decommissioning

After its intended service, it is recommended to perform the following actions:

- Detach all the signal/input/output cable
- Wrap the device in its protective packaging
- Insert the device in its packaging (if present)

THE DEVICE SHALL BE STORED ONLY AT THE ENVIRONMENT CONDITIONS SPECIFIED IN THE MANUAL, OTHERWISE PERFORMANCES AND SAFETY WILL NOT BE GUARANTEED

17 Disposal

The disposal of the equipment must be managed in accordance with Directive 2012/19 / EU on waste electrical and electronic equipment (WEEE).

The crossed bin symbol indicates that the device shall not be disposed with regular residual waste.

18 Technical Support

To contact CAEN specialists for requests on the software, hardware, and board return and repair, it is necessary a MyCAEN+ account on www.caen.it:

https://www.caen.it/support-services/getting-started-with-mycaen-portal/

All the instructions for use the Support platform are in the document:

A paper copy of the document is delivered with CAEN boards.

The document is downloadable for free in PDF digital format at:

https:/www.caen.it/safety-information-product-support

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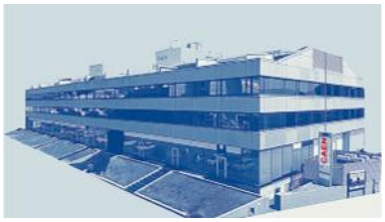
www.caen-india.in



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