PRELIMINARY

Technical Information Manual

Revision n. 2

16 July 2012

DEMO4

GATE AND DELAY GENERATOR

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1 Introduction

This Demo is a design example that implements a *Gate and Delay Generator* and shows how to use the programmable and the free running delay lines of the V1495 General Purpose VME board. For more detail, in this Demo you will see:

- AND/OR function between I/Os;
- Use of PLL to synthesize high clock frequency;
- Use of FIFO to save events;
- Single read/write access on VME using Local Bus Interface;
- read access on VME with BLock Transfer mode (BLT) using Local Bus Interface

Notice that hereafter we do not use anymore the HAL (Hardware Abstraction Layer) that is a HDL module used in the old demos to help the hardware interfacing. This was done not to limit but to offer to the end user a further degree of freedom.

1.1 Assumption

We assume that you have a basic knowledge of FPGA and QuartusII software, as well as the VHDL language in which the design (firmware) is written.

1.2 Before you Begin

The design and simulation of this demo was done working on Windows O.S. Before proceeding, you must install on your computer Altera QuartusII 8.0 or later Web/Full edition (to generate the programming file for the V1495 board), ModelSim-Altera 6.1 or later (to simulate the Demo) and the CAEN V1495 Tool (windows) http://www.caen.it/nuclear/lista-sw.php?mod=V1495 to test the V1495 board.
You can freely download the Web edition of Altera QuartusII and ModelSim-Altera at Altera website: http://www.altera.com/index.jsp
The Demo 4 *Gate and Delay Generator* is available at CAEN website:
http://www.caen.it/nuclear/lista-sw.php?mod=V1495

1.3 Demo Folder Structure

Below is shown the structure and the content of the file Demo4.zip. A short description about the organization of this folder follows.

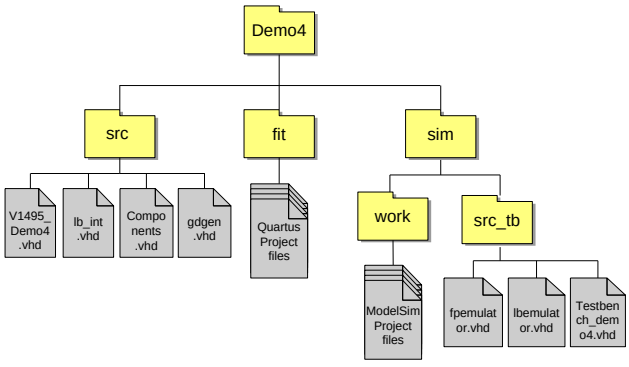

Fig. 1.1: Demo Folder Structure

The “src” folder contains the source VHDL files of the reference design where the main file is *V1495_Demo2.vhd*. The “fit” folder contain the Demo’s Quartus project. This project provides a complete pinout of the FPGA and it is also enabled to generate RBF type file (*v1495_Demo2.rbf*) used to program the USER FPGA of the V1495 board. The “sim” folder contains the ModelSim project for the functional simulation of this Demo. In addition, the “src_tb” folder hosts the testbench files for the functional simulation that are included into the ModelSim project. The main testbench file is *Testbench_Demo2.vhd*.

2 Gate and Delay Generator Demo

2.1 Gate and Delay Generator

As we have seen in the introduction, the purpose of this Demo is to show how to use and to configure the delay devices that the V1495 provides. We used both Programmed Delay Line and Free running Delay Line devices. The G0/G1 LEMO ports are configured as input ports for the V1495 board where in the G1 goes the start signal and in the G0 port goes the external asynchronous reset signal. The output of the PDL is mapped in the D7 LEMO port and the FDL output in the D0 LEMO port. We have used the A395D expansions. The output signal is triggered by the rising edge of the input start signal and after a *offsetDelay* + *Delay* time it goes and stays high for a time equal to *offsetGate* + *Gate*. After the first rising edge of the start signal, the device is not more sensitive to the input signal until the generator of the output signal is finished. If the user press the asynchronous reset, that is, generates an asynchronous signal in the G0 pots, the output is reset instantly and the system become ready for a new gate and delay output generation. The Fig. below shows the timing diagram of the gate and delay generator.

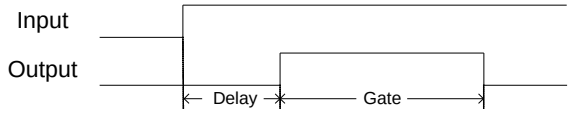

Fig. 2.1: Main block diagram of Pattern Recorder

PORT	FUNCTION
Port G0	Asynch Reset (Input)
Port G1	Start (Input)
Port D0	FDL Output
Port D7	PDL Output

Table 2.1: Port Map

2.2 Registers

In this example, there are 4 registers called *delay_fdl* (REG_RW4), *gate_fdl* (REG_RW5), *delay_pdl* (REG_RW 6) and *gate_pdl* (REG_RW 7) that can be written and read from the VME (through the local bus) and where the user can set the gate and delay time for both of the proposed solution. The registers are 32/8 bit wide and can be accessed in single mode. The Tab below reports the address map of the register where *Base* is the base address of the V1495 board

ADDRESS	REGISTER/CONTENT	DEFAULT VALUE (HEX)	REGISTER	ADDR/DATA	R/W
Base + 0x1018	ctrlreg	0x00000013	Reg_RW3	A32/D32	R/W
Base + 0x101C	delay_fdl	0x0000004F	Reg_RW4	A32/D32	R/W
Base + 0x1020	gate_fdl	0x0000000F	Reg_RW5	A32/D32	R/W
Base + 0x1024	delay_pdl	DIP SW6 Configuration	Reg_RW6	A32/D32	R/W
Base + 0x1028	gate_pdl	DIP SW5 Configuration	Reg_RW7	A32/D32	R/W
Base + 0x100C[1]	Demo Version	0x00000041	Reg_R6	A32/D32	R

Table 2.2: Register address map

[1] 0x100C is the firmware release register. The user must provide this register in read mode and make sure to use only the first eight bit (LSB [7 … 0]). The other bits should be set at '0' logic level otherwise malfunction in the V1495 board may occur.

2.2.1 CRTL_REG Register (B.A + 0x1018, A32, D32, R/W)

In addition, there is a fifth register called *ctrlreg* where the user can set the output level for the LEMO ports and the direction of PDL data. The table below describes the allowed settings of the *ctrlreg* register.

Bit	CTRL_REG Function
[0]	Port D level select: 0 = NIM level 1 = TTL level
[1]	Port G level select: 0 = NIM level 1 = TTL level
[4]	Direction of PDL data: 0 = Read Dip Switches 1 = Write from FPGA

Table 2.3: ctrlreg register function settings

DIP SW6 DELAY0 sets the delay value and the DIP SW5 DELAY1 sets the gate value.
It is recommended that both ports (D and G) are set to the same level NIM or TTL and the direction of PDL is set to "1" so the user can determine the delay and the gate of the output signal setting the corresponding register.

2.3 Implementation

In figure Top-Down files hierarchy is shown for this demo where, as we see before, *V1495_Demo2.vhd* is the top level file of this Demo and the *Testbench_Demo2.vhd* is the top level file of the simulation process.

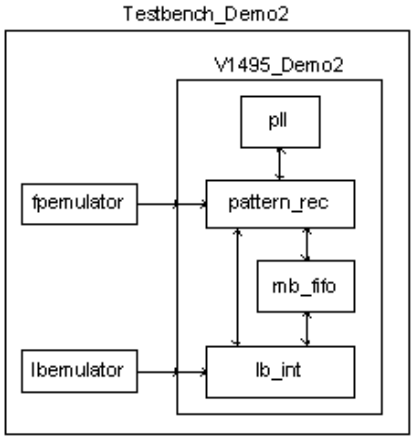

Fig. 2.2: Top Down files hierarchy

We must point out that in the VHDL *gdgen.vhd* file, all the signal that belong to the PDL have the suffix "_pdl" and the signals that belong to FDL have the suffix "_fdl".

2.4 Programmable Delay Line

To generate the gate and delay signal, in this proposed solution, we have used both Monolithic 8-bit Programmable Delay Line (Series 3D3428S-1) devices. The following figure shows the timing diagram for programming the PDL device.
For more information see: http://www.datadelay.com/datasheets/3d3428.pdf

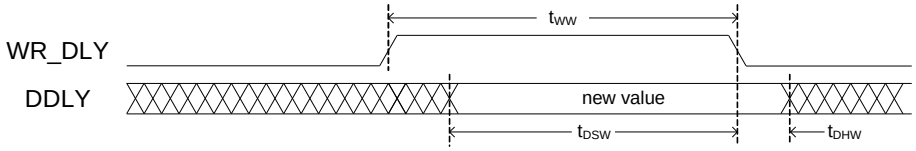

Fig. 2.3: Programming PDL time diagram

Parameter	Symbol	MIN	Units
Write Width	t_{WW}	10	ns
Data Setup to Write	t_{DSW}	10	ns
Data Hold from Write	t_{DHW}	3	ns

Table 2.4: Timing PDL parameters

In figure below the functional block diagram is shown of this example to generate a gate and delay signal using the PDL devices. As you can see the *pulse(0)* signal is the *start(0)* signal delayed by a Delay time that you can set into the *delay_pdl* register. The maximum value that you can set is 255ns with a resolution of about 1ns given by the PDL device.

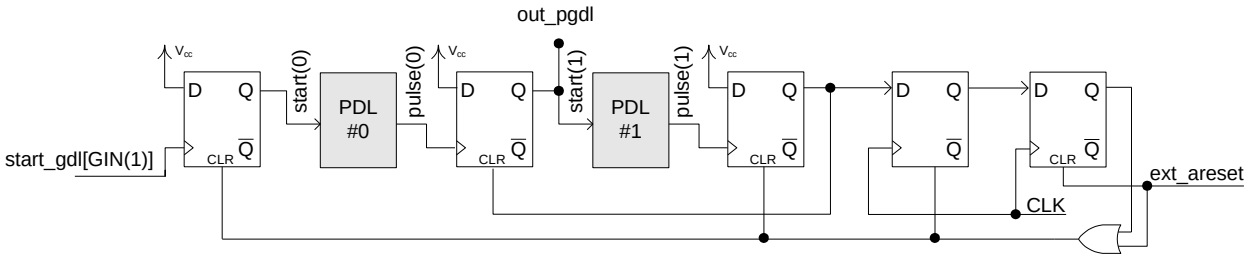

Fig. 2.4: Functional block diagram of gate and delay generation using PDL

The minimum value of the gate is equal to the *offset gate* (24ns) and the minimum delay is equal to the *offset delay* (56ns). Both *delay_pdl* and *gate_pdl* registers are 8 bit wide.

2.5 Free Running Delay Line

The Free Running Delay Line is a 2*25.7” STRIPLINE in the V1495 board which delay the input signal by 5,00 ns. In order to have multiple value of this intrinsic delay, two oscillators are used to perform a simple clock signal with period T=10,00 ns.

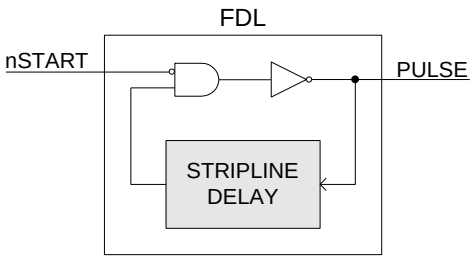

Fig. 2.5: Functional block diagram of Free Running Delay Line

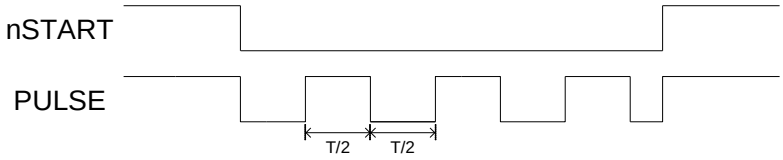

Fig. 2.6: Timing diagram of Free Run ning Delay Line

In Fig. 2.5 and Fig. 2.6 the functional and timing diagram of the FDL is shown. Counting the rising edge of the pulse signal you can obtain a span of N*T ns where N is the number given by the

counter and T=10,00 ns . In this way, compared with the solution with PDL, the maximum time we can obtain is (2^{32} – 1)*T. Note that both *delay_fdl* and *gate_fdl* register are 32 bit wide. The Fig. below shows the proposed solution for generating a gate and delay signal using one of the V1495 board's FDL.

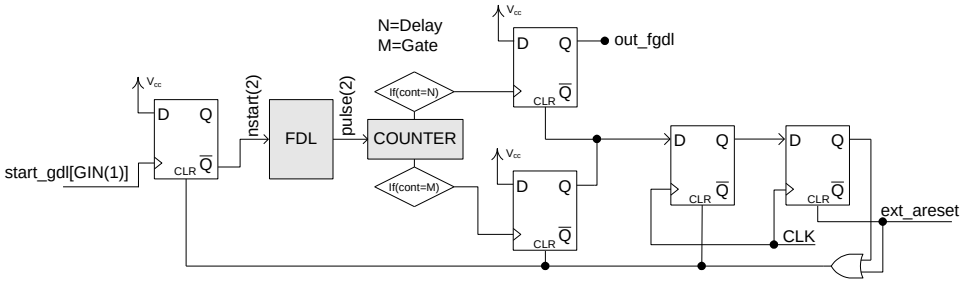

Fig. 2.7: Functional block diagram of gate and delay generation using FDL

The *offset gate* = 3ns and the *offset delay* = 34ns. If you set a 0 value in *gate or delay* register the output signal is 0.

3 Programming V1495 User FPGA

This instructions refer to Windows OS and upgrade your cvUpgrade Software and V1495 board firmware.

The first step is to ungrade your *cvUpgrade* Software so you need to download and install on your computer the latest software *cvUpgrade* Release 2.1. http://www.caen.it/nuclear/lista-sw.php?mod=V1495

Find *cvUpgrade* under *Control Software* list. Download it, unzip and then launch cvUpgradeSetup-2.1.exe file (Do not need to uninstall your old version of *cvUngrade,* it will be upgraded automatically).

It is necesary V1495 VME FPGA firmware release 1.0 or greater.

Upgrade the V1495 USER FPGA (see manual for more detail) with the demo firmware.

To do this, perform these steps:

1. launch windows command line from the same folder where the *cvUpgrade.exe* is located (ex: “C:\.....\CAEN\CVUpgrade\bin”);
2. Copy to the folder, indicated above, the *V1495_Demo4.rbf (*row binary format) configuration file that you find in fit folder.
3. Execute from the windows command line the command: “cvUpgrade.exe V1495_Demo4.rbf USB -link 0 -VMEbaseaddress 32100000 -param Cvupgrade_params_V1495_USER.txt” to program the user FPGA of the V1495 board with base address 0x32100000 by using a V1718 CAEN VME Bridge. If you use a V2718 CAEN VME Bridge you should put PCI_OPTLINK option instead of USB option in the command line above.(Note: instead of base address value above 0x32100000 should be the base address set on your V1495 board ex. 0xXXXX0000)
4. When the firmware is updated successfully power cycle the Crate.

For more information and examples how to upgrade WME/USER FPGA read the *readme.txt* file in the CVUpgrade folder installed on your computer.

4 Setup and Functional Simulation

4.1 Demo Setup

To setup the Demo follow the steps below:

1. Use a V1495 board with an A395D I/O expansion;
2. Program the V1495 USER FPGA (see Chapter 3);
3. Create a connection with the V1495 board to achieve a read/write access on VME.

For example, for this test we have used a V1718 bridge and the CAEN VME .NET Demo (C:\.....\CAEN\VME\CAENVMEDemoDotNet CaenVMEDemoDotNet.exe) to read/write the registers.

4. Set *CTRLREG* register;

This register configures the port level and the direction of the PDL data. The default port level value for both ports D and G is TTL and the direction of PDL data is “write from FPGA” , that is, the delay and gate value are set from the user via firmware and not from the “Dip Switches”

5. Set the Delay and Gate registers with the value you want to test.

Using an oscilloscope you’ll see the desired gate and delay output signal. It is recommended to use a SEC/DIV = 250ns oscilloscope setting.

6. Verify output 0 and output 7 signal of A395D.

N.B.: The A395D mezzanine card has a special pinout assignment, and there is not a direct correspondence between VHDL port signal and mezzanine channels; the following table explains the correspondence between A395D channels and the Mezzanine Expansion Ports lines (see also the V1495 User’s manual):

Table 4.1: A395D channels vs. Mezzanine Expansion Ports lines

Channel	Slot Data In Bus	Slot Data Out Bus
0	2	0
1	18	16
2	3	1
3	19	17
4	14	12
5	30	28
6	15	13
7	31	29

4.2 Functional Simulation

In order to run the functional simulation of this Demo, it is necessary to launch the *Testbench_Demo4.vhd* file. This file includes two other files, *lbemulator.vhd* and *fpemulator.vhd* that emulate the Local Bus Interface and the Front Panel of the V1495 Interface. The Fig. below shows the simulation result of the gate and delay generator using PDL. As you can see, with the gold color is marked the start signal and with the blue color is marked the output signal. In this simulation was set a Delay of 10 ns and a Gate of 7 ns.
To review this simulation load the *wave_pdl.do* file you find in the ModelSim “sim” folder.

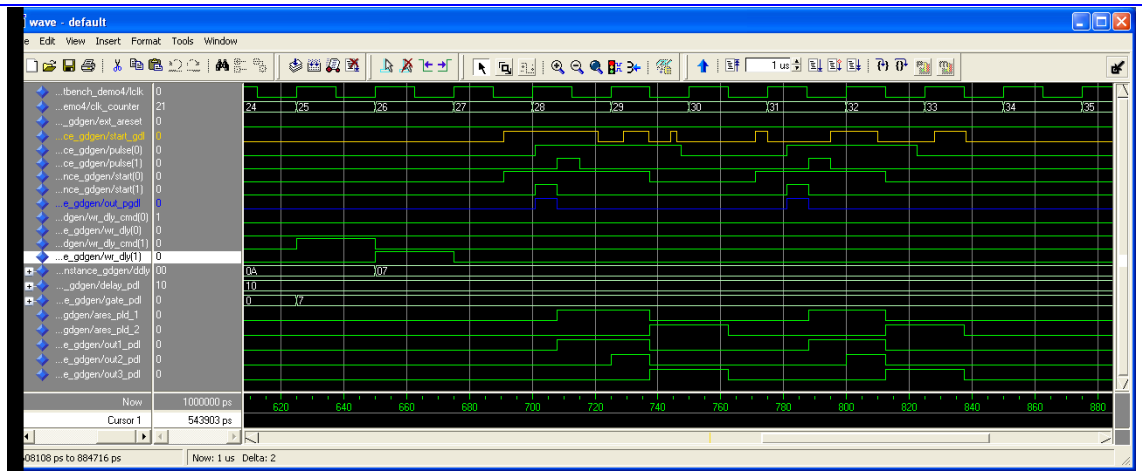

Fig. 4.1: Functional simulation result of PDL

Instead, Fig.below shows the simulation result of the gate and delay generator using FDL. With the gold color is marked the start signal and with the blue color is marked the output signal. In this simulation was set a Delay of 3*T ns and a Gate of 3*T ns where T=10,00 ns.
To review this simulation load the *wave_fdl.do* file in the “sim” folder.

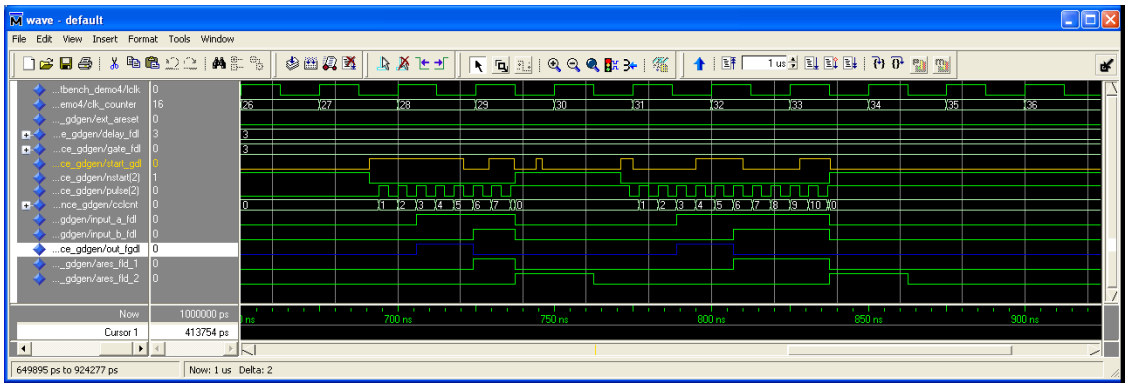

Fig. 4.2: Functional simulation result of FDL

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This CAEN SwFw Licence and the relationship between you and C.A.E.N. is governed by the laws of Italy.
This Agreement shall be construed and governed by Italian Law.
The United Nations Convention on the International Sale of Goods does not apply to this CAEN SwFw Licence.
Any dispute arising out of or in connection with this Agreement shall be referred to and finally resolved by Arbitration under the provisions of Italian Law (c.p.c. art 816 and following.) by one Arbitrator.
The Arbitrator shall be nominated from Chairman of the Court of Milan.
The place of Arbitration shall be Milan, Italy and the language shall be English.

9. Precedence.

This CAEN SwFw Licence constitute the entire understanding between the parties respecting use of the CAEN SwFw, superseding all prior agreements between you and C.A.E.N.. In the event of any conflict between the terms and conditions of this CAEN SwFw Licence, the terms and conditions of this CAEN SwFw Licence will control

10. Surviving Provisions.

Sections 2, and 4 through 10, will survive any termination of this Agreement.

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