PRELIMINARY

Technical Information Manual

Revision n. 3

19 November 2012

DEMO3

DIGITAL TO ANALOG CONVERTER (DAC)

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1 Introduction

This Demo is a design example that implements the interface and shows how to use a mezzanine card A395E (DAC) with the V1495 General Purpose VME board. For more detail, in this demo you will see:

- Use of I/O Expansion (A395E);
- DAC Interface;
- Single read/write access on VME using Local Bus Interface;

Notice that hereafter we do not use anymore the HAL (Hardware Abstraction Layer) that is a HDL module used in the old demos to help the hardware interfacing. This was done not to limit but to offer to the end user a further degree of freedom.

1.1 Assumption

We assume that you have a basic knowledge of FPGA and QuartusII software, as well as the VHDL language in which the design (firmware) is written.

1.2 Before you Begin

The design and simulation of this demo was done working on Windows O.S. Before proceeding, you must install on your computer Altera QuartusII 8.0 or later Web/Full edition (to generate the programming file for the V1495 board), ModelSim-Altera 6.1 or later (to simulate the Demo) and the CAEN V1495 Tool (windows) http://www.caen.it/nuclear/lista-sw.php?mod=V1495 to test the V1495 board.

You can freely download the Web edition of Altera QuartusII and ModelSim-Altera at Altera website: http://www.altera.com/index.jsp

The Demo 3 *Digital to Analog Converter* is available at CAEN website:

http://www.caen.it/nuclear/software_download.php

1.3 Demo Folder Structure

The Fig. 1.1 shows the structure and the content of the file Demo3.zip. Below we will give a short description about the organization of this folder.

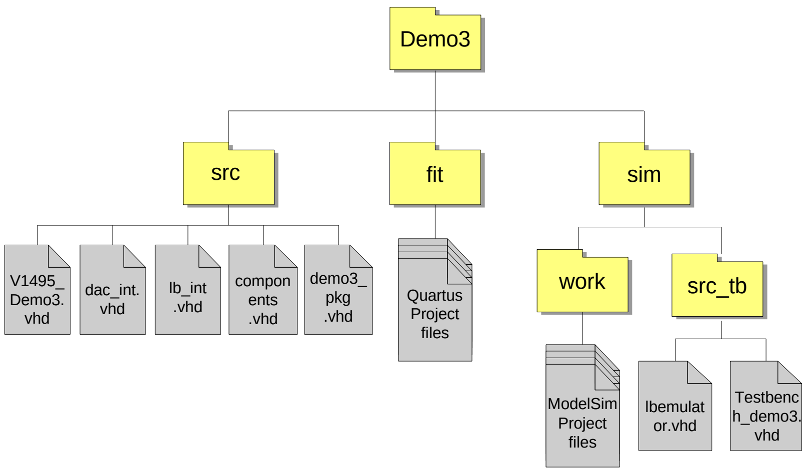

Fig. 1.1: Demo Folder Structure

In the “src” folder you find the source VHDL files of the reference design were the main file is *V1495_Demo3.vhd*. The “fit” folder contain the Demo’s Quartus project. This project provides a complete pinout of the FPGA and it is also enabled to generate RBF type file (*v1495_Demo3.rbf*) used to program the USER FPGA of the V1495 board. The “sim” folder contain the ModelSim project for the functional simulation of this Demo. In addition, under the “src_tb” folder you find the testbench files for the functional simulation that are included into the ModelSim project. The main testbench file is *Testbench_Demo3.vhd*.

2 DAC Demo

2.1 DAC

This Demo is an example of a possible implementation of the DAC interface for the control of the A395E mezzanine. The Fig. 2.2 shows a simple block diagram of the Demo implementation; in the figure only one DAC interface is represented but it is possible to install up to 3 DAC interfaces in the slots D, E, F of the V1495 board.

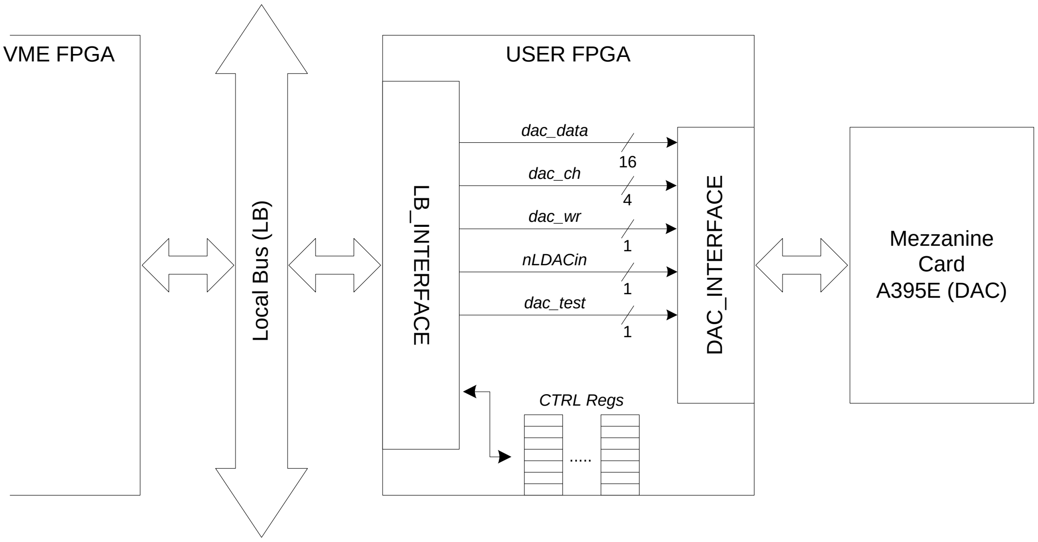

Fig. 2.1: DAC block diagram

The principle of operation of the Demo is the following: the DAC has two main operation mode *Normal/Testmode* that can be set configuring the CTRL register. In the Testmode each DAC channel generates a sawtooth signal to evidence the correct function of all the channels. In Normal mode, the user can select one channel or all the channels simultaneously through the *'dac_ch signal'* and set the analog value to be converted using the *'dac_data signal'*. All this settings are made by means of a write access to the specific registers. Once the voltage setting has been sent to the DAC, depending on the "Update Mode" bit in the CTRL register (see Tab. 2.3), the analog output can be updated immediately or in a second time by the user, by means of a write access to the Update register.

For test and debug purpose, it is possible to read the CTRL register and the identification code of the mezzanine that is mounted in the slot D or E or F.

2.2 Registers

In this example, there are 9 registers reported in Tab. 2.1. All the registers can be written and/or read (see label Read/Write) from the VME (through the local bus).
The registers are 32 bit wide and can be accessed in single mode. The Tab. 2.1 reports the address map of the register where *Base* is the base address of the V1495 board.

ADDRESS	REGISTER/CONTENT	ADDR	DATA	Read/Write
Base + 0x1000	Control Register	A32	D32	R/W
Base + 0x1004	Control Set Register	A32	D32	W
Base + 0x1008	Control Clear Register	A32	D32	W
Base + 0x100C[1]	Firmware Revision	A32	D32	R
Base + 0x1010	Dac Update	A32	D32	W
Base + 0x1014	ID Slot D	A32	D32	R
Base + 0x1018	ID Slot E	A32	D32	R
Base + 0x101C	ID Slot F	A32	D32	R
Base + 0x1100 -0x115C	Individual DAC Setting	A32	A32	R/W
Base + 0x1160	All slot DAC Setting	A32	A32	R/W

Table 2.1: Register address map

2.2.1 Slot ID Register (B.A + 0x1014/8/C, A32, D32, R)

The table below reports the identification code of all types of mezzanine, produced by CAEN, that can be mounted on slots D, E, F. This is achieved by reading the registers ID Slot D/E/F.

Bit	Function
[2:0]	Identification Mezzanine: “000” = A395A “001” = A395B “010” = A395C “011” = A395D “100” = A395E (expected value for V1495 DAC) “111” = No piggy back added

Table 2.2: Mezzanine identification code

N.B.: The A395D mezzanine card has a special pinout assignment, and there is not a direct correspondence between VHDL port signal and mezzanine channels; the following table explains the correspondence between A395D channels and the Mezzanine Expansion Ports lines (see also the V1495 User’s manual):

Table 2.3: A395D channels vs. Mezzanine Expansion Ports lines

Channel	Slot Data In Bus	Slot Data Out Bus
0	2	0
1	18	16
2	3	1
3	19	17
4	14	12
5	30	28
6	15	13
7	31	29

[1] 1 0x100C is the firmware release register. The user must provide this register in read mode and make sure to use only the first eight bit (LSB [7 … 0]). The other bits should be set at ‘0’ logic level otherwise malfunction in the V1495 board may occur.

2.2.2 CTRL Register (B.A + 0x1000, A32, D32, R/W)

In the Control Register (see Tab. 2.3) the user can set the *DAC Mode* Normal/Test and the *Update Mode*. If the CTRL register is set to *Automatic Update,* the output is updated immediately once the user sets the analog value to convert; If the CTRL register is set to *On Command Update* the output is not updated when the user sets the analog value to convert but is updated by means of a write access to the DAC Update register (writing any value).

In Test Mode, each DAC channel generates a sawtooth signal from -5V to 5V (high impedance termination) or -4V to 4V (200Ω termination), with about 160 ms period.

Bit	Function
[1]	DAC Update Mode: 0 = Automatic Update Mode (default) 1 = On Command Update Mode
[0]	DAC Mode: 0 = Normal (default) 1= Test Mode

Table 2.4: DAC register function settings

2.2.3 Control Set/Clear Register (B.A + 0x1004/8, A32, D32, W)

A write access in the Control Set Register with a bit ‘1’ sets the relevant bit to 1 in the Control Register. A write access with the bit set to ‘0’ does not change the Control Register content.

A write access in the Control Clear Register with a bit to ‘1’ clears the relevant bit in the Control Register.

A write access with the bit set to ‘0’ does not change the Control Register content.

2.2.4 DAC Setting Register (B.A + 0x1100/5C, A32, D32, R/W)

In the DAC Setting Register (seeTab. 2.4) the user can set for each channel a digital value that will be converted into analog voltage by the following relationship:

$$V_{out} = (DAC\_setting * 0.15 - 5000)mV$$

Bit	Funcion
[15÷0]	Digital value to be converted

Table 2.5: DAC Setting content

The correspondence between channels, slot V1495 and the address of the Dac Setting register is arranged as follows where the *SLOT* is the Slot Identifier (see Tab. 2.5) of the V1495 board. Each A395E mezzanine has 8 channels so the three bits *CHANN* are used to encode the 8 channels.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Addr***** [15:0]	0	0	0	1	0	0	0	1	0	SLOT		CHANN			0	0

Addr*	Slot Identifier
[6÷5]	"00" = Slot F "01" = Slot E "10" = Slot D "11" = select all channels of all slots; Allows to set the Output Dac at the same value for all channel.

Table 2.6: Slot D/E/F identifier

The address (Addr*) is different for each channel and the table below reports all the channel addresses

Slot	Chann.	Addr* (Hex)
Slot F	0	0x1100
	1	0x1104
	…	…
	7	0x111C
Slot E	0	0x1120
	1	0x1124
	…	…
	7	0x113C
Slot D	0	0x1140
	1	0x1144
	…	…
	7	0x115C
All Slots	ALL	0x1160

Note: At power-on 0800 is read on register (0V output)

2.3 Implementation

In Fig. 2.3 Top-Down files hierarchy is shown for this demo where, as we see before, *V1495_Demo3.vhd* is the top level file of this Demo and the *Testbench_Demo3.vhd* is the top level file of the simulation process.

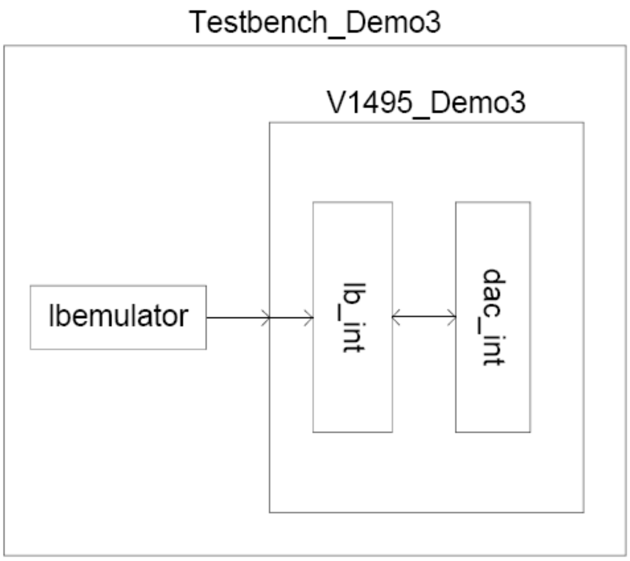

Fig. 2.2: Top Down files hierarchy

2.3.1 DAC Interface

The DAC interface provides a simple way for the user to drive the A395E mezzanine. The Fig. 2.4 shows the timing diagram of DAC interface. The outputs are updated after a T_{min} the data acquiring time of the A395E mezzanine.

The channel *"dac_ch signal"* and the value to be convert *"dac_data signal"* are obtained by the address of the DAC Setting Register.

The *"nLDACin"* is the signal that updates the output channels. This signal can be always active low (set by the user through the Control Register) so the updating of the output channels comes when a new value for the DAC is ready or the updating can be generated on Command by means of a write access to the Dac Update register.

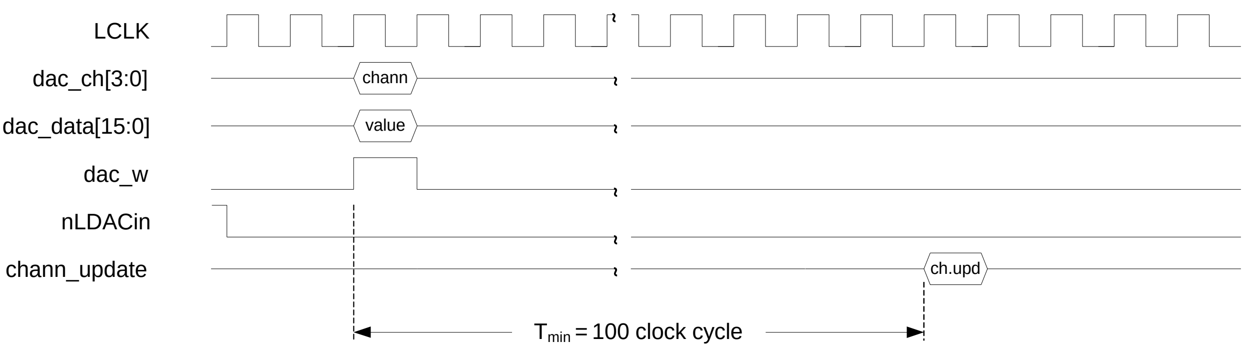

Fig. 2.3: Timing diagram of the DAC interface

Instead, in Fig. 2.5 is shown the timing diagram but in this case the updating of the output channels is on command by means of a write access on the DAC Update register. Notice that the write access on the DAC Register must be done after T_{min} time where the T_{min} is the data acquiring time of the A395E mezzanine.

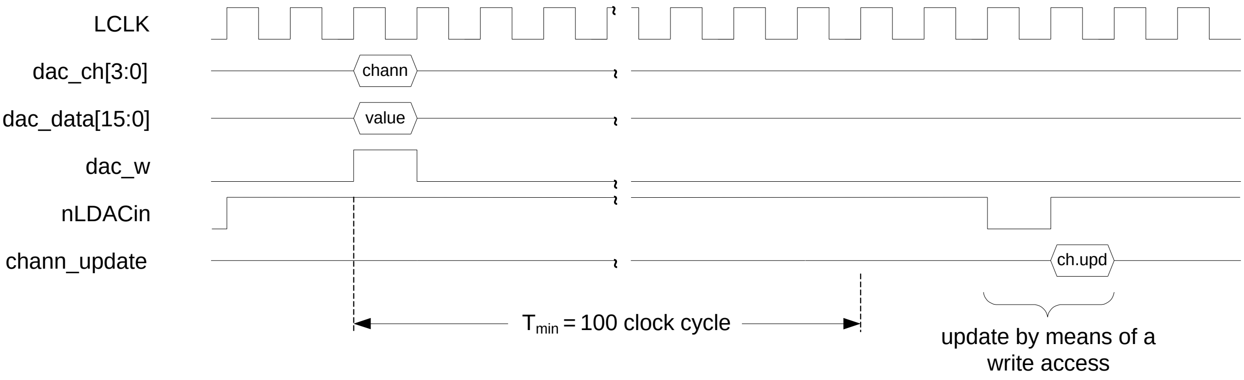

Fig. 2.4: Channel update by means of a write access on the Dac Update register

Take into account that in the system start up phase the A395E mezzanine becomes ready after 13,6 µs (at 40MHz).

For more information about the timing and the A395E mezzanine interface see

http://www.analog.com/static/imported-files/data_sheets/AD5668-EP.pdf

3 Programming V1495 User FPGA

This instructions refer to Windows OS in order to install the demo on V1495.

The first step is to upgrade your *cvUpgrade* Software so you need to download and install on your computer the latest software *cvUpgrade*. http://www.caen.it/nuclear/lista-sw.php?mod=V1495

Find *cvUpgrade* under *Control Software* list. Download it, unzip and then launch cvUpgradeSetup-2.1.exe file (Do not need to uninstall your old version of *cvUpgrade,* it will be upgraded automatically).

It is necesary V1495 VME FPGA firmware release 1.0 or greater.

Upgrade the V1495 USER FPGA (see manual for more detail) with the demo firmware.

To do this, perform these steps:

launch windows command line from the same folder where the *cvUpgrade.exe* is located (ex: “C:\.....\CAEN\CVUpgrade\bin”);

Copy to the folder, indicated above, the *V1495_Demo3.rbf (*row binary format) configuration file that you find in fit folder.

Execute from the windows command line the command: “cvUpgrade.exe V1495_Demo3.rbf USB -link 0 -VMEbaseaddress 32100000 -param Cvupgrade_params_V1495_USER.txt” to program the user FPGA of the V1495 board with base address 0x32100000 by using a V1718 CAEN VME Bridge. If you use a V2718 CAEN VME Bridge you should put PCI_OPTLINK option instead of USB option in the command line above.(Note: instead of base address value above 0x32100000 should be the base address set on your V1495 board ex. 0xXXXX0000)

When the firmware is updated successfully power cycle the Crate.

For more information and examples how to upgrade WME/USER FPGA read the *readme.txt* file in the CVUpgrade folder installed on your computer.

4 Setup and Functional Simulation

4.1 Demo

To test the Demo follow the steps below:

1. See Chapter 3;
2. Create a connection with the V1495 board to achieve a read/write access on VME.

For example, for this test we have used a V1718 bridge and the CAEN VME .NET Demo to read/write the registers; see download section of th webpage:

http://www.caen.it/nuclear/product.php?mod=V1718

3. Set *CTRL* register;

To test the DAC set the CTRL register in *Test Mode* via a write access on the relevant address (B.A. + 0x1000 in A32); using an oscilloscope (1 Mohm termination) you see at the output of each channel a sawtooth wave between –5V e +5V.

To use the DAC set the CTRL register in *Normal Mode*

4. Set Dac Setting registers;

4.2 Functional Simulation

To run the functional simulation of this Demo you have to launch the *Testbench_Demo3.vhd* file. This file includes the *lbemulator.vhd* that emulate the Local Bus Interface of the V1495 Interface. The Fig. 3.6 shows the simulation result of the Digital to Analog Converter (DAC).
To review this simulation load the *wave_pdl.do* file you find in the ModelSim "sim" folder.

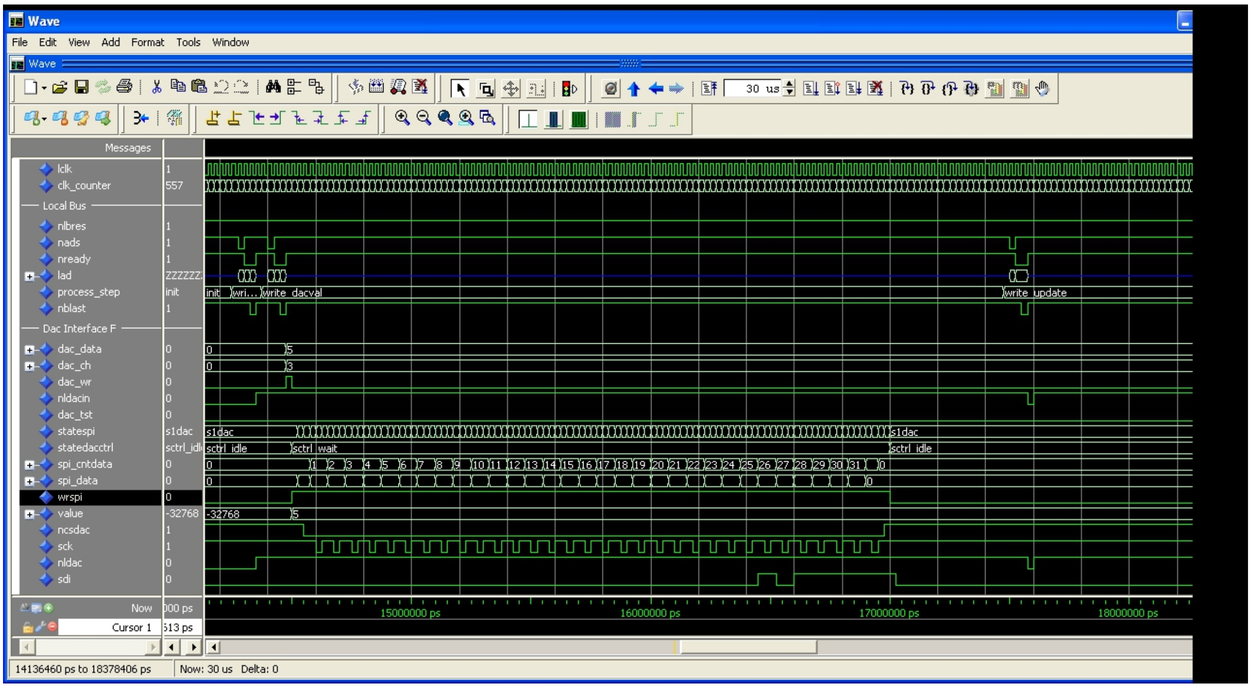

Fig. 4.1: Functional simulation result

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