PRELIMINARY

Technical Information Manual

Revision n. 1

28 July 2010

DEMO2

PATTERN RECORDER

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1 Introduction

This Demo is a design example that implements a pattern recorder and shows how to use the block transfer mode with the V1495 General Purpose VME board. For more detail, this demo provides:

- AND/OR function between I/Os;
- Use of PLL to synthesize high clock frequency;
- Use of FIFO to save events;
- Single read/write access on VME using Local Bus Interface;
- read access on VME with BLock Transfer mode (BLT) using Local Bus Interface

Notice that hereafter we do not use anymore the HAL (Hardware Abstraction Layer) that is a HDL module used in the old demos to help the hardware interfacing. This was done not to limit but to offer to the end user a further degree of freedom.

1.1 Assumption

We assume that you have a basic knowledge of FPGA and QuartusII software, as well as the VHDL language in which the design (firmware) is written.

1.2 Before you Begin

The design and simulation of this demo was done working on Windows O.S. Before proceeding, you must install on your computer Altera QuartusII 8.0 or later Web/Full edition (to generate the programming file for the V1495 board), ModelSim-Altera 6.1 or later (to simulate the Demo) and the CAEN V1495 Tool (windows) http://www.caen.it/nuclear/lista-sw.php?mod=V1495 to test the V1495 board.
You can freely download the Web edition of Altera QuartusII and ModelSim-Altera at Altera website: http://www.altera.com/index.jsp
The Demo 2 *Pattern Recorder* is available at CAEN website:
http://www.caen.it/nuclear/lista-sw.php?mod=V1495

1.3 Demo Folder Structure

Below is shown the structure and the content of the file Demo2.zip. A short description about the organization of this folder follows.

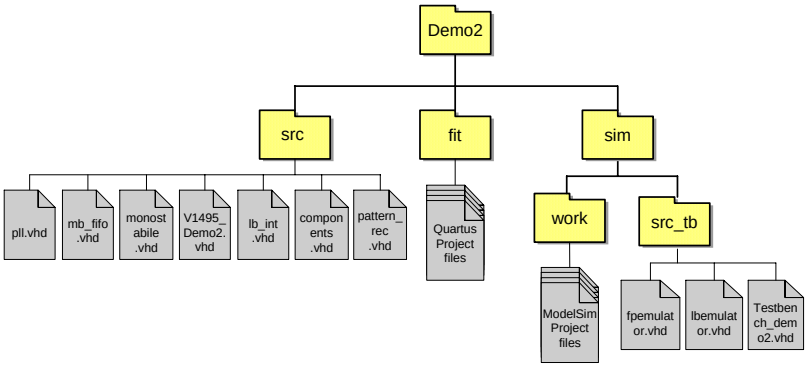

Fig. 1.1: Demo Folder Structure

The “src” folder contains the source VHDL files of the reference design where the main file is *V1495_Demo2.vhd*. The “fit” folder contain the Demo’s Quartus project. This project provides a complete pinout of the FPGA and it is also enabled to generate RBF type file (*v1495_Demo2.rbf*) used to program the USER FPGA of the V1495 board. The “sim” folder contains the ModelSim project for the functional simulation of this Demo. In addition, the “src_tb” folder hosts the testbench files for the functional simulation that are included into the ModelSim project. The main testbench file is *Testbench_Demo2.vhd*.

2 Pattern Recorder Demo

2.1 Digital Pattern Recorder

This demo shows the implementation of a digital pattern recorder. The principle of operation is the following: when the START signal is received, the 32 digital inputs coming from the port A or B are sampled at a specific sampling rate and a certain number of samples (Record Length) are saved into the relevant FIFO; once all samples have been stored, they become available for the readout from the VME (through the local bus), Fig. 2.1: .

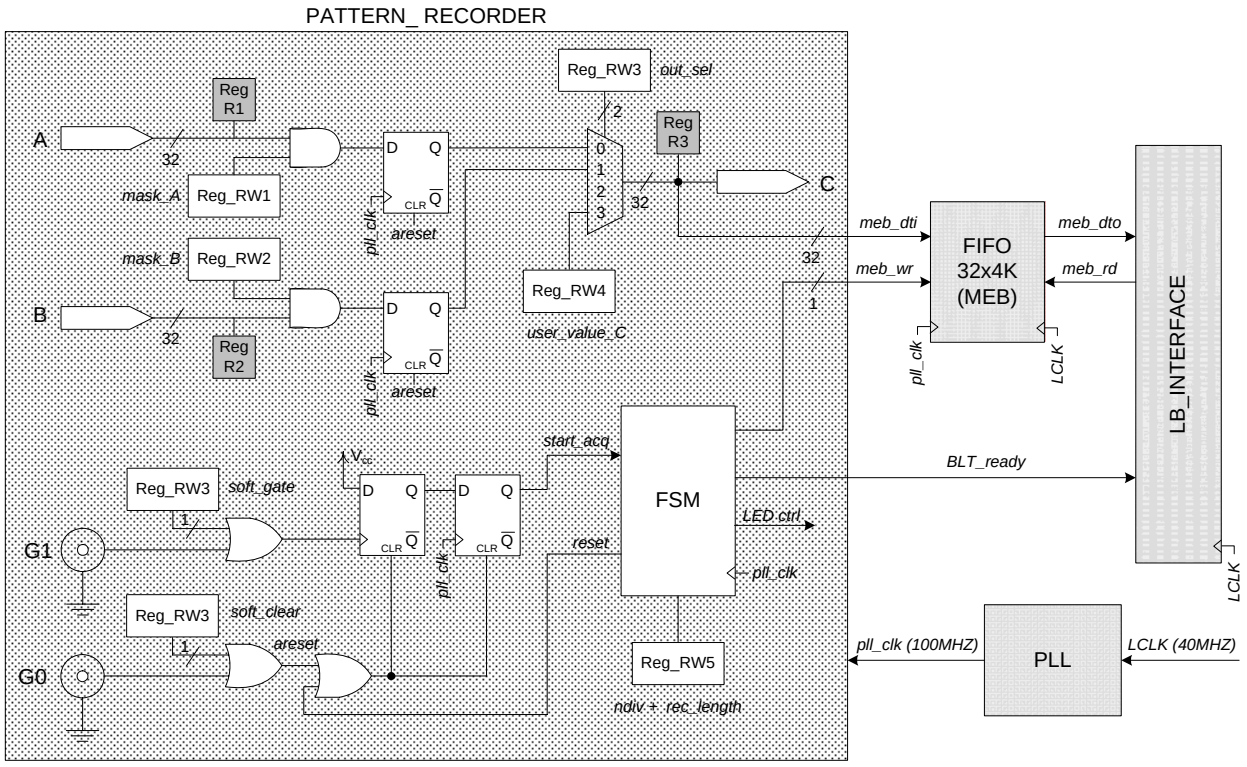

Fig. 2.1: Main block diagram of Pattern Recorder

The 32 bit output port C is used to reproduce the samples during the acquisition. Both the sampling frequency and the record length are programmable.
The START signal can come from the port G1 or be generated internally by means of a write access to a specific register. The acquisition starts on the rising adge of the Start signal; once started, the system is no longer sensitive to any further START until a reset is asserted; this can be done by the user either sending a pulse into the G0 input or making a write access to the relevant register.
For test and debug purpose, it is possible to read on the fly the 32 bit digital patterns on the inputs A and B as well as on the output C. It is possible to force the output C with a user defined pattern.

2.2 Registers

In this example, there are 9 registers reported in the table below. The first five register can be written and read from the VME (through the local bus) where the user can set different value and setting for the pattern recorder. The last four register can only be read from the user. All the registers are 32 bit wide and can be accessed in single mode. The table below reports the content and the address map of the register where *Base* is the base address of the V1495 board.

ADDRESS	REGISTER/ CONTENT	DEFAULT VALUE (HEX)	REGISTER	ADDR/ DATA	READ/ WRITE
Base + 0x1010	Mask_A	0xFFFFFFFF	Reg_RW1	A32/D32	R/W
Base + 0x1014	Maks_B	0x00000000	Reg_RW2	A32/D32	R/W
Base + 0x1018	Ctrl_reg	0x00000001	Reg_RW3	A32/D32	R/W
Base + 0x101C	User_output_C	0xDEADBEEF	Reg_RW4	A32/D32	R/W
Base + 0x1020	Ndiv_length	0x00000402	Reg_RW5	A32/D32	R/W
Base + 0x1030	Port A value	0x00000000	Reg_R1	A32/D32	R
Base + 0x1034	Port B value	0x00000000	Reg_R2	A32/D32	R
Base + 0x1038	Port C value	0x00000000	Reg_R3	A32/D32	R
Base + 0x103C	(not used)		Reg_R4	A32/D32	R
Base + 0x1040	(not used)		Reg_R5	A32/D32	R
Base + 0x100C	Demo Version	0x00000021	Reg_R6	A32/D32	R
Base + 0x0000	FIFO Content			A32/D32	R

Table 2.1: Register address map

2.2.1 CRTL_REG Register (B.A + 0x1018, A32, D32, R/W)

In the *ctrlreg* (REG_RW3) register the user can set the input level for the LEMO port, the mux selection value and the software clear/start control.

Bit	CTRL_REG Function
[0]	Port G level select: 0 = NIM level 1 = TTL level
[5÷4]	Output MUX selection 0 = Channel A 1 = Channel B 2/3 = user output C
[8]	Soft clear (active high)
[9]	Soft start (active high)

Table 2.2: ctrlreg register function settings

2.2.2 NDIV_LENGTH Register (B.A + 0x1020, A32, D32, R/W)

In the *ndiv_length* (REG_RW5) register the user can set the number of sample (Record Length) and the frequency divider factor that determines the sampling:

$$f_{sample} = {}^{100}/_{ndiv}\ MHz.$$

The table below describes the allowed settings of the *ndiv_length* register.

Bit	Ndiv_length REGISTER Function
[3÷0]	Frequency divider (ndiv)
[15÷4]	Length of Data (rec_length)

Table 2.3: ndiv_length register function settings

Note: 0x100C is the firmware release register. The user must provide this register in read mode and make sure to use only the first eight bit (LSB [7 … 0]). The other bits should be set at '0' logic level otherwise malfunction in the V1495 board may occur.

2.3 Implementation

The FSM, see Fig. 2.1: , handles all the calculation and drives all the control signals for the FIFO and for the block transfer. It consists of 3 state (IDLE, ACQ, WAIT_END). The ACQ state performs the frequency divider and drives the writing signal of the FIFO. When the number of requested samples is reached, the acquisition of data is stopped and a BLT ready (BLT_ready signal) is send to the LB_INTERFACE. In the WAIT_END state, when the FIFO (MEB) has no more data, the BLT ready signal is reset and the system becomes ready for a new data acquisition. In the table below are described some of the functions indicated by the color light of the user LED located in the Front Panel of the V1495 board.

Color Light	Description
Red	The system is in reset state.
Red pulse[1]	The reset of the system was performed.
Green	IDLE state; ready for a new data record.
Orange pulse	Start acquisition process

Table 2.4: User led color description

In figure below Top-Down files hierarchy is shown for this demo where, as we see before, *V1495_Demo2.vhd* is the top level file of this Demo and the *Testbench_Demo2.vhd* is the top level file of the simulation process.

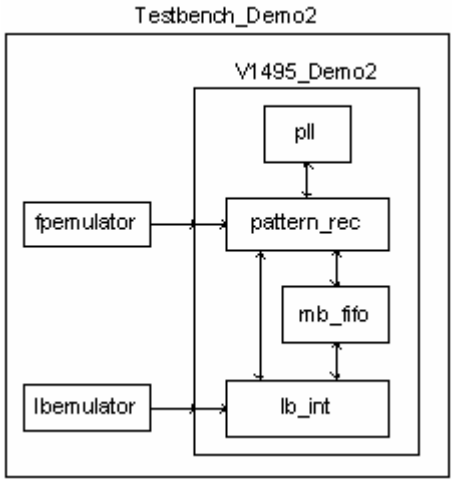

Fig. 2.2: Top Down files hierarchy

2.3.1 PLL/MB_FIFO

PLL and the MB_FIFO entities have been generated using the Quartus Megawizard Plug-In Manager. Note: MB_FIFO is a show-ahead synchronous FIFO.

[1] The pulse is generated by a monostable and has a duration of 167ms;

3 BLock Transfer Mode and the Local Bus Interface

3.1 Address Space

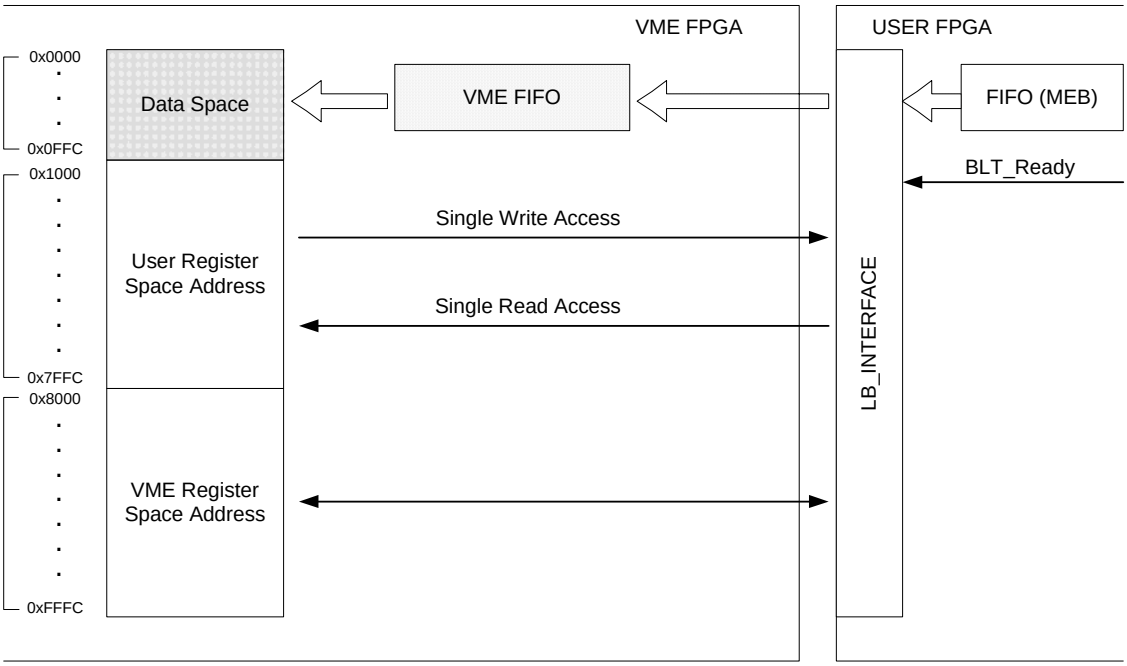

Fig. 3.1: Address Space block diagram

Before proceeding let's have a look how the address space is mapped. All the internal addresses are referred to the Base Address of the board. The space addresses, figure above, are the offsets to be added to the board Base Address (Base + offset).
The first range 0x0000 ÷ 0x0FFC is the *Data Space* where you can carry out Single/BLT access (no MBLT access). The second range of addresses is the space where the user can map its own registers and the third range is the VME register space address.
As you can see in figure above, to increase the performance for the BLT, the VME FPGA makes use of an internal FIFO (VME FIFO) that is used to anticipate the transfer of some user data. The buffer memory for the Block Transfer (in V1495 boards) is structured as a FIFO (not to confuse with VME FIFO) therefore it hasn't addresses. On VME, during the BLT cycles, address is incremented each cycle. For these reasons, to permit the reading in BLT mode up to 4KB, the FIFO (buffer memory) is mapped in the range from 0x0000 to 0x0FFC and the user, to perform the BLT, must read only the 0x0000 address. In this demo, inside the *lb_int.vhd* file (line 95) A_MEB constant is set to 0x0000 and this value should not be modified.

3.2 Single Read/Write Access

The figure below shows the timing diagram for single access in D32 read and write mode.

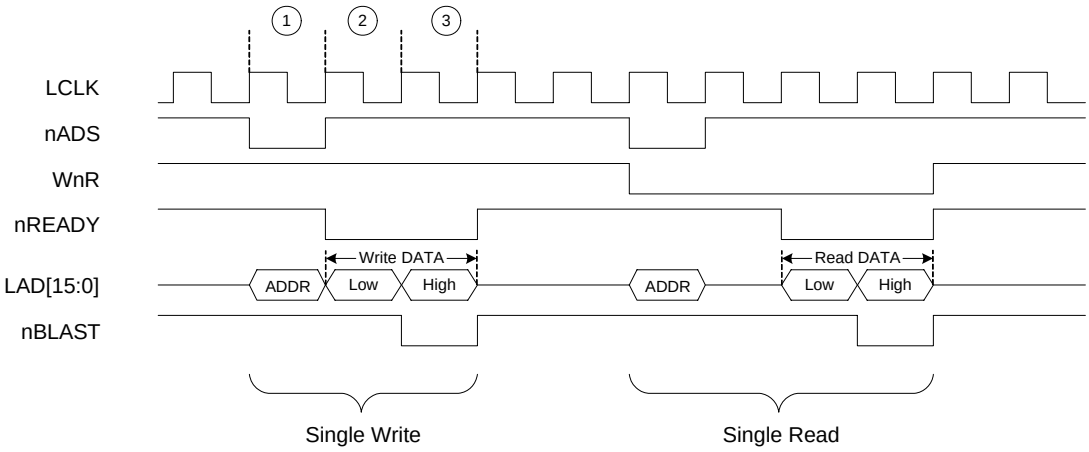

Fig. 3.2: AddSingle read/write timing diagram

In figure below, a simple diagram of the FSM that manages the write access cycles is shown. In the same way the FSM works to run both single read access and BLT access.

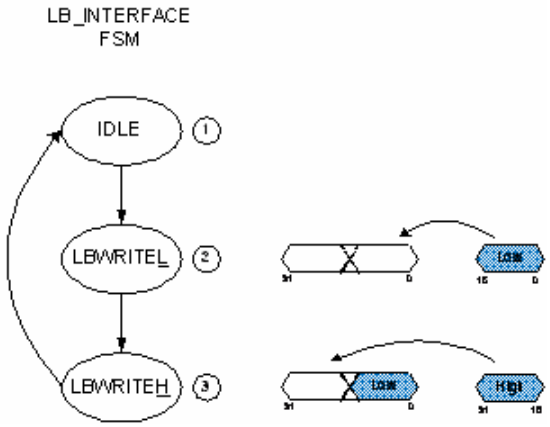

Fig. 3.3: A FSM for the write access

3.3 BLT Mode Access

A block transfer cycle consists of a single address cycle followed by the data cycles. When the BLT ends, an nBLAST pulse is drove by the VME. The figure below shows the BLT timing diagram. To start the block transfer the user must drive the nREADY signal (see figure below), that is, set it at '0' logic to start the BLT and keep it at '0' until all the data are transferred. This signal is driven, in turn, by the combination of signals coming from the FIFO and the *blt_ready* signal.

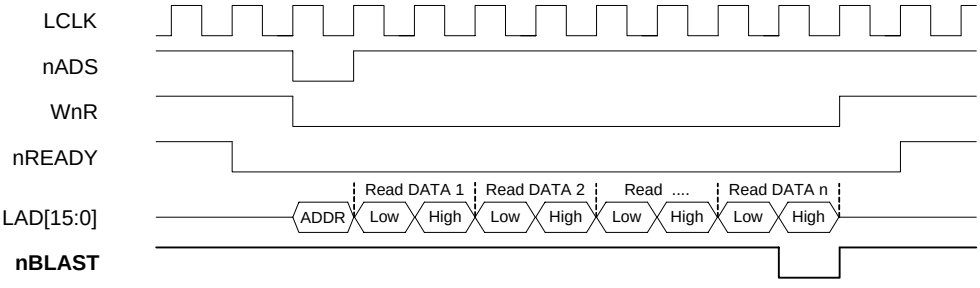

Fig. 3.4: BLT timing diagram

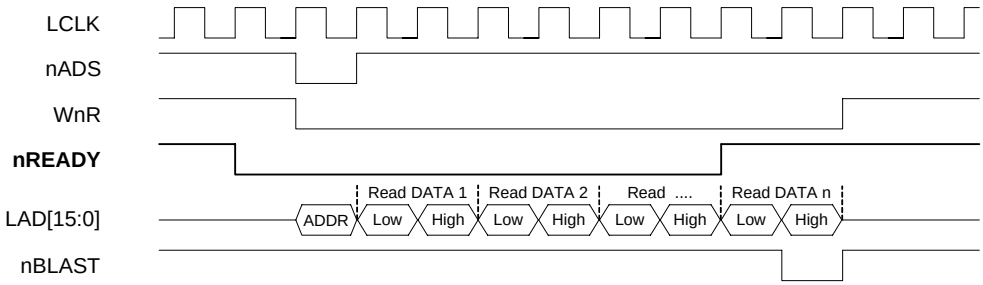

Fig. 3.5: BLT timing diagram. The user control the start/stop of the BLT

4 Programming V1495 User FPGA

This instructions refer to Windows OS and upgrade your cvUpgrade Software and V1495 board firmware.

The first step is to upgrade your *cvUpgrade* Software so you need to download and install on your computer the latest software *cvUpgrade* Release 2.1. http://www.caen.it/nuclear/lista-sw.php?mod=V1495
Find *cvUpgrade* under *Control Software* list. Download it, unzip and then launch cvUpgradeSetup-2.1.exe file (Do not need to uninstall your old version of *cvUngrade,* it will be upgraded automatically).
It is necesary V1495 VME FPGA firmware release 1.0 or greater.

Upgrade the V1495 USER FPGA (see manual for more detail) with the demo firmware.

To do this, perform these steps:

1. launch windows command line from the same folder where the *cvUpgrade.exe* is located (ex: “C:\.....\CAEN\CVUpgrade\bin”);
2. Copy to the folder, indicated above, the *V1495_Demo2.rbf (*row binary format) configuration file that you find in fit folder.
3. Execute from the windows command line the command: “cvUpgrade.exe V1495_Demo2.rbf USB -link 0 -VMEbaseaddress 32100000 -param Cvupgrade_params_V1495_USER.txt” to program the user FPGA of the V1495 board with base address 0x32100000 by using a V1718 CAEN VME Bridge. If you use a V2718 CAEN VME Bridge you should put PCI_OPTLINK option instead of USB option in the command line above.(Note: instead of base address value above 0x32100000 should be the base address set on your V1495 board ex. 0xXXXX0000)
4. When the firmware is updated successfully power cycle the Crate.

For more information and examples how to upgrade WME/USER FPGA read the *readme.txt* file in the CVUpgrade folder installed on your computer.

5 Setup and Functional Simulation

5.1 Demo Setup

To setup the Demo follow the steps below:

1. Program the V1495 USER FPGA (see Chapter 4);
2. Create a connection with the V1495 board to achieve a read/write access on VME.

   For example, for this test we have used a V1718 bridge and the CAEN VME .NET Demo (C:\.....\CAEN\VME\CAENVMEDemoDotNet CaenVMEDemoDotNet.exe) to read/write the registers.
3. Set *ndiv_length* register; Default value: *ndiv_length* <= X"00000402" (freq. divider = 2, Record Length = 64);
4. Set *mask_A/B* registers; Default value: *mask_A* <= X"FFFFFFFF", *mask_B* <= X"00000000";
5. Set *ctrl_reg* register; Default value: *ctrl_reg* <= X"00000001" (Port G = TTL level, Mux Sel = Chann.A);
6. Send a clear signal on G0 port.
7. Send a START signal on G1 port and the input pattern on port A.
8. Read FIFO

5.2 Functional Simulation

To run the functional simulation of this Demo you have to launch the *Testbench_Demo2.vhd* file. This file includes two other files, *lbemulator.vhd* and *fpemulator.vhd* that emulate the Local Bus Interface and the Front Panel of the V1495 Interface. The figure below shows the simulation result of the pattern recorder generator.
To review this simulation load the *wave_pdl.do* file you find in the ModelSim "sim" folder.

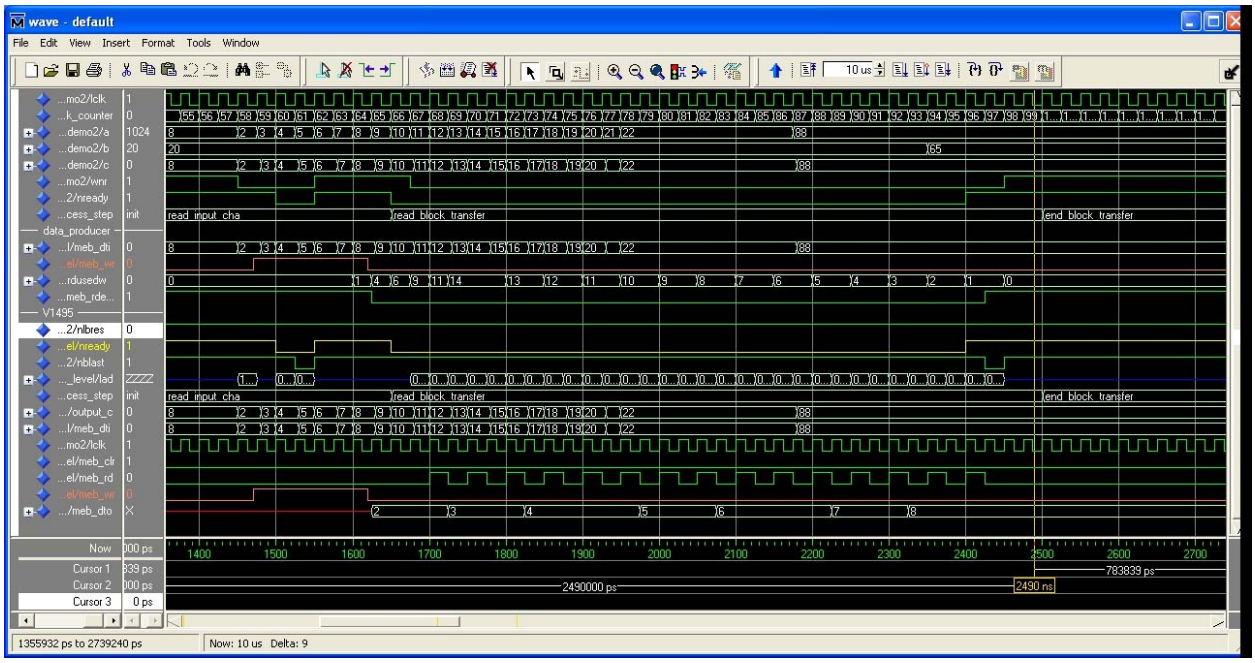

Fig. 5.1: Functional simulation result

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The place of Arbitration shall be Milan, Italy and the language shall be English.

9. Precedence.

This CAEN SwFw Licence constitute the entire understanding between the parties respecting use of the CAEN SwFw, superseding all prior agreements between you and C.A.E.N.. In the event of any conflict between the terms and conditions of this CAEN SwFw Licence, the terms and conditions of this CAEN SwFw Licence will control

10. Surviving Provisions.

Sections 2, and 4 through 10, will survive any termination of this Agreement.

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