

PRELIMINARY

Technical Information Manual

Revision n. 1

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DEMO1
GATE PATTERN

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1 Introduction

In this Demo we propose an example of the design of a gate pattern that shows how to use the I/O ports of the V1495 General Purpose VME board. For more detail, in this demo you will see:

- AND/OR function between I/Os;
- Single read/write access on VME using Local Bus Interface;

Notice that hereafter we do not use anymore the HAL (Hardware Abstraction Layer) that is a HDL module used in older demos to help the hardware interfacing. This is done in order to offer to the end user a further degree of freedom.

1.1 Assumption

We assume that you have a basic knowledge of FPGA and QuartusII software, as well as the VHDL language in which the design (firmware) is written.

1.2 Before you Begin

The design and simulation of this demo was done working on Windows O.S. Before proceeding, you must install on your computer Altera QuartusII 8.0 or later Web/Full edition (to generate the programming file for the V1495 board), ModelSim-Altera 6.1 or later (to simulate the Demo) and the CAEN V1495 Tool (windows) <http://www.caen.it/nuclear/lista-sw.php?mod=V1495> to test the V1495 board.

You can freely download the Web edition of Altera QuartusII and ModelSim-Altera at Altera website: <http://www.altera.com/index.jsp>

The Demo 1 *Gate Pattern* is available at CAEN website:

<http://www.caen.it/nuclear/lista-sw.php?mod=V1495>

1.3 Demo Folder Structure

Below is shown the structure and the content of the file Demo1.zip. A short description about the organization of this folder follows.

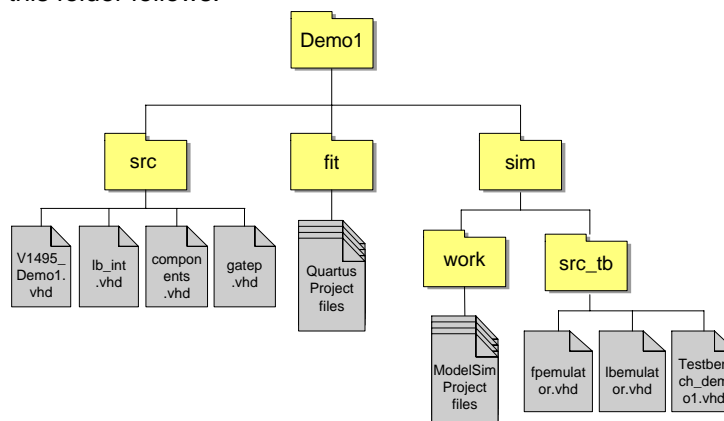


Fig. 1.1: Demo Folder Structure

In the “src” folder you find the source VHDL files of the reference design where the main file is V1495_Demo1.vhd. The “fit” folder contain the Demo’s Quartus project. This project provides a complete pinout of the FPGA and it is also enabled to generate RBF type file (v1495_Demo1.rbf) used to program the USER FPGA of the V1495 board. The “sim” folder contains the ModelSim project for the functional simulation of this Demo. In addition, under the “src_tb” folder you find the testbench files for the functional simulation that are included into the ModelSim project. The main testbench file is Testbench_Demo1.vhd.

This demo shows the implementation of a gate pattern. The principle of operation is the following: when the GATE signal is received, the 32 digital inputs coming from the port A or B are sampled and become available for the readout from the VME (through the local bus). The 32 bit output port C is used to reproduce the samples during the gate signal.

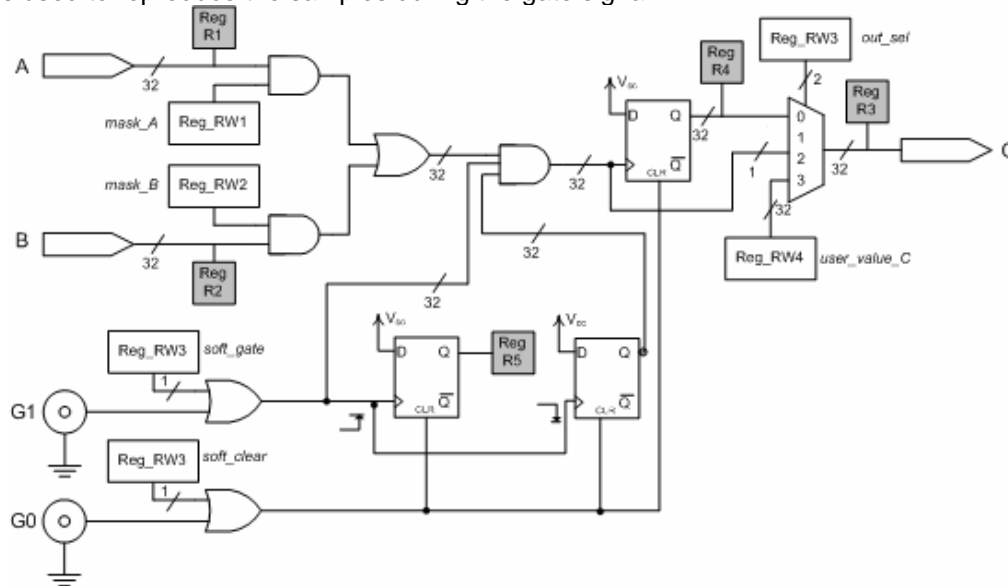


Fig. 2.1: Gate Pattern

The GATE signal can come from the port G1 or be generated internally by means of a write access to a specific register. The acquisition starts on the rising edge of the GATE signal; once started, the system is no longer sensitive to any further GATE until a reset is asserted; this can be done by the user either sending a pulse into the G0 input or making a write access to the relevant register. For test and debug purpose, it is possible to read on the fly the 32 bit digital patterns on the inputs A and B as well as on the output C. It is possible to force the output C with a user defined pattern.

In this example, there are 11 registers reported below. The first five register can be written and read from the VME (through the local bus) where the user can set different value and setting for the pattern recorder. The last four register can only be read from the user. All the registers are 32 bit wide and can be accessed in single mode. The table reports the content and the address map of the register where *Base* is the base address of the V1495 board.

ADDRESS	REGISTER/CONTENT	REGISTER	ADDR/DATA	Read/Write
Base + 0x1010	Mask_A	Reg_RW1	A32/D32	R/W
Base + 0x1014	Maks_B	Reg_RW2	A32/D32	R/W
Base + 0x1018	Ctrl_reg	Reg_RW3	A32/D32	R/W
Base + 0x101C	User_value_C	Reg_RW4	A32/D32	R/W
Base + 0x1020	Reserved	Reg_RW5	A32/D32	R/W
Base + 0x1030	Port A value	Reg_R1	A32/D32	R
Base + 0x1034	Port B value	Reg_R2	A32/D32	R
Base + 0x1038	Port C value	Reg_R3	A32/D32	R
Base + 0x103C	Pattern value	Reg_R4	A32/D32	R
Base + 0x1040	Circuit Status	Reg_R5	A32/D32	R
Base + 0x100C ¹	Demo Version	Reg_R6	A32/D32	R

Table 2.1: Register address map

Note: If the user do not drive the port A or B the default value of these ports is "FFFFFFFF"

¹ 0x100C is the firmware release register. The user must provide this register in read mode and make sure to use only the first eight bit (LSB [7 ... 0]). The other bits should be set at '0' logic level otherwise malfunction in the V1495 board may occur.

2.1.1 CTRL_REG Register (B.A + 0x1018, A32, D32, R/W)

The table below describes the allowed settings of the *ctrl_reg* register.

Bit	CTRL_REG Function
[0÷1]	Output MUX selection 0 = capture input event 2 = input event 3 = output value user
[4]	Input software gate (active high)
[5]	Input software clear (active high)
[8]	Port G level select: 0 = NIM level 1 = TTL level

Table 2.2: *ctrl_reg* register function settings

2.2 Implementation

Below Top-Down files hierarchy is shown for this demo where, as we have seen before, V1495_Demo1.vhd is the top level file of this Demo and the Testbench_Demo1.vhd is the top level file of the simulation process.

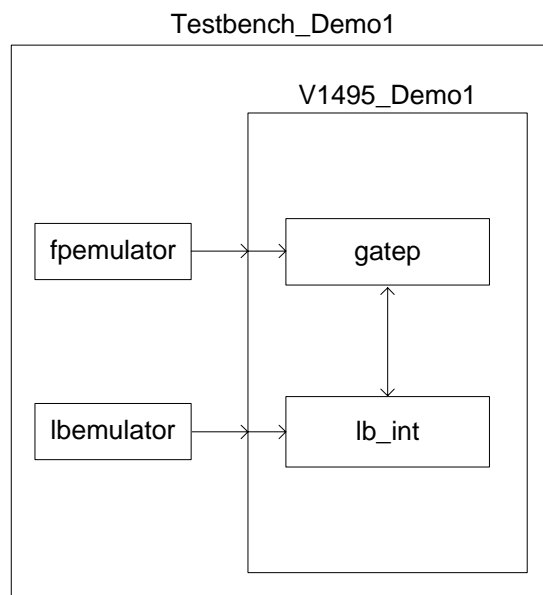


Fig. 2.2: Top Down files hierarchy

3 Programming V1495 User FPGA

This instructions refer to Windows OS and upgrade your cvUpgrade Software and V1495 board firmware.

The first step is to upgrade your *cvUpgrade* Software so you need to download and install on your computer the latest software *cvUpgrade* Release 2.1. <http://www.caen.it/nuclear/lista-sw.php?mod=V1495>
Find *cvUpgrade* under *Control Software* list. Download it, unzip and then launch *cvUpgradeSetup-2.1.exe* file (Do not need to uninstall your old version of *cvUpgrade*, it will be upgraded automatically).

It is necessary V1495 VME FPGA firmware release 1.0 or greater.

Upgrade the V1495 USER FPGA (see manual for more detail) with the demo firmware.

To do this, perform these steps:

1. launch windows command line from the same folder where the *cvUpgrade.exe* is located (ex: "C:\.....\CAEN\CVUpgrade\bin");
2. Copy to the folder, indicated above, the *V1495_Demo1.rbf* (row binary format) configuration file that you find in fit folder.
3. Execute from the windows command line the command: "cvUpgrade.exe V1495_Demo1.rbf USB -link 0 -VMEbaseaddress 32100000 -param Cvupgrade_params_V1495_USER.txt" to program the user FPGA of the V1495 board with base address 0x32100000 by using a V1718 CAEN VME Bridge. If you use a V2718 CAEN VME Bridge you should put PCI_OPTLINK option instead of USB option in the command line above.(Note: instead of base address value above 0x32100000 should be the base address set on your V1495 board ex. 0xFFFF0000)
4. When the firmware is updated successfully power cycle the Crate.

For more information and examples how to upgrade WME/USER FPGA read the *readme.txt* file in the CVUpgrade folder installed on your computer.

4 Setup and Functional Simulation

4.1 Demo Setup

To setup the Demo follow the steps below:

1. Program the V1495 USER FPGA ;
2. Create a connection with the V1495 board to achieve a read/write access on VME.

For example, for this test we have used a V1718 bridge and the CAEN VME .NET Demo (C:\.....\CAEN\VME\CAENVME DemoDotNet CaenVME DemoDotNet.exe) to read/write the registers.

3. Set *CTRL_REG* register; Default value: *ctrl_reg* <= X"00000103" (*out_sel* = 3, Port Level G = TTL);
4. To test the board connection read the port C with address X"*base*+1038". You receive the value X"deadbeef".

ADDRESS	REGISTER/CONTENT	DEFAULT VALUE
<i>Base</i> + 0x1010	Mask_A	X"FFFFFFFF"
<i>Base</i> + 0x1014	Maks_B	X"00000000"
<i>Base</i> + 0x1018	Ctrl_reg	X"00000103"
<i>Base</i> + 0x101C	User_value_C	X"DEADBEEF"
<i>Base</i> + 0x100C	Demo Version	X"00000011"

Table 4.1: Default setup values

4.2 Functional Simulation

In order to run the functional simulation of this Demo you have to launch the *Testbench_Demo1.vhd* file. This file includes two other files, *lbemulator.vhd* and *fpemulator.vhd* that emulate the Local Bus Interface and the Front Panel of the V1495 Interface.

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