Rev. 25 - March 19th, 2025

CoMPASS

Multiparametric DAQ Software for Physics Applications

CAEN
Tools for Discovery

User Manual
UM5960

Purpose of this Manual

The User Manual contains the full description of the CoMPASS readout software release **2.5.0**, which is compliant with the following board firmware versions:

Board Family	Firmware Type	Firmware revision
720	DPP-PSD	**4.29_131.16**
DT5790	DPP-PSD	**4.29_131.16**
725	DPP-PSD	**4.29_136.21**
725S	DPP-PSD	**4.29_136.138**
730	DPP-PSD	**4.29_136.21**
730S	DPP-PSD	**4.29_136.138**
751	DPP-PSD	**4.23_132.09**
751	DPP-PSD	**4.29_132.38**
724	DPP-PHA	**4.29_128.39**
724	DPP-PHA	**4.29_128.80**
780	DPP-PHA	**4.29_128.80**
781	DPP-PHA	**4.29_128.80**
V1782	DPP-PHA	**4.29_128.80**
725	DPP-PHA	**4.29_139.10**
725S	DPP-PHA	**4.29_139.137**
730	DPP-PHA	**4.29_139.10**
730S	DPP-PHA	**4.29_139.137**
740D	DPP-QDC	**4.29_135.17**
2740	DPP-PHA	**2025012205**
2745	DPP-PHA	**2025012205**
2740	DPP-PSD	**2025012305**
2745	DPP-PSD	**2025012305**
2730	DPP-PSD	**2024092000**

For future release compatibility check the release notes files.

Change Document Record

Date	Revision	Changes
September 28th, 2017	0	Initial Release
November 9th, 2017	1	Added support to CoMPASS for Linux OS. Added Tof plot which was missing in the previous version.
December 12th, 2017	2	Modified Statistics tab. Added ”Real time playback” in the Offline run.
February 6th, 2018	3	Added ”Channel time offset” option in the Sync/Trg tab.
February 23rd, 2018	3.1	Modified Sec. **The Time Selection Tab** and added Sec. **The Trigger/Veto/Coincidences Tab**.
May 18th, 2018	4	Modified Sec. **The Acquisition Tab**, Sec. **Menu Bar Items** and Sec. **Data Saving Options**.

September 27th, 2018	5	Modified Sec. **Data Saving Options** and Sec. **The Statistics Table**.
October 19th, 2018	6	Modified Sec. **The Synchronization Tab**, Sec. **The Trigger/Veto/Coincidences Tab** and Sec. **The Time Selection Tab**. Added Sec. **The Virtual Channel Tab**.
January 14th, 2019	7	Modified binary list file format. Updated software GUI to rev. 1.1.0.
March 13th, 2019	8	Updated binary list file format. Added Time stamp limits in Sec. **Save the list of Trigger Time Stamp, Energy, PSD and waveforms**.
July 30th, 2019	9	Included description of the new MCS graph and the ROIs management windows in the Sec. **The Plotter Window**. Updated Sec. **The Acquisition Tab** and Sec. **Save the list of Trigger Time Stamp, Energy, PSD and waveforms**. Added support to V1782 Octal MCA.
December 13th, 2019	10	Added support to x725S and x730S. Added support to DT5790. Included description of the new HV tab in the Sec. **GUI Description**. Updated Sec. **The Acquisition Tab**. Modified Sec. **Data Saving Options**.
April 1st, 2020	11	Added support to DT5780 family. Updated **Introduction**, **Charge Integration and γ-N discrimination: the DPP-PSD Firmware** and **Pulse Height Analysis and Digital MCA: the DPP-PHA Firmware**. Updated Sec. **GUI Description**, **Data Saving Options**, **The Plotter Window**.
August 7th, 2020	12	Added support to x740D family and DPP-QDC firmware. Updated **Introduction**. Updated Sec. **GUI Description**.
January 10th, 2021	13	No changes on this release.
February 17th, 2021	14	Added Section **Digitizer Synchronization Guide**. Modified Sec. **The Input Tab**.
December 23rd, 2021	15	Added Support to 2740 family. Updated Sec. **Introduction**, **Pulse Height Analysis and Digital MCA: the DPP-PHA Firmware**, **GUI Description Data Saving Options**, **Digitizer Synchronization Guide** and **Dead time evaluation in CoMPASS**.
January 14th, 2022	16	Added Support to V4718.
February 8th, 2022	17	Added Support to 2745 family. Updated Sec. **GUI Description**.
February 15th, 2022	18	SNAP installation package available again. Updated Sec. **Data Saving Options**.
July 1st, 2022	19	Added support to 2740 and 2745 DPP-PSD firmware. Updated Sec. **Introduction**, **The Settings Tab**, **The Waveform Plot Icon Bar**
September 23rd, 2022	20	Updated board firmware releases compliance table.
September 13th, 2023	21	Updated **Copyright** Section, Chapt. **Technical Support** and End Page. Updated Chapt. **Software Interface** and Sec. **The Acquisition Tab**.
November 30th, 2023	22	Updated Sec. **Save the list of Trigger Time Stamp, Energy, PSD and waveforms**. Updated Sec. **The Synchronization Tab**.
April 8th, 2024	23	Added support to 2730 DPP-PSD. Added support to A5818 PCI Express Gen 3 CONET2 Controller. Updated Sec. **The Rejection Tab**, **The Trigger/Veto/Coincidences Tab**, **The Time Histogram Icon Bar**, **The Tof Histogram Icon Bar**, **The MCS Plot Icon Bar**, **Tools**.

September 25th, 2024	24	Added Sec. **The Information Menu**. Updated Sec. **GUI Description**, **The Acquisition Tab**, **The Miscellaneous Tab**, **Veto**, **Icon Bar**, **Data Saving Options**.
March 19th, 2025	25	Extended Multilanguage Support. Updated Sec. **Software Interface**

Symbols, abbreviated terms and notation

ADC	Analog-to-Digital Converter
AMC	ADC & Memory Controller
DAQ	Data Acquisition
DAC	Digital-to-Analog Converter
DC	Direct Current
DPP	Digital Pulse Processing
DPP-QDC	DPP for Charge to Digital Converter
DPP-PHA	DPP for Pulse Height Analysis
DPP-PSD	DPP for Pulse Shape Discrimination
LVDS	Low-Voltage Differential Signal
ROC	ReadOut Controller
USB	Universal Serial Bus

All CAEN documents can be downloaded at:
`www.caen.it/support-services/documentation-area`

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Limitation of Responsibility

If the warnings contained in this manual are not followed, CAEN will not be responsible for damage caused by improper use of the device. The manufacturer declines all responsibility for damage resulting from failure to comply with the instructions for use of the product. The equipment must be used as described in the user manual, with particular regard to the intended use, using only accessories as specified by the manufacturer. No modification or repair can be performed.

Disclaimer

The information contained herein has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies. CAEN SpA reserves the right to modify its products specifications without giving any notice; for up to date information please visit www.caen.it.

Made in Italy

We remark that all our boards have been designed and assembled in Italy. In a challenging environment where a competitive edge is often obtained at the cost of lower wages and declining working conditions, we proudly acknowledge that all those who participated in the production and distribution process of our devices were reasonably paid and worked in a safe environment (while this is true for the boards marked ”MADE IN ITALY”, we cannot guarantee for third-party manufactures).

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1 Introduction

The function of the Front End electronics in nuclear physics applications is to acquire the electrical charge pulses generated by a detector, to extract the quantities of interest and to convert them into a digital format. These information are then acquired, saved and analyzed by a computer. In most applications, relevant quantities are the particle energy (proportional to the charge released by the particle in the detector) and the time of arrival; in some cases the acquisition is restricted to the pulse counting, actually a “selective” counting, meaning that one or more energy intervals or other criteria are used to select which particles must be counted. In some other cases, it is necessary to discriminate the type of the particle by means of the pulse shape; for example, the γ-n discrimination is based on a detector response variation when stimulated by a gamma or a neutron; this variation leads to a different rise and/or decay time of the pulse. The acquisition system is usually completed by digital logic units whose purpose is to perform (anti)coincidences, generate triggers, vetoes and other signals that take into account the correlation between different channels and may give further information such as the particle position or trajectory.

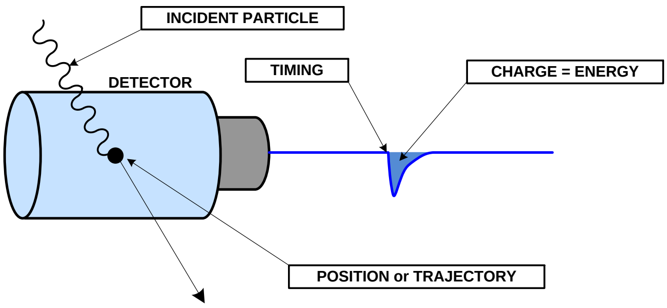


Fig. 1.1: Electrical charge pulse generated by a particle interacting with a detector.

Nowadays, the availability of very fast and high precision flash ADCs permits to design acquisition systems in which the Analog to Digital conversion occurs as close as possible to the detector. In principle, this acquisition system allows to minimize the information loss. Actually, the acquisition will be affected by uncertainties due to the quantization noise and to other sources of electronic noise. In general, the applications that require precise timing measurements are more oriented to the use of high sample frequency digitizers (500 MS/s or more), while the 12-14 bit digitizers are well suited for acquisitions where high energy resolution is a pre-requisite.

In recent years, the use of waveform digitizers for readout of radiation detectors has become popular in many different physics applications: the conventional analog electronics is going to be replaced by a full digital approach, where the detector output (with or without preamplifier, depending on the detector type) is directly connected to the digitizer input. This approach is especially beneficial in multi-parametric acquisition systems, where the analysis involves different quantities and parameters, such as energy, pulse shape and timing. In fact, thanks to Digital Pulse Processing (DPP) it is possible to apply dedicated algorithms online (typically in the FPGAs), to extract the information of interest from the raw waveform. DPP algorithms allow the digitizer to implement in “one single box” the different functionalities of the old fashion TDC, QDC, Peak Sensing ADC, discriminator and other analog and logic modules **[leo]**. Furthermore, the DPP allows the digital readout to be sustainable in terms of data throughput because the full waveform is not necessarily read out but used for debugging purposes only. This results in an “all-in-one, multi-parametric digital DAQ for physics applications”.

CAEN has developed a complete family of waveform digitizers well suited for physics, medical, homeland

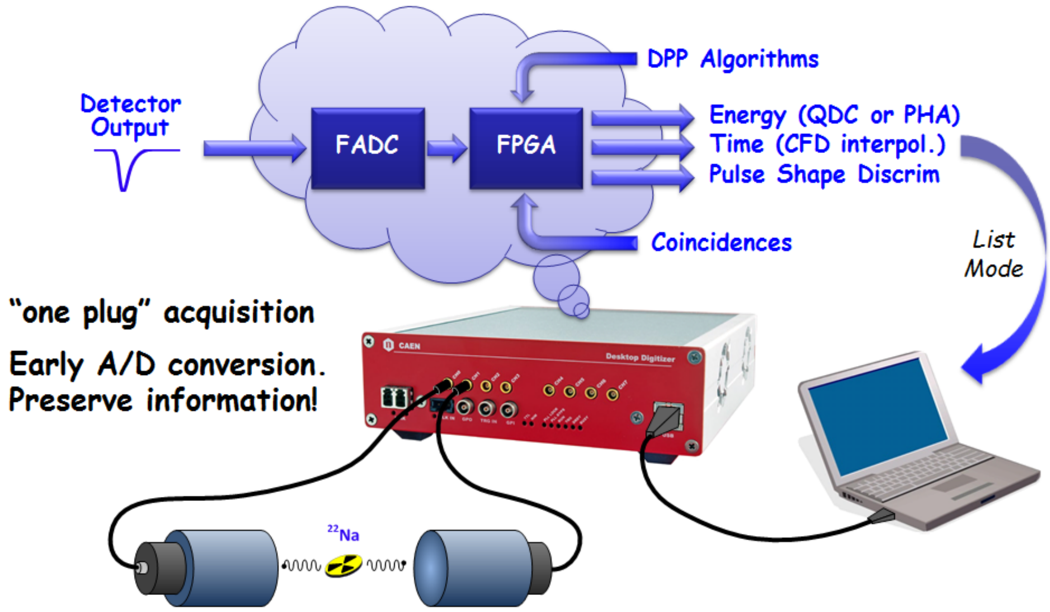


Fig. 1.2: All-in-one Spectroscopy DAQ.

security and industrial applications. They are available in different form factors (VME, Desktop and NIM) as showed in Tab. **1.1**. In addition, CAEN developed also several digital pulse processing algorithms that allows the user to extract a set of significant information like energy, precise timing, PSD and so on **[leo]**. Tab. **1.2** shows the functionalities supported by the different models and that will be described in the following sections.

MODEL(1)	Form Factor	# channels	Sampling Frequency (MS/s)	# Bits	Input Dynamic Range (Vpp)	Bandwidth (MHz)	DPP firmware
x724	VME	8	100	14	0.5 - 2.25 - 10	40	PHA
	Desktop/NIM	4					
x720	VME	8	250	12	2	125	PSD
	Desktop/NIM	4					
x730	VME	16	500	14	0.5 and 2	250	PHA, PSD
	Desktop/NIM	8					
x725	VME	16	250	14	0.5 and 2	125	PHA, PSD
	Desktop/NIM	8					
x751	VME	8	1000/2000	10	1	500	PSD
	Desktop/NIM	4					
x740D	VME	64	62.5	12	2	30	QDC
	Desktop/NIM	32					
x781	Desktop/NIM	4	100	14	0.3 - 1 - 3 - 10	5	PHA
V1782	VME	8	100	14	Gain: x1, x2, x4, x8 (Gain 1 = 1 Vpp); gain attenuation x0.2 by on-board jumper	5	PHA
x780	Desktop/NIM	2	100	14	Gain: x1, x3, x7, x16	40	PHA
DT5790	Desktop	2	250	12	2	125	PSD
x2740	VME/Desktop	64	125	16	2	50	PHA, PSD
x2745	VME/Desktop	64	125	16	4 - VGA with Gain up to x 100	50	PHA, PSD
X2730	VME/Desktop	32	500	14	4 - VGA with Gain up to x 20	250	PHA, PSD

Tab. 1.1: CAEN Waveform Digitizers selection table.

CoMPASS is the new software from CAEN able to implement a Multi-parametric DAQ for Physics Applications, where the detectors can be connected directly to the digitizers inputs and the software acquires energy, timing, and PSD spectra. CoMPASS software has been designed as a user-friendly interface to manage the acquisition with all the CAEN DPP algorithm. CoMPASS can manage multiple boards, even in synchronized mode, and the event correlation between different channels (in hardware and/or software), apply energy and PSD cuts, calculate and show the statistics (trigger rates, data throughput, etc...), save the output data files (raw data, lists, waveforms, spectra) and use the saved files to run off-line with different processing parameters.
CoMPASS Software supports CAEN **first generation digitizers** x720, x724, x725, x730, x740D, x751 digitizer families running the DPP-PSD, DPP-PHA and DPP-QDC firmware, the x780, x781 and x782 **MCA family**, the DT5790 **Pulse Processor** and the **second generation digitizer** x2740, x2745 and x2730 running the DPP-PSD and DPP-PHA firmware. More details about the supported boards and firmware are given in the following sections.

Model	Waveform Recording	PHA	PSD	CFD	QDC
x730	√	√	√	√	√
x725	√	√	√	√	√
x751	√		√	√	√
x724	√	√			
x720	√		√		√
x740D	√				√
x781	√	√			
V1782	√	√			
x780	√	√			
DT5790	√		√		√
x2740	√	√	√	√	√
x2745	√	√	√	√	√
x2730	√	√	√	√	√

Tab. 1.2: Functionalities implemented in the CAEN digital algorithms and supported by the digitizers.

Note: 725, 730 and 751 series requires the calibration of the ADCs before starting the acquisition. CoMPASS performs the calibration at every start acquisition. 725S and 730S series do not require the ADC calibration.

Note: From now on 725/730 series will include 725 and 725S/730 and 730S respectively unless otherwise specified.

2 Charge Integration and γ-N discrimination: the DPP-PSD Firmware

A digitizer running the DPP-PSD firmware becomes a multichannel data acquisition system for nuclear physics or other applications requiring radiation detectors. The digitizer accepts signals directly from the detector and implements a digital replacement of *Dual Gate QDC*, *Discriminator* and *Gate Generator*. All these functionalities are performed inside the board FPGA without any use of external cables, nor additional boards or delay lines. The acquisition is therefore performed by a single compact system which replaces the traditional analog boards. It is also possible to operate with multi-board systems: the front panel clock, the trigger and the general purpose LVDS I/Os connectors (VME only) make possible the synchronization of several boards.
Finally, both the board configuration and the acquisition can be completely managed by the CAEN CoMPASS Software, which allows the user to set the parameters for the acquisition, to configure the boards, and to perform the data readout. It allows also to collect and plot the time, energy and PSD spectra, to apply filters and to save the data.

The main functionalities of a digitizer running DPP-PSD firmware are listed below, where any parameter can be programmed by the provided software:

- Selection of the events with a digital leading edge discrimination or a digital constant fraction discrimination (725, 730, 751, 2740, 2745 and 2730 series);
- Input signal baseline (pedestal) calculation and pedestal subtraction for energy calculation;
- Single gate integration for the energy spectra calculation;
- Double integration of the prompt and delayed charge for Pulse Shape Discrimination.

Fig. **2.1** shows a typical example of signals from neutrons and gamma, where it is possible to see a difference in the waveform shapes. The slow and fast components are used by the algorithm to compute the PSD, according to the formula:

$$\mathrm{PSD} = \frac{(Q_{\mathrm{Long}} - Q_{\mathrm{Short}})}{Q_{\mathrm{Long}}} \tag{2.1}$$

which corresponds to the ratio between the integral of the tail ($Q_{\mathrm{long}} - Q_{\mathrm{short}}$) and the total charge ($Q_{\mathrm{long}}$).

See **[Stevanato]** for an example of DPP-PSD application for gamma-neutron discrimination in liquid scintillators, **[Energy_time_compass]** for a mixed Energy/Timing measurement application and **[gN_discr]** for an application of the performances of the event selection based on the described algorithm.

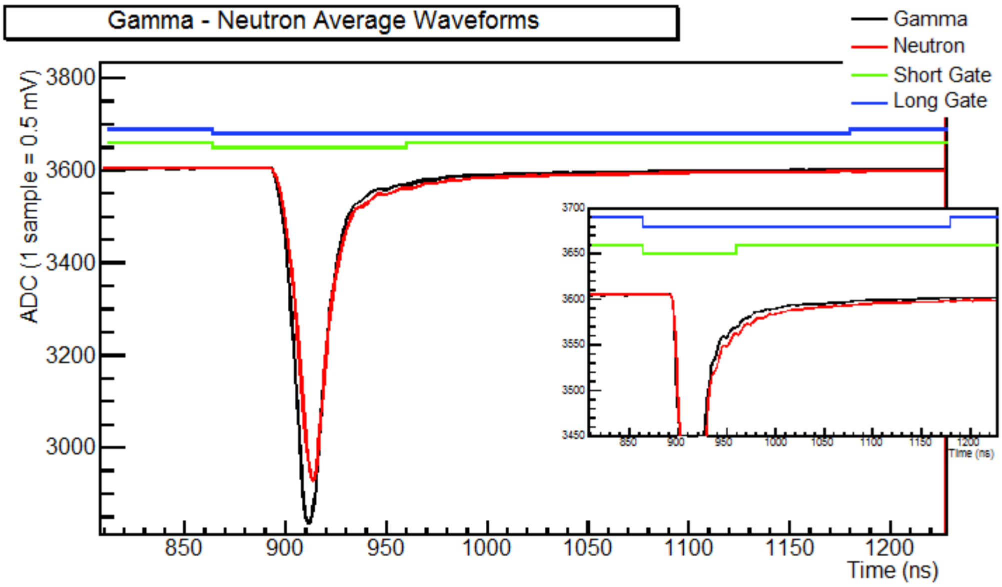


Fig. 2.1: Plot of typical γ-Neutron waveforms.

2.1 Principle of Operation

The figure below shows the functional block diagram of the DPP-PSD firmware:

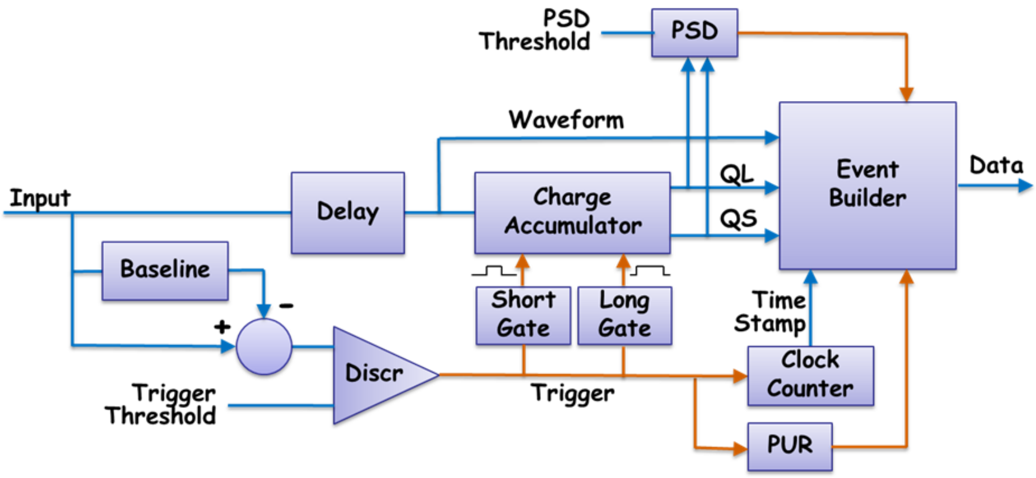


Fig. 2.2: Functional Block Diagram of the DPP-PSD.

The aim of the DPP-PSD firmware is to perform a charge integration of the input signal and to calculate the PSD factor performing a double gate integration of the input (Q_{short} and Q_{long}). Fig. **2.3** shows the short and long gates position for two signals of different shapes.

The following sub-sections summarizes the DPP-PSD features.

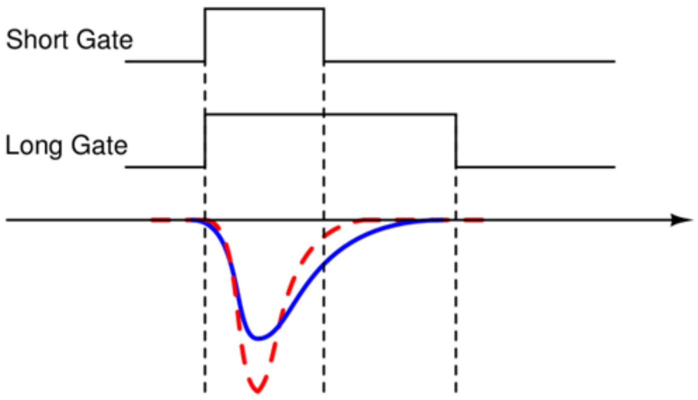


Fig. 2.3: Long and short gate graphic position with respect to a couple of input pulses. The blue pulse has a longer tail than the red one.

2.1.1 Baseline calculation

The digitizer continuously receives the input signal and digitizes it. The position of the signal baseline can be adjusted in the ADC scale to exploit the full dynamics of the digitizer using the **DC Offset** parameter.

The baseline value is an important parameter of the DPP-PSD firmware, since its value is used as a reference value for the charge integration of the input pulses. Moreover, most of the DPP parameters are related to the baseline value, like the trigger threshold.
The user can set either a fixed value for the baseline, or let the DPP firmware calculate it dynamically. In the first case the user must set the baseline value in LSB units through the command **Fixed BLR**. This value remains fixed for the entire acquisition run. In the latter case, the firmware dynamically evaluates the baseline as the mean value of N points inside a moving time window. The user can choose the N value among `8, 32, and 128` for 720 series and DT5790; `8, 16, 32, 64, 128, 256, and 512` for 751 series, and `16, 64, 256, 1024` for 725, 730, 2740, 2745 and 2730 series. The baseline is then frozen from few clocks before the gates start, up to the end of the maximum value between the long gate and the trigger hold-off[1]. For 751 series the freeze lasts some trigger clocks more than this maximum value. After that the baseline restarts again its calculation considering in the mean value also the points before the freeze. This allows to have almost no dead-time due to the baseline calculation.

Note: In case of 725 and 730 series, the user can set the time before the gate for the baseline freeze start, through register 0x1nD8 (default value = 16 ns). The same option can be set for the 2740 and 2745 digitizer using the ADCInputBaselineGuardT and ADCInputBaselineGuardS. This option can be useful when the gate does not cover the beginning of the signal, and the baseline becomes distorted. The baseline freeze lasts for the maximum value among the long gate, the trigger hold-off, and the over-threshold signals.

Note: In case of 725, 730, 2740, 2745 and 2730 series, the baseline remains frozen also on events clipping in the gate (saturation) and on opposite polarity. Refer to Sect. **Veto** for additional details.

Fig. **2.4** shows how the baseline calculation and freeze work. The trigger threshold dynamically follows the baseline variations. Note that in case of overshoots before the charge integration, the baseline can be distorted and the reference for the trigger threshold might not be accurate. In that case it might be more convenient to use the fixed baseline value.

In case of the x751 family an additional parameter comes in play, the **Baseline Threshold**. The **Baseline Threshold** defines the acceptance band for the baseline calculation and it is expressed in LSB. The figure below shows the trend of the baseline calculation and its safety band. When input signal outsides this

[1] The trigger hold-off defines the time window after the trigger where other triggers are inhibited

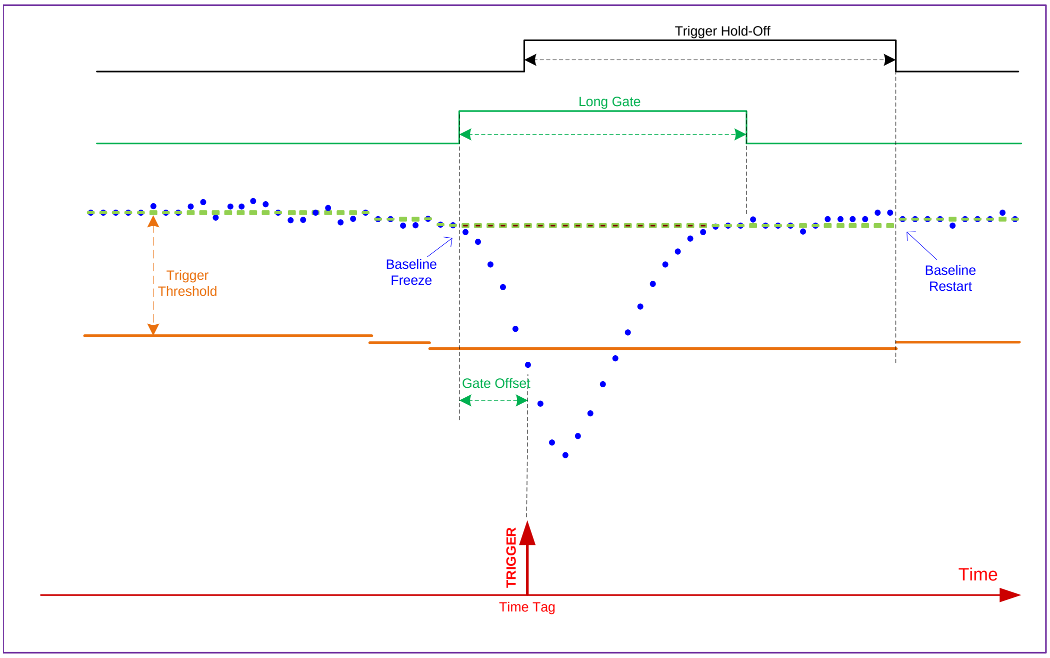


Fig. 2.4: Baseline calculation as managed by the DPP-PSD algorithm.

interval (band), these samples are not included in the baseline mean calculation. In other words, when abs(baseline – signal) < baseline_threshold the baseline mean is calculated.

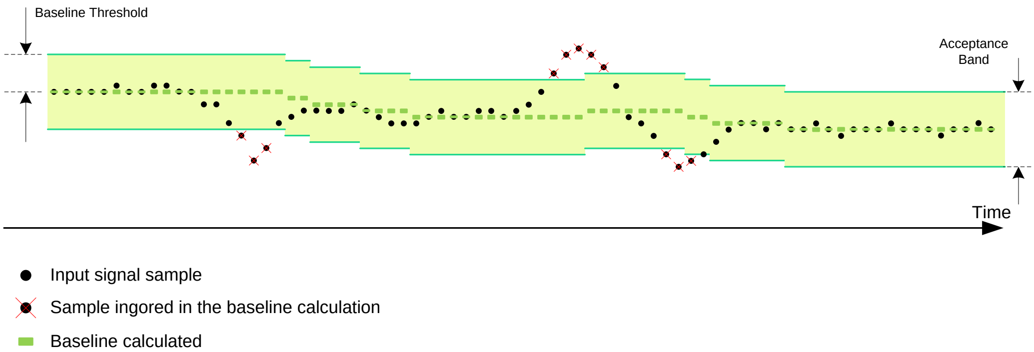


Fig. 2.5: Baseline calculation and acceptance band.

2.1.2 Trigger Management

The DPP-PSD allows the user to select the pulses according to two methods: leading edge, where a pulse is identified when its samples crosses a programmable threshold value, or through a digital constant fraction discrimination to have a better timing information.

In both cases once the event is selected, the signal is delayed by a programmable number of samples (corresponding to the “pre-trigger” value in ns) to be able to integrate the pulse before the trigger (“Pre-Gate”). The gates for charge integration are then generated and received by the charge accumulator before the signal. While the gates are active, the baseline remains frozen until the last averaged value and its value is used as charge integration reference. For the whole duration of a programmable “trigger hold-off” (or ”retrigger guard”) value, other trigger signals are inhibited. It is recommended to set a trigger hold-off value compatible with the signal width. The baseline remains frozen for the whole trigger hold-off duration. For 751 series the baseline remains frozen for a longer time. Fig. **2.6** summarizes all the DPP-PSD parameters.

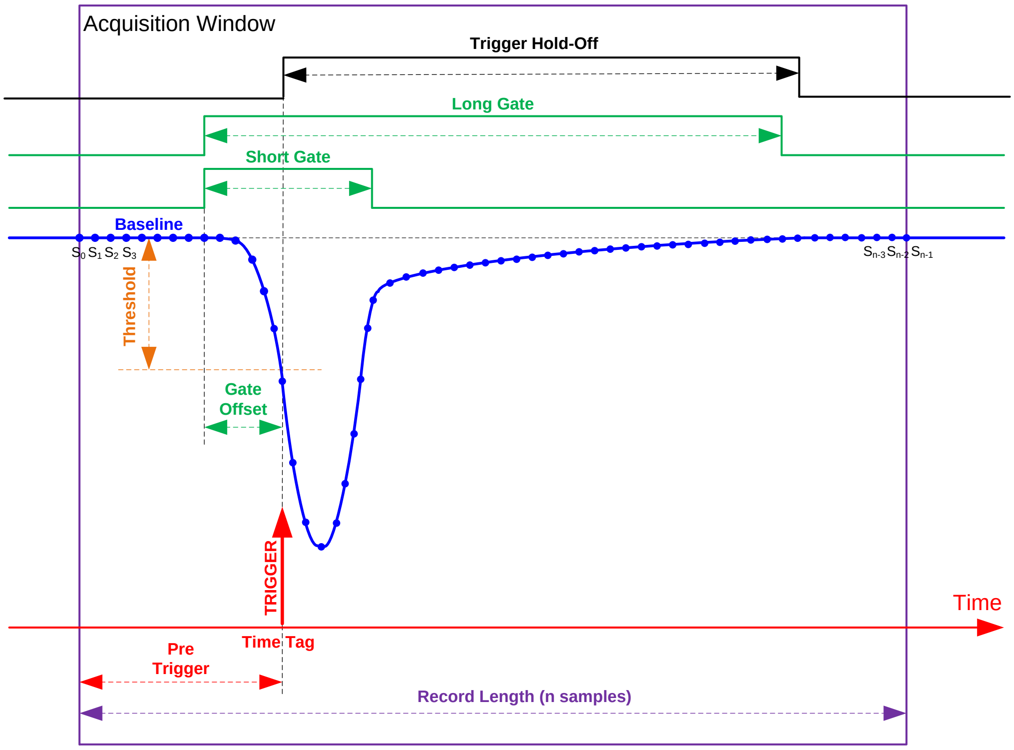


Fig. 2.6: Diagram summarizing the DPP-PSD parameters. The trigger fires as soon as the signal crosses the threshold value. Long Gate, Short Gate, Gate Offset, Pre-Trigger, Trigger Hold-Off/Retrigger guard, and Record Length are also shown for one acquisition window.

2.1.2.1 Digital Leading Edge

The baseline value, which can be a fixed value selected by the user, or continuously calculated by the firmware is then subtracted from the input signal, giving input_sub= input – baseline (Digital Baseline Restorer). The input_sub value is compared with the value of the trigger threshold and the event is selected as soon as the input_sub signal crosses the threshold (see Fig. **2.6**). The time stamp precision in the pulse identification is equal to the ADC sampling (8 ns for the 2740 and 2745 series, 4 ns for 720 and 725 series, 2 ns for 730 and 2730, and 1 ns for 751).

2.1.2.2 Digital Constant Fraction Discrimination (725, 730, 751, 2740, 2745 and 2730 series)

Note: The CFD for 751 series is supported from DPP-PSD firmware release **greater than 132.32**.

Using analog signals the Time Stamp determination is traditionally done with CFD (Constant Fraction Discriminator) modules. This technique sets the time stamp of a pulse to the time when the amplitude reaches a fixed fraction of the full amplitude. The DPP-PSD firmware for 725, 730, 751, 2740, 2745 and 2730 families intends to exploit the advantages of a CFD technique using a digital sampling device. The standard implementation of the leading edge trigger (refer to Sec. **Digital Leading Edge**), may suffer from amplitude walk issues. Conversely, triggering on a constant fraction of the input may reduce this issue since it is independent from the amplitude pulse. On the other side, a simple linear interpolation between two points can solve the problem of the sampling clock granularity, thus improving the timing resolution.

The digital CFD signal has been implemented in the classical way. The input waveform is attenuated by a factor f equal to the desired timing fraction of full amplitude, then the signal is inverted and delayed by a time d equal to the time it takes the pulse to rise from the constant fraction level to the pulse peak; the latest two signals are summed to produce a bipolar pulse, the CFD, and its zero crossing – corresponding to the fraction f of the input pulse – is taken as the trigger time (see Fig. **2.7**).

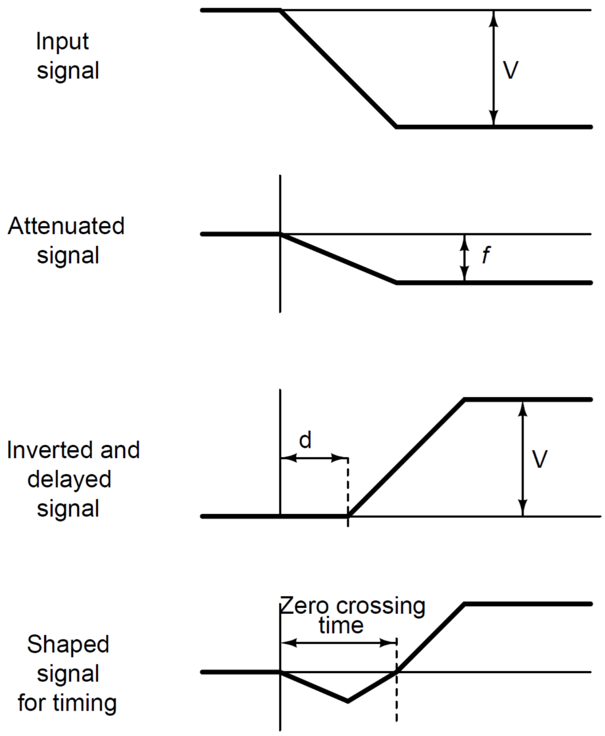


Fig. 2.7: Classical implementation of the Constant Fraction Discriminator. The input signal is first attenuated by a factor f, then inverted and delayed. The resulting signal has its zero crossing corresponding to the set fraction f.

The digital implementation of the CFD is shown in Fig. **2.8**. The input sample is split into two paths: the first performs the delay in steps of the sampling clock (8ns, in case of 2740 and 2745, 4 ns in case of 725, 2 ns in case of 730 series, 1 ns in case of 751 series), the second performs the attenuation. Possible choices of attenuation are: 25%, 50%, 75%, and 100% (i.e. no attenuation) with respect to the input amplitude. The CFD signal is referred to the mid-scale of the dynamics, i.e. channel 32768 in case of 2740 and 2745 series, channel 8192 in case of 725 and 730 series, channel 512 for 751 series.

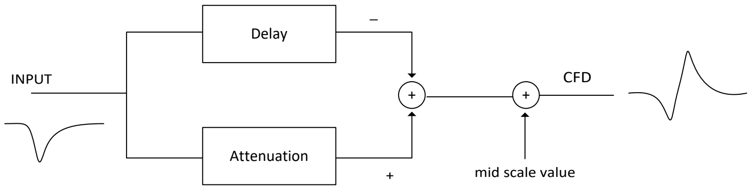


Fig. 2.8: Implementation of the digital CFD in the DPP-PSD firmware of 725, 730, 751, 2740, 2745, 2730 series. Mid-scale value corresponds to 32768 in case of 2740 and 2745 series, 8192 in case of 725, 730 and 2730 series, 512 for 751 series.

To enable the CFD discrimination, the user must set the related option in the Discrimination tab of the Settings (see Sec. **The Discriminator Tab**).

It is also possible to select which samples are used for the zero crossing linear interpolation. The n-th sample before and after the zero crossing must be chosen according to the CFD signal, in such a way they are in the linear slope of the CFD itself. By default, the first samples before and after the zero crossing are used by CoMPASS. To modify this value the user must use a FreeWrites command (refer to Sec. **The Acquisition Tab**) writing at 0x1n3C **[725_730PSD_Reg]**, **[751PSD_Reg]**.

Note: The interpolation points are used also in case of Leading Edge Discrimination.

A typical signal from CFD is shown in Fig. **2.9**, where the red points are the digital samples. The Sample Before the Zero Crossing (SBZC) and the Sample After the Zero Crossing (SAZC) are the samples before and after the zero crossing (in case of interpolation they are the n-th samples before and after the ZC).

The SBZC corresponds to the Coarse Time Stamp (T_{coarse}), that is the trigger time stamp as evaluated by the standard PSD algorithm (leading edge). The value of the Fine Time Stamp T_{fine} (see Fig. **2.9**) is calculated as the linear interpolation of the SBZC and the SAZC according to the formula:

$$T_{fine} = \frac{\text{midScale} - \text{SBZC}}{\text{SAZC} - \text{SBZC}} \cdot T_{sampl} \tag{2.2}$$

where midScale corresponds to 3768 in case of 2740 and 2745 series, 8192 in case of 725 and 730 series, and 512 for 751 series, and T_{sampl} is the sampling period of the specific series (4 ns in case of 725, 2 ns for 730, 1 ns in case of 751).

The “Interpolated Zero Crossing” (ZC) then corresponds to the sum of the Coarse Time Stamp and the Fine Time Stamp.

$$ZC = T_{coarse} + T_{fine} \tag{2.3}$$

The fine time stamp is reported as a 10 bit number by the FPGA, thus corresponding to a precision of $T_{samp}/1024$, which is about 1 ps for 751 series, 2 ps for 730 and 2730, and 4 ps for 725.

2.1.2.3 Multi Trigger Options

The DPP-PSD firmware allows for several way of trigger generation:

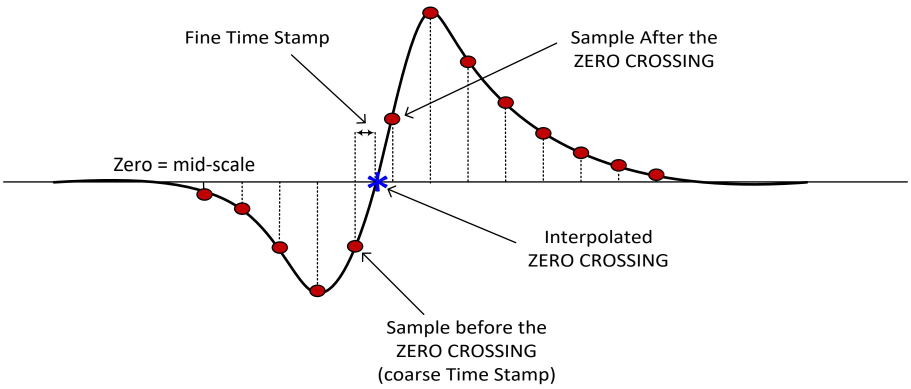


Fig. 2.9: A typical CFD signal. Red points are the digital samples. The Sample Before the Zero Crossing (SBZC) and the Sample After the Zero Crossing (SAZC) are the samples before and after the zero crossing. The SBZC corresponds to the Coarse Time Stamp. The algorithm can also evaluate the Fine Time Stamp, and the corresponding time will be the sum of the SBZC and the Fine Time Stamp.

1. each channel can "self-trigger" on its own input signal when the input crosses a programmable threshold, or through the CFD (725, 730, 751, 2740, 2745 and 2730 only). The self-trigger works on each channel independently from the other channels;
2. each channel triggers independently, then only those events satisfying programmable conditions are saved.
   For what concern V17XX, DT57xx and N67xx digitizer, referring to Fig. **2.10**: the IND_TRG_LOGIC (Individual Trigger Logic) can combine (AND/OR/MAJ) the trigger request (TRG_REQ) from each self-trigger. When the logic condition is met, a trigger validation (TRG_VAL) is sent back to each channel individually to enable the acquisition of that event. Events not receiving a TRG_VAL signal are discarded. This technique allows to make coincidence and anti-coincidence requests among different channels (refer to **[Coincidence]** for further details);
   For what concern 27xx digitizer a similar mechanism is present and it is based on the so called "Internal Trigger Logic" (ITL). For more details please refer to **[2740PSD_Param]**.
3. the board can accept an external trigger on the TRG IN/LVDS connectors. The external trigger can be used in OR logic operation with the channel self-trigger, or it can be used as a VETO to inhibit the individual self-trigger. If the self-trigger is disabled, the acquisition is managed by the external trigger only;
4. individual trigger and logic combination of self-trigger of different channels (AND/OR/MAJ) can be propagated through the TRG-OUT/LVDS connectors.

In case of 725 and 730 series, each channel can manage the self-trigger independently but it shares the same memory buffer with the other channel of the couple (0-1, 2-3, etc.) (see Fig. **2.11**). The user must take care in case he/she wants to acquire large waveform length. Indeed, the DPP-PSD algorithm is meant to acquire small size events, typically time stamps and charges, and possibly small portions of the waveform for post-processing. In case of **record length less than 1792 samples**, each channel has enough memory in its local buffer to acquire events independently from the other channel. For record length greater than 1792 samples, the couple must use an external SRAM memory, and a memory arbiter decides in "fair mode" which event of the two channels is saved.

Note: In case of List mode, the Record Length is ignored.

Moreover, the channels of the couple share the same TRG_REQ for the coincidence logic. This means that it is not possible to set different coincidence logic among channels of two different couples (refer to **[Coincidence]** for further details). Anyway a great advantage comes in case of coincidences between

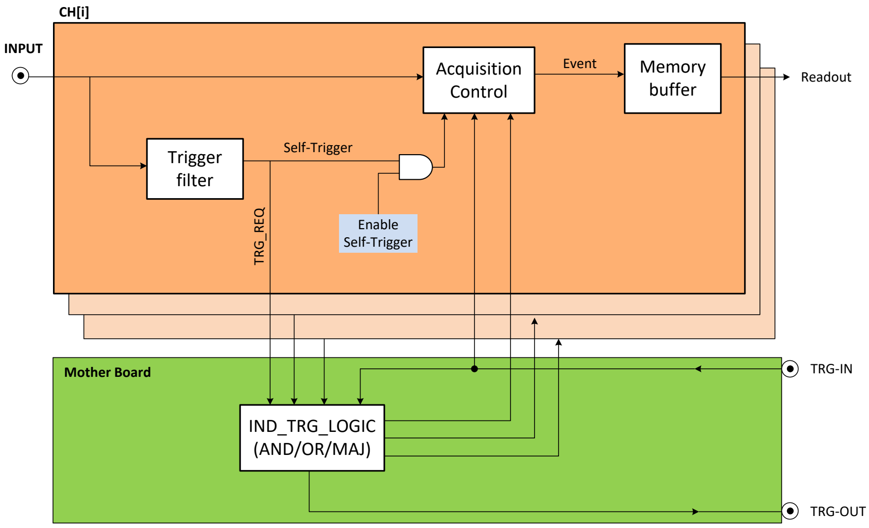


Fig. 2.10: Diagram showing the structure of the trigger management of the DPP-PSD firmware.

channels of the same couple, which can be managed inside the channel FPGA, with no propagation to the mother board.

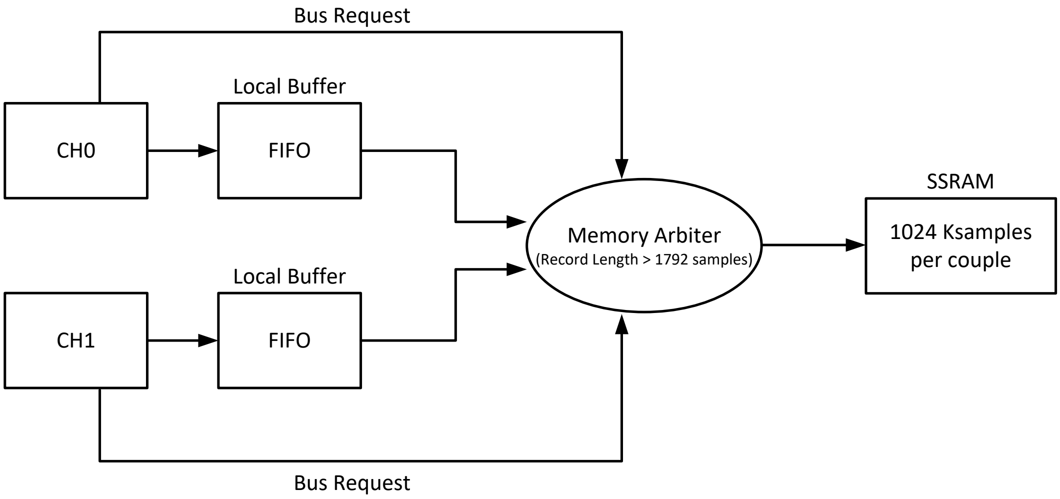


Fig. 2.11: Memory management of 725 and 730 series.

The TRG_REQ from couple and the TRG_VAL to the couple are managed by bits[6:0] of register 0x1n84, according to the bit scheme reported in Fig. **2.12**.

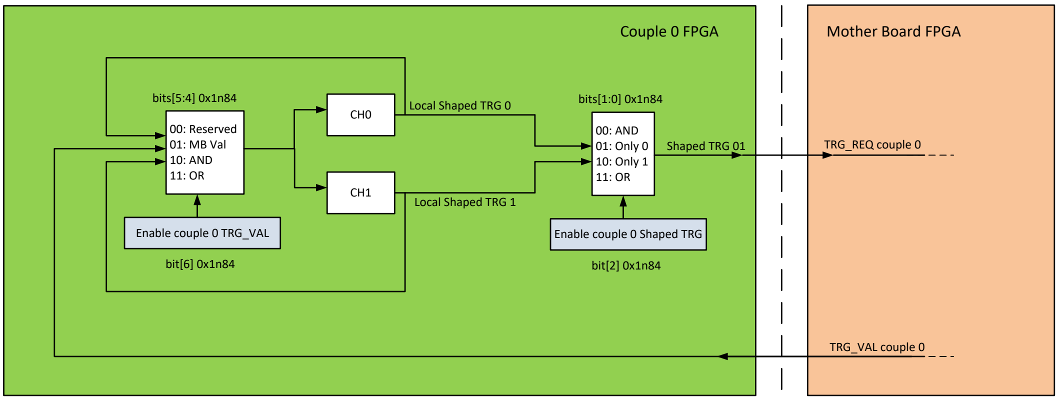


Fig. 2.12: Local Trigger Management inside couple 0 of 725-730 digitizer series. Couple 0 is made of channel 0 and channel 1. The same applies for the other couples of the 725 and 730.

2.1.2.4 Trigger Hysteresis (725, 730, 2740, 2745 and 2730 series)

When the input signal is no more over-threshold, the trigger could fire again in the tail of the pulse, especially in case the tail contains spikes or noise. The “Trigger Hysteresis” feature inhibits any trigger until the input pulse reaches half of the threshold value itself. See Fig. **2.13** for a diagram of this feature. This option is enabled by default. To modify this value use a FreeWrites command (refer to Sec. **The Acquisition Tab**) writing at 0x1n80 **[725_730PSD_Reg]** for the 725 and 730 series or modify the parameter **TriggerHysteresis** for the 2740, 2745 and 2730 families.

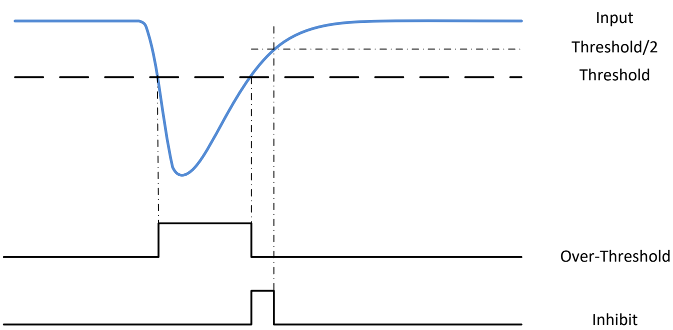


Fig. 2.13: Trigger Hysteresis in DPP-PSD firmware. Any other triggers are inhibited after the over-threshold until the input reaches the value of half the threshold.

2.1.2.5 Input Smoothing (725, 730, 2740, 2745 and 2730 series)

The smoothing is a moving average filter, where the input samples are replaced by the mean value of the previous n samples, where n is: `2, 4, 8 and 16` samples

When enabled, the trigger is applied on the smoothed samples, thus reducing triggering on noise. Both CFD and LED triggering modes can be used on the smoothed input. The charge integration is either performed on the input samples or on the smoothed samples, according to bit [11] of register 0x1n84 **[725_730PSD_Reg]** for the x725 and x730 families and according to the ChargeSmoothing and TimeFilterSmoothing parameters for the 27xx families **[2740PSD_Param]**.

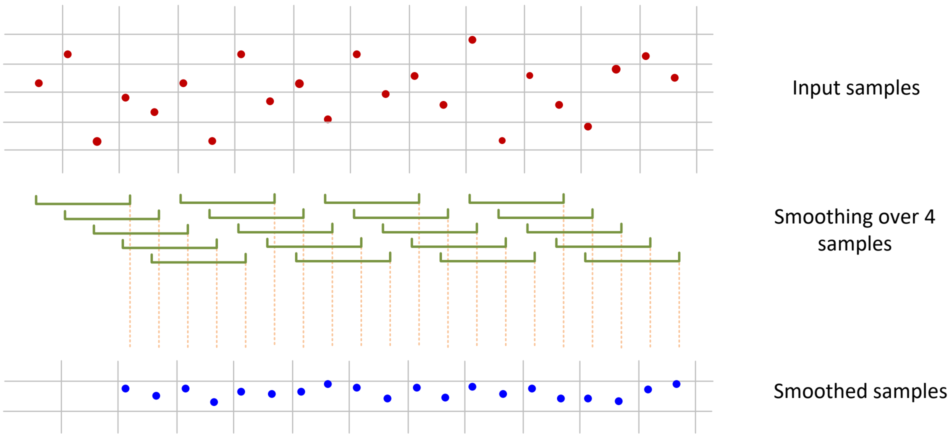


Fig. 2.14: Example of smoothing over four samples. The input samples are averaged over four samples and replaced in the smoothed samples by the mean value.

2.1.2.6 Veto

Note: Veto options can be enabled via register writes using the FreeWrites options (refer to Sec. **The Acquisition Tab**).

In case of 720 and 751 series CoMPASS allows the user to directly manage the veto coming from an external signal through the digitizer TRG-IN connector (see Sec. **The Trigger/Veto/Coincidences Tab**). The other veto options are managed by the Global Trigger Mask register (0x810C) and Trigger Validation Mask (0x8180 + 4n).

In case of 725 and 730 series CoMPASS allows the user to directly manage the veto coming from an external signal through the digitizer TRG-IN connector as well (see Sec. **The Trigger/Veto/Coincidences Tab**).

Besides this, the user can set a different coincidence logic between channels inside the couple and extra couples. For example, it is possible to set the AND between the channels inside the couple, and set a veto from external trigger for all couples (see **[Coincidence]** for additional examples). The 720 and 751 series can handle just one type of coincidence logic and do not have this additional veto management of 725 and 730 series.

In particular, while the coincidence inside the couple is managed by bits[6:0] of register 0x1n84 (see Fig. **2.12**), bits[19:18] of the same register **[725_730PSD_Reg]** manage the veto source, which can be common among all channels (set it through register 0x810C which can be generated by an external trigger or by a combination of the trigger requests from couples), or individually set for the couples of channels (each couple can have a different veto, which can be set through register 0x8180 (+4n), where n is the couple index, and it can be generated by an external trigger or by a combination of the trigger requests from couples). Finally a veto can come from events saturating inside the gate (clipping) or from events with opposite polarity, as for example, in case of undershoot/overshoot, the signal can trigger on noise while it returns to zero. The firmware automatically detects pulses with opposite polarity and in case of LED discrimination freezes the baseline. This avoid distortions in the baseline and triggering of wrong pulses (see bottom left of Fig. **2.15**). In case of CFD discrimination, since the CFD is a bipolar signal, there is a zero crossing even for opposite polarity (see bottom right of Fig. **2.15**). Triggers on opposite polarity are inhibited by default; set bit[31] = 1 of register 0x1n80 to disable this option

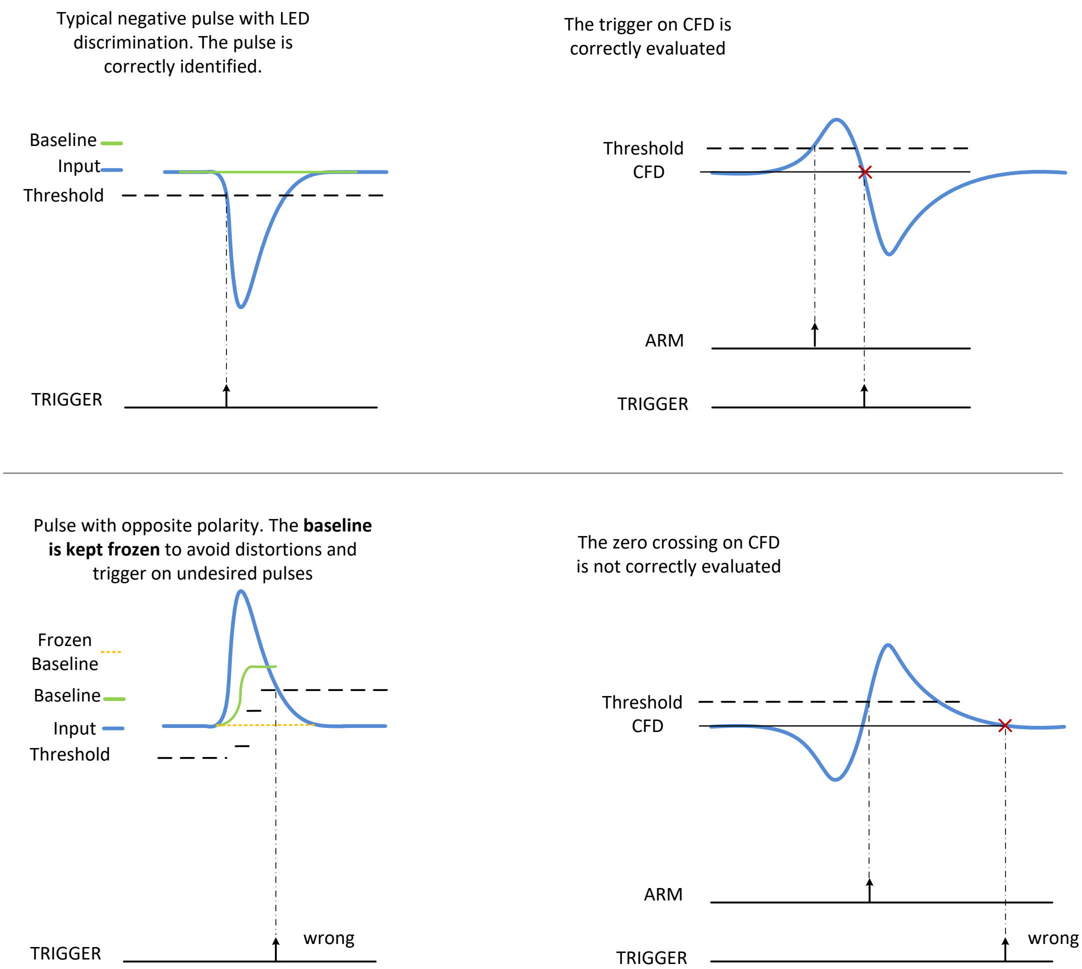


Fig. 2.15: Example of input of opposite polarity. Top left and top right pictures shows the case of a negative pulse polarity, where the trigger is correctly evaluated both for LED and CFD discrimination. Bottom left picture shows an opposite pulse polarity (positive) and the corresponding CFD (right). To avoid distortions on the baseline (green line) the baseline is kept frozen (yellow) and the event is not triggered.

The user can set the width of the veto duration through register 0x1nD4. In particular bits[15:0] define the width, and bits[17:16] define the step, that can be chosen among 8 ns, 2 us, 524 us, and 134 ms.

Note: A veto width equal to 0 means that the veto lasts for the duration of the signal that generated it. A veto width different from 0 extends the veto duration by the amount of time written in the register.

In case of the 2740, 2745 and 2730 series CoMPASS allows the user to directly manage the veto coming from an external signal through the digitizer S-IN and GPIO front panel connector as well (see Sec. **The Trigger/Veto/Coincidences Tab**).

2.1.3 Online PSD Selection

The PSD value as defined in Sec. **Principle of Operation** can be used to online select the events. Indeed, it is possible to select events under or below a programmable PSD threshold. Referring to the example of neutron/gamma discrimination shown in Fig. **2.16**, the cut on PSD allows the user to reject most of the gamma events, thus recording only neutrons and the small amount of gamma overlapping with the neutrons.

The user has 2 possible ways to perform the online PSD selection:

1. Setting a PSD Cut on CoMPASS through **The Rejection Tab** or directly in the PSD plot (see Sec. **The Plotter Window**). In this case the cut will be applied at a software level and will not affect the data throughput from the digitizer.
2. Setting a PSD Cut on onboard:
   - x720, x725, x730, x751 series: Set the FPGA registers 0x1n78 and 0x1n80 (**[720PSD_Reg]**, **[725_730PSD_Reg]**, **[751PSD_Reg]**) using the FreeWrites commands (refer to Sec. **The Acquisition Tab**).
   - 27xx series: Set the parameters **NeutronThreshold** and **EventNeutronReject[2740PSD_Param]**

   In this case the data throughput after the cut can be significantly reduced.

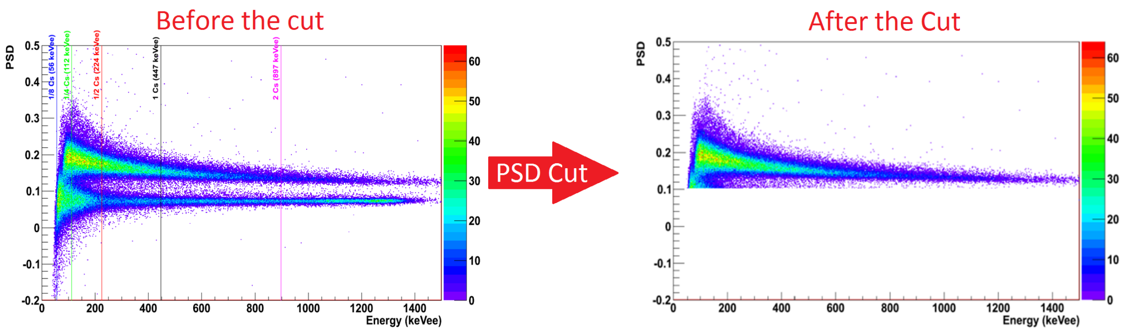


Fig. 2.16: 2D scatter plot of PSD parameter vs Energy in a neutron-gamma application. On the left the 2D plot before the cut, on the right the plot after the cut on PSD.

2.1.4 Zero Suppression Based on Charge (725, 730, 2740, 2745, 2730 series)

Input signals of small amplitude can be selected by setting a small threshold level. Unfortunately, this might result in an increase of the noise level. The noise can be distinguished by real signals in the energy spectrum, since it usually appears as a peak close to the 0 energy.

1. In case of the x725 and x730 series: register Charge Zero Suppression Threshold 0x1n44 allows the user to set a threshold in the spectrum (Q_{thr}) to cut events with charge $Q_{long} < Q_{thr}$. This option can be enabled by setting bit[25] of register 0x1n80. Q_{thr} is expressed as a 16 bit number, where 1 LSB corresponds to a specific value of charge which depends on the *Energy Coarse Gain* factor (refer to **The Energy Calibration Tab**).
2. In case of the 27xx series: parameters EnergySkimLowDiscriminator, EnergySkimHighDiscriminator and EventSelector allows to select and reject event falling outside the Low and High discriminator levels**[2740PSD_Param]**.

2.1.5 Pile-Up Management

The DPP-PSD firmware is mainly designed to work with fast signals like those coming from scintillation detectors coupled with Photomultiplier Tubes. The relevant output signals do not show long decay tails as in the case of charge sensitive preamplifiers, and the probability of pile-up between two pulses is quite low. In particular, the case of a second pulse sitting on the exponential tail of the previous one is rather rare. However, with the PSD algorithm, it is important to separate fast and slow components of the light emitted by the scintillation detector. Typically, the fast component is a quick pulse (few tens of ns) while the slow component is a quite long tail (typically a few µs) having amplitude much smaller than the fast component (see **[syncNote]**). To get the best results in the pulse shape discrimination, it is necessary to set the “Long Gate” as long as the full duration of the slow component. Under this conditions, most likely the events in pile-up occur during the long gate and cause an error in the calculation of the charge of the slow component. For this reason, it is important to detect these cases, especially high rate PSD acquisitions.

2.1.5.1 Pile-up management (751 family)

In the DPP-PSD firmware (751 family only) two events are considered in pile-up only when they both cross the threshold within the same integration gate. When the first signal triggers, the short and long gates are opened for integration. If another event crosses the threshold within the long gate, they are flagged as pile-up. If the second event does not cross the threshold, then the pile-up condition is not detected. Referring to Fig. **2.17**, from top to bottom there are three possible cases:

1. two distinct events do not overlap into the same integration gate. This is the case when no pile-up occurred;
2. two events trigger into the same gate. The pile-up flag is high and three possible scenarios are available:
   - no action is taken and the two pulses are integrated into the same integration gate;
   - the event is discarded and no charge is evaluated and saved;
   - a second gate is opened for the second pulse.

   See next section for further details;
3. two pulses overlap into the same gate, and the second pulse does not overcome the threshold. The event is not recognized as pile-up.

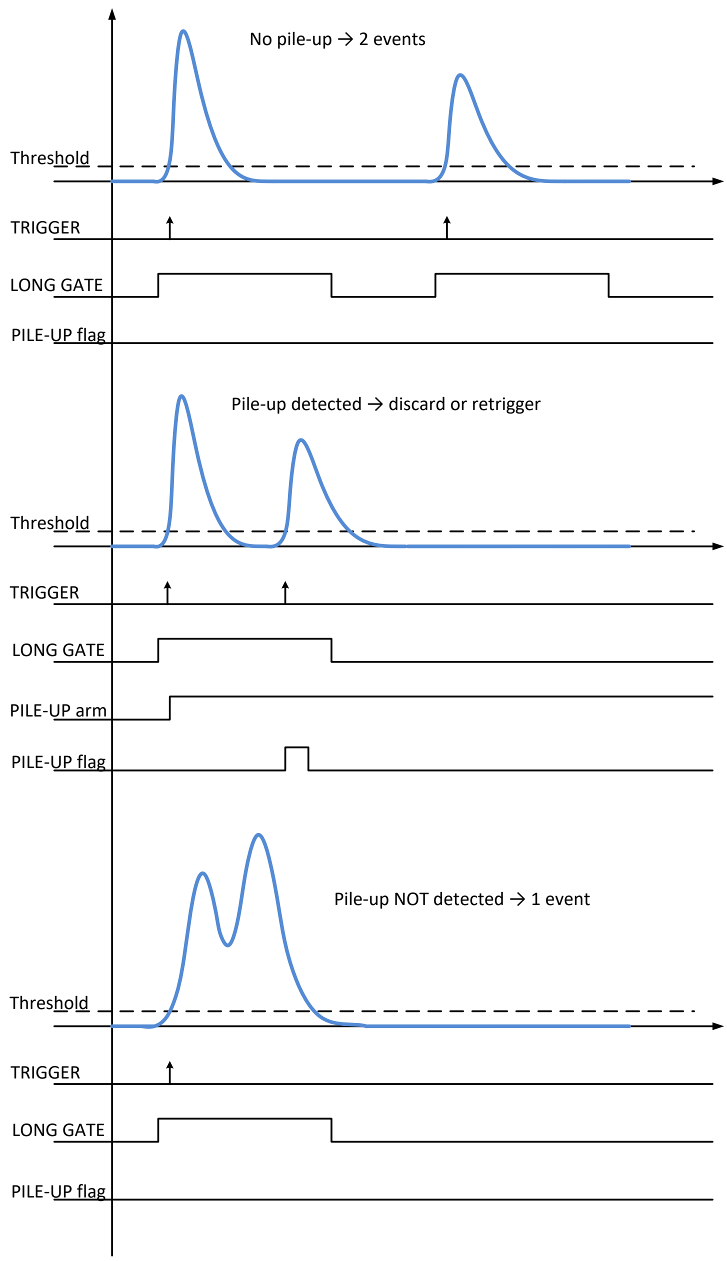
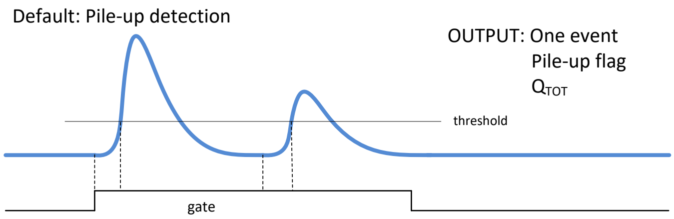


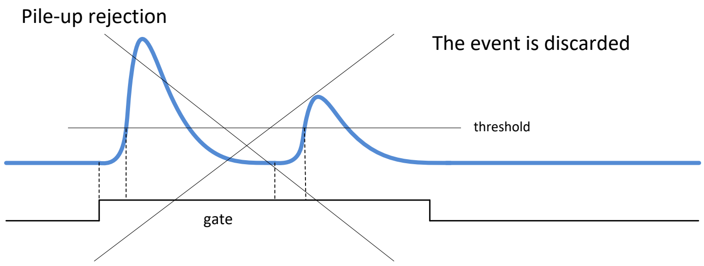
Fig. 2.17: From top to bottom: (1) two distinct events do not overlap into the same integration gate. This is the case when no pile-up occurred. (2) Two events trigger into the same gate. The pile-up flag is high and three possible scenarios are available: (a) no action is taken and the two pulses are integrated into the integration gate; (b) the event is discarded and no event is saved; (c) a second gate is opened for the second pulse (see next section for further details). (3) Two pulses overlap into the same gate, but the second pulse does not overcome the threshold. The event is not recognized as pile-up.

In the DPP-PSD firmware there are three options for the pile-up management:

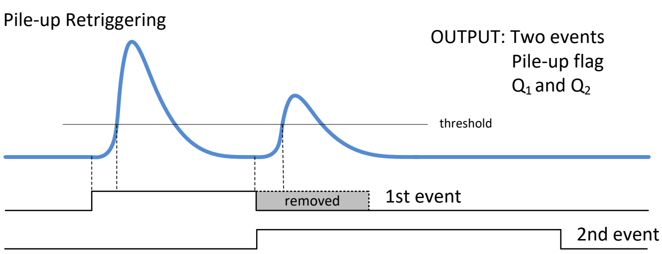
1. **Default**: in the default configuration the algorithm detects pile-up events, evaluates the total charge of the two pulses – which is therefore considered as a single "event", and flags that event as "pile-up".



2. **Pile-up rejection**: this configuration is enabled by setting bit [26] = 1 of register 0x1n80 (where n is the channel number) through a FreeWrites command (refer to Sec. bf The Acquisition Tab). In this way the events are rejected at board level, thus reducing the throughput rate. If the user wants to acquire them and discard at software level it is possible to enable the option **PUR enable** of **The Rejection Tab**.



3. **Pile-up Retriggering**: this configuration is enabled by setting bit [25] = 1 of register 0x1n80 (where n is the channel number) through a FreeWrites command (refer to Sec. **The Acquisition Tab**). In this case, when another pulse arrives within the long gate (and after the end of the short gate), the charge integration is stopped prematurely. A new event is created, by opening short and long gate again. The charge in the first event is the result of the integration of the signal up to the start of the new gate; because of the truncation of the gate (see figure below), it is not guaranteed that the full charge (i.e. energy) of the first pulse is completely integrated in the first gate. The second gate will integrate the charge of the second pulse, including the pre-gate region; it is worth noticing that the second gate can integrate also part of the charge belonging to the first gate. The user can apply some corrections to the charge of the two events based on the two time stamps, that give information about the separation between pulses. Both events are tagged as "pile-up".



2.1.5.2 Pile-up management (720, 725, 730, 2740, 2745, 2730 series)

In the DPP-PSD firmware of 720, 725 730, 2740 and 2745 families, two events are considered in pile-up when there is a situation of peak-valley-peak inside the same gate, where the gap between the valley and the peak is a programmable value. Referring to Fig. **2.18**, when the peak value is reached the algorithm evaluates the point corresponding to the PUR-GAP value and gets ready to detect a pile-up event (PILE-UP ARMED). If there is a condition of "valley", and the input signal overcomes the PUR-GAP threshold, then the event is tagged as pile-up. In the default configuration the firmware does not take any action and the total charge of the event is evaluated within the gate and saved into memory.

Note: CoMPASS allows the user to enable the pile-up rejection and to set the PUR gap value. Refer to **The Rejection Tab** section for more details.

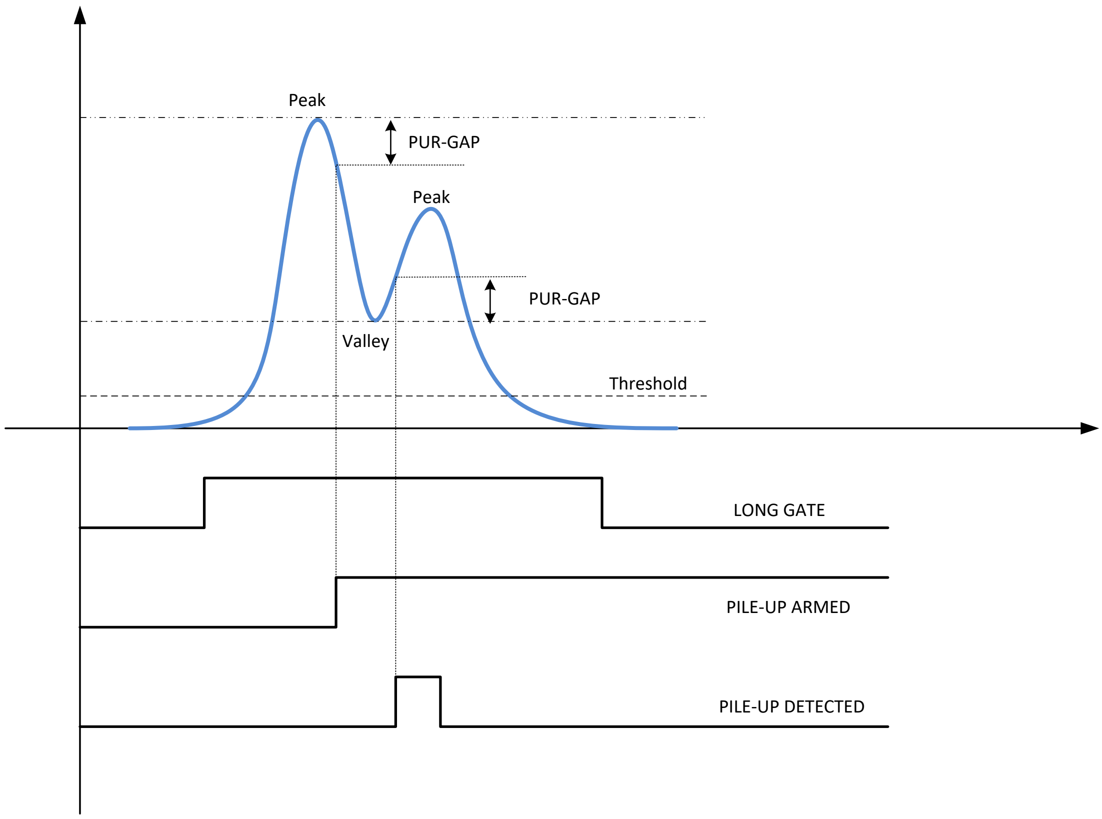


Fig. 2.18: Pile-up definition for 720, 725, 730 and 27xx series.

2.2 Supported Models

The following table lists the digitizer models supported by CoMPASS and able to run the DPP-PSD firmware:

Desktop Digitizer	Description
DT5720B	4 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE
DT5720C	2 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE
DT5720D	4 Ch. 12 bit 250 MS/s Digitizer: 10MS/ch, C20, SE
DT5720E	2 Ch. 12 bit 250 MS/s Digitizer: 10MS/ch, C20, SE
DT5725	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
DT5725B	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
DT5725S	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
DT5725SB	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
DT5730	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
DT5730B	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
DT5730S	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
DT5730SB	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
DT5751	2/4 Ch. 10 bit 2/1 GS/s Digitizer: 1.8/3.6MS/ch, EP3C16, SE
DT5790	2 Ch. 12 bit 250 MS/s Pulse Processor, SE
DT2740	64 Ch. 16 bit 125 MS/s Digitizer, DIFF
DT2740B	64 Ch. 16 bit 125 MS/s Digitizer, SE
DT2745	64 Ch. 16 bit 125 MS/s Digitizer with Programmable Input Gain, DIFF
DT2745B	64 Ch. 16 bit 125 MS/s Digitizer with Programmable Input Gain, SE
DT2730	32 Ch. 14 bit 500 MS/s Digitizer with Programmable Input Gain, SE
NIM Digitizer	**Description**
N6720B	4 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE
N6720C	2 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE
N6720D	4 Ch. 12 bit 250 MS/s Digitizer: 10MS/ch, C20, SE
N6720E	2 Ch. 12 bit 250 MS/s Digitizer: 10MS/ch, C20, SE
N6725	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
N6725B	8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
N6725S	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
N6725SB	8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
N6730	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
N6730B	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
N6730S	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
N6730SB	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
N6751	2/4 Ch. 10 bit 2/1 GS/s Digitizer: 1.8/3.6MS/ch, EP3C16, SE
N6751C	2/4 Ch. 10 bit 2/1 GS/s Digitizer: 14.4/28.8 MS/ch, EP3C16, SE
VME Digitizer	**Description**
V1720E	8 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE
V1720F(*)	8 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, DIFF
V1720G	8 Ch. 12 bit 250 MS/s Digitizer: 10MS/ch, C20, SE
V1725	16 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
V1725B	16 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
V1725C	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
V1725D	8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
V1725S	16 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
V1725SB	16 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
V1725SC	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
V1725SD	8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE

V1730	16 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
V1730B	16 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
V1730C	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
V1730D	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
V1730S	16 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
V1730SB	16 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
V1730SC	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
V1730SD	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
V1751	4/8 Ch. 10 bit 2/1 GS/s Digitizer: 1.8/3.6MS/ch, EP3C16, SE
V1751B(*)	4/8 Ch. 10 bit 2/1 GS/s Digitizer: 1.8/3.6MS/ch, EP3C16, DIFF
V1751C	4/8 Ch. 10 bit 2/1 GS/s Digitizer: 14.4/28.8MS/ch, EP3C16, SE
V2740	64 Ch. 16 bit 125 MS/s Digitizer, DIFF
V2740B	64 Ch. 16 bit 125 MS/s Digitizer, SE
V2745	64 Ch. 16 bit 125 MS/s Digitizer with Programmable Input Gain, DIFF
V2745B	64 Ch. 16 bit 125 MS/s Digitizer with Programmable Input Gain, SE
VX1720E	8 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE
VX1720F(*)	8 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, DIFF
VX1725	16 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
VX1725B	16 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
VX1725C	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
VX1725D	8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
VX1725S	16 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
VX1725SB	16 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
VX1725SC	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
VX1725SD	8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
VX1730	16 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
VX1730B	16 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
VX1730C	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
VX1730D	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
VX1730S	16 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
VX1730SB	16 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
VX1730SC	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
VX1730SD	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
VX1751	4/8 Ch. 10 bit 2/1 GS/s Digitizer: 1.8/3.6MS/ch, EP3C16, SE
VX1751B(*)	4/8 Ch. 10 bit 2/1 GS/s Digitizer: 1.8/3.6MS/ch, EP3C16, DIFF
VX1751C	4/8 Ch. 10 bit 2/1 GS/s Digitizer: 14.4/28.8MS/ch, EP3C16, SE
VX2740	64 Ch. 16 bit 125 MS/s Digitizer, DIFF
VX2740B	64 Ch. 16 bit 125 MS/s Digitizer, SE
VX2745	64 Ch. 16 bit 125 MS/s Digitizer with Programmable Input Gain, DIFF
VX2745B	64 Ch. 16 bit 125 MS/s Digitizer with Programmable Input Gain, SE
VX2730	32 Ch. 14 bit 500 MS/s Digitizer with Programmable Input Gain, SE
DPP-PSD Firmware	**Description**
DPP-PSD (8ch x720)	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (8ch x720)
DPP-PSD (4/2ch x720)	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (4/2ch x720)
DPP-PSD (16ch x725)	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (16ch x725)
DPP-PSD (8ch x725)	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (8ch x725)
DPP-SUP (16ch x725)	DPP-SUP - Super Licence for 16ch x725 Digital Pulse Processing
DPP-SUP (8ch x725)	DPP-SUP - Super Licence for 8ch x725 Digital Pulse Processing
DPP-PSD (16ch x730)	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (16ch x730)
DPP-PSD (8ch x730)	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (8ch x730)

DPP-SUP (16ch x730)	DPP-SUP - Super License for 16ch x730 Digital Pulse Processing
DPP-SUP (8ch x730)	DPP-SUP - Super License for 8ch x730 Digital Pulse Processing
DPP-PSD (8ch x751)	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (8ch x751)
DPP-PSD (4ch x751)	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (4ch x751)
DPP-SUP 2.0	DPP-SUP 2.0 - Super License for Digital Pulse Processing Digitizer 2.0 series

(*) The board is currently obsolete but still supported.

Tab. 2.1: CoMPASS supported boards with DPP-PSD firmware.

3 Multichannel Charge Integration: the DPP-QDC Firmware

This Chapter is intended to describe the Digital Pulse Processing for Charge to Digital Converter firmware (DPP-QDC) running exclusively on 740 digitizer series equipped with the Altera Cyclone III: x740D model). The complete list of digitizers running the DPP-QDC firmware is summarized on Tab. **3.1**. A x740D digitizer running the DPP-QDC firmware becomes a multichannel data acquisition system for nuclear physics and other applications requiring radiation detectors. The digitizer accepts signals directly from the detector and implements a digital replacement of a Single Gate QDC, Discriminator and Gate Generator. All these functionalities are performed inside the board FPGA without any use of external cables, nor additional boards or delay lines. The acquisition is therefore performed by a single compact system which is able to self-trigger on 32/64 channels independently, according to the form factor (Desktop-NIM/VME-VX64). In addition the trigger filter can be programmed independently on each channel to get the best resolution from different detector systems. The integration gate width can be set for groups of eight consecutive channels. The DPP-QDC is particularly suitable in case of segmented detectors, and in any case where a large number of detectors has to be read simultaneously. Considering the 740D sampling rate, it is indicated in case of spectroscopy with slow scintillation detectors, such as NaI(Tl), $LaBr_3$(Ce), $CeBr_3$, etc. Both the board configuration and the acquisition can be completely managed by the ComPASS Software, that allows the user to set the parameters for the acquisition, to configure the hardware, and to perform the data readout.

The main functionalities of a digitizer running DPP-QDC firmware are listed below:

- Auto selection of the events with a digital leading edge discrimination;
- Input signal baseline (pedestal) calculation and pedestal subtraction for energy calculation;
- Single gate integration for the energy spectra calculation.

Note: The description of the DPP-QDC system of this Manual is compliant with DPP-QDC firmware release 4.15_135.12. For future releases compatibility, check in the firmware and software revision history files.

3.1 Principle of Operation

The figure below shows the functional block diagram of the DPP-QDC firmware

The aim of the DPP-QDC firmware is to evaluate the charge of the input signal in a multi-channel system. Each channel can be programmed and acquired independently from the other channels. The main operations of the DPP-QDC firmware can be summarized as follows:

- receive an input signal directly from the detector and digitize it continuously. It is possible to adjust the dynamic range with a programmable DC offset to exploit the full dynamics of the digitizer;
- the algorithm continuously calculates the baseline of the input signal by averaging the samples belonging to a moving window of programmable size (see Sect. Baseline). The baseline is subtracted from the input signal, giving input_sub= input – baseline (Digital Baseline Restorer);
- the input_sub value is compared with the value of the trigger threshold and the event is selected as soon as the input_sub signal crosses the threshold (see Fig. 2.2). The threshold value can be set independently on each channel of the board. Once the event is selected a local trigger is generated (refer to Sect. DPP-QDC trigger management for further details);

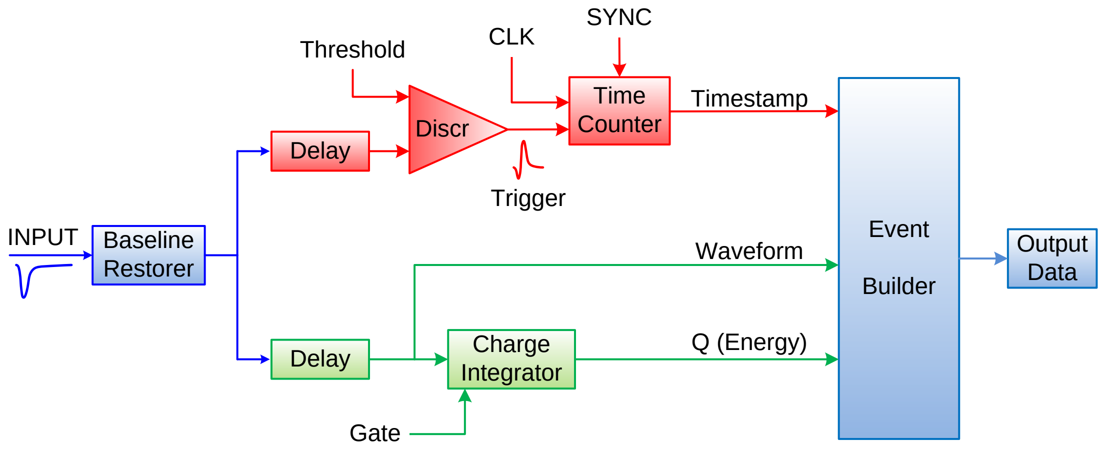


Fig. 3.1: Functional Block Diagram of the DPP-QDC.

- at the trigger fire, the signal is delayed by a programmable number of samples (corresponding to the "Pre Trigger" value in ns) to be able to integrate the pulse before the trigger ("Gate Offset"). The gate for charge integration is then generated and it is therefore received by the charge accumulator before the signal. While the gate is active the baseline remains frozen to the last averaged value and its value is used as charge integration reference. The gate width can be set independently for each group of eight channels. Fig. **3.2** summarizes all the DPP-QDC parameters;

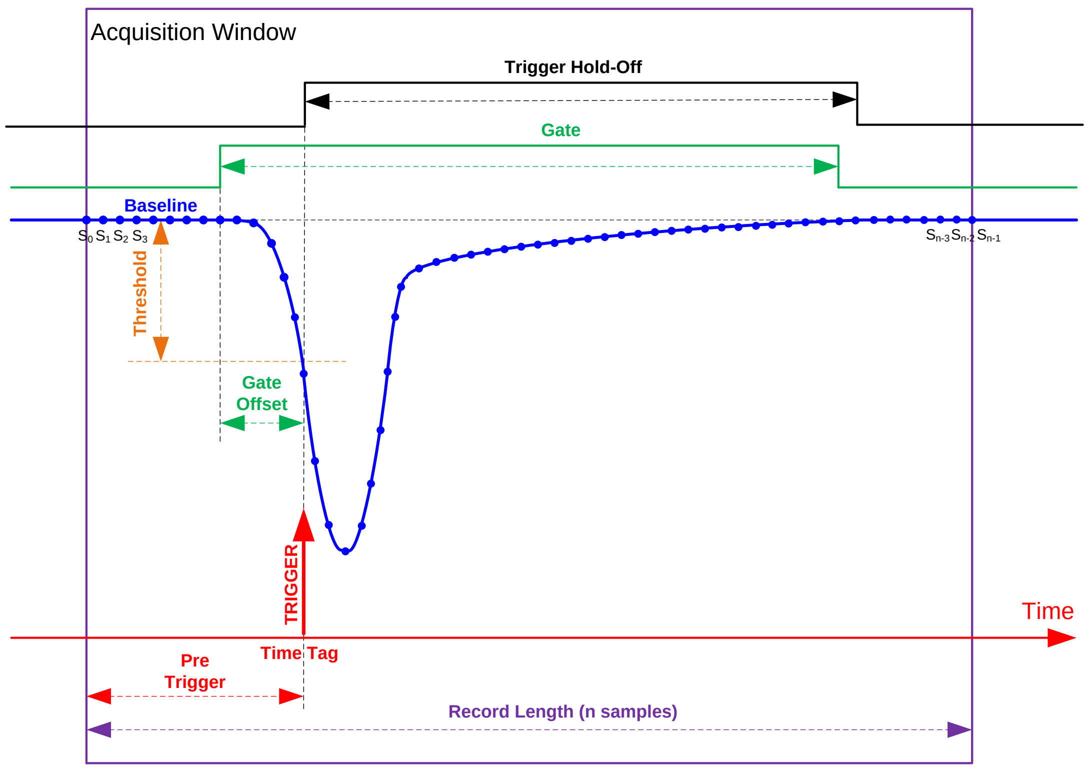


Fig. 3.2: Diagram summarizing the DPP-QDC parameters. The trigger fires as soon as the signal crosses the threshold value. Gate, Gate Offset, Pre-Trigger, Trigger Hold-Off, and Record Length are also shown for one acquisition window.

- for the whole duration of a programmable "trigger hold-off" value, other trigger signals are inhibited.

It is recommended to set a trigger hold-off value comparable with the signal width. The baseline remains frozen for the whole trigger hold-off duration;

- the trigger enables the event building, that includes the waveforms (i.e. the raw samples) of the input, the trigger time stamp, the baseline, and the charge integrated within the gate. After that the system gets ready for a new event;

Note: The DPP-QDC firmware is not designed to acquire continuous stream of waveforms. Only a statistical portion of the waveforms is saved, also in case of low rate.

- the event data is saved into a memory buffer. The user can choose both the number of events inside the buffer, and the number of total buffers that the memory is divided in. If the buffer contains only one event, that buffer becomes immediately available for the readout and the acquisition continues into another buffer. If more events are written in one buffer, only when the buffer is complete those events become available for the readout;
- the software can then plot the signal waveforms for debugging and adjust the parameters, as well as plot the energy spectrum and timing distribution;
- finally output files (list and waveform) can be generated in different formats suitable for external spectroscopy analysis software tools. Energy and time spectra are not managed onboard but they can be generated and saved by the CoMPASS Software.

3.1.1 Baseline

The baseline calculation is an important feature of the DPP-QDC firmware, since its value is used as reference for the charge integration of the input pulses. Moreover, most of the DPP parameters are related to the baseline value. This paragraph describes in detail how the baseline calculation works. The user can choose to set a fixed value for the baseline, or to let the DPP firmware calculate it. In the first case the user must set the *baseline value in LSB units*, where **1 LSB = 0.49 mV**. The firmware can dynamically evaluate the baseline as the mean value of N points inside a moving time window. The user can choose the N value among 4, 16, and 64. The baseline is then frozen from few clocks before the gates start up to the end of the maximum value between the long gate and the trigger hold-off. After that the baseline restarts again its calculation considering in the mean value also the points before the freeze. This allows to have almost no dead-time due to the baseline calculation. Fig. **3.3** shows how the baseline calculation and freeze work. The trigger threshold dynamically follows the variation of the baseline.

3.1.2 DPP-QDC Trigger Management

The DPP-QDC firmware allows for several way of trigger generation:

1. Normal Mode: each channel can “self-trigger” on its own input signal when the input crosses a programmable threshold. The self-trigger works on each channel independently from the other channels;
2. Paired Mode: Each channel can both acquire on its own self-trigger and on the self-trigger of the paired channel. Pair “n” corresponds to channel n and channel n+2;
3. External Trigger Mode: the board can accept an external trigger on the TRG IN connector. The external trigger acquisition mode can be configured according to bits[21:20] of register 0x8000 (Board Configuration) (see also **[740QDC_Reg]**). The following options are available:
   - The acquisition is synchronized with the external trigger edge. All channels acquire simultaneously and their self-trigger is disabled;
   - Veto: the acquisition is inhibited when the external trigger is active high;
   - Anti-Veto: the acquisition is inhibited when the external trigger is active low.

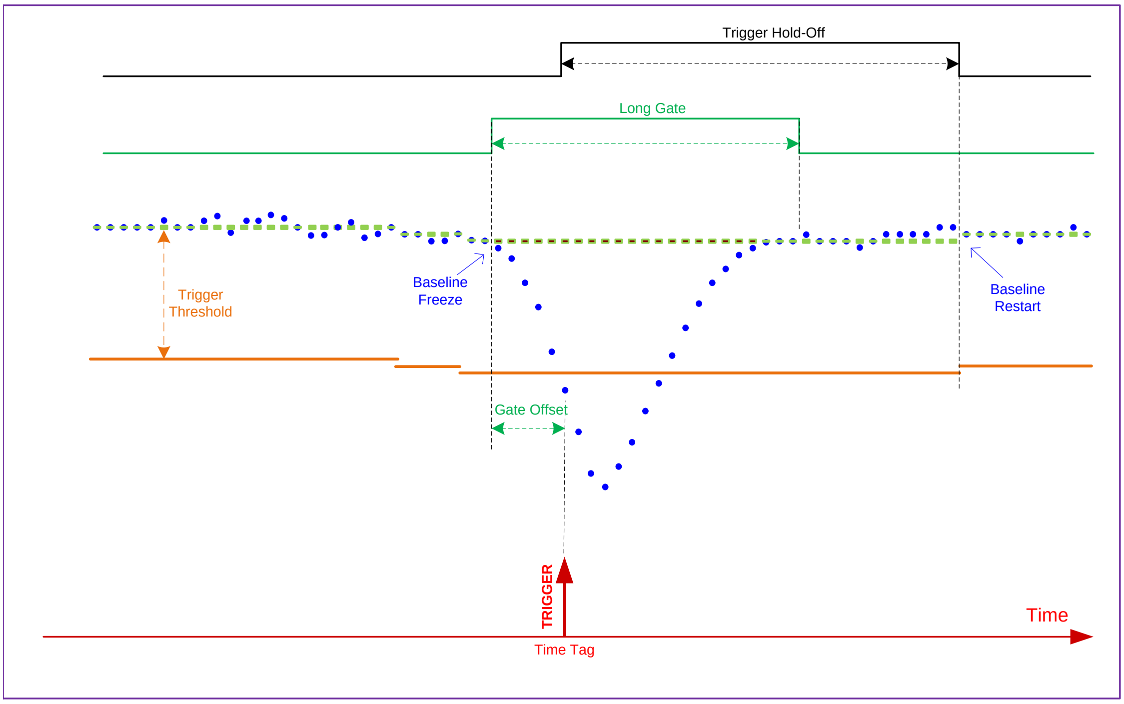


Fig. 3.3: Baseline calculation as managed by the DPP-QDC algorithm.

Note: In case of external trigger mode it might be useful to disable the individual channel self-trigger. To disable the channel self-trigger the user must set bit[24] = 1 of register 0x8040 (DPP Algorithm Control) (see also **[740QDC_Reg]**).

3.1.2.1 Trigger Hysteresis

When the input signal is no more over-threshold, the trigger could fire again in the tail of the pulse, especially in case the tail contains spikes or noise. The “Trigger Hysteresis” feature inhibits the trigger until the input pulse reaches half of the threshold value itself. See Fig. **3.4** for a diagram of this feature. This option is enabled by default. To disable set bit[30] = 1 of register 0x8040 (DPP Algorithm Control) **[740QDC_Reg]**.

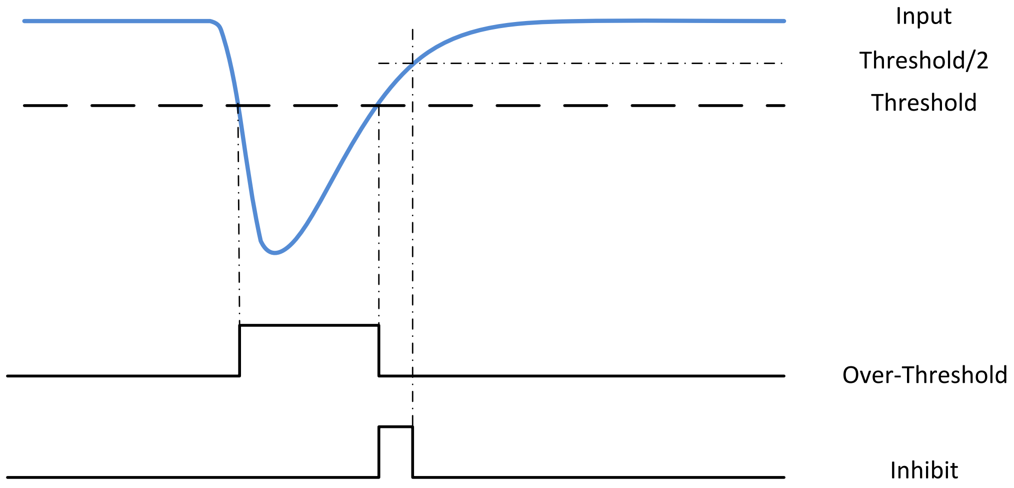


Fig. 3.4: Trigger Hysteresis in DPP-QDC firmware. The trigger is inhibited after the over-threshold until the input reaches the value of half the threshold.

3.1.2.2 Input Smoothing

The smoothing is a moving average filter, where the input samples are replaced by the mean value of the previous n samples. n is defined by bits[14:12] of register 0x8040 (DPP Algorithm Control) **[740QDC_Reg]**, and the number of samples for the smoothing is defined as n = 2^m, where m = 0, ..., 6. Option m = 0 disables the smoothing. When enabled, the trigger is applied on the smoothed samples, thus reducing triggering on noise. The charge integration is either performed on the input samples or on the smoothed samples, according to the Analog Probe selection from bits[13:12] of register 0x8000 **[740QDC_Reg]**.

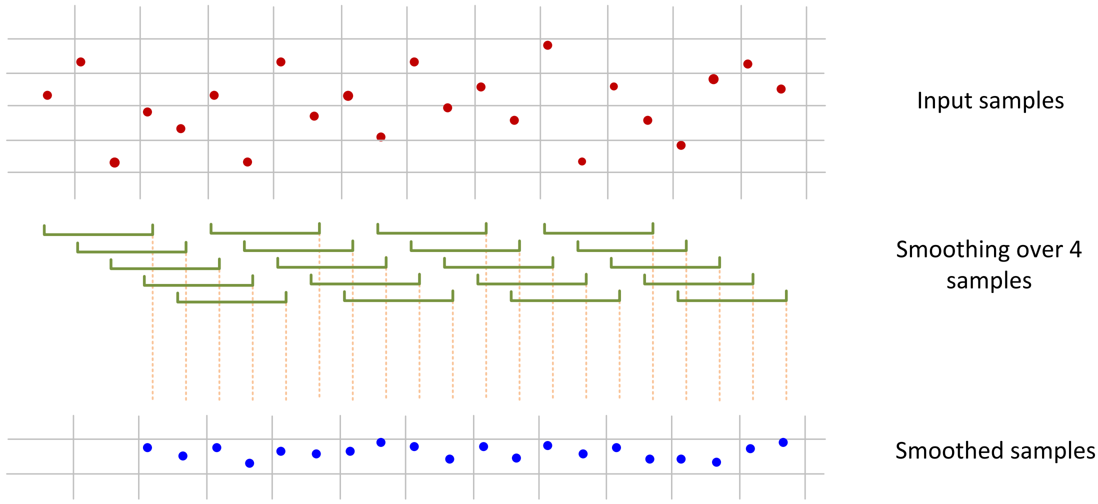


Fig. 3.5: Example of smoothing over four samples. The input samples are averaged over four samples and replaced in the smoothed samples by the mean value.

3.2 Supported Models

The following table lists the digitizer models supported by CoMPASS and able to run the DPP-QDC firmware:

Desktop Digitizer	Description
DT5740D	32 Ch. 12 bit 62.5 MS/s Digitizer: 192kSch, EP3C40, SE
NIM Digitizer	**Description**
N6740D	32 Ch. 12 bit 62.5 MS/s Digitizer: 192kSch, EP3C40, SE
Desktop Digitizer	**Description**
V1740D	64 Ch. 12 bit 62.5 MS/s Digitizer: 192kS/ch, EP3C40, SE
VX1740D	64 Ch. 12 bit 62.5 MS/s Digitizer: 192kS/ch, EP3C40, SE
DPP-QDC Firmware	**Description**
DPP-QDC (64ch x740)	DPP-QDC - Digital Pulse Processing for Time Stamped Digital QDC (64ch x740)
DPP-QDC (32ch x740)	DPP-QDC - Digital Pulse Processing for Time Stamped Digital QDC (32ch x740)

Tab. 3.1: CoMPASS supported boards for DPP-QDC firmware.

4 Pulse Height Analysis and Digital MCA: the DPP-PHA Firmware

The aim of the DPP-PHA firmware is to implement a digital version of the analog chain made by Shaping Amplifier + Peak Sensing ADC (Multi Channel Analyzer). CoMPASS supports the following digitizers running the DPP-PHA firmware: Mod. **x724** (14 bit, 100MS/s), Mod. **x725** (14 bit, 250 MS/s), Mod. **x730** (14 bit 500 MS/s) and the Digital MCAs Mod. **DT5780/N6780**, Mod. **DT5781/N6781** and Mod. **V1782**. It is mainly used for high resolution spectroscopy (Germanium and Silicon detectors) but it is also well suited for inorganic scintillators like NaI or CsI. The output of the charge sensitive preamplifier or of the photomultiplier is directly connected to the input of the digitizer/MCA with **no use of the Shaping Amplifier**.

4.1 Traditional Analog Approach

The traditional analog chain for signal readout from nuclear radiation detector usually makes use of almost all-analog chains, where the electronics rely upon three fundamental devices: the Charge Sensitive Preamplifier, the Shaping Amplifier and the Peak Sensing ADC (refer to Fig. **4.1**).

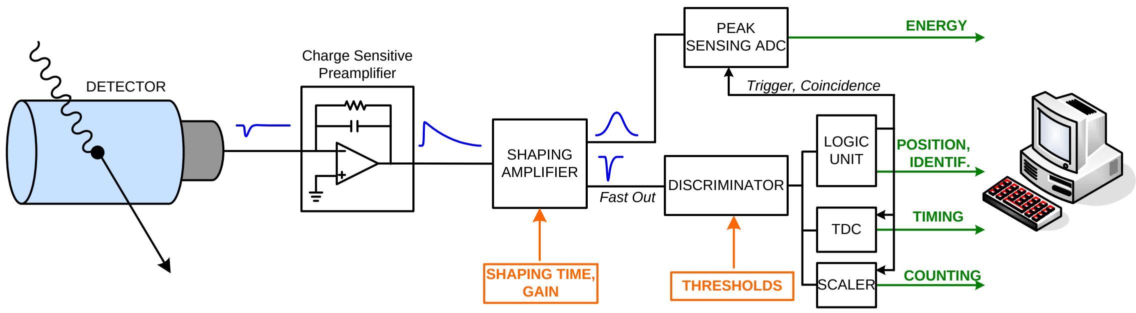


Fig. 4.1: Nuclear Radiation Detector (with Charge Sensitive Preamplifier) Analog Chain Block Diagram.

The Charge Sensitive Preamplifier (Fig. **4.2**) integrates the signal coming from the detector, as the HPGe, thus converting the collected charge into a voltage step. The integrating capacitor is put in parallel with a discharging resistor, so that the preamplifier output will have pulses with a fast rise time and a long exponential tail with decay time τ. The charge information (proportional to the energy released by the particle in the detector) is therefore represented by the pulse height. The charge-amplitude proportionality is set by the capacitor value $V_{OUT} = \frac{Q}{C}$ and the decay time of the output signal is $\tau = RC$.

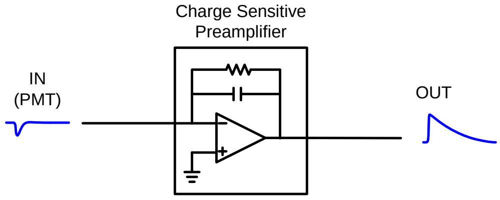


Fig. 4.2: Simplified schematic of a RC-type Charge Sensitive Preamplifier.

To have a good charge-amplitude conversion and to minimize the noise, the decay time τ is much larger than the width of the detector signal, typically 50-100 µs, and for this reason pile-up of different particle detections can arise (Fig. **4.3**).

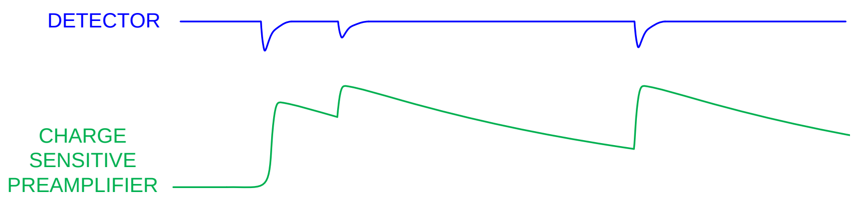


Fig. 4.3: Pile-up of detector signals due to the large decay time of the Preamplifier output.

Another drawback when using a Charge Sensitive Preamplifier is when the peak is too sharp for the Peak Sensing ADC to be detected with the required precision.

To avoid these problems the pre-amplified signal is usually feed into a Shaping Amplifier, that provides out a quasi-Gaussian output whose height is still proportional to the energy released by the detected particle. Finally, the signal from the Shaping Amplifier is fed into a Peak Sensing ADC, which is able to evaluate and digitize the height of the pulses, and filling a histogram with these values, which corresponds to the energy spectrum.
To preserve the timing information, the fast component of the signal (rising edge) is usually treated by a Fast Amplifier (or Timing Amplifier) that derives the signal; the output of the fast amplifier usually feeds a chain made of a Discriminator (CFD), a TDC and/or a Scaler for the timing/counting acquisition. Further modules can be present to implement logic units, to make coincidences (giving the position and the trajectory of the particles), to generate triggers or to give information about the pulse shape (time over threshold, zero crossing, etc.) for the particles identification. Usually, the Fast Amplifier is included into the Shaping Amplifier module and the relevant signal is provided as a separate fast output (or timing output). The typical signal shapes from the analog chain is shown in Fig. **4.4**.

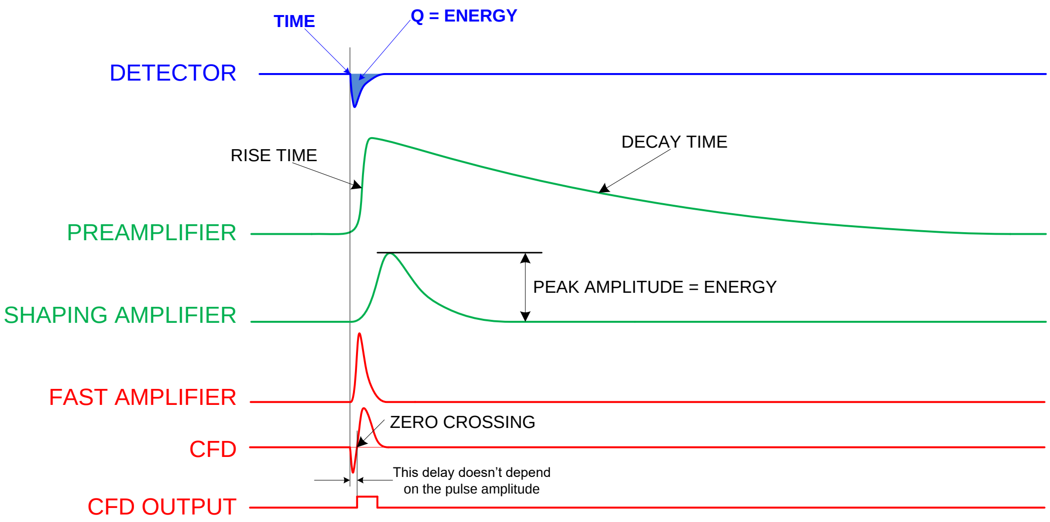


Fig. 4.4: Signals in the traditional analog chain.

4.2 CAEN Digital Approach

In the CAEN digital approach all blocks from the shaping amplifier to the PC are synthesized into a single device, the digitizer (see Fig. **4.5**).

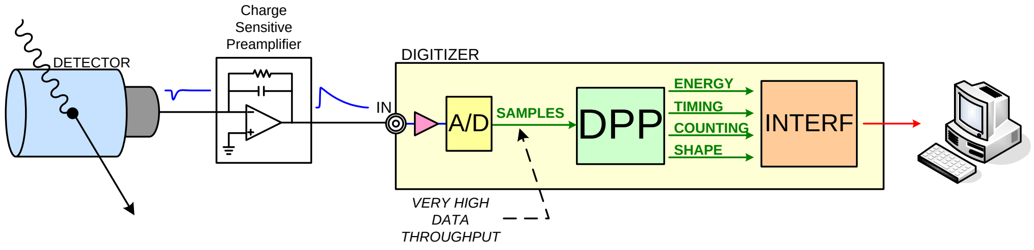


Fig. 4.5: Block Diagram of a Digitizer-based Spectroscopy System.

The new FPGA based techniques allow the user to change the readout parameters according to the detector characteristics, thus enabling the measurement of different radiations with different detectors using the same hardware. The digitizer becomes itself a Digital Multi Channel Analyzer (MCA).
In the technique called Multi Channel Analysis, the energy spectrum histogram X- axis can be segmented in "bins" or "Channels", each one representing a pulse height value, in V (or, if calibrated, the corresponding radiation Energy in keV). The spectrum resolution should be matched with the detector Energy resolution for optimal results (i.e. a 1K Channels Spectrum is good enough of basic gamma spectroscopy with NaI detectors while at least an 8K Channels Spectrum is needed to appreciate the intrinsic Energy resolution of HPGe Detectors). The histogram Y-axis values indicate the number of counts accumulated during the measuring time in the corresponding x-axis "bin" or "Channel".

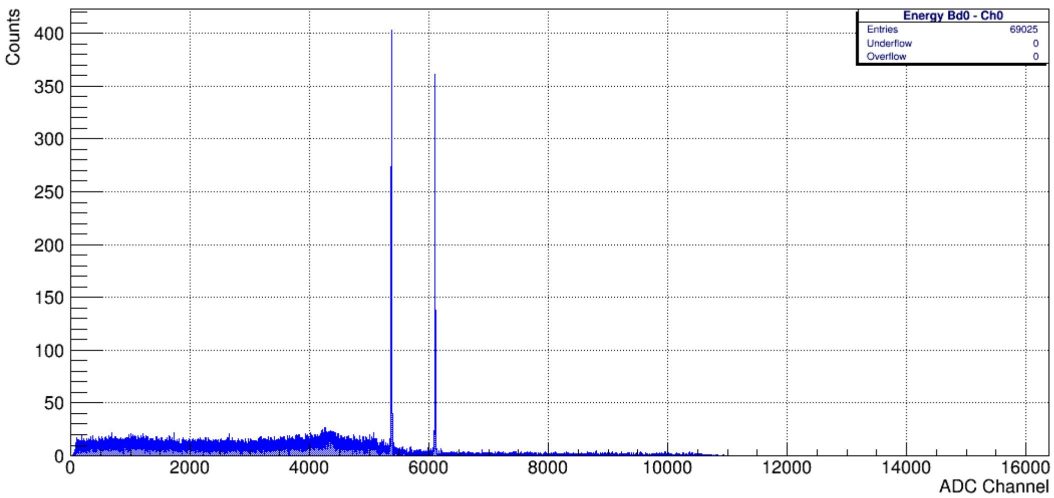


Fig. 4.6: ^{60}Co energy spectrum from HPGe detector.

The algorithm implemented in the digitizer FPGA is based on the Jordanov trapezoidal filter **[Jordanov]** and it is called **DPP-PHA (Digital Pulse Processing for Pulse Height Analysis)**. The trapezoidal filter is a filter able to transform the typical exponential decay signal generated by a charge sensitive preamplifier into a trapezoid whose flat top height is proportional to the amplitude of the input pulse (that is to the energy released by the particle in the detector) (see Fig. **4.7**). The trapezoid plays almost the same role of the shaping amplifier in a traditional analog acquisition system. There is an analogy between the two systems: both have a "shaping time" constant and must be calibrated for the pole-zero cancellation. For both, a long shaping time gives a better resolution but has higher probability of pile-up. Both are AC coupled with respect to the output of the preamplifier whose baseline is hence removed, but both have their own output DC offset and this constitutes another baseline for the peak detection.

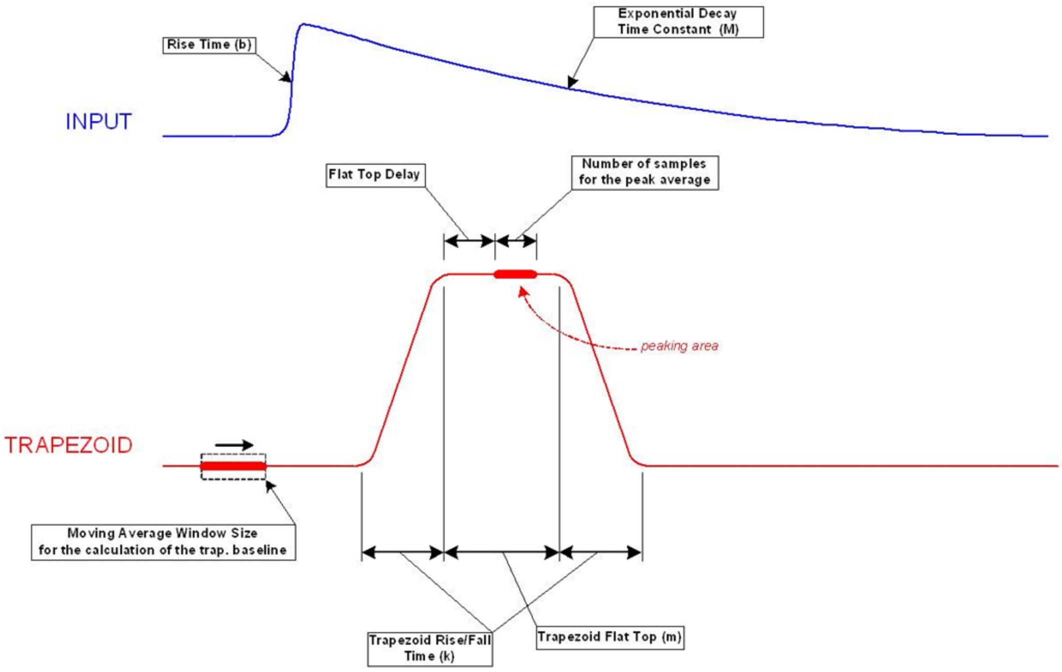


Fig. 4.7: Pulse Height Analysis with Trapezoid Method.

The block diagram of the processing chain inside the digitizer FPGA is shown in Fig. **4.8**.

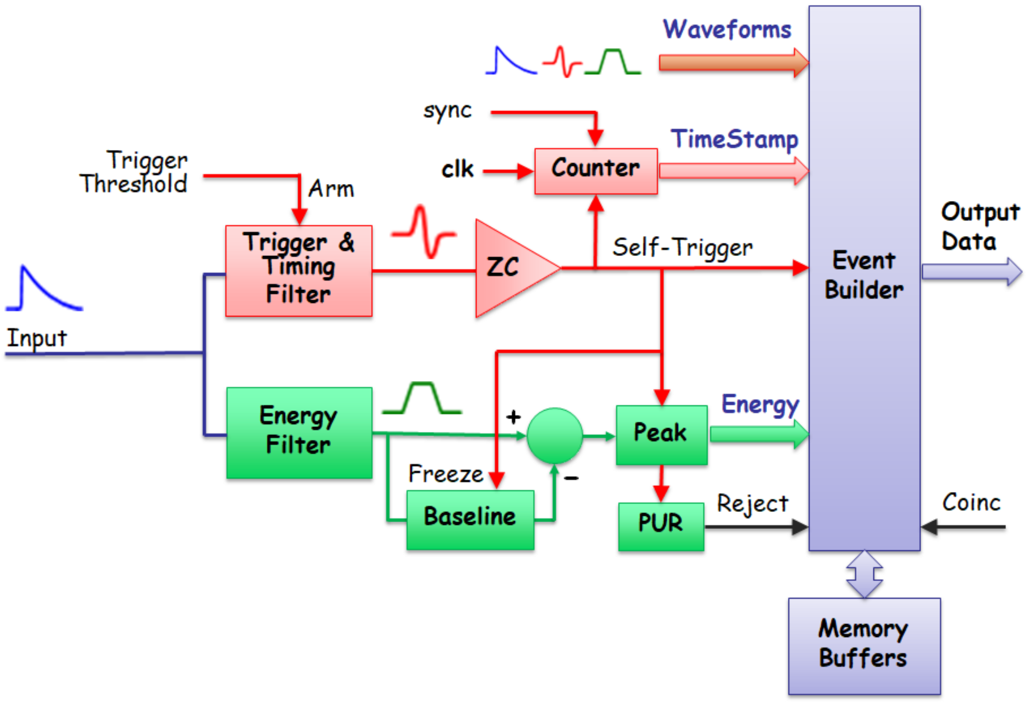


Fig. 4.8: Block Diagram of the DPP-PHA firmware.

4.2.1 Trigger and Timing Filter

4.2.1.1 The RC-CR2 filter

The aim of the Trigger and Timing Filter (TTF) is to identify the input pulses, generate a digital signal called *trigger* that identifies the pulse, and calculate the time of occurrence of the event (trigger time stamp). The TTF performs a digital RC-CR^2 filter, whose zero crossing corresponds to the trigger time stamp. In analogy with a CFD – Constant Fraction Discrimination – the RC-CR^2 signal is bipolar and its zero crossing is independent of the pulse amplitude. The integrative component of the RC-CR^2 is a smoothing filter based on a moving average filter that reduces the high frequency noise and prevents the trigger logic to generate false triggers on spikes or fast fluctuation of the signals. The derivative component allows to subtract the baseline, so that the trigger threshold is not affected by the low frequency fluctuation. Moreover the pile up effect is significantly reduced (see Sec. **Pile-up Rejection**).

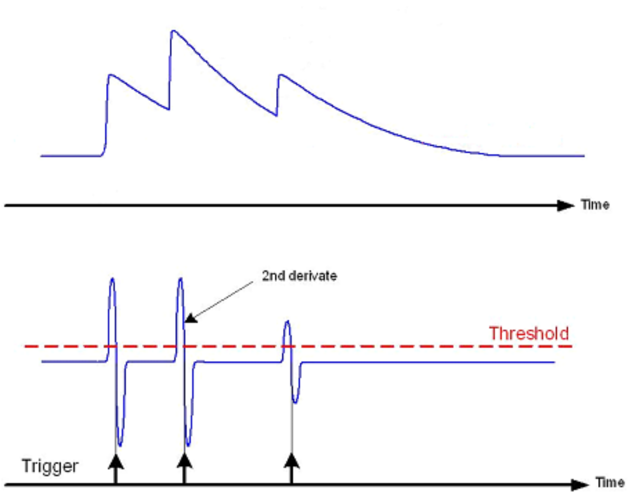


Fig. 4.9: The Trigger and Timing Filter allows to detect pulses on the zero-crossing of the RC-CR^2 signal, which corresponds to a 2nd derivative of the input pulse. The derivative component of the RC-CR^2 subtracts the baseline and makes easier to perform a zero-crossing calculation.

The trigger logic gets armed at the **Threshold** crossing, then it generates the trigger signal at the RC-CR^2 zero crossing. Setting the threshold value corresponds to set the LLD (lower level discrimination) of the energy spectrum. The user can check from the histogram which value corresponds to the set threshold level. Another important parameter for the trigger logic is the **RC-CR^2 smoothing**, corresponding to the number of samples used for the RC-CR^2 signal formation. Increasing this parameter may help in reducing high frequency noise, but have the drawback to make the signal slower and smaller, due to the smoothing. Finally the **Input Rise Time** is the time the RC-CR^2 reaches its maximum value. This value should correspond to the input rise time, in such a way the RC-CR^2 peak value corresponds to the height of the input signal. Examples on how to proper set the trigger and timing filter can be found in **[CompassQS]**.

4.2.1.2 The triangular filter

In case of the 2740 and 2745 the DPP-PHA firmware discriminates events based on a triangular filter whose rise time can be defined by the user in the range 0.08 to 2 µs

The trigger threshold is then referred to the derivative of the triangle itself, and the threshold crossing arms the event selection. The trigger fires at the zero crossing of the derivative signal itself. The user can see the derivative trace on the signal inspector.

The triangual filter has the same timing performance of the RC-RC2 one, while it improves the noise immu-

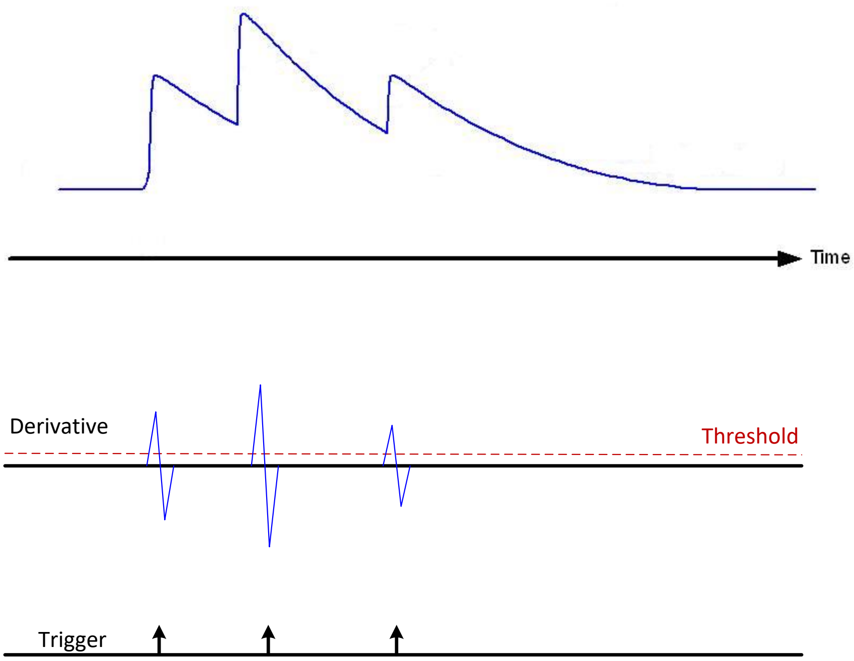


Fig. 4.10: Triggering on the triangular signal (2740 and 2745 only).

nity and so the capability to reach lower trigger threshold lower. This is important in some spectroscopy measurements in which low energy peaks have to be discriminated. Another advantage of the triangular filter is that it is less sensitive to pulse over-shuts that sometimes cause re-triggering with consequent wrong pile-up identification.

4.2.2 Trapezoidal Filter (Energy Filter)

As in the traditional analog chain, the Shaping Amplifier is able to convert the exponential shape from the Charge Sensitive Preamplifier into a Gaussian shape whose height is proportional to the pulse energy, in the same way the Trapezoidal filter is able to transform it into a trapezoidal signal whose amplitude is proportional to the input pulse height (energy). In this analogy, the **Trapezoid Rise Time** corresponds to the Shaping Time times a factor of 2/2.5. Therefore for an analog shaping of 3us the user can set a trapezoid rise time of 7-8 us (see also **[CompassQS]**).

In case of high rate signal, the trapezoid rise time value should be reduced in order to avoid pile-up effects (see Sec. **Pile-up Rejection**), choosing a compromise between high resolution (high value of trapezoid rise time) and pile-up rejection (and corresponding dead time).

The energy value of the input pulse is evaluated as the height of the trapezoid in its **Flat Top** region. The user must take care that the flat top is really flat and that the **Peaking** (i.e. the samples used for the energy calculation) is in the flat region. Moreover, the correct setting of flat top and peaking helps in the correct evaluation of the energy especially when large volume detectors are involved and the ballistic deficit may cause a significant error in the energy calculation. In this case, it may be convenient to increase the flat top duration and delay the peaking time to wait for the full charge collection.

Fig. **4.11** summarizes the settings for both the Trigger and Timing Filter and for the Trapezoid Filter.

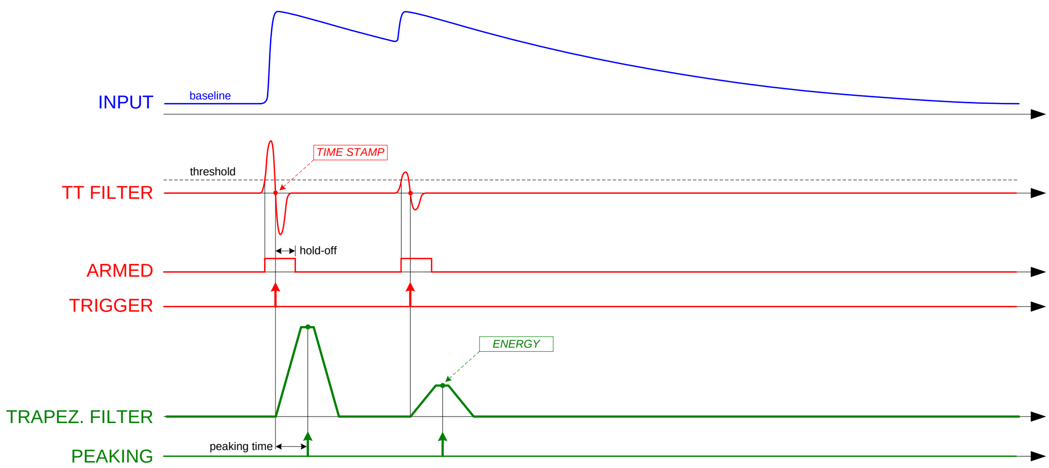


Fig. 4.11: Simplified signals scheme of the Trigger and Timing filter (red) and the Trapezoidal Filter (green). In blue the input pulses from Preamplifier.

4.2.3 Pole-Zero Adjustment

Like the Gaussian pulse of the Shaping Amplifier, also the trapezoid requires an accurate pole-zero adjustment to guarantee the correct return to the baseline at the end of the falling edge. To correctly set the pole-zero the user must take care of setting the proper **Trap. Pole Zero** value (which corresponds also to the Input Decay Time) to avoid either undershoot or overshoot effects (as can be seen in Fig. **4.12** and **4.13**). Pole Zero Adjustment can reduce signal artifacts due to pulses pile up occurring when the counting rate is high compared to the pulse decay.

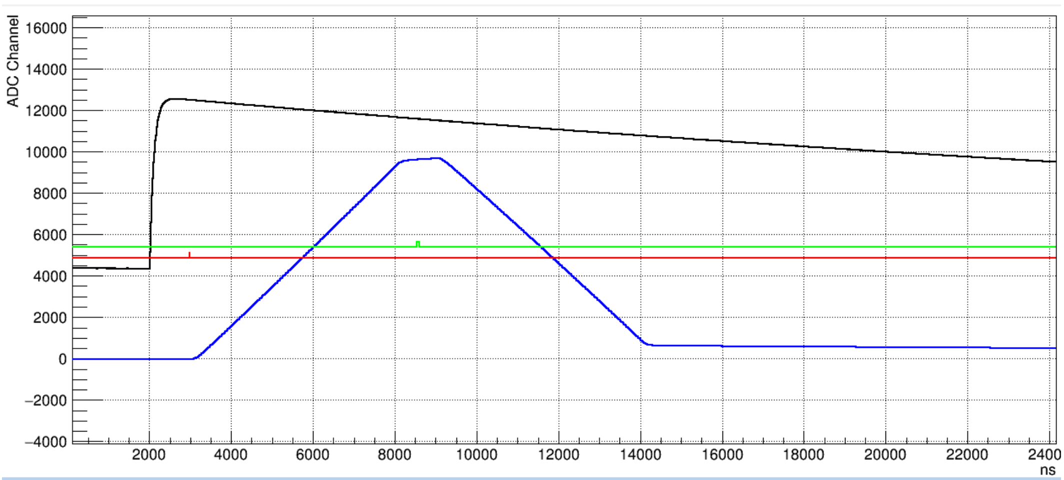


Fig. 4.12: Pole Zero effects of overshoot of the trapezoid (blue curve).

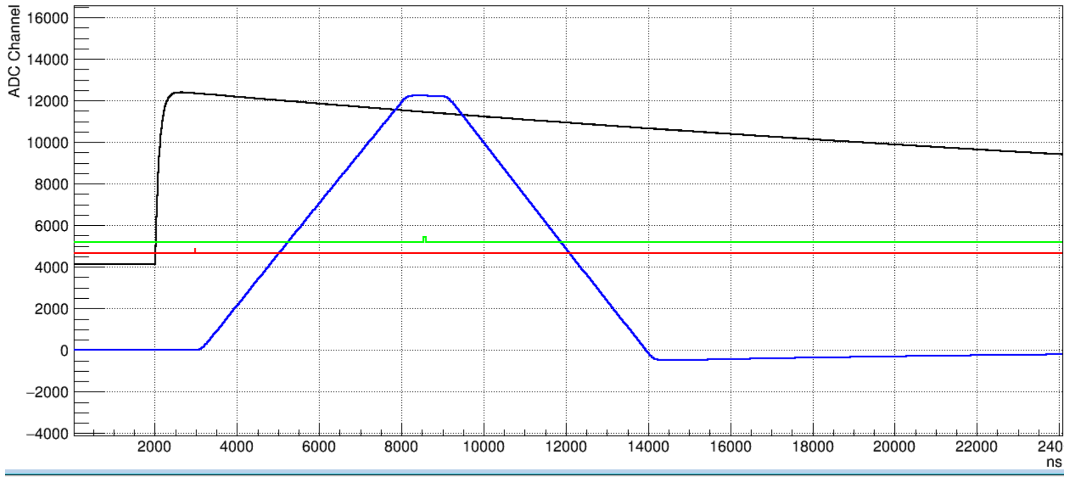


Fig. 4.13: Pole Zero effects of undershoot of the trapezoid (blue curve).

4.2.4 Baseline Restoration

The energy filter includes also a baseline restorer that operates on the trapezoidal filter output and calculates the baseline by averaging a programmable number of points before the start of the trapezoid. The baseline is then frozen for the trapeze duration and used for the height calculation. Once the trapezoid is returned to the baseline, the averaging restarts to run. The pulse height (i.e. the trapezoid amplitude) is given as the distance between the flat top and the baseline taken in the programmed position; to further reduce the fluctuation of this distance due to the noise, it is possible to average a certain number of points in the flat top before subtracting the baseline. In case of high resolution measurements, it is strongly suggested to increase the number of **Baseline Mean** samples at the maximum allowed value.

4.2.5 Pile-up Rejection

If two events are separated by less than the trapezoid duration, then the relevant trapezoids overlap. The trapezoid duration pkrun is defined as $pkrun = RT + FT + pkho$, where RT is the trapezoid Rise Time, FT is the trapezoid Flat Top, and pkho is the Peak Hold-Off, which starts at the end of the Flat Top. There are four different cases (Fig. **4.14**):

- $\Delta T > pkrun$, the two events are well separated and none of them is flagged as pile-up.
- $RT + FT < \Delta T < pkrun$, the rising edge of the 2nd trapezoid overlaps on the pkho of the 1st one. In this case only the first event has a correct value of energy, while the second one is tagged as pile-up.
- $1.5 * IRT < \Delta T < RT + FT$, where IRT is the Input Rise Time, which corresponds to the time the RC-CR^2 signal reaches its maximum value, and 1.5 * IRT is the time the RC-CR^2 signal crosses the zero. The two events are both flagged as pile-up, since the two trapezoids overlap.
- $\Delta T < 1.5 * IRT$, the two pulses are too close and the trigger filter is unable to resolve the double pulse condition. In this case, the pile-up cannot be recognized and the two pulses are treated as a single pulse. The algorithm returns only one time stamp and one energy, whose value corresponds to about the sum of the two energies (‘sum peak’ in the spectrum).

Except for the case 4, the DPP-PHA algorithm is able to save into the memory buffer all the incoming events, including the piled-up pulses; in case of pile-up the energy value is anyhow meaningless. During the readout of the event list, these events will not be accumulated into the histograms (that are calculated in the software), although they participate to the total counts, thus giving an accurate estimation of the Input Count Rate. Furthermore, the energy spectrum can be corrected run-time by a statistical redistribution of the missed energies over the spectrum acquired within a specific time slot.

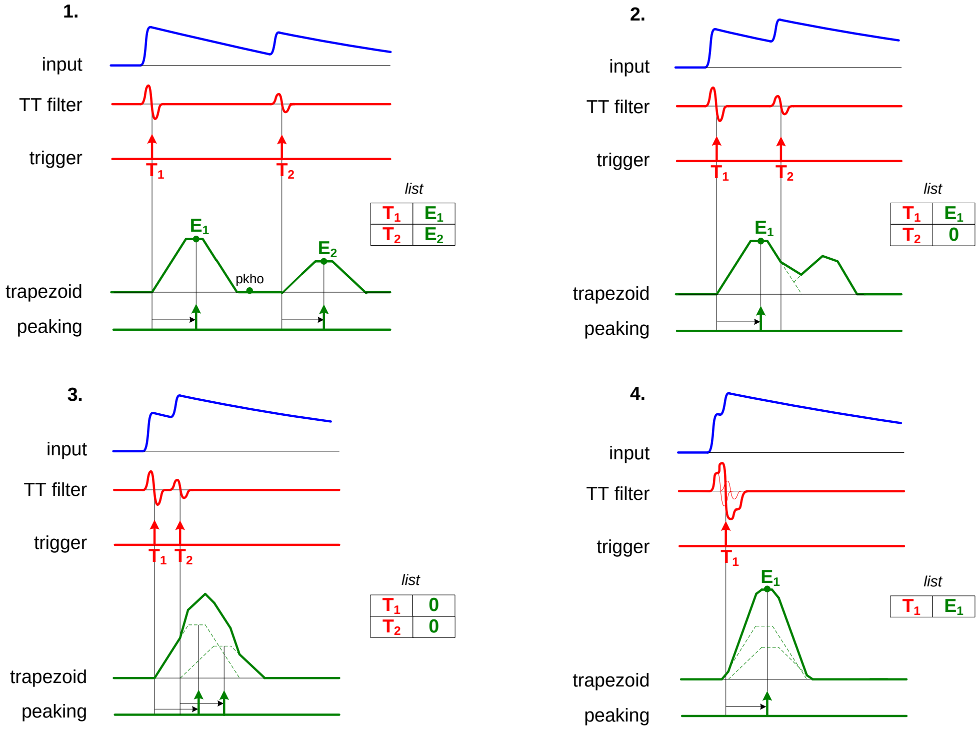


Fig. 4.14: The effect of trapezoid overlapping in the four main cases: 1. The two trapezoids are well separated (top left); 2. The second trapezoid starts on the falling edge of the first one (top right). 3. The second trapezoid starts on the rising edge of the first one (bottom left). 4. The two input pulses pile-up in the input rise time (bottom right).

4.2.5.1 Veto

Note: Veto options can be enabled via register writes using the FreeWrites options (refer to Sec. **The Acquisition Tab**).

In case of 724, 780, 781 and V1782 series CoMPASS allows the user to directly manage the veto coming from an external signal through the digitizer TRG-IN connector (see Sec. **The Trigger/Veto/Coincidences Tab**). The other veto options are managed by the Global Trigger Mask register (0x810C) and Trigger Validation Mask (0x8180 + 4n). In case of DPP-PHA firmware release higher than **128.64**, the firmware allows the user to select several sources of veto (**[724_781PHAReg] [780PHAReg]**). They are:

- Global Trigger from register 0x810C. The coincidence mode (bit[19:18] = 10 @ 0x1n80) must be enabled to identify the global trigger as veto;
- Individual Trigger from register 0x8180+4n. Coincidence mode (bit[19:18] = 10 @ 0x1n80) must be enabled to identify the individual trigger as veto;
- Over saturation;
- Under saturation;
- Channel Trigger i.e. any possible source of the channel trigger (Global Trigger, Individual Trigger, Software Trigger, Self Trigger);
- Global busy (OR of channel busy lines). This option is mainly suggested for neighbor trigger mode (bit[19:18] = 01 @ 0x1n80), when the trigger logic is the OR of the channels.

The user can select them acting on the bits[5:0] of the register 0x1nA0 and can set the width of the veto duration through register 0x1nD4. In particular bits[23:0] define the width in steps of 10 ns.In case of DPP-PHA firmware release lower than **128.64**, CoMPASS does not support any veto option while the firmware supports only the option of the veto coming from an external signal through the digitizer TRG-IN connector. To use this option the user has to enable the bit[2] of the register 0x8000, the bits [19:18] of the register 0x1n80 (where n is the number of the vetoed channel) and the bits[11:10] of the register 0x811C.

In case of 725 and 730 series CoMPASS allows the user to directly manage the veto coming from an external signal through the digitizer TRG-IN connector as well (see Sec. **The Trigger/Veto/Coincidences Tab**).

Besides this the user can set a different coincidence logic between channels inside the couple and extra couples. For example, it is possible to set the AND between the channels inside the couple, and set a veto from external trigger for all couples (see **[Coincidence]** for additional examples). The 724, 780, 781 and V1782 series can handle just one type of coincidence logic and do not have the veto management of 725 and 730 series.

In particular, while the coincidence inside the couple is managed by bits[6:0] of register 0x1nA0, bits[19:18] of the same register **[725_730PHAReg]** manage the veto source, which can be common among all channels (set it through register 0x810C, and it can be generated by an external trigger or by a combination of the trigger requests from couples), or individually set for the couples of channels (each couple can have a different veto, which can be set through register 0x8180 (+4n), where n is the couple index, and it can be generated by an external trigger or by a combination of the trigger requests from couples). Finally a veto can come from events with negative saturation: the user can set this option acting on the bits[15:14] of the register 0x1nA0. The user can set the width of the veto duration through register 0x1nD4. In particular bits[15:0] define the width, and bits[17:16] define the step, that can be chosen among 8 ns, 2 us, 524 us, and 134 ms.

In case of the 2740 and 2745 series CoMPASS allows the user to the user to directly manage the veto coming from an external signal through the digitizer S-IN and GPIO front panel connecto connector as well (see Sec. **The Trigger/Veto/Coincidences Tab**).

4.2.6 Dead Time

When a pulse is processed by an analog chain block, the maximum read-out rate is limited by the need to complete the processing of the current pulse before being able to process a successive valid signal. When the processing time of a pulse is larger than the time interval before the arrival of the next pulse, the analog chain is “temporarily blind” and misses one or more successive pulses. The actual live counting time is therefore smaller than the total counting time, and the difference between total time and live counting time is called “Dead time”. The Digital MCA read out capability is rather independent from the ADC sampling time and processing speed than from the signal width, and in general allows for higher counting rates than the analog chain. The digital MCA dead time is also an information on the relationship between total measurement time and live counting time values. The CoMPASS software is able to automatically evaluate the dead-time including the contributions of *pile-up events*, saturation events, and Trigger Hold-Off (see Sec. **Dead time evaluation in CoMPASS**).

4.3 Supported Models

The following table lists the digitizer models supported by CoMPASS and able to run the DPP-PHA firmware:

Desktop Digitizer and MCAs	Description
DT5724(*)	4 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C4, SE
DT5724A(*)	2 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C4, SE
DT5724B	4 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C20, SE
DT5724C	2 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C20, SE
DT5724D(*)	4 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C4, SE
DT5724E(*)	2 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C4, SE
DT5724F	4 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, SE
DT5724G	2 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, SE
DT5725	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
DT5725B	8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
DT5725S	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
DT5725SB	8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
DT5730	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
DT5730B	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
DT5730S	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
DT5730SB	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
DT5781	Quad Digital MCA
DT5781A	Dual Digital MCA
DT5780SDM	Dual Digital MCA - 1 HVPS +500V/3mA, 1 HVPS -500V/3mA, 2 LVPS ±12V/100mA ±24V/50mA
DT5780SDN	Dual Digital MCA - 2 HVPS -500V/3mA, 2 LVPS ±12V/100mA, ±24V/50mA
DT5780SDP	Dual Digital MCA - 2 HVPS +500V/3mA, 2 LVPS ±12V/100mA, ±24V/50mA
DT5780M	Dual Digital MCA - 1 HVPS +5kV/300uA, 1 HVPS -5kV/300uA, 2 LVPS ±12V/100mA, ±24V/50mA
DT5780N	Dual Digital MCA - 2 HVPS -5kV/300uA, 2 LVPS ±12V/100mA, ±24V/50mA
DT5780P	Dual Digital MCA - 2 HVPS +5kV/300uA, 2 LVPS ±12V/100mA, ±24V/50mA
DT5780SCM	Dual Digital MCA - 1 HVPS +4kV/3mA, 1 HVPS -4kV/3mA, 2 LVPS ±12V/100mA ±24V/50mA
DT5780SCN	Dual Digital MCA - 2 HVPS -4kV/3mA, 2 LVPS ±12V/100mA, ±24V/50mA
DT5780SCP	Dual Digital MCA - 2 HVPS +4kV/3mA, 2 LVPS ±12V/100mA, ±24V/50mA
DT2740	64 Ch 16 bit 125MS/s Digitizer, Diff
DT2740B	64 Ch 16 bit 125MS/s Digitizer, SE
DT2745	64 Ch 16 bit 125MS/s Digitizer with Programmable Input Gain, Diff
DT2745B	64 Ch 16 bit 125MS/s Digitizer with Programmable Input Gain, SE
NIM Digitizer and MCAs	**Description**
N6724(*)	4 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C4, SE
N6724A(*)	2 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C4, SE
N6724B	4 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch,C20, SE
N6724C	2 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C20, SE
N6724F	4 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch,C20, SE
N6724G	2 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, SE
N6725	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
N6725B	8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
N6725S	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
N6725SB	8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
N6730	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE

N6730B	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
N6730S	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
N6730SB	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
N6780M	Dual Digital MCA - 1 HVPS +5kV/300µA, 1 HVPS - 5kV/300uA, 2 LVPS ±12V/100mA, ±24V/50mA
N6780N	Dual Digital MCA - 2 HVPS -5kV/300µA, 2 LVPS ±12V/100mA, ±24V/50mA
N6780P	Dual Digital MCA - 2 HVPS +5kV/300µA, 2 LVPS ±12V/100mA, ±24V/50mA
N6781	Quad Digital MCA
N6781A	Dual Digital MCA
VME Digitizer and MCAs	**Description**
V1724(*)	8 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C4, SE
V1724B(*)	8 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C4, SE
V1724C(*)	8 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C4, DIFF
V1724D(*)	8 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C4, DIFF
V1724E	8 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, SE
V1724F(*)	8 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, DIFF
V1724G	8 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C20, SE
V1725	16 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
V1725B	16 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
V1725C	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
V1725D	8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
V1725S	16 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
V1725SB	16 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
V1725SC	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
V1725SD	8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
V1730	16 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
V1730B	16 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
V1730C	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
V1730D	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
V1730S	16 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
V1730SB	16 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
V1730SC	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
V1730SD	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
V2740	64 Ch 16 bit 125 MS/s Digitizer, Diff
V2740B	64 Ch 16 bit 125 MS/s Digitizer, SE
V2745	64 Ch 16 bit 125 MS/s Digitizer with Programmable Input Gain, Diff
V2745B	64 Ch 16 bit 125 MS/s Digitizer with Programmable Input Gain, SE
VX1724(*)	8 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C4, SE
VX1724B(*)	8 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C4, SE
VX1724C(*)	8 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C4, DIFF
VX1724D(*)	8 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C4, DIFF
VX1724E	8 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, SE
VX1724F(*)	8 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, DIFF
VX1725	16 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
VX1725B	16 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
VX1725C	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
VX1725D	8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
VX1725S	16 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
VX1725SB	16 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
VX1725SC	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
VX1725SD	8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE

VX1730	16 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
VX1730B	16 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
VX1730C	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
VX1730D	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
VX1730S	16 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
VX1730SB	16 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
VX1730SC	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
VX1730SD	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
V1782	Octal Digital MCA
VX2740	64 Ch 16 bit 125 MS/s Digitizer, Diff
VX2740B	64 Ch 16 bit 125 MS/s Digitizer, SE
VX2745	64 Ch 16 bit 125 MS/s Digitizer with Programmable Input Gain, Diff
VX2745B	64 Ch 16 bit 125 MS/s Digitizer with Programmable Input Gain, SE
DPP-PHA Firmware	**Description**
DPP-PHA (8ch x724)	DPP-PHA - Digital Pulse Processing for Pulse Height Analysis (8ch x724)
DPP-PHA (4/2ch x724)	DPP-PHA - Digital Pulse Processing for Pulse Height Analysis (4/2ch x724)
DPP-PHA (16ch x725)	DPP-PHA - Digital Pulse Processing for Pulse Height Analysis for (16ch x725)
DPP-PHA (8ch x725)	DPP-PHA - Digital Pulse Processing for Pulse Height Analysis for (8ch x725)
DPP-SUP (16ch x725)	DPP-SUP - Super License for 16ch x725 Digital Pulse Processing
DPP-SUP (8ch x725)	DPP-SUP - Super License for 8ch x725 Digital Pulse Processing
DPP-PHA (16ch x730)	DPP-PHA - Digital Pulse Processing for Pulse Height Analysis (16ch x730)
DPP-PHA (8ch x730)	DPP-PHA - Digital Pulse Processing for Pulse Height Analysis (8ch x730)
DPP-SUP (16ch x730)	DPP-SUP - Super License for 16ch x730 Digital Pulse Processing
DPP-SUP (8ch x730)	DPP-SUP - Super License for 8ch x730 Digital Pulse Processing
DPP-SUP 2.0	DPP-SUP 2.0 - Super License for Digital Pulse Processing Digitizer 2.0 series

(*) The board is currently obsolete but still supported.

Tab. 4.1: CoMPASS supported CAEN boards for DPP-PHA firmware.

5 Software Interface

5.1 Introduction

The CoMPASS software is an application that manages the communication and the data acquisition from digitizers where a DPP firmware is installed. The software automatically detects the connected boards despite the communication interface, allows the user to set the DPP settings, displays the waveforms and histograms, and saves the data as it will be described in Sec. **GUI Description**.

5.2 System Requirements

In order to be able to install CoMPASS, the host station needs **Windows 10 or higher 64 bit OS or Linux 64 bit OS**.

In case of Linux OS please check the following:

- `getconf LONG_BIT` = 64
- `gcc -v` $\geq$ 11.4.0
- `g++ -v` $\geq$ 11.4.0
- `glibc -v` $\geq$ 2.34
- `glibcxx -v` $\geq$ 3.4.30

Alternately, it is possible to make use of the software manager Snap for Linux (refer to `https://snapcraft.io/`) for an automatic management of all the dependencies.

For additional details about the requirements and software installation refer to **[CompassQS]**

5.3 Block Diagram

The CoMPASS software block diagram is depicted in Fig. **5.1**. CoMPASS is composed by three main parts: the Graphic User Interface (GUI), the Server and the Plotter.

The GUI allows the user to easily scan and connect to the present hardware, set and optimize all acquisition parameters, to start/stop the acquisition, to set the spectra, to monitor the acquisition statistics and to save the data on the disk in several formats.

The server has the following mains functions:

- configures the digitizers according to the settings stored in a configuration file that the user modifies via the GUI;
- manages the acquisition from the digitizers;
- redirects the data streaming to the online processing and visualization algorithms;
- saves and process the board buffer data that can be used for a further offline run.

The Plotter provides:

- the visualization of Waveforms, time, energy, PSD, MCS and 2D scatterplot spectra;
- Energy calibration, zoom/pan, ROIs and filters definitions;

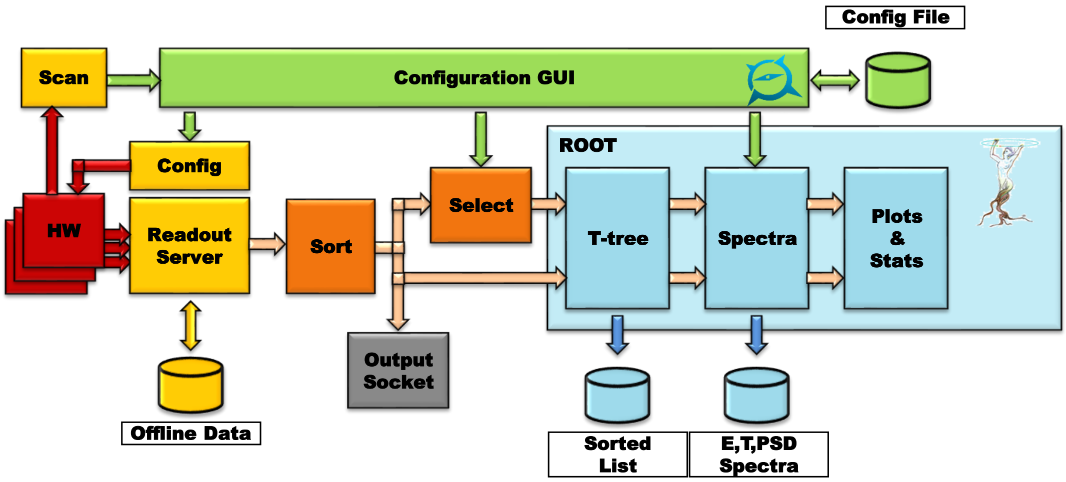


Fig. 5.1: CoMPASS block diagram.

- generation of Virtual channel(s) according to the specified criteria (AddBack,...)
- saves the histograms
- saves the list with different options:
  - One file per channel: there is one list file per channel which includes: Channel Number and Board ID in the file name, TimeStamp, Energy, Flags and optionally waveforms samples for each event;
  - Single file: there is one list file for the whole system which includes: Channel Number and Board ID in the file name, TimeStamp, Energy, Flags and optionally waveforms samples for each event. Such single file can be optionally saved already time sorted;
- import, sum and subtraction of previously saved spectrum;
- import and process of previously saved list files.

The acquisition software can also perform offline runs in which the data are coming from the raw files saved during the standard online run, and apply different filters to produce new spectra.

5.4 GUI Description

Note: Refer to **[CompassQS]** for a detailed description of the installation procedure both for Windows and Linux and to to **[Energy_time_compass]** for an example of mixed Energy/Time acquisition application.

When the CoMPASS software is launched, the following Initial Main Screen is displayed:

Fig. 5.2: CoMPASS Start window.

From the main panel of the CoMPASS software GUI (Fig. **5.2**) select

FILE -> New Project, or press the button 

A pop-up windows will appear asking the user to select the folder in which the project will be saved. Each project will include all the details about the involved boards and respective firmware and settings.

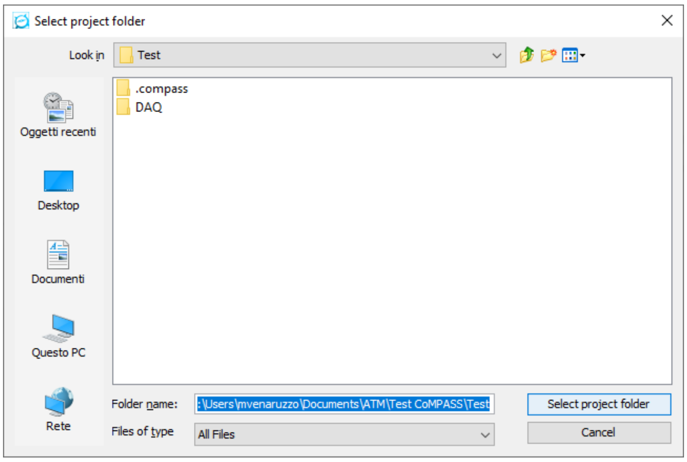


Fig. 5.3: CoMPASS New Project window.

Select an already existing folder or create a new one by pressing the button 

The following window will appear and allowing the user to choose whether to leave CoMPASS automatically scanning the all the active connection or to manually add the board(s).

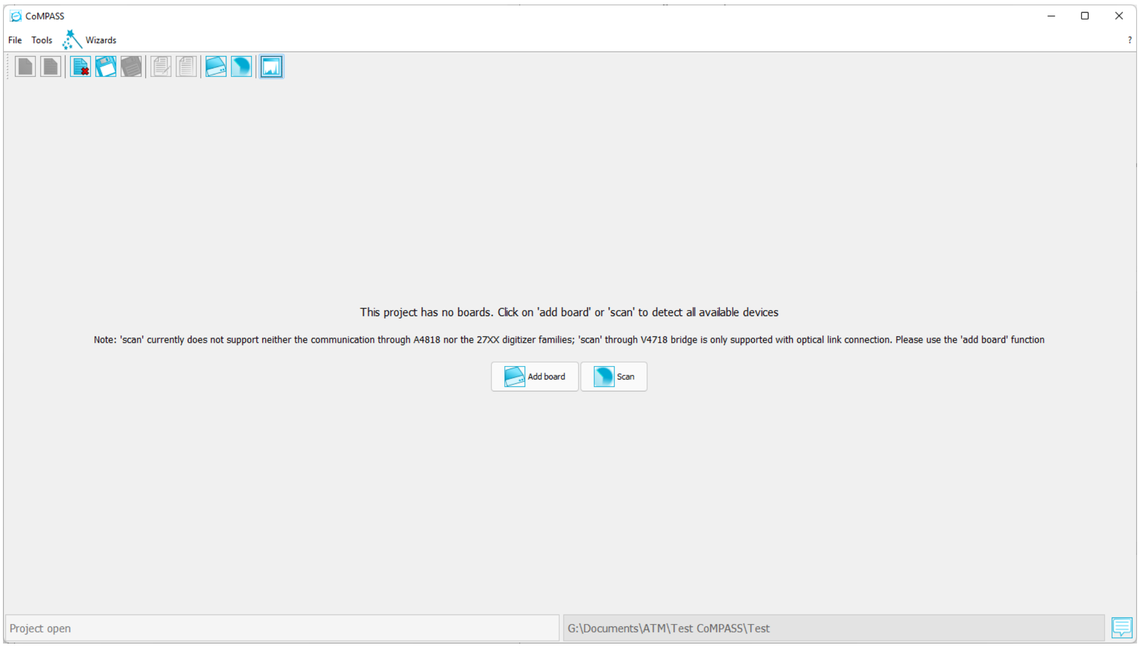
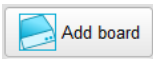


Fig. 5.4: CoMPASS Scan Tab.

Pressing the button  or the 

the user can add a single board manually providing the connection parameters. Press ok to do the connection to the board.

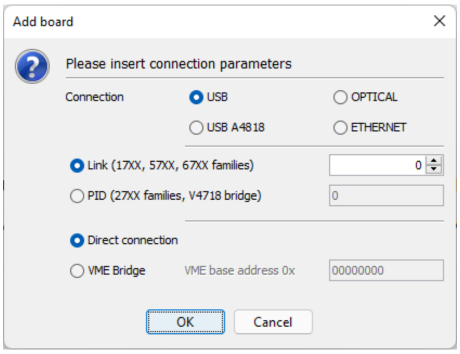
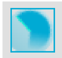
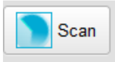


Fig. 5.5: CoMPASS Add Board window.

Note: When connecting to 27xx digitizer through the Ethernet connection, it is possible to use their hostname (CAEN-ETH-*PID*, where *PID* is the actual PID of the digitizer) instead of their IP address[**2740QuickStart**]. This option cannot be used in a point-to-point connection. In order to be able to use this option, the network in which the digitizer is connected has to provide a **DHCP and DNS** service. Check with your IT department that an 'A record' in your DNS server does exist and in case of any doubts.

Pressing the button  or the 

the user let CoMPASS search for all the active connection interfaces searching for the connected boards and automatically to the connection.

Note: Scan functionality is not supported for 27xx digitizer, for connection through the A4818 adapter and V/VX4718 bridge USB 3 and Ethernet connection and for the A5818 PCIe card.

After the scan/add has completed CoMPASS will show the detected board as different sub-tabs in the Acquisition and Settings tab (Fig. **5.6**, **5.7** and **5.8**).

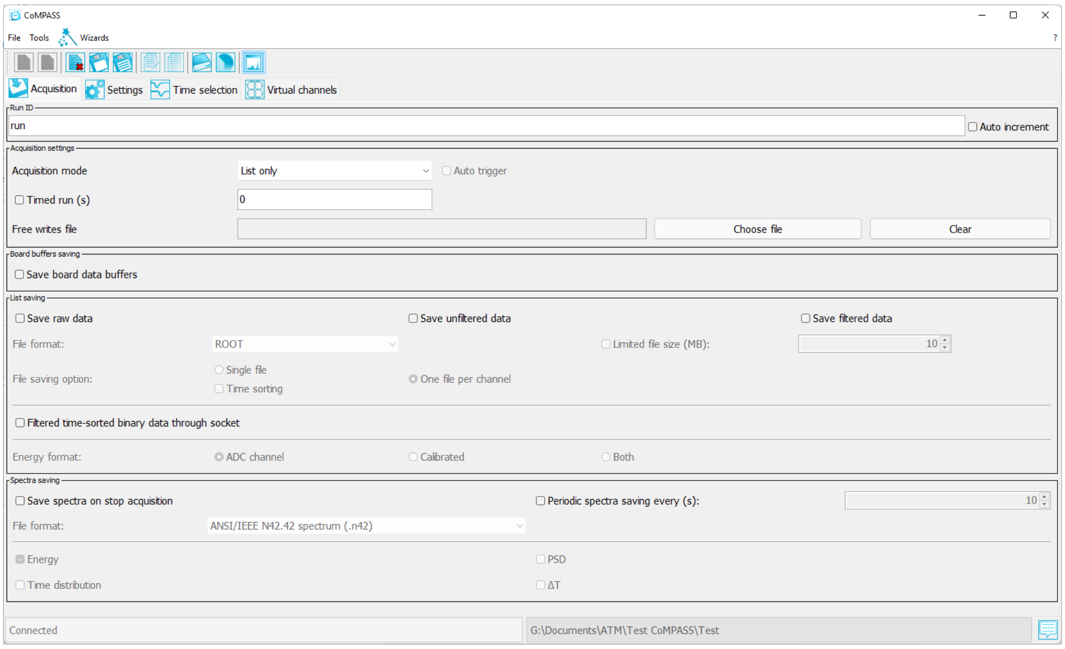


Fig. 5.6: CoMPASS Acquistion Tab.

5.4.1 Menu Bar Items

The menu bar is constituted by the following items: File, Tools, Wizards.

5.4.1.1 File

The pull-down Menu shows the following items: New Project/Open Project/Save Project/Save Project As/Close Project/Exit

- **New Project**: this function allows the user to start a new project (Fig. **5.3**). The user has to select the folder in which the project will be created and then press on the button "Select Project Folder". If the folder already contains a CoMPASS project a pop-up appears informing the user that can decide to overwrite the selected folder content or change it.

  Clicking Yes, CoMPASS will try to connect to the boards, while clicking No, CoMPASS will return to the starting window.
- **Open Project**
- **Save Project**

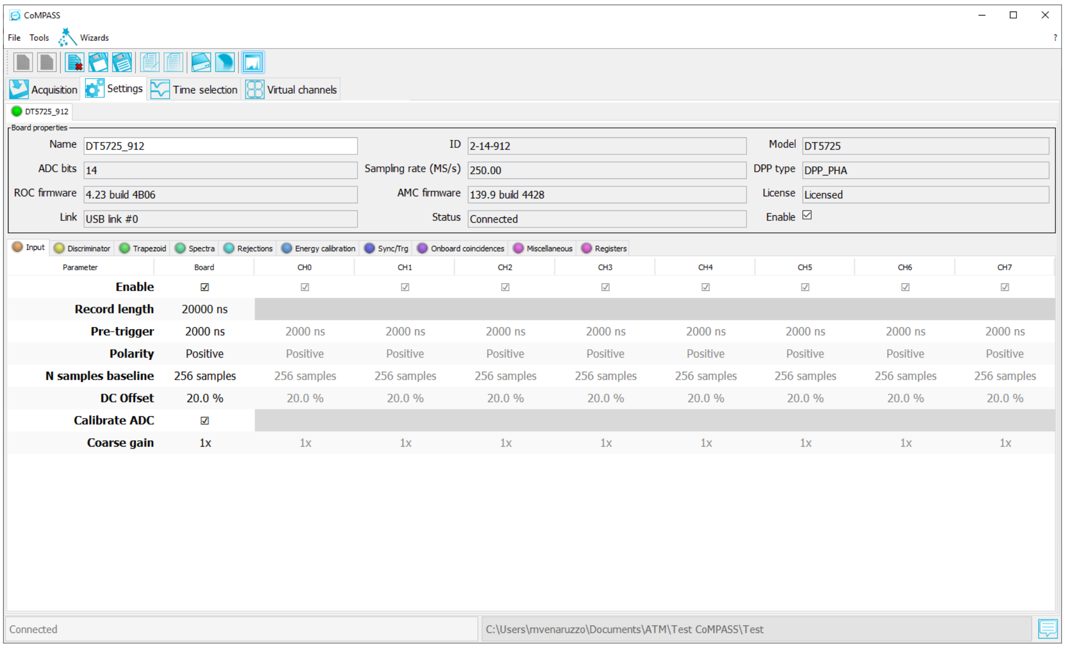


Fig. 5.7: CoMPASS Settings Tab.

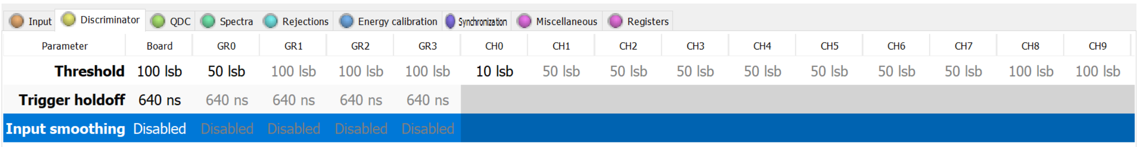
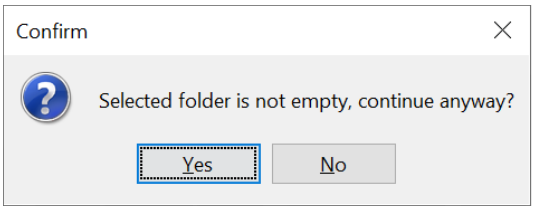
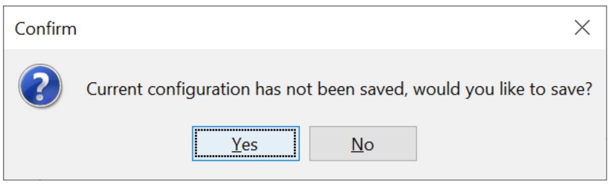


Fig. 5.8: CoMPASS Settings Tab in case of the x740D family.



- **Save Project As**
- **Close Project**: close the current project.
  If the configuration has not been saved, CoMPASS notifies the user asking for the action to do.



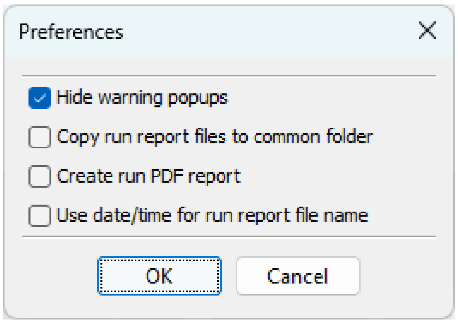
- **Save configuration file as**
- **Load configuration file**
- **Import**:
  - Import list: import a list not included in a CoMPASS Project folder

  - Import spectrum: import a spectrum not included in a CoMPASS Project folder
  - Sum energy spectra: import and sum a set of energy spectra from the same folder
- **Exit**: completely close CoMPASS

5.4.1.2 Tools

The pull-down Menu shows the following items:

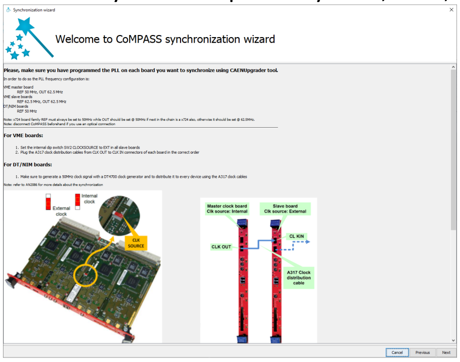
- **Application log**: this function allows the user to open the system log and check for possible errors or warning messages
- **Add Board**: this function allows the user to add a board to the project, providing manually connections parameters. The user has to press ”Connect” to connect to the board.
- **Scan**: this function allows the user to scan for the connected boards through all the interfaces supported by CAEN digitizers. Boards are automatically connected.
- **Show Plot/Hide Plot**: this function allows the user to open/close the CoMPASS plotter
- **Copy Board Configuration**: this function allows the user to copy all parameters values from a board to another
- **Energy Calibration**: this function allows the user to import/export energy calibration parameters for a single board channel or for an entire board
- **Select Language**: this section allows the user to change the CoMPASS language
- **Preferences**: this function allows to set some additional CoMPASS general settings. Specifically, the Preference section allows to:
  - Hide the Warning message pop-up
  - Copy run report file to a common folder
  - Create a run report in PDF format
  - Use date and time information for the run information and report file name



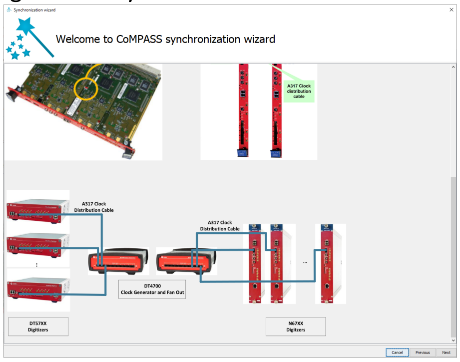
5.4.1.3 Wizards

The pull-down Menu shows the following items:

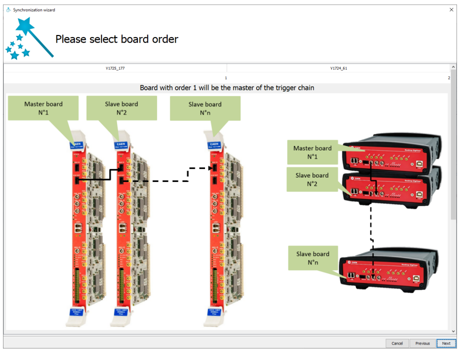
- **Synchronization wizard**: allows the user to configure the synchronization among multiple boards. Each page of the wizard guides the user throughout the configuration. In particular:
  - In case on a system composed by 17xx, 67xx, 57xx digitizers only:



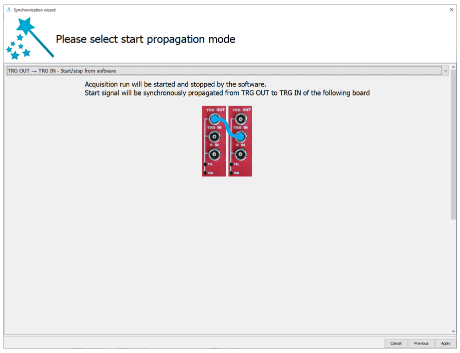
1



1a



2

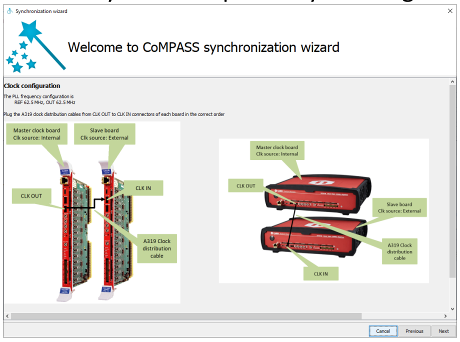


3

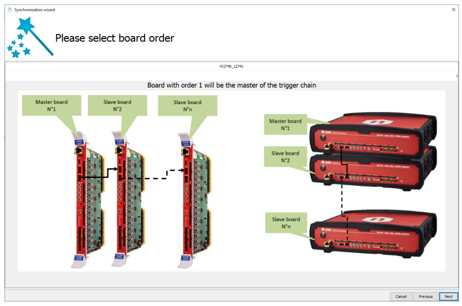
1. and 1a defines the steps to be done in advance to properly setup the system: i.e. program the PLL of the boards using the CAEN Toolbox, connect the clock cables, and set the dip switch ”Clock source” to EXT (VME boards) or enable the ”External clock source” (Desktop/NIM boards) from the Settings window, Sync/Trg tab.
2. select the board order, where 1 is the master.
3. select the desired start/stop acquisition modes:
   - GPO_TRGIN_AUTO (Desktop/NIM only), propagates the run through GPO to TRGIN front panel connectors. The start acquisition is automatically sent through the software command (press PLAY).
   - GPO_TRGIN_EXTERN (Desktop/NIM only), propagates the run through GPO to TRGIN front panel connectors. The start acquisition is done by the first trigger on the MASTER board and automatically propagated to the SLAVES.
   - TRGOUT_TRGIN_AUTO (VME only), propagates the run through TRG-OUT to TRGIN front panel connectors. The start acquisition is automatically sent through the software command (press PLAY).
   - TRGOUT_TRGIN_EXTERN (VME only), propagates the run through TRG-OUT to TRGIN front panel connectors. The start acquisition is done by the first trigger on the MASTER board and automatically propagated to the SLAVES.
   - TRGOUT_SYNCIN (VME only), propagates the run through TRG-OUT to S-IN front panel connectors. The run is synchronized with the level of an external signal on S-IN of the MASTER and propagated to the SLAVES.
   - GPO_GPI (Desktop/NIM only), propagates the run through GPO to GPI front panel connectors. The run is synchronized with the level of an external signal on GPI of the MASTER and propagated to the SLAVES.

A picture shows the cable connection for the run propagation

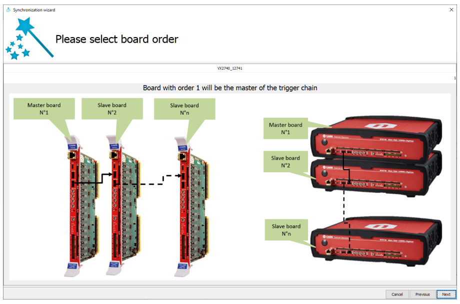
- In case of a system composed by 27xx digitizers only:



1



2



3

1. defines the steps to be done in advance to properly setup the system: i.e. connect the clock cables.

2. select the board order, where 1 is the master.

3. select the desired start/stop acquisition modes:

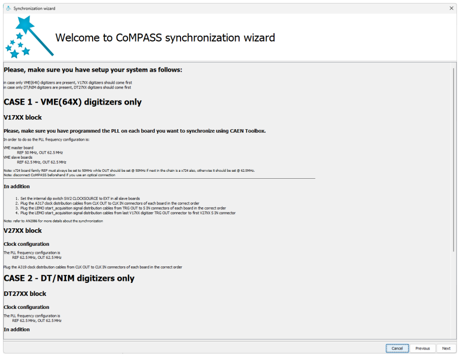
   - CLK_OUT → CLK_IN Start/Stop from software, propagates the clock and the run through CLK_OUT to CLK_OUT front panel connectors. The start and stop acquisition both provided by the software to the MASTER board and automatically propagated to the SLAVES.

   - CLK_OUT → CLK_IN Start from external pulse and Stop from software, propagates the clock and the run through CLK_OUT to CLK_OUT front panel connectors. The start acquisition is provided by an external pulse on the MASTER S_IN front panel connector and stop acquisition is provided by the software to the MASTER board. Both are then automatically propagated to the SLAVES.

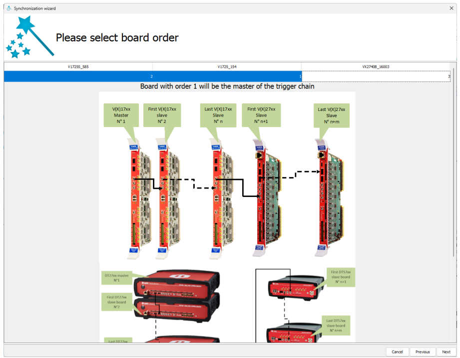
   - CLK_OUT → CLK_IN Start/Stop from external high level, propagates the clock and the run through CLK_OUT to CLK_OUT front panel connectors. The start and stop acquisition both provided by an external level sent to the MASTER S_IN front panel connector and automatically propagated to the SLAVES.

   A picture shows the cable connection for the run propagation

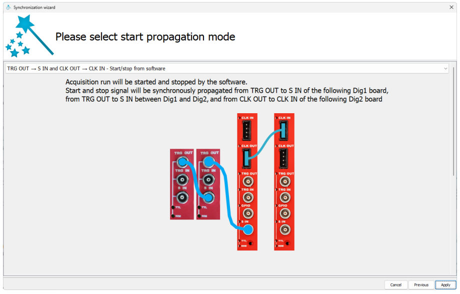
- In case of a system composed by all kind of digitizers:



1



2

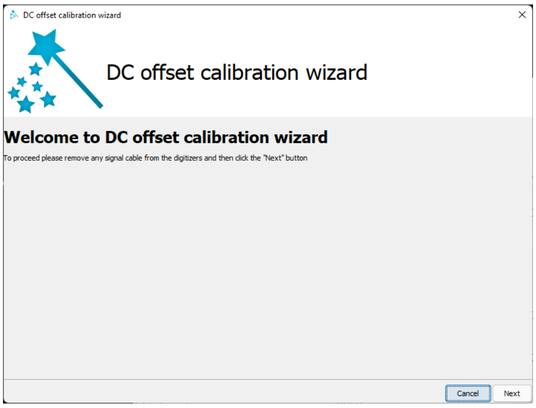


3

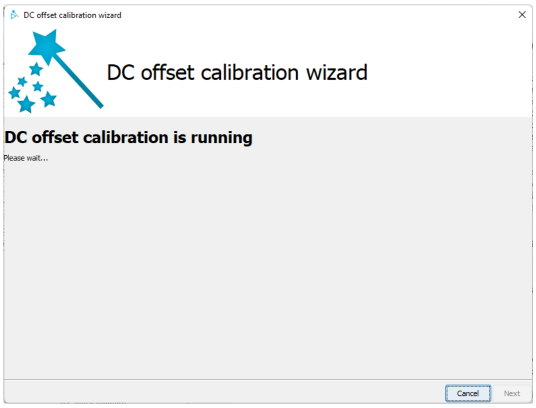
1. defines the steps to be done in advance to properly setup the system: i.e. connect the clock cables.
2. select the board order, where 1 is the master.
3. select the desired start/stop acquisition modes:
   - TRG_OUT → S_IN and CLK_OUT → CLK_IN Start/Stop from software. Acquisition run is started and stopped by the software; start and stop signal will be synchronously propagated from TRG_OUT to S_IN of the following Dig1 (digitizer generation 1) board, from TRG_OUT to S_IN between Dig1 and Dig2 (digitizer generation 2) and from CLK_OUT to CLK_IN of the following Dig2 board.
   - TRG_OUT → S_IN and CLK_OUT → CLK_IN Start from external pulse/Stop from software. Acquisition run is started on the rising edge of an external pulse on TRG_IN and stopped by the software; start and stop signal will be synchronously propagated from TRG_OUT to S_IN of the following Dig1 board, from TRG_OUT to S_IN between Dig1 and Dig2 and from CLK_OUT to CLK_IN of the following Dig2 board.
   - TRG_OUT → S_IN and CLK_OUT → CLK_IN Start from external high level/Stop from software. Acquisition run is started according to the high level of an esternal signal on S_IN; run signal will be synchronously propagated from TRG_OUT to S_IN of the following Dig1 board, from TRG_OUT to S_IN between Dig1 and Dig2 and from CLK_OUT to CLK_IN of the following Dig2 board.
   - CLK_OUT → CLK_IN and GPO → GPI Start/Stop from software. Acquisition run is started and stopped by the software; start and stop signal will be synchronously propagated from CLK_OUT to CLK_IN of the following Dig2 board, from GPIO to S_IN between Dig2 and Dig1 and from GPO to GPI of the following Dig1 board.
   - CLK_OUT → CLK_IN and GPO → GPI Start from external pulse/Stop from software. Acquisition run is started on the rising edge of an external pulse on and will be stopped by the software; start and stop signal will be synchronously propagated from CLK_OUT to CLK_IN of the following Dig2 board, from GPIO to S_IN between Dig2 and Dig1 and from GPO to GPI of the following Dig1 board.
   - CLK_OUT → CLK_IN and GPO → GPI Start from external high level/Stop from software.Acquisition run is started according to the high level of an esternal signal on S_IN; run signal will be synchronously propagated from CLK_OUT to CLK_IN of the following Dig2 board, from GPIO to S_IN between Dig2 and Dig1 and from GPO to GPI of the following Dig1 board.

   A picture shows the cable connection for the run propagation

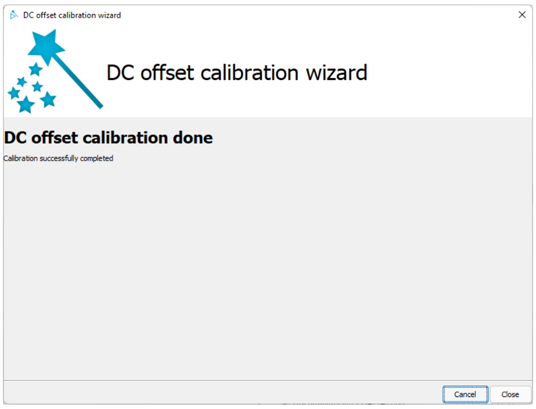
- **DC offset calibration wizard (17xx, 67xx, 57xx only)**: allows the user to perform the DC offset calibration and save the calibration into the project. The user must make sure that no input cable is fed into the input connectors. The DC offset calibration then proceeds automatically.



1



2



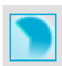
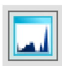
3

5.4.2 Icon Bar

The following Icon Bar is present under the MenuBar, where the different buttons are enabled/disabled depending on the process in progress

Fig. 5.9: CoMPASS Icon Bar.

The above icons implements the same function of the below listed Menu Bar commands (from left to right):

1. New Project : Menu Bar/ File / New Project
2. Open Project : Menu Bar/ File / Open Project
3. Close Project : Menu Bar/ File / Close Project
4. Save Project : Menu Bar/ File / Save Project
5. Save Project as :Menu Bar/ File / Save Project Project
6. Save Configuration File as : Menu Bar/ File / Save configuration file
7. Load Configuration File : Menu Bar/ File / Load configuration file
8. Add Board : Menu Bar/ Tools / Add Board
9. Scan : this icon allows the user to scan for connected boards
10. Show/Hide Plot : Menu Bar/ Tools / Show/Hide Plot

5.4.3 The System Information Bar

The System Information bar shows on the left side the **status** (connected of disconnected) of the boards included in the project and on the right side the **current project folder path**.

Fig. 5.10: CoMPASS System Information bar.

When Warning message popups are hidden, the user is in any case notified of their occurrence by the CoMPASS main GUI Information bar that becomes partially yellow on the left section and that show a notification triangle on the bottom left corner

Fig. 5.11: CoMPASS System Information with warnings.

Pressing on the  the user can open the System Log panel in the diagnostic messages provided by CoMPASS are included.

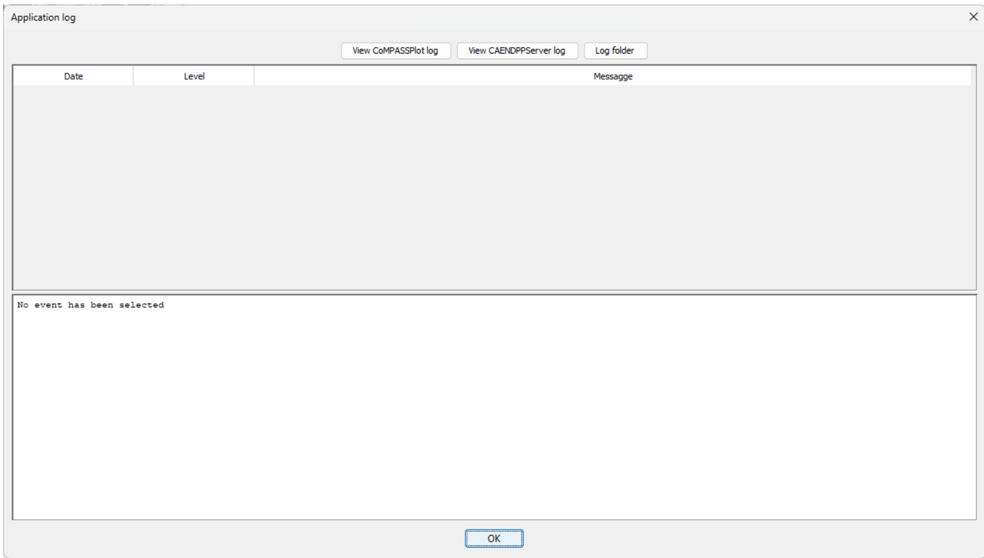


Fig. 5.12: CoMPASS System Log Windows.

The CoMPASS log files are stored at the following path:

- in Windows: C : \Users\ < USER_NAME > \AppData\Local\Compass\logs)
- in Linux: /home/ < USER_NAME > /Compass/logs

and can be accessed pressing on the ”Log Folder” button.

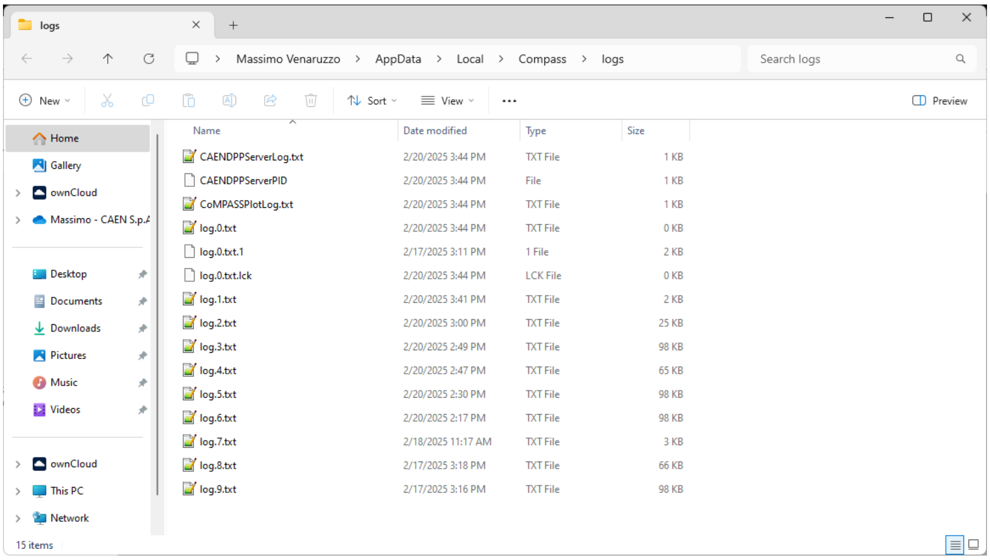


Fig. 5.13: CoMPASS Log Folder (Windows case).

5.4.4 The Acquisition Tab

The Acquisition Tab allows the user to set and view the global acquisition parameters.

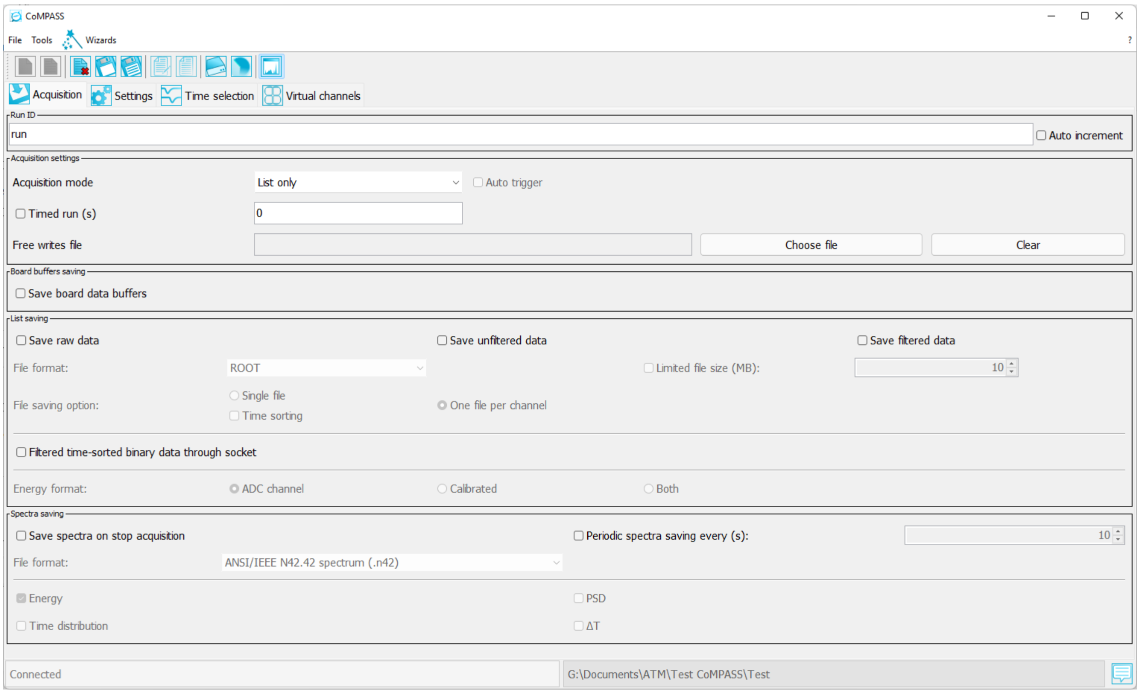


Fig. 5.14: CoMPASS Acquisition Tab.

The Acquisition Tab is divided into 5 different fields:

1. **Run ID**: in this field the user can write a custom run name and click on the Auto-Increment tick will let the software to add a progressive number that will be incremented at each start of run.
2. **Acquisition settings**: in this section the user can:

- select the **Acquisition Mode** (Waves or List)
- enable or disable the **Auto trigger** functionality by clicking on the corresponding tick. The Auto trigger is a software trigger sent at a frequency of 300 Hz. It works like the Force Trigger function of the oscilloscope. If enabled, it works in OR with the channels self-trigger and asynchronous with respect to it.
- enable or disable a **Timed run** and set the run duration
- include a FreeWrites file to make special board configurations using firmware register writes. It is possible to **Choose a file** or to **Clear** the settings if no longer required.

The **FreeWrites** file must be written according to the following formats:

(a) For V/VX17xx, DT57xx, N67xx digitizers:

- `boardID address value` (legacy)
- `boardID address value mask` (legacy)
- `boardID address value FirstBit LastBit` (legacy)
- `boardID address/mask value` (new)
- `boardID address/FirstBit-LastBit` (new)

where ”mask” corresponds to the bit/bits to be written, ”FirstBit” and ”LastBit” can be used when there are consecutive bits to be written.

(b) For 27xx digitizers:

- `boardID path value` (new)

Note: Writes must be done for individual addresses only, **do not** use the broadcast addresses.

Note: The writes operation performed by the **FreeWrites** are applied at the end of the configuration so they will not be overwritten.

For example:

(a) For V/VX17xx, DT57xx, N67xx digitizers:

i. (board ID = 2-14-967) to write register 0x810C equal to 0xC0000000 use the notation:
`2-14-967 0x810C 0xC0000000` (legacy)

ii. (board ID = 2-14-967) to set bit[12] = 1 of register 0x1080 either use the notation:
`2-14-967 0x1080 0x1000 0x1000` (legacy)
`2-14-967 0x1080 0x1 12 12` (legacy)

iii. (board ID = 2-14-967) to set bit[20:22] = 100 (bin) of register 0x1080 either use the notation:
`2-14-967 0x1080 0x400000 0x700000`(legacy)
`2-14-967 0x1080 0x4 20 22` (legacy)

iv. (board ID = 2-14-967) to set bit[12] = 1 of register 0x1080 either use the notation:
`2-14-967 0x1080 0x1000/0x1000`
`2-14-967 0x1080/0x1 12-12` (new)

v. (board ID = 2-14-967) to set bit[20:22] = 100 (bin) of register 0x1080 either use the notation:
`2-14-967 0x1080 0x400000/0x700000`
`2-14-967 0x1080/0x4 20-22` (new)

(b) For 27xx digitizers:

i. (board ID = 2-14-967) to set parameter GlobalTriggerSource use the notation:
`2-14-967 /par/GlobalTriggerSource SwTrg|TrgIn` (new)

Note: FreeWrites files do accepts comments provided that each comment is preceded by the special character #.

Note: The FreeWrites are loaded every time the acquisition is started and the write commands are executed at the end of the digitizer programming (settings might be overwritten by the FreeWrites commands).

Note: Legacy FreeWrites file format is still supported.

3. **Boards data buffers saving**: in this field the user can select if saving or not the boards data buffer (ie raw data from digitizer not even decoded by CoMPASS). Acquisition data are saved in a .cae proprietary format file. This file includes the whole acquisition dataset and allows the user to reprocess the entire acquisition changing the events selection parameters, if any.
4. **List saving**: Time, Energy, PSD and possibly waveform can be saved for each event in different file format for both unfiltered and filtered dataset. See the following section for more details.
5. **Spectra saving**: in this field the user can select if and which kind of spectra are saved both periodically and at the end of the acquisition. See the following section for more details.

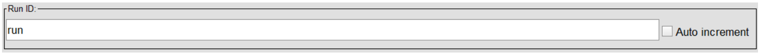
5.4.5 Data Saving Options

It is possible to save data in different ways:

1. Save the board data buffers data
2. Save the Energy, Time, PSD, ΔT and MCS spectra
3. Save the 2D PSD vs E, E vs E and ΔT vs E spectra
4. Save the list of Trigger Time Stamp, Energy, PSD and possibly waveform for each event
5. Save a picture of the Energy, PSD, Time, ΔT, Waveforms and 2D spectrum

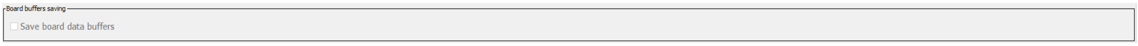
Select the run name and tick the ”Auto increment” box to increase the run index at every start acquisition.

All saved files are available in the project folder, under the ”DAQ\run” sub-folder. For each run, **run.info** and **settings.xml** files are saved, reporting general run information and the board settings respectively.



5.4.5.1 Save the board data buffer file

In order to save the board data buffer file the user must select the **”Save boards data duffer”** option tick into the Board buffers saving section of the Acquisition Tab.



The board data buffer file is saved into a proprietary file format and can be processed again performing an offline run where the user can run again the full acquisition possibly setting different data selection.

5.4.5.2 Save the list of Trigger Time Stamp, Energy, PSD and waveforms

In order to save a list file in which the Trigger Time Stamp, Energy, PSD and possibly waveform samples information are included, the user must select the **”Save raw data”** and/or **”Save unfiltered data”** and/or the **”Save filtered data”** tick into the List Saving section of the Acquisition Tab:

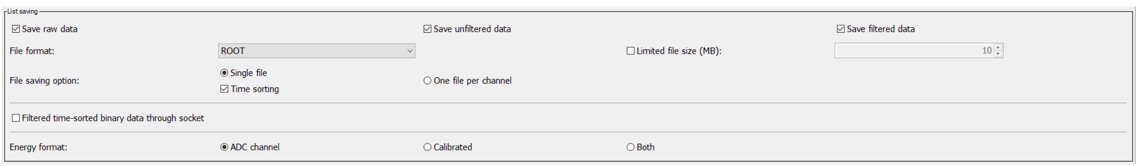
1. **Raw data** correspond to all the events acquired by the digitizer including pile-up and saturation events. Raw data are useful if the user would like to evaluate the acquistion dead time by his/her own (see Sec. **Dead time evaluation in CoMPASS**).
2. **Unfiltered data** correspond to the events acquired by the digitizer excluding pile-up and saturation events
3. **Filtered data** correspond to the events that passed the filters in the ”Rejection” tab of the Settings window and in the Time Selection tab (if any).

Per each of the above kind of data, the user has two possible choices:

1. save one file per each enabled channel: the file is generated for filtered and/or unfiltered data under the path ”DAQ\run\RAW/FILTERED/UNFILTERED”.
2. save one single file in which the data from all the enabled channels are included: the file is generated for filtered and/or unfiltered data under the path ”DAQ\run\RAW/FILTERED/UNFILTERED”. This single file can be *time ordered* if the option ”Time sorting” is selected.

The energy information can be saved in ADC channel, keV/MeV (in case of energy calibration), or both.

The user can also customize the maximum size of the list chunk file. As soon as the set size is reached, CoMPASS will automatically close the chunked file and open a new one.



The available file formats are root (.root), *Comma Separated Values* (.csv) and Binary (.bin).

1. In case of **.root** format, a TTree is generated with all the information. The TTree name is ”Data” and it contains the following TBranches:
   - Channel (Short)
   - Timestamp (Long Long Int)

- Board (Short)
- Energy (Short)
- EnergyShort (DPP-PSD case only) (Short)
- Flags (Integer)
- Probe (Integer)
- Samples (if enabled) (TArrayS)

2. In case of **.csv** format, the first row indicates the meaning of the subsequent values, which are:
    - PSD (+ waveform) = Time stamp, Energy, Energy short, Flags, (samples);
    - PHA (+ waveform) = Time stamp, Energy, Flags, (samples).

Note: The time stamp is expressed in ps and it has the following limits for all the supported digitizer families: $[0,2^{64}]$ ps.

3. In case of **.bin** format, the output file is represented as follows:

Header	(16 bit, 0xCAEx)
Board	(int, 16 bit)
Channel	(int, 16 bit)
Time Stamp (ps)	(int, 64 bit)

if bit 0 of the Header is 1:

Energy (ch)	(int, 16 bit)

if bit 1 of the Header is 1:

Energy (keV/MeV)	(double, 64 bit)

if both bit 0 and of the Header are 1:

Energy (ch)	(int, 16 bit) +	Energy (keV/MeV)	(double, 64 bit)

if bit 2 of the Header is 1, the following field is present:

Energy Short (ch)	(int, 16 bit)
Flags	(bit-by-bit, 32 bit)

if bit 3 of the Header is 1, the following fields are present:

Waveform code	(int, 8 bit)
Number of Wave samples to be read	(int, 32 bit)
Sample1 ... SampleN	(int, 16 bit each)

Note: In the **.bin** format, the Header is present just once at the beginning of the file and not in each event.

The **x** in the Header is:

- bit 0: if 1, Energy in Channels is present
- bit 1: if 1 ,Energy in KeV/MeV (according to the calibration) is present
- bit 2: if 1, Energy short is present
- bit 3: if 1, Waveform samples are present

Waveform codes are listed below:

1	Input
2	RC-CR (DPP-PHA firmware only)
3	RC-CR2 (DPP-PHA firmware only)
4	Trapezoid (DPP-PHA firmware only)
5	Baseline
6	Threshold
7	CFD (DPP-PSD firmware only)
8	Trapezoid-Baseline (DPP-PHA firmware only)
33	Fast Triangle (x27xx DPP-PHA firmware only)
41	Smoothed Input (DPP-PSD firmware only)

Flags are listed below:

0x1	A dead-time is occurred before this event (includes input stage saturation and board memory full conditions. x724 family DPP-PHA firmware release < 128.64 only.)
0x2	Time stamp roll-over
0x4	Time stamp reset from external
0x8	Fake event
0x10	A memory full is occurred before this event
0x20	A trigger lost is occurred before this event
0x40	N triggers have been lost (N can be set through bits[17:16] of register 0x1n84 in case of x725 and x730 family **[725_730PSD_Reg]** or through bits[17:16] of register 0x1nA0 in case of x724, x780, x781 and V1782 family **[724_781_782PHAReg][780PHAReg]**)
0x80	The event is saturating inside the gate (DPP-PSD) - The trapezoid is saturating (DPP-PHA)
0x100	1024 triggers have been counted
0x200	First event after a board busy condition
0x400	The input is saturating
0x800	N triggers have been counted (N can be set through bits[17:16] of register 0x1n84 in case of x725 and x730 family **[725_730PSD_Reg]** or through bits[17:16] of register 0x1nA0 in case of x724, x780, x781 V1782 family **[724_781_782PHAReg][780PHAReg]**)
0x1000	Event not matched in the time correlation filter
0x4000	Event with fine time stamp
0x8000	Piled-up event
0x80000	Identifies a fake event reporting a PLL lock loss
0x100000	Identifies a fake event reporting an over-temperature condition
0x200000	Identifies a fake event reporting an ADC shutdown

Note: When more than one of the listed condition applies to the same event, flags do sum up. For example a pile-up event in which input has saturated will be flagged as 0x8000 (pile-up event) + 0x400 (input is saturating), so flag will be 0x8400.

Here an example of how to read a binary list file in case of DPP-PSD (enabled options: ADC Channel and waveform with 56 samples):

```
DataR_CH0@DT5725_912_run.BIN
Offset 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10 11 12 13 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F 20 21 22 23 24 25 26 27 28 29 2A 2B 2C 2D 2E 2F 30 31
000000 ED CA 00 00 00 00 09 12 0B 4A 00 00 00 00 EF 00 32 00 00 40 00 00 01 38 00 00 00 1F 33 1D 33 1F 33 23 33 1D 33 1E 33 21 33 20 33 21 33 1E 33 1D 33 20
000050 33 21 33 1E 33 1E 33 1D 33 1E 33 1D 33 1D 33 1D 33 1D 33 1E 33 20 33 1E 33 16 33 1F 33 1E 33 1E 33 1B 33 1E 33 1D 33 20 33 1C 33 1E 33 1F 33 1D 33 20
000100 33 1D 33 1F 33 1F 33 1E 33 20 33 1D 33 1E 33 20 33 1F 33 20 33 1C 33 1E 33 21 33 1F 33 1C 33 1E 33 1C 33 1D 33 1F 33 00 00 00 00 2B 98 42 62 00 00 00
000150 00 FF 0F 00 00 80 40 00 00 01 38 00 00 00 20 33 1F 33 1E 33 1F 33 20 33 1E 33 1B 33 21 33 1C 33 1C 33 1E 33 1F 33 1F 33 1E 33 1F 33 1E 33 20 33 1C 33
000200 1E 33 1C 33 1F 33 1B 33 20 33 1E 33 16 33 1E 33 1C 33 20 33 20 33 1C 33 1F 33 1C 33 21 33 1E 33 1E 33 22 33 1D 33 1E 33 1E 33 20 33 1F 33 1D 33 1B 33
000250 1E 33 1B 33 20 33 1E 33 1F 33 1E 33 1C 33 1E 33 1C 33 23 33 1E 33 22 33 1E 33 00 00 00 00 65 8A 6F BD 00 00 00 00 FF 0F 00 00 80 40 00 00 01 38 00 00
000300 00 1E 33 1D 33 21 33 1C 33 1D 33 20 33 1F 33 1E 33 1E 33 1C 33 1D 33 1C 33 1F 33 20 33 1D 33 1B 33 1D 33 20 33 1C 33 1F 33 1C 33 20 33 1E 33 20 33 16
000350 33 1E 33 1F 33 22 33 1E 33 1C 33 20 33 1D 33 22 33 20 33 20 33 1D 33 1E 33 22 33 1E 33 1E 33 1E 33 1D 33 20 33 1E 33 22 33 1C 33 1F 33 20 33 1D 33 1D
000400 33 1D 33 1F 33 1D 33 20 33 1F 33 21 33 00 00 00 00 2A C2 EE D6 00 00 00 00 00 00 00 00 00 40 00 00 01 38 00 00 00 20 33 20 33 1F 33 21 33 20 33 1F 33
000450 20 33 20 33 1C 33 21 33 1C 33 1D 33 1D 33 1E 33 22 33 1E 33 1C 33 22 33 1F 33 1B 33 1C 33 1C 33 1D 33 1E 33 16 33 1E 33 1B 33 1E 33 20 33 1D 33 21 33
000500 18 33 1F 33 1D 33 1B 33 20 33 1C 33 1F 33 1F 33 1D 33 1D 33 1E 33 1E 33 1F 33 20 33 22 33 1B 33 1E 33 1E 33 1D 33 20 33 1E 33 1E 33 1C 33 20 33 1D 33
000550 00 00 00 00 43 F7 7C 44 01 00 00 00 00 00 00 00 00 40 00 00 01 38 00 00 00 1E 33 1F 33 20 33 1F 33 22 33 1F 33 21 33 1E 33 21 33 21 33 21 33 1D 33 20
```

where the colors correspond to:

- black = header = 0xCAED → Energy is in channels, Energy short and samples are present
- green = board = 0
- orange = channel = 0

- light blue= time stamp = 0x4A0B1209 = 1242239497 (dec) ps
- purple = ELong = 0xEF = 239 ch
- brown = Eshort = 0x32 = 50 ch
- red = flags
- yellow = number of samples = 0x38 = 56 (dec)
- pink = wave samples

After 56 samples data start again from board, channel, etc...

The user has also the possibility to access the filtered list files generated by CoMPASS through a socket and redirect them directly to his/her own post-processing code. The user just need to select the **"Filtered time-sorted binary data through socket"** to access this functionality. In the CoMPASS installation folder under the path

"C:\CoMPASS\demo" in Windows

and
"/CoMPASS-vX.Y.Z/demo in Linux"

a C demo code allowing the user to access the data through the socket is provided. The user can write his/her own code starting from this demo code.

The TCP/IP port used by CoMPASS is fixed and specified in the demo code. In case this port is already used by any other process, CoMPASS will automatically select another port and will specify it in the log files. The demo code will not work in this case and will exit notifying the refused connection. The user has then two possible solutions:

1. look into the CoMPASS log files to check the new port and replace the one written in the demo code;
2. restart the computer for an automatic re-assignment of the TCP/IP port.

5.4.5.3 Save the spectra

All the spectra can be saved choosing between two options:

- save selected spectra at the end of the run;
- save selected spectra periodically, with a programmable period (minimum is 0.1 s).

Both options can be checked together.
The available file formats are:

1. Energy spectrum
   - Single column spectrum (.txt)
   - 3 column spectrum (.txt3)
   - ANSI/IEEE N42.42 spectrum (.n42)
   - PC-Toolkit spectrum (.tka)
   - IEC 1455 spectrum (.iec)
   - IAEA spectrum data file (.spe)
   - JSON
2. PSD spectrum
   - Single column spectrum (.txt)

  - JSON
3. Time distribution spectrum
   - Single column spectrum (.txt)
   - 3 column spectrum (.txt3)
   - JSON
4. ΔT spectrum
   - Single column spectrum (.txt)
   - 3 column spectrum (.txt3)
   - JSON
5. 2D PSD vs E spectrum
   - Comma Separated Values (.csv)
   - JSON
6. 2D E vs E spectrum
   - Comma Separated Values (.csv)
   - JSON
7. 2D ToF vs E spectrum
   - Comma Separated Values (.csv)
   - JSON
8. MCS spectrum
   - Comma Separated Values (.csv)

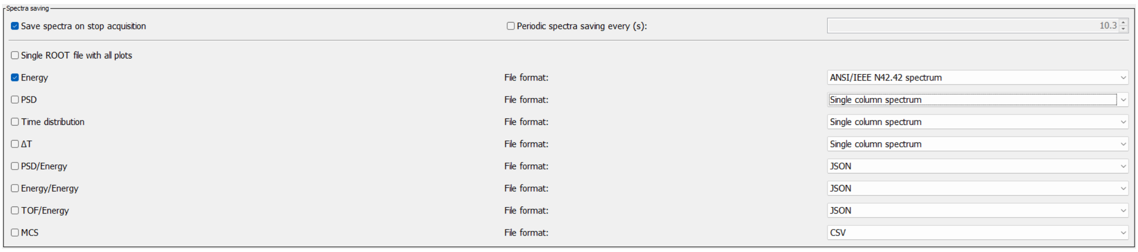
In the Energy three columns text file the order of the columns is: channel number, counts, energy (given as low edge of the calibrated histogram bin) and it includes the calibration parameters and the Real/Live time information.

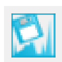
In the Time distribution three columns text file the order of the columns is: channel number, counts, time value (given as low edge of the histogram bin) and it includes Real/Live time information.

In the ΔT three columns text file the order of the columns is: channel number, counts, ΔT (given as low edge of the histogram bin) and it includes the Real/Live time information.

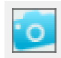
It is also possible, selecting the related option, to save all the spectrum in a single ROOT file.

One file for each enabled channel is generated for filtered and/or unfiltered spectra under the path ”DAQ\run \FILTERED/UNFILTERED”. If no cuts are applied to the spectrum, only the unfiltered one is saved.



The user can also save a spectrum ”on the fly” by pressing the  in the plot window. The spectrum is saved under the path ”DAQ\run\UNFILTERED” or ”DAQ\run\FILTERED” according to the format specified in the Acquisition Tab - Spectra Saving section.

5.4.5.4 Save an image of the energy, PSD, time, ΔT 2D spectrum and MCS graph

In order to save a picture of the energy, PSD, time and 2D spectrum, the user must press the button  in the plot window. The picture is saved in the .png format under the path ”DAQ\run\SCREENSHOTS”.

5.4.5.5 The run_name_info.txt file

At the end of each run, CoMPASS automatically saves a text file in which several useful information about the just completed run are included. The name of this file is the same as the run name (so it can be customized changing the run name in the Acquisition tab) to which a ”_info” suffix is added.

Such file includes the following infomation:

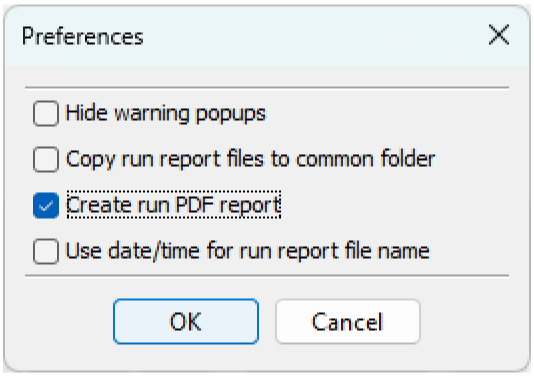
- the run ID
- the run start date and time
- the run stop date and time
- channel by channel:
  - Energy calibration coefficients and units;
  - Real time as hh:mm:ss.000;
  - Live time as hh:mm:ss.000;
  - Dead time as percentage;
  - Input counts and average rate (cps);
  - Pile up counts and average rate (cps);
  - Saturation counts and average rate (cps);
  - E cut (events rejected because of energy selection) counts and average rate (cps);
  - PSD cut (events rejected because of PSD selection) count sand average rate (cps);
  - T cut (events rejected because of time selection) counts and average rate (cps);
  - Singles (events rejected because not matching the time correlation selection) counts and average rate (cps);
  - Output counts and average rate (cps);
  - (DPP-PSD only) ”Particle 1 name” (events tagged as ”Particle 1 name”) counts and average rate (cps). ”Particle 1 name” can be specified by the user in the Particle ID tab;
  - (DPP-PSD only) ”Particle 2 name” (events tagged as ”Particle 2 name”) counts and average rate (cps). ”Particle 2 name” can be specified by the user in the Particle ID tab;

5.4.5.6 Report generation

CoMPASS allows the user to automatically generate a report of the current run at the end of the acquisition. In order to enable this funcionality, before staring the data acquisition run, select from the CoMPASS main menu Tool → Preferences. The Preferences popup will appear allowing the user to select the report generation option.

Report will be generated in PDF format and, for each of the enabled boards and channels will include:

- Board Information
- Run Start/Stop date and time
- Run statistics information
- Pictures of the spectra



The run report is saved within the specific run folder.

Selecting the option ”Copy run report file to a single folder”, CoMPASS will save all the PDF report files as well as the TXT run info files within the same folder that currently is

”C:\Users\<USER_NAME>\AppData\Local\Compass\data.

CoMPASS report generation functionality is still preliminary. Report format and content will be improved in the following releases.

5.4.6 The Settings Tab

The Settings Tab and the subtabs there included allows the user to set all the acquisition parameters at the board, group (x740D only) and single channel level. For each parameter, acting on the the "All" column, the modified setting will be applied to all the channel of the board, acting on the "GRn" columns, the modified setting will be applied to all the channel of the group n (x740D only), while acting on the "CHn" column the modified setting will be applied only to the selected channel.

Note: The group settings on "GRn" (x740D only) and the individual settings on "CHn" are not modified by the global setting on the "All" column.

In the following sections a detailed description of all the subtabs is provided.

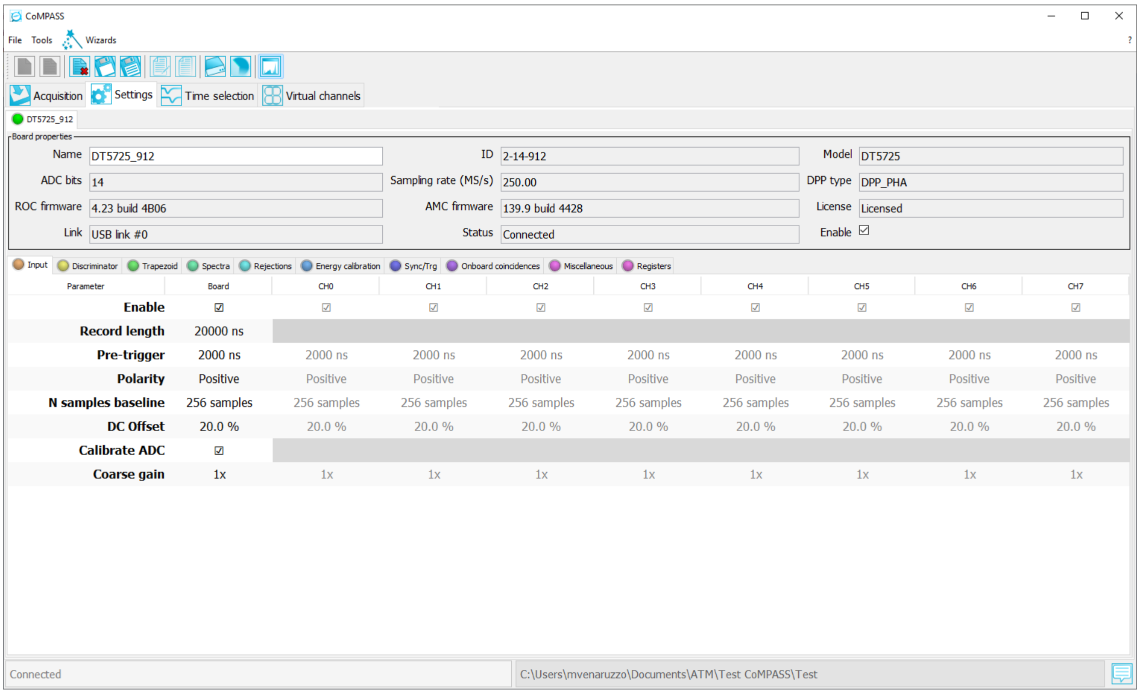


Fig. 5.15: CoMPASS Settings Tab.

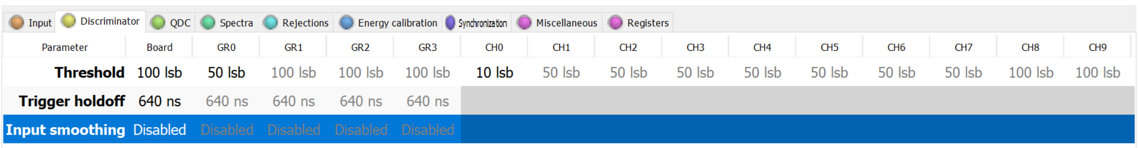


Fig. 5.16: CoMPASS Settings Tab in case of the x740D family.

In the top part of the Settings Tab, the **Board Properties** section includes as many tab as the number of connected boards. In each tab there are reported the "**Board properties**", like board ID and model, firmware type and release, DPP licence information, communication link used and the global board status.

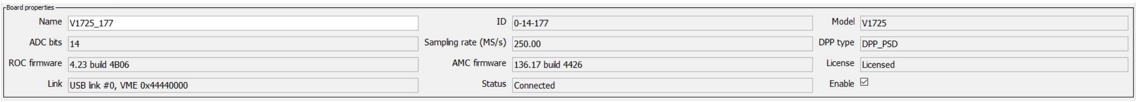


Fig. 5.17: Board Properties section in the Settings Tab.

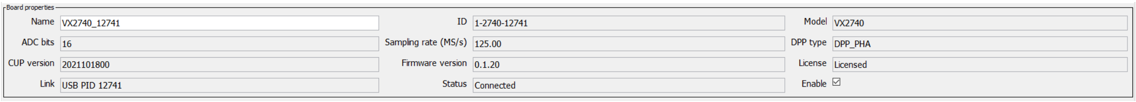


Fig. 5.18: Board Properties section in the Settings Tab for the 27xx digitizer family.

5.4.6.1 The HV Tab (x780 family and DT5790 Only)

The **HV Tab** is shown in Fig. **5.20**.

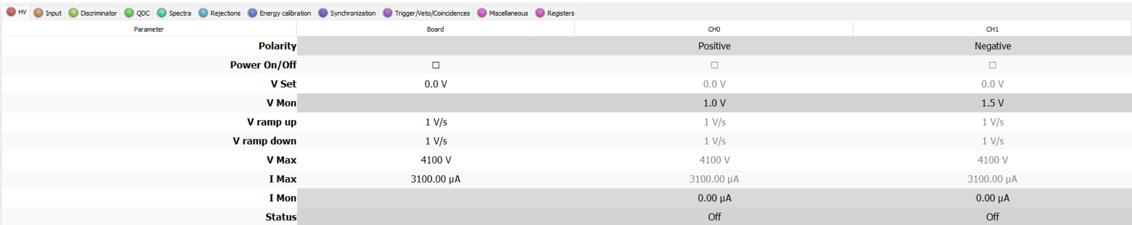


Fig. 5.19: CoMPASS HV Tab.

The **HV Tab** allows the user to check and operate on the High Voltage settings:

- **Polarity**: shows the HV channels polarity (read only)
- **Power On/Off**: to power on/off the HV channels
- **V Set**: sets the values of the voltage provided by the HV channels
- **V Mon**: shows the voltage value actually provided by the HV channels
- **V ramp up**: sets the speed (in V/s) of the voltage ramp up
- **V ramp down**: sets the speed (in V/s) of the voltage ramp down
- **V Max**: sets a software limitation of the maximum voltage that can be set in the VSet field
- **I Max**: sets the maximum allowed current value. If the HV channels are forced to provide more current, they go into the TRIP status and the voltage is switched off
- **I Mon**: shows the current value actually provided by the HV channels
- **Status**: shows the HV channels status (Off, On, Ramping up, Ramping Down, Trip)

5.4.6.2 The Input Tab

The **Input Signal Tab** is shown in Fig. **5.20**.

The **Input Signal Tab** allows the user to operate on the following hardware and firmware parameters:

- **Enable**: to enable or disable the channel(s) or the group(s) (x740D only)
- **Record Length**: selects the length of the acquisition window expressed in ns
- **Waveform Downsampling**: selects the waveform downsapling (ie how many waveform samples are saved: all, one every second, etc) (2740 and 2745 only).

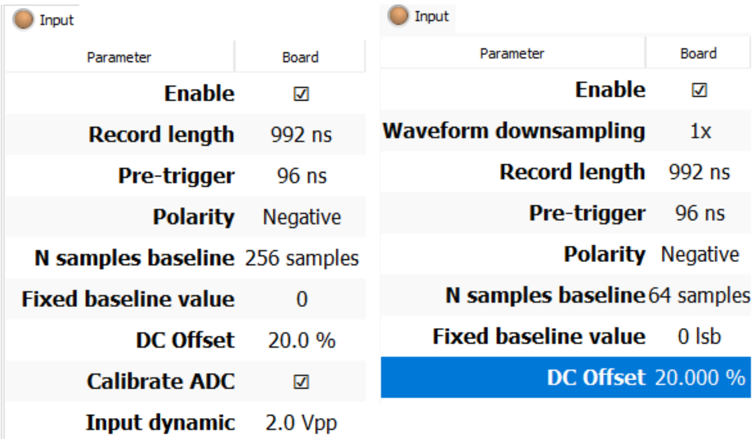


Fig. 5.20: CoMPASS Input Tab for a 17xx/57xx/67xx digitizer (left) and for a 27xx digitizer (right).

- **Pre-Trigger**: sets the portion of the waveform acquisition window to be saved before the trigger. Its value is expressed in ns.
- **Polarity**: selects the polarity (Negative/Positive) of the input signal to be processed by the DPP-PSD/PHA algorithm. In case of DPP-PHA firmware, the algorithm works with positive pulses only; by setting "Negative" the algorithm will invert the digital samples of the input and the input will always appear as positive in the waveform inspector.
- **N samples baseline**: sets the number of samples used by the mean filter to calculate the input pulse baseline. Allowed values are:
  - for the 720/DT5790 series: "Fixed", 8, 32, 128;
  - for the 724, 780, 781, V1782 series: "Fixed, 16, 64, 256, 1024, 4096, 16384;
  - for the 725 and 730 series (DPP-PSD): "Fixed", 16, 64, 256, 1024;
  - for the 725 and 730 series (DPP-PHA): "Fixed", 16, 64, 256, 1024, 4096, 16384;
  - for the 751 series: "Fixed", 8, 16, 32, 64, 128, 256, 512
  - for the 740D series: "Fixed", 4, 16, 64
  - for the 27xx series: "Fixed", 16, 64, 256, 1024, 4096, 16384

  The "Fixed" option enables the absolute baseline calculation and requires the definition of "**Fixed baseline value**" (the value of fixed baseline) in the GUI. In case of DPP-PHA "Fixed" means that the baseline is not evaluated.
- **DC Offset** sets the value of the DC Offset applied to the channel (to the group in case of the x740D series), expressed as the percentage of the Full Scale Range. Moving the DC Offset corresponds to moving the baseline level of the input signal upward or downward in the dynamic scale to cover the full width of the pulse itself, thus avoiding saturation. It is usually recommended to move the baseline upward for negative pulse, downward for positive signals. Mid-scale are fine for bipolar signals, or for small pulses. In case of saturation (both in the upper or lower limit) the algorithm stops any calculation.

  The ADC scale goes (from bottom to top) from 0 to 100% for positive polarity, and from 100% to 0 for negative polarity. 50% sets the signal baseline to mid-scale. It is also possible to calibrate the DC Offset to have the same value among different channels (refer to Sec. **Wizards**).
- **DC Offset correction** (x740D only): sets a fine correction, in LSB, of the DC Offset applied to the single channel.
- **Calib. ADC**: performs the calibration of the channel ADCs at every start acquisition (725, 730 and 751 series only). It is recommended to leave it enabled. The new x725S and x730S series do not require the ADC calibration.
- **Input dynamic/Coarse Gain**: select the digitizer input dynamic range/coarse gain. Options are:

- 0.5, 2 V_{pp} for 725 and 730 family;
- Gain x1, x3, x10, x33 (corresponding to 10Vpp-3Vpp-1Vpp-0.3Vpp ranges) for DT5781/N6781;
- Gain x1, x3, x7, x16 (corresponding to 9.5Vpp-3.7Vpp-1.4Vpp-0.6Vpp ranges)for DT5780/N6780;
- Gain x1, x2, x4, x8 for the V1782;
- not available for x720, DT5790, x724, x751 and x740D digitizer family;
- not available fro the 2740 family;
- Gain up to 40 dB in steps of 0.5 dB for the 2745 family.
- Gain up to 20 dB in steps of 1 dB for the 2730 family.

Note: When adjusting the DC Offset of a digitizer the user should keep in mind that the digitized samples are represented in a 0-(2^{Nbit}) LSB (least significant bit) scale (when Nbit is the number of bit of the digitizer ADC) but the digitizer input dynamic range scale is **not calibrated** and cannot be used as a reference for *absolute measurements* like a standard oscilloscope but just for *relative* ones (e.g. counting, timing, energy discrimination).
The 0-Volt level of the input signal does not correspond to the 0 in the ADC scale. The conversion from LSB to Volt (1 LSB = (Input dynamic range in Vpp)/2^{Nbit}) could be useful to check the relative difference between consecutive samples, but there might be small discrepancies between the "real" signal amplitude and what is observed in the waveform plot. In addition, there are also small differences in the DC offset among each channel: in absence of input signals and for a fixed DAC value programmed, the same value on each channel, few mV discrepancy are expected because of various effects, such as tolerances in offset and gain of the DACs regulating the DC Offset on the input stage of the ADCs, as there's not internal calibration (HW calibration) for that. A compensation for such effects can be done in the software if required.

Note: (V17xx, N67xx, DT57xx only) In CoMPASS the digitizer DC Offset can be calibrated with the dedicated Wizard. After such calibration, setting the same DC offset value in all the digitizer channel allows to have the baseline level in all of them.

Note: V27xx digitizer input dynamic range scale is **calibrated** and so can be used as a reference for *absolute measurements* like a standard oscilloscope.

While running in Waves mode, it is possible to plot two different waveforms, i.e. for example the Input and the Baseline. This possibility is called *dual trace*. When the dual trace is enabled, the samples of the two signals are interleaved, thus each waveform is recorded at half of the ADC frequency. When disabled only the Input is recorded at the ADC frequency. To disable this option for all the digitizer families, except the x751, it is sufficient to disable the second trace from plot by selecting the option **"None"**. In case of 751 family there is an additional field called **"Analog Traces Fine Resolution"**. The option "Analog Traces Fine Resolution" allows the user to visualize the first trace at full sampling.

Input

Parameter	Board
Enable	☑
Record length	996 ns
Pre-trigger	96 ns
Polarity	Negative
N samples baseline	256 samples
Fixed baseline value	0
DC Offset	20.000 %
Calibrate ADC	☑
Input dynamic	1.0 Vpp
Analog Traces Fine Resolution	☐

Fig. 5.21: CoMPASS Input Tab for 751 series.

Parameter	Board	GR0	GR1	GR2	GR3	CH0	CH1	CH2	CH3	CH4
Enable	☑	☑	☑	☑	☑	☑	☑	☑	☑	☑
Record length	1024 ns									
Pre-trigger	192 ns	192 ns	192 ns	192 ns	192 ns					
Polarity	Negative	Negative	Negative	Negative	Negative					
N samples baseline	64 samples	64 samples	64 samples	64 samples	64 samples					
Fixed baseline value	0 lsb	0 lsb	0 lsb	0 lsb	0 lsb					
DC Offset	20.0 %	20.0 %	20.0 %	20.0 %	20.0 %					
DC Offset correction	0 lsb	0 lsb	0 lsb	0 lsb	0 lsb	0 lsb	0 lsb	0 lsb	0 lsb	0 lsb

Fig. 5.22: CoMPASS Input Tab for 740D series.

5.4.6.3 The VGA Tab (2730 and 2745 family only)

The **VGA Tab** is shown in Fig. **5.23**.

Parameter	Board	VGA0	VGA1	VGA2	VGA3
Gain	0.0 dB	0.0 dB	0.0 dB	0.0 dB	0.0 dB

Fig. 5.23: CoMPASS VGA Tab (2730 and 2745 only).

It allows the user to operate on the 2730 and 2745 family Variable Gain Amplifier in steps of 1 dB up to 20 dB and in steps 0.5 dB up to 40 dB respectively. The gain is set individually for the 2730 and commonly to a group of 16 channels for the 2745.

5.4.6.4 The Discriminator Tab

The **Discriminator Tab** is shown in Fig. **5.24** (DPP-PSD only) and in Fig. **5.25** (DPP-PHA only).

Parameter	Board
Discriminator mode	Leading edge
Threshold	100 lsb
Trigger holdoff	1024 ns
CFD delay	6 ns
CFD fraction	75%
Input Smoothing	Disabled

Parameter	Board
Discriminator mode	Leading edge
Threshold	150 lsb
Trigger holdoff	296 ns
CFD delay	144 ns
CFD fraction	100%
Smoothing factor	4 samples
Charge smoothing	☐
Time filter smoothing	☐

Fig. 5.24: CoMPASS Discriminator Tab (DPP-PSD with CFD for 725, 730, and 751 series (left) and 27xx (right)).

Parameter	Board
Threshold	100 lsb
Trigger holdoff	480 ns
Fast Discriminator smoothing	4 samples
Input rise time	96 ns

Parameter	Board
Threshold	50 lsb
Trigger holdoff	1000 ns
Timing filter rise time	296 ns

Fig. 5.25: CoMPASS Discriminator Tab (DPP-PHA Only) for a 17xx/57xx/67xx digitizer (left) and for a 27xx digitizer (right).

The **Discriminator Tab** allows the user to operate on the following hardware and firmware parameters:

- **Discriminator mode** (DPP-PSD only): when available, sets the discriminator mode, Leading Edge or CFD;
- **CFD delay** (DPP-PSD only): when available, sets the CFD delay in ns;
- **CFD fraction** (DPP-PSD only): when available, sets the CFD fraction. Option are 25%, 50%, 75% and 100%;
- **Input smoothing/Smoothing Factor** (DPP-PSD and DPP-QDC only): the smoothing is a moving average filter, where the input samples are replaced by the mean value of the previous n samples. When enabled, the trigger is applied on the smoothed samples, thus reducing triggering on noise. Both CFD and LED triggering modes can be used on the smoothed input.
- **Charge smoothing (27xx only)**: allows to apply the Smoothing factor to the charge integration algorithm.
- **Time filter smoothing (27xx only)**: allows to apply the Smoothing factor to the Time filter algorithm.
- **Threshold**: The threshold value can be set from 0 to the Max Number of Channels (Bins) in LSB.
- **Trigger holdoff**: during the Trigger Hold-Off Time other trigger signals are not accepted by the digitizer. It can be set in ns;
- **Fast discriminator smoothing** (DPP-PHA only): the RC-CR^2 input signal second derivative smoothing value can be selected between 2, 4, 8, 16, 32 samples for 724-781-782 series; 2, 4, 8, 16, 32, 64, 128 samples for 725-730 series;
- **Input Rise Time** (DPP-PHA only): this is a value set to optimize the shape of the RC-CR^2 signal used to trigger the board channels. Maximum allowed value is 2.55 µsand 2 µsfor the 2740/2745 Triangular signal;
- **Fast Filter Rise Time** (DPP-PHA only, 27xx only): this is a value set to optimize the shape of the Triangular signal. Maximum allowed value is 2 µsfor the 2740/2745 Triangular signal.

5.4.6.5 The QDC/Trapezoid Tab

The tab corresponding to the energy calculation is called **QDC** for the DPP-PSD firmware (see Fig. **5.26**) and **Trapezoid** for DPP-PHA firmware (see Fig. **5.27**).

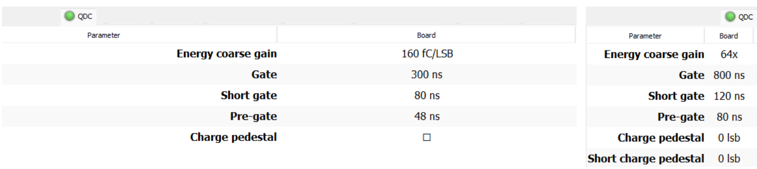


Fig. 5.26: CoMPASS QDC Tab for the x725, x730, x740D, x751 series (left) and for 274x series (right)(DPP-PSD Only).

The two tabs allow the user to evaluate the pulse energy, by means of a charge integration of the pulse inside a gate (DPP-PSD), or by means of a trapezoidal filter (DPP-PHA). The programmable parameters are the following:

- **Energy coarse gain** (DPP-PSD only): the Energy coarse gain allows to rescale the signal charge. This is useful especially when the charge exceeds the full-scale range. In the DPP-PSD case the energy coarse gain is given in the form of a charge sensitivity (fC/(LSB x V_{pp})) where V_{pp} is the Input Dynamic Range).The user sets the weight of the LSB for the charge data. For instance, if Q = 100 counts and Coarse Gain = 40 fC/LSB, the integrated charge is 4 pC. When the charge pulse exceeds the full scale range, it is recommended to reduce the "Energy coarse gain" in order to avoid saturation. The allowed values (fC/(LSB x V_{pp})) are:
  - for the 720 (DT5790) series: 40, 160, 640, 2560;
  - for the 725 and 730 series: 2.5, 10, 40, 160, 640, 2560;

Trapezoid

Parameter	Board
Trap. rise time	5.000 µs
Trap. flat top	1.000 µs
Trap. pole zero	50.000 µs
Peaking time	80.0 %
N samples peak	1 sample
Peak holdoff	0.960 µs
Energy fine gain	1.000

Fig. 5.27: CoMPASS Trapezoid Tab (DPP-PHA Only).

- for the 751 series: 20, 40, 80, 160, 320, 640;
- for the 740D series: 160, 320, 640, 1280, 2560, 5120, 10240;
- for the 27xx series: x1, x4, x16, x64, x256;

- **Gate** (DPP-PSD only): sets the gate width for the Energy and Q_{long} calculation. Values are expressed in ns and can vary in steps of clock units (i.e. 4 ns if 720 series and 725 series, 2 ns for 730 series, and 1 ns if 751 series);
- **Short gate** (DPP-PSD only): sets the short gate width for the Q_{short} calculation. Values are expressed in ns and can vary in steps of clock units;
- **Pre-gate** (DPP-PSD only): sets the "pre-gate" parameter, i.e. the starting position of the gate and short gate before the trigger signal. Values are expressed in ns and can vary in steps of clock units.

  Pre-gate and Pre-trigger must follow the relation:

  - For 720(DT5790) series

$$\mathrm{Pre-gate} \leq \mathrm{Pre-trigger} - 32\mathrm{ns} \tag{5.1}$$

  - For 725-730-274x series the firmware automatically adjusts wrong combinations of pre-gate and pre-trigger to the minimum allowed values.
  - For 751 series

$$\mathrm{Pre-gate} \leq \mathrm{Pre-trigger} - 8\mathrm{ns} \tag{5.2}$$

  - For the 740D series

$$\mathrm{Pre-gate} \leq \mathrm{Pre-trigger} - 112\mathrm{ns} \tag{5.3}$$

- **Charge pedestal** (x740D): when enabled a fixed value of 1024 is added to the charge. This feature is useful in case of energies close to zero.
- **Charge pedestal** (274x only): when enabled the fixed value set by the user is added to the charge. This feature is useful in case of energies close to zero. The user should note that the value set by the user is supposed to be on a 65K spectrum. In case of lower number of channel spectrum the value set by the user is accordingly automatically rescaled by the board firmware.
- **Short charge pedestal** (274x only): when enabled the fixed value set by the user is added to the charge. This feature is useful in case of energies short values close to zero. The user should note that the value set by the user is supposed to be on a 65K spectrum. In case of lower number of channel spectrum the value set by the user is accordingly automatically rescaled by the board firmware.
- **Trap. rise time** (DPP-PHA only): Allowed values for the Trapezoid Rise time are from 0 to 40.96 µs (10.20 µs in case of the legacy AMC firmware revision < 128.64) with 10 ns steps for 724, 780, 781 and V1782 series, from 0 to 8.184 µs with 8 ns steps for 730 series, and from 0 to 16.368 µs with 16 ns steps for 725 series, from 0.08 to 13 µs in steps of 8 ns for the 2740 and 2745 series.

- **Trap. flat top** (DPP-PHA only): Allowed values for the Trapezoid Rise time are from 0 to 40.96 µs (10.20 µs in case of the legacy AMC firmware revision < 128.64) with 10 ns steps for 724, 780, 781 and V1782 series, from 0 to 8.192 µs with 8 ns steps for 730 series, and from 0 to 16.384 µs with 16 ns steps for 725 series, from 0.08 to 3 µs in steps of 8 ns for the 2740 and 2745 series.

Note: the *sum of the Trapezoid Rise Time and Flat Top* should not exceed 40 µs (15 µs times the Decimation value in case of the legacy AMC firmware release < 128.64) for 724, 780, 781 and V1782 series, 16 µs times the Decimation value for 725 series, and 8 µs times the Decimation value for 730 series.

- **Trap. pole zero** (DPP-PHA only): The user can set the Trapezoid pole zero compensation from 0 up to 655.35 µs with 10 ns steps for 724, 780, 781 and V1782 series, from 0 to 524.280 µs with 8 ns steps for 730 series, and from 0 to 1048.560 µs with 16 ns steps for 725 series, from 0.08 to 524 µsin steps of 8 ns for the 2740 and 2745 series.
- **Peaking time** (DPP-PHA only): The user can set the Peaking time value from 0% to 100% in 0.1% steps, which corresponds to the percentage of the flat top duration;
- **Ns peak** (DPP-PHA only): The user can set how many Flat Top samples are used for the energy mean evaluation. Options are: 1, 4, 16, 64. For a correct energy calculation the Ns peak should be contained in the flat region of the Trapezoid Flat Top.
- **Peak holdoff** (DPP-PHA only): The user can set the Peak hold off time that defines how close must be two trapezoids to be considered piled-up.
- **Energy fine gain** (DPP-PHA only): The user can set the Energy fine Gain from x1 to x10.

5.4.6.6 The Spectra Tab

The **Spectra Tab** summarizes the number of channels and the limits of all the spectra that can be done with CoMPASS (see Fig. **5.28**).

Spectra

Parameter	All
Energy N channels	4096
PSD N channels	4096
Time intervals N channels	8192
Time intervals Tmin	0.000 µs
Time intervals Tmax	1000.000 µs
Start/stop Δt N channels	8192
Start/stop Δt Tmin	-10 ns
Start/stop Δt Tmax	20 ns
2D Energy N channels	512
2D PSD N channels	512
2D Δt N channels	512

Fig. 5.28: CoMPASS Spectr Tab.

Allowed values are

- **Energy N channels**: 256, 512, 1024, 2048, 4096, 8192, 16384, 32768 (the latter only for 2740 and 2745 series).

- **PSD N channels**: 1024, 2048, 4096, 8192, 16384.
- **Time Intervals/Start-Stop Δt N channels**: 256, 512, 1024, 2048, 4096, 8192.
- **2D Energy/2D PSD/2D Δt N channels**: 128, 256, 512, 1024.

Note: In the Δt histogram case the actual Tmax value might differ from the set one because the restriction related to the fact that each histogram bin must correspond to an integer number of ps must be respected.

5.4.6.7 The Rejection Tab

The **Rejection Tab** allows the user to apply filters on the histogram and select the corresponding events.

It is also possible to apply the cut directly on the plot by pressing the button 

A cursor will then become available and the user have to click on the histogram points that will be the ”Low Cut” and ”High Cut”.

To apply the cut the user have to press the button 

The allowed cuts are shown in Fig. **5.29**:

Rejections

Parameter	Board
Saturation rejection	☑
Pileup rejection	☑
PUR gap	1000 lsb
E low cut	0.000
E high cut	0.000
E cut enable	☐
PSD low cut	0.000
PSD high cut	0.000
PSD cut enable	☐
Time intervals low cut	0 ns
Time intervals high cut	0 ns
Time intervals cut enable	☐

Fig. 5.29: CoMPASS Rejection Tab.

- **Saturation rejection enable**: enable/disable the event rejection in case of saturation. Saturation is defined as:
  - saturation of the input dynamics;
  - (DPP-QDC and DPP-PSD only) saturation of the long gate, which means that the value of the total integrated charge exceeds the maximum value allowed by the firmware for the ”total charge” integration range (16-bit);
  - (DPP-PSD only) saturation of the short gate, which means that the value of the charge integrated over the short gate exceeds the maximum value allowed by the firmware for the ”short charge” integration range (15-bit);
  - (DPP-PHA only) saturation of the trapezoid, which means that the value of the trazpeid height exceeds the maximum value allowed by the firmware for the trapezoid heigth evaluation (15-bit);

  Saturation rejection is **enabled by default**;
- **PUR enable**: enable/disable the event rejection in case of pile-up. Pile-up rejection is **enabled by default**. Not supported by x740D series yet;

Note: When saturation and PUR rejection are enabled, the rejected events are discarded both from lists and spectra, even from the unfiltered data.

- **PUR gap**: the value (in LSB units) of the PUR gap for the pile-up identification. Refer to Sec. **Pile-up management (720, 725, 730, 2740, 2745, 2730 series)**.
- **Energy Low cut**: the value (in LSB or Energy units when the Energy calibration is performed - refer to Sec. **The Energy Histogram Icon Bar**) to use as a lower value for a user defined filter;
- **Energy High cut**: the value (in LSB or Energy units) to use as a higher value for a user defined filter;
- **Energy cut enable**: enable/disable the energy cut;
- **PSD Low cut**: the value (between 0 and 1) to use as a lower value for a user defined filter;
- **PSD High cut**: the value (between 0 and 1) to use as a higher value for a user defined filter;
- **PSD cut enable**: enable/disable the PSD cut;
- **Time intervals low cut**: the value (in ns) to use as a lower value for a user defined filter;
- **Time intervals high cut**: the value (in ns) to use as a higher value for a user defined filter;
- **Time intervals cut enable**: enable/disable the Time intervals cut;

5.4.6.8 The Energy Calibration Tab

The **Energy Calibration Tab** is shown in Fig. **5.30**.

Energy calibration	
Parameter	Board
C0	0.000
C1	1.000
C2	0.000
Calibration units	keV

Fig. 5.30: CoMPASS Energy Calibration Tab.

The **Energy Calibration Tab** allows the user to operate on the following commands:

- **C0/C1/C2**: the energy spectrum calibration parameters (Read-Only). The calibration panel and procedure will be described in the following paragraphs;
- **Calibration Units**: the energy spectrum calibration units (Read-Only). The calibration panel and procedure will be described in the following paragraphs;

5.4.6.9 The Synchronization Tab

The **Sync/Trg Tab** is shown in Fig. **5.31**.

The **Sync/Trg Tab** allows the user to operate on the following commands:

- **External clock source (DT/NIM only)**: enables the CLOCK IN front panel connector to receive an external clock. Options are: enabled/disabled.
- **Clock source (27xx only)**: allows to select the digitizer reference clock source (Internal or External from the Front Panel Input CLK_IN).
- **Output clock (27xx only)**: allows to have the digitizer propagating the reference clock on the on the front panel output CLK_OUT connector.
- **SyncOut signal (27xx only)**: allows select the source of the SyncOut signal to be progatated throughthe front panel output CLK_OUT connector. Options are:

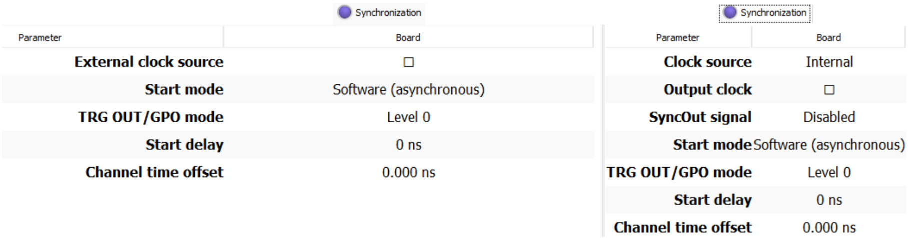


Fig. 5.31: CoMPASS Synchronization Tab for V17xx/N67xx/DT57xx digitizer (left) and 27xx digitizer (right).

  - **Disabled**: SyncOut is disabled.
  - **SyncIn signal**: SyncIn signal (if provided with reference clock on CLK_IN) connector.
  - **Internal Test Pulse**
  - **Internal clock**: Internal reference clock at 62.5 MHz.
  - **Run**: propagation of the RUN signal.

- **Start mode**: decides how the acquisition is started/stopped.
  For the V17XX, DT57XX, N67XX digitizers, options are:
  - **Software (asynchronous)**: start/stop commands are made via software by pressing the relative buttons. In case of multiple boards, the start/stop command is not synchrounous among the boards.
  - **S_IN/GPI controlled**: the acquisition is synchronized with an external signal level on the S_IN (GPI in case of Desktop/NIM form factors) front panel connector.
  - **First TRG controlled**: the acquisition starts on the first trigger received by the board and stops on the software command.

  For the V27XX, DT27XX digitizers, options are:
  - **Software (asynchronous)**:start/stop commands are made via software by pressing the relative buttons. In case of multiple boards, the start/stop command is not synchrounous among the boards.
  - **CLK_IN signal**: Start from CLK_IN/SYNC connector on the front panel.
  - **S_IN/GPI high level**: Start from S_IN (1=run, 0=stop).
  - **S_IN edge**: Start from S_IN (rising edge = run; stop from SW).
  - **S_IN/GPI controlled**: the acquisition is synchronized with an external signal level on the S_IN front panel connector.
  - **LVDS**: Start from LVDS.
  - **P0 backplane**: Start from P0 backplane.
- **TRG OUT mode (V17XX, DT57XX, N67XX digitizers only)**: decides which signal is propagated to the TRG-OUT (GPO in case of Desktop/NIM form factors) front panel connector. Options are:
  - **0 level test signal**: propagates a low-level test signal.
  - **1 level test signal**: propagates a high-level test signal.
  - **External Trigger**: propagates the external trigger.
  - **Software Trigger**: propagates the software trigger.
  - **Global ch. OR**: propagates the logical OR of the channels self trigger
  - **Run**: propagates a signal which is high when the acquisition is on.
  - **Delayed Run**: propagates a signal which is high when the acquisition is on, delayed by an amount of time specified in the Start Delay field.
  - **Sampling clock**: propagates a signal which is synchronous with the sampling clock of the ADCs.
  - **PLL clock**: propagates a signal which is synchronous with the PLL clock.
  - **Busy**: propagates a signal which is synchronous with the busy.

- **User**: from DPP-PHA release 2023112703 this option propagates the OR of the channel self trigger.
- **PLL lock loss**: propagates a signal which identifies a PLL lock loss.
- **Virtual Probe**: propagates signal probes from channels.
- **S-IN**: propagates the signal from S-IN (GPI) front panel connector.

- **GPO Mode (V27XX, DT27XX digitizers only)**: decides which signal is propagated to the TRG-OUT/GPIO front panel connector. Options are:

  - **Trigger In**: propagates the Front Panel TRGIN (TRGOUT is a replica, with some delay, of the TRGIN signal).
  - **P0 trigger**: propagates the P0 trigger (not implemented yet).
  - **Software Trigger**: propagates the Software trigger.
  - **LVDS mode**: propagates the LVDS trigger in signal .
  - **ITLA Internal Trigger Logic A**: propagates the combination of channel self-triggers according to the combination specified in the parameter ITLAMainLogic (see the 27xx DPP firmware parameters description section in the 27xx digitizer Web Interface).
  - **ITLB Internal Trigger Logic B**: propagates the combination of channel self-triggers according to the combination specified in the parameter ITLBMainLogic (see see the 27xx DPP firmware parameters description section in the 27xx digitizer Web Interface).
  - **ITLA_AND_ITLB**: propagates the second level Trigger logic signal making the AND of ITL A and B.
  - **ITLA_OR_ITLB**: propagates the second level Trigger logic signal making the OR of ITL A and B.
  - **Sampling clock** Propagation of the Encoded CLK-IN trigger (not implemented yet)
  - **Run** Propagation of the RUN signal (acquisition start/stop), before applying the delay given by the Srat Delay parameter.
  - **PLL Clock**: propagates the 62.5 MHz reference clock signal (to be used for phase alignment)
  - **Test Pulse**: propagates the Internal Test Pulse signal according to the settings specified in the TestPulsePeriod and TestPulseWidth parameters (see see the 27xx DPP firmware parameters description section in the 27xx digitizer Web Interface).
  - **Busy signal**: propagates the Busy signal of the board.
  - **Logical level '0'**: propagates a low-level test signal.
  - **Logical level '1'**: propagates a high-level test signal.
  - **Sync In**: propagates the SyncIn signal.
  - **S IN**: propagates the input signal on the S IN front panel connector.
  - **GPIO (Trg Out only)**: propagates the input signal on the GPIO front panel connector.
  - **Trigger (Trg Out only)**: propagates the OR of the accepted Triggers signal.
  - **Trigger Clock (Trg Out only)**: propagates the Trigger Clock signal.

- **Start delay**: sets the delay between master and slaves in case of multi-board synchronization.
- **Channel time offset**: sets a time offset for the board channels. This option can be used for fine adjustment of the delay in case of multi-board synchronization.

5.4.6.10 The Trigger/Veto/Coincidences Tab

The **Trigger/Veto/Coincidences Tab** is shown in Fig. **5.32**.

Note: Onboard coincidences can be set for single boards only. In case of multiple boards, each board can have its own coincidence logic. See also Sec. **The Time Selection Tab**.

Note: Trigger/Veto/Coincidences tab is not available for x740D series.

For V17xx/DT57xx/N67xx digitizers, the **Trigger/Veto/Coincidences Tab** allows the user to configure the following on-board coincidence types:

Trigger/Veto/Coincidences

Parameter	Board
Coincidence Mode	Disabled
Coincidence window	100 ns

Trigger/Veto/Coincidences

Parameter	Board
Veto source	Disabled
Veto polarity	Active high (inhibit)
Veto width	0 ns
Ch trigger mask enable	☐
Ch trigger mask	0x00000000
Coincidence Mode	Disabled
Coincidence window	0 ns

Fig. 5.32: CoMPASS Trigger/Veto/Coincidences Tab for V17xx/N67xx/DT57xx digitizer (left) and 27xx digitizer (right).

Note: Only events passing the coincidence criteria are acquired by the board, while events not passing the criteria are discarded. This might imply a significant data throughput reduction. Using the settings in **The Time Selection Tab** both filtered and unfiltered events are saved with no throughput reduction.

- **Paired AND**: events are acquired when they are in logic AND between couples of channels. The coincidence logic is: (Ch0 & Ch1), (Ch2 & Ch3), etc.;
- **Ch0 AND any**: All channels acquire in logic AND with Ch0, while Ch0 acquires events in logic OR with the other channels. The coincidence logic is: (Ch0 & Ch1) || (Ch0 & Ch2) || etc.;

  Note: In case of the x725 and x730 families, due to hardware limitations, this mode requires the Ch1 to be disabled. The coincidence logic is then: (Ch0 & Ch2) || (Ch0 & Ch3) || etc.;

  Note: In case of single digitizer board, for the correct functioning of this option, Ch_ref_and_any from Time Selection tab **MUST** be enabled too, choosing Ch_ref = Ch0 and setting the same Coincidence window. If not, some not coincidence events might occur in Ch0 and in the corresponding list file (if saved).

- **Ch0 veto**: Ch0 acquires events with its own self-trigger, while the other channels acquire events in anti-coincidence with Ch0, i.e. Ch0 acts as a veto for the other channels.
- **TRG IN level veto** (first generation digitizer only): the TRG IN signal acts as a veto for all the board channels. The acquisition veto is synchronized with the whole duration of the TRG IN signal. The Coinc. Window field is not used.
- **TRG IN level gate** (725/730 series only): the TRG IN signal acts as a gate for all the board channels. The acquisition gate is synchronized with the whole duration of the TRG IN signal. The Coinc. Window field is not used.
- **Trigger mode** (x740D only): decides how the acquisition is started/stopped. Options are:
  - **Independent**: each channel can "self-trigger" on its own input signal when the input crosses a programmable threshold. The self-trigger works on each channel independently from the other channels;
  - **Paired**: each channel can both acquire on its own self-trigger and on the self-trigger of the paired channel. Pair "n" corresponds to channel n and channel n+2.

In the field **Coinc. Window** it is possible to write the desired coincidence time window.

For V27xx/DT27xx digitizers, the **Trigger/Veto/Coincidences Tab** allows the user to configure:

1. the board VETO (if any), setting the following parameters:
   - the **Board veto source**: the front pannel S IN or GPIO connector;
   - the **Board veto polarity**: Active High (Inhibit) or Active Low (Gate);
   - the **Board veto width**: the veto signal width. 0 means that the VETO width is the width of the external signal.

2. the Channel Trigger Mask ie the mask over 64 bits to generate a channel trigger. It can be used to trigger a channel using a trigger coming from another channel. The following parameters cna be set:
    - **Ch trigger mask enable**
    - **Ch trigger mask high**: 32-bit enable mask (for Ch 32-63), each bit representing a channel;
    - **Ch trigger mask low**:32-bit enable mask (for Ch 0-31), each bit representing a channel;

5.4.6.11 The Particle ID Tab (DPP-PSD only)

The **Particle Tab** is shown in Fig. **5.33**.

Particle ID

Parameter	Board
Label (below threshold)	Gamma
Label (above threshold)	Neutron
PSD threshold	0.000

Fig. 5.33: CoMPASS Particle ID Tab.

The **Particle Tab** allows the user to set a PSD threshold for counting **(and not rejecting)** events whose PSD value is above or below the set threshold. The user can also modify the label corresponding to the particle name to adapt it to the specific requirements.

This counting procedure is applied on the Output counts so on those events already passing any other possible user's defined event selection (including the PSD one). The user should indeed take into account that, while the PSD selection is done setting a selection area and rejecting all the events outside of that area (see section **How to set Energy, PSD and Time selections** in the CoMPASS Quick Start Guide), this particle ID counting is done using a fixed dicrimination threshold. In order to reject all the event of one kind and count only the event of the other one, the user should take the PSD threshold value of this tab as the starting/end point of the PSD event selection done through the procedure explained in the CoMPASS Quick Start Guide.

5.4.6.12 The Miscellaneous Tab

The **Miscellaneous Tab** is shown in Fig. **5.34**.

Miscellaneous

Parameter	Board	CH0	CH1	CH2
Label	CH	CH	CH	CH
FPIO type	NIM			
Rate optimization	511			
ADC temperature		43 °	43 °	43 °

Miscellaneous

Parameter	Board
Label	CH
FPIO type	NIM
Rate optimization	65536
First ADC temperature	34 °
Last ADC temperature	43 °
FGPA core temperature	56 °
DC/DC converter temperature	36 °

Fig. 5.34: CoMPASS Miscellaneous Tab.

The **Miscellaneous Tab** allows the user to operate on the following commands:

- **Label**: writing in this field the user can customize the channel label;
- **FPIO type**: the user can select the signal type of the front panel I/O. Options: NIM, TTL.
- **Rate optimization**: in case of low input rate (typ. < 100 Hz) it is required to set it to smaller value to optimize the throughput. In Waves mode CoMPASS automatically evaluates the appropriate value.
- **ADC temperature**: temperature of each channel ADC (x725, x725S, x730, x730S only)
- **First ADC temperature**: temperature of the first digitizer ADC (x27xx only)

- **Last ADC temperature**: temperature of the last digitizer ADC (x27xx only)
- **FOGA Core temperature**: temperature of the FPGA (x27xx only)
- **DC/DC converter temperature**: temperature of the DC/DC converter (x27xx only)

5.4.6.13 The Register Map Tab (17xx, 67xx, 57xx only)

The **Register Map Tab** is shown in Fig. **5.35**.

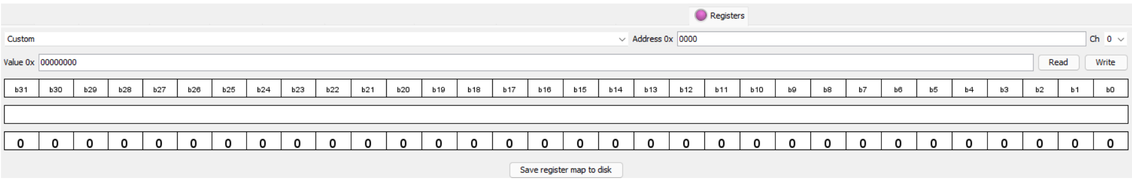


Fig. 5.35: CoMPASS Register Map Tab.

The **Register Map Tab** allows the user to operate directly on the firmware registers. The user can select the desired register in the top left combo box, as well writing the corresponding **Address** value. The channel number (if required) can be selected in the **Ch** field.

If the register has a Read-Only address, only the **Read** button will be selectable. Clicking on the Read button, the register value will be reported in the **Value** field.

If the register has a Write-Only address, only the **Write** button will be selectable. The user has to write the desired value in the **Value** field and then press the Write button.

If the register has a Read/Write address, both functions described here above become available.

The three lines in the middle of the tab show the map of the selected register displaying the value of each single bit and including together with a quick description of the associated functionality (in the central line).

The user can also save on the local disk the full register map by clicking on the **Save register map to disk** button.

In case of a long list of registers to be written, it is recommended to use an external file to be provided in the FreeWrites field of **The Acquisition Tab**.

Note: Please note that since the FreeWrites are loaded every time the acquisition is started and the write commands are executed at the end of the digitizer programming, if a FreeWrites is used the settings write using the Register Tab might be overwritten by the FreeWrites commands).

Note: The Register map Tab is not available for the V27XX and DT27XX series.

5.4.7 The Time Selection Tab

The **Time Selection Tab** is shown in Fig. **5.36**.

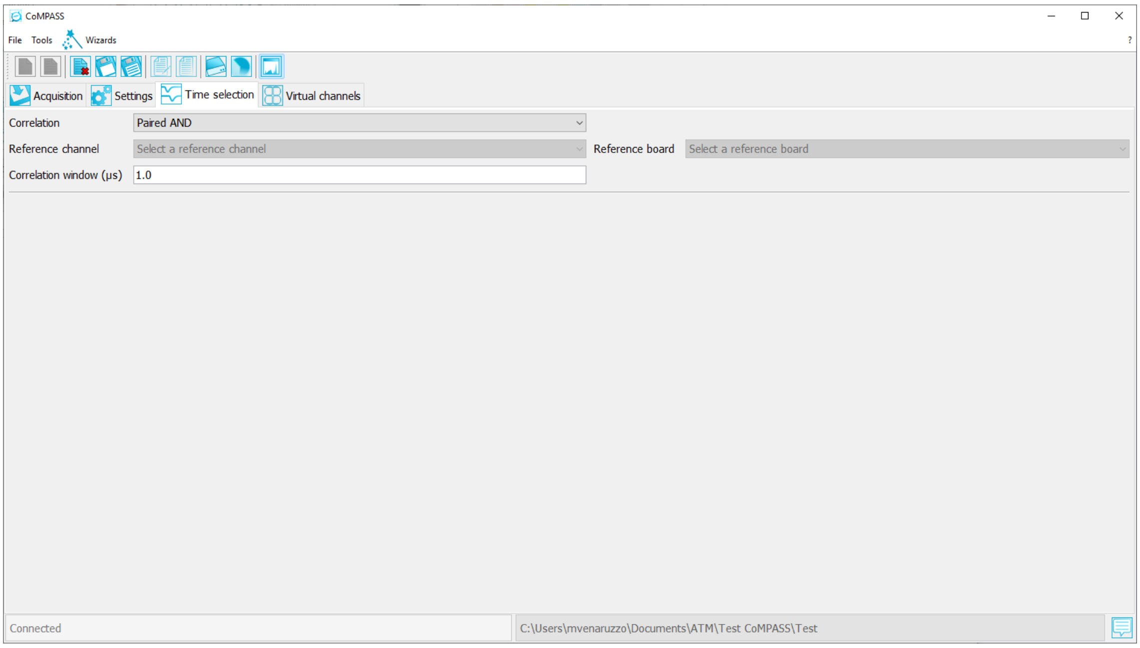


Fig. 5.36: CoMPASS Time Selection Tab.

The **Time Selection Tab** allows the user to operate on event selection based on time. The correlation is performed at the software level, i.e. without any modification of the boards firmware registers.

Note: Software selection implies that there is no data throughput reduction and that both filtered and unfiltered events are saved. In case of **The Trigger/Veto/Coincidences Tab** events not passing the criteria are completely discarded.

Using the **Correlation** combo box, the user can select the following options:

- **Disabled**: no correlation between the digitizer channels;
- **Paired AND**: the software correlates the digitizer channels n and n+1, i.e. Ch0 with Ch1, Ch2 with Ch3 and so on by evaluating the time difference T_{Chn+1} - T_{Chn};
- **Ch_ref AND any**: it corresponds to the option **Common Start** in the traditional analog electronics with TDCs. One channel is meant to provide the reference time (T_{start}) while all the others will be the evaluated with respect to it (T_{stop}). The user must specify the reference channel in the **Starting channel** field. The width of the correlation window (in µs) has to be specified in the **Correlation window** field.
- **Ch_ref veto**: the reference channel acts as a veto for the other channels. Filtered events have a time difference with respect to the reference channel greater than the correlation window. The user must specify the reference channel in the **Starting channel** field. The width of the correlation window (in µs) has to be specified in the **Correlation window** field.
- **Bd_ref veto**: the reference board acts as a veto for the other boards. The veto signal is the logical OR of the reference board channels signal. The veto width (in µs) has to be specified in the **Correlation window** field.

The time difference of correlated events is shown in the ΔT plot (see Sec. **The Plotter Window**).

5.4.8 The Virtual Channel Tab

The **Virtual Channel Tab** is shown in Fig. **5.37**.

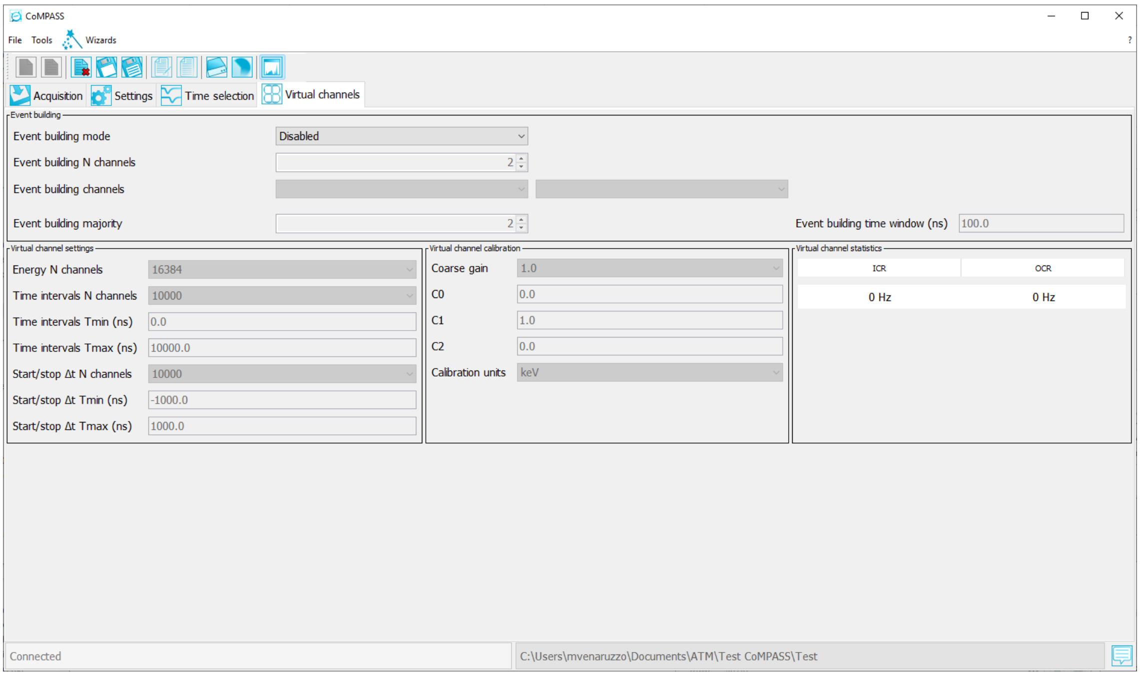


Fig. 5.37: CoMPASS Time Selection Tab.

The **Virtual Channel Tab** allows the user to operate with segmented detectors (like Clover detectors) or, in general, when it is required to do an event building operation starting from the information coming from different channels of the digitizer (like in case of a single detector read by multiple PMTs).

The "Event building" section allows to set the Event Building in Add-Back mode, to set the number of channels to be included in the event building, the majority level and the width of the time windows (in ns) to be used in the event building procedure.

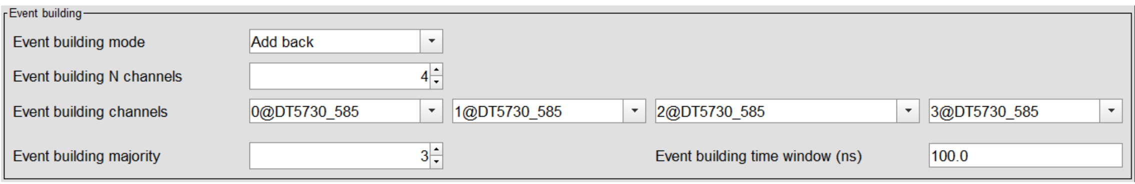


Fig. 5.38: Virtual Channels Tab - Event building section

Note: Before proceeding with the event building make the **energy calibration** of the individual channels to perform the correct energy summing.

The time-stamp of the built events is the average of the single events time-stamps. The virtual channel events are filtered according to the same selection set for the events coming from the single channels, i.e. an event discarded by the energy/PSD/time/correlation filter applied in the single channels is not used in the event building procedure.

The "Virtual channel settings" section summarizes the number of channels and the limits of the spectra for the virtual channel (see Fig. **5.38**).

Allowed values are:

- **Energy N channels**: 256, 512, 1024, 2048, 4096, 8192, 16384.
- **Time Intervals/Start-Stop Δt N channels**: 100, 200, 500, 1000, 2000, 5000, 10000.

Note: Choose the same value of **Energy N channels** as for the individual channels.

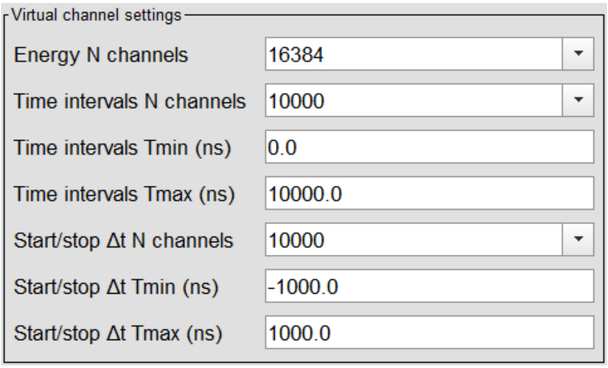


Fig. 5.39: Virtual Channels Tab - Virtual channel settings section

The ”Virtual channel calibration” section shows and allows the user to modify the calibration parameters of the virtual channel energy spectrum.

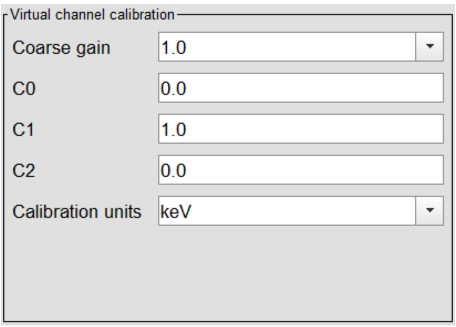


Fig. 5.40: Virtual Channels Tab - Virtual channel calibration section

The ”Virtual channel statistics” section shows the virtual channel ICR and OCR statistics.

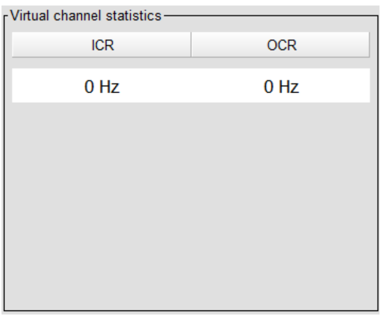


Fig. 5.41: Virtual Channels Tab - Virtual channel statistics section

5.4.9 The Information Menu

Pressing the "?" button in the top right corner of the CoMPASS Main GUI, the user does access the CoMPASS Information Menu.

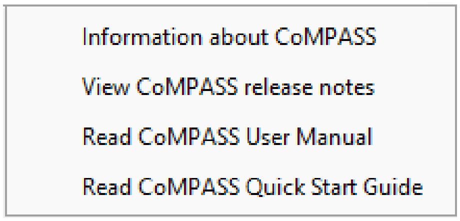


Fig. 5.42: CoMPASS Information Menu.

Such menu allows the user to:

1. open the CoMPASS Information window in which the release and build numbers are included;

Fig. 5.43: CoMPASS Information Window.

2. open the CoMPASS release notes file (opened as external TXT file);
3. read the CoMPASS User Manual and Quick Start Guide (opened as external PDF files).

5.4.10 The Plotter Window

Pressing on the  button, the user can open the Plotter window. In this window the user can display all the plots and histograms supported by CoMPASS with the only limitation that only one waveform plot, only one scatterplot and a maximum of six different histogram can be displayed at once.

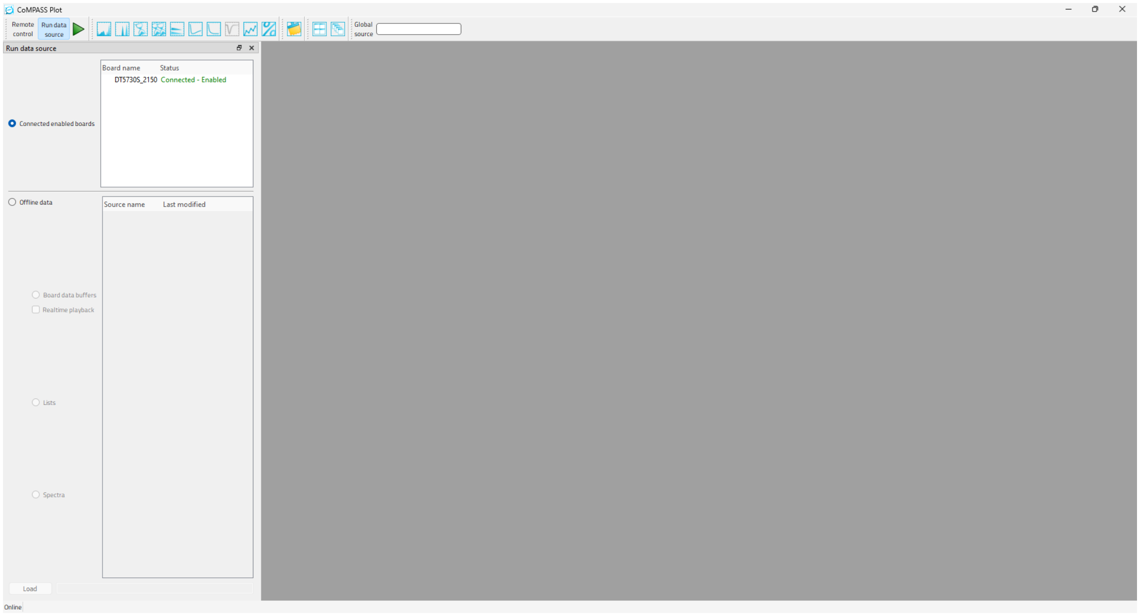
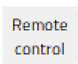
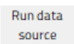
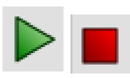
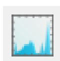


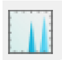
Fig. 5.44: CoMPASS Plotter Window.

5.4.10.1 The Plotter Window Icon Bar

Fig. 5.45: CoMPASS Plotter Window Icon Bar.

The above icons correspond to the following functions (from left to right):

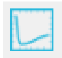
1. **Remote control** : this icons enable the possibility of controlling CoMPASS from a (remote) external script via HTTP requests;
2. **Run Data Source** : this icons open the Run Data Source section of the CoMPASSPlot;
3. **Acquisition Jobs** : this icons allows to set consecutive acquisitions (jobs) - COMING SOON;
4. **Start/Stop Acquisition** : these icons have the same function of the Menu Bar/ Tools / Start/Stop Acquisition command;
5. **New Energy Histogram** : this icon opens a new Energy Histogram;

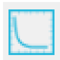
6. **New PSD Histogram** : this icon opens a new PSD Histogram;

7. **New Time Histogram** : this icon opens a new Time Histogram;

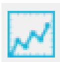
8. **New Tof Histogram** : this icon opens a new Δt (time difference between two channels) Histogram. This icon is active only when ”Time Correlations” are enabled;

9. **New PSD vs Energy Scatterplot Histogram** : this icon opens a new Scatterplot (Energy/PSD) Histogram;

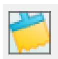
10. **New Energy vs Energy Scatterplot Histogram** : this icon opens a new Scatterplot (Energy/Energy) Histogram;

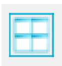
11. **New Δt vs Energy Scatterplot Histogram** : this icon opens a new Scatterplot (Δt/Energy) Histogram;

12. **New Waveform** : this icon opens the Waveform inspector. This icon is active only if ”Acquisition mode = Waves”;

13. **New MCS Graph** : this icon opens a new Multichannel Scaler graph;

14. **New Stat Graph** : this icon opens a new Statistics summary table;

15. **Clear All Histograms** : this icon resets all the histograms;

16. **Tile** : this icon allows to display the plots in tile mode;

17. **Cascader** : this icon allows to display the plots in cascade mode;

18. **Global source** 

: this combo box allows the user to select the global source to which all the plot will be referred.

Fig. **5.46** shows an example of the CoMPASS plotter in which a waveform plot, an energy histogram, a PSD histogram, a time histogram and a energy/PSD scatterplot are shown all together.

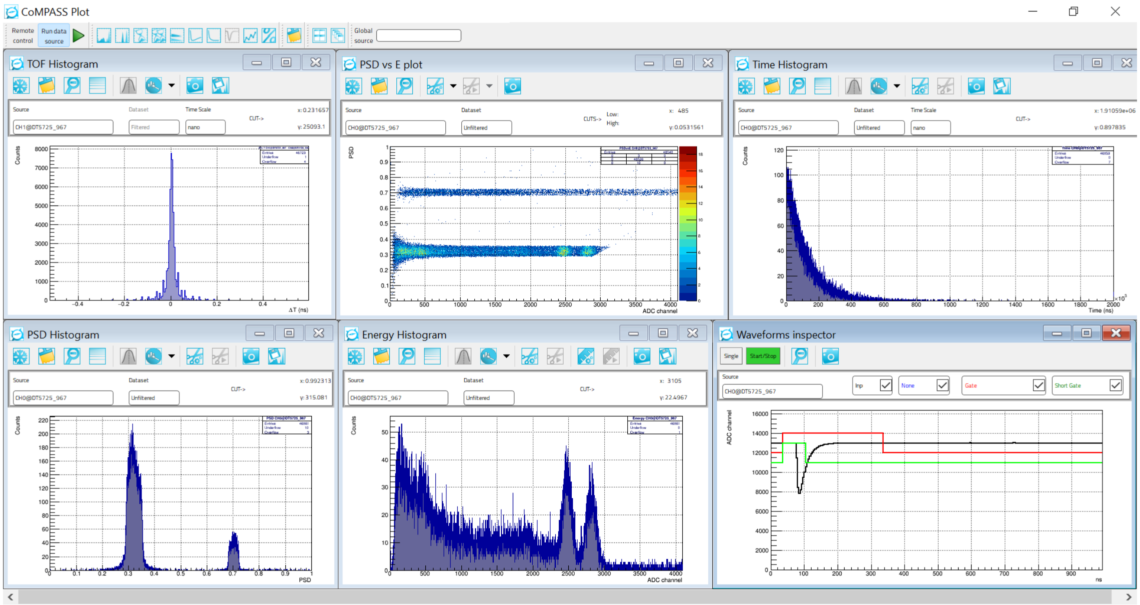


Fig. 5.46: CoMPASS Plotter Window with several plot displayed.

5.4.10.2 The Run Data Source section

The Run Data Source section allows the user to select the data source for the processing, be it the online data taking or the offline post-processing.

The upper part of the section shows the boards part of the project and their current status.

The lower part of the section is composed by a radio button selection that allows the user to choose the offline processing data source among Board Data Buffers, Lists and Spectra.

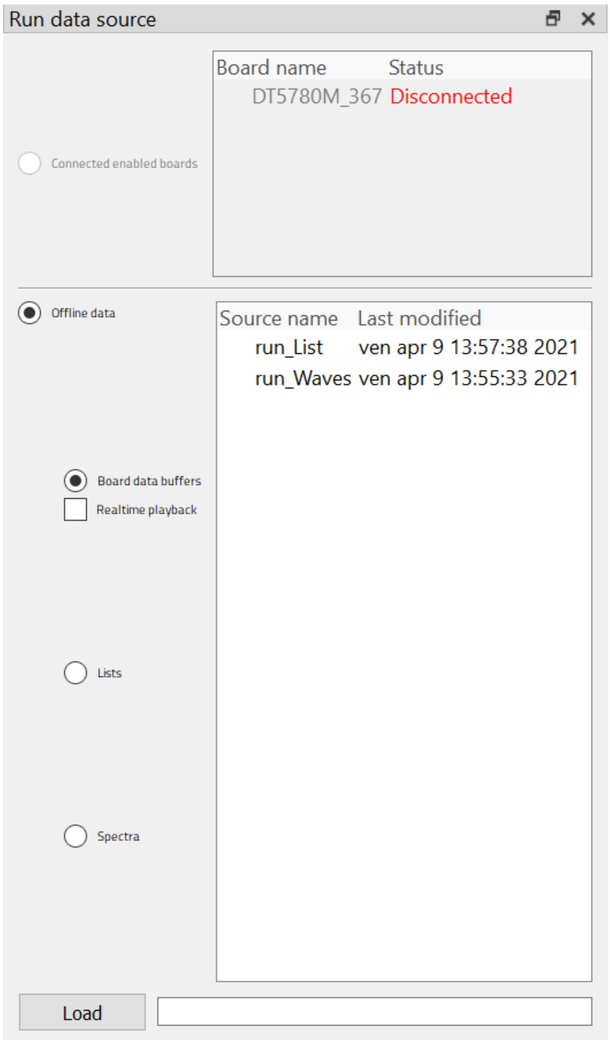


Fig. 5.47: CoMPASSPlot Run Data Source section.

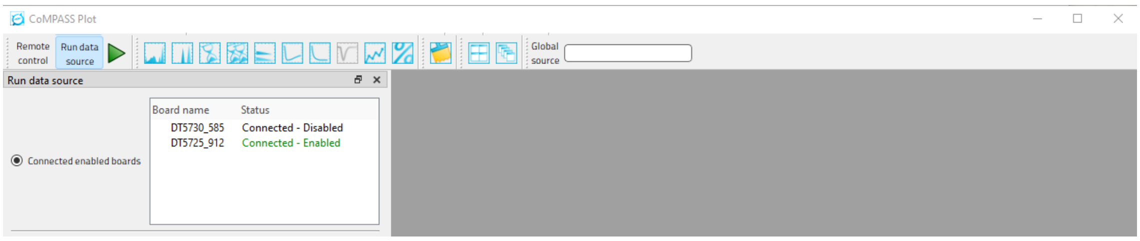


Fig. 5.48: Connected and disconnected digitizer status shown in the CoMPASS Plot Run Data Source section.

In case of Board Data Buffers option, the user can select the speed of the run reproduction. Default is high speed, otherwise select **Real time playback** for reproducing the run at the real speed.

The dataset to be processed can be selected either double clicking on the file name or clicking on the file name and then pressing the Load button.

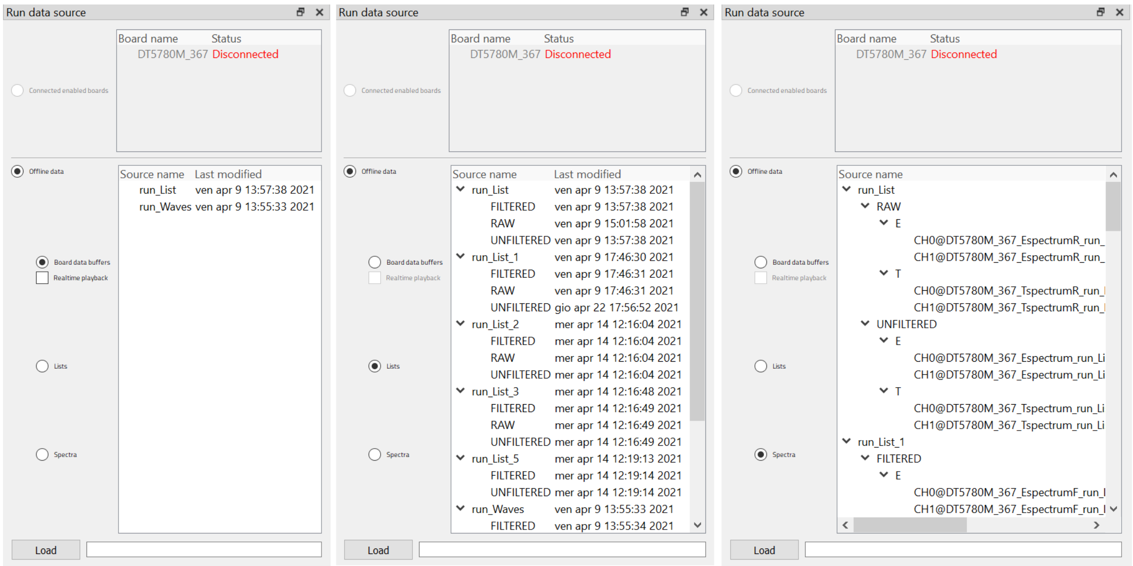


Fig. 5.49: Run Data Source offline section options.

The offline run status is also reflected in the main GUI status bar

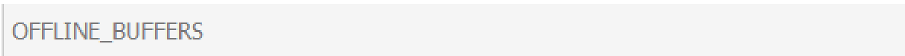


Fig. 5.50: Offline run - Board data buffer option - GUI status bar.

and in the CoMPASSPlot Status bar.

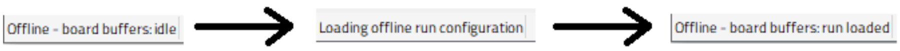


Fig. 5.51: Offline run - Board data buffer option - GUI status bar.

5.4.10.3 The Waveform Plot Icon Bar

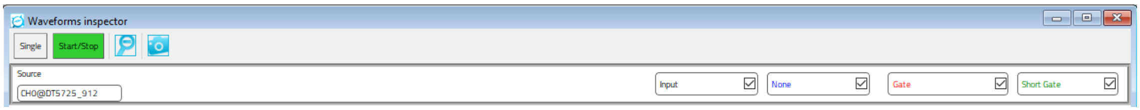
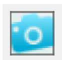
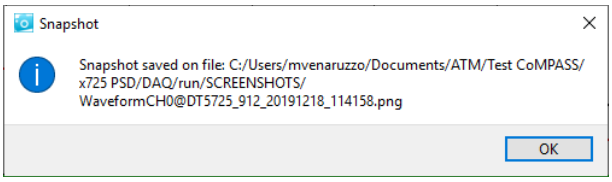


Fig. 5.52: CoMPASS Waveform Plot Icon Bar.

The above icons correspond to the following functions (from left to right):

1. **Single** : allows to display a single waveform and disable/enable the automatic refresh of the plot.
2. **Start/Stop** : disable/enable the automatic refresh of the plot.
3. **Unzoom** : unzoom the plot. **Note**: to zoom the plot select an interval in the x-axis or in the y-axis.
4. **Snapshot**:  This button takes a screenshot of the current plot.

   Screenshots are saved in .png format and stored in the DAQ/run/SCREENSHOTS folder of the CoMPASS project in use.

   The top part of the Waveform Inspector Plot allows to select the signal *Source* and the traces (analog and digital) to be displayed.

Note: In Waves mode, it is possible to plot two different waveforms, i.e. for example the Input and the Baseline. This possibility is called *dual trace*. When the dual trace is enabled, the samples of the two signals are interleaved, thus each waveform is recorded at half of the ADC frequency. When disabled only the Input is recorded at the ADC frequency. To disable the *dual trace*, select *None* as second analog trace to be displayed. In case of 751 family use the **"Analog Traces Fine Resolution"** parameter of the GUI Input tab. The option "Analog Traces Fine Resolution" allows the user to visualize the first trace at full sampling.

The available traces are:

- x720/DT5790 with DPP-PSD
  (a) Analog Trace 1: **Input**
  (b) Analog Trace 2: **Baseline**
  (c) Digital Trace 1: **Trigger**
  (d) Digital Trace 2: **Long Gate**
  (e) Digital Trace 3:
    * **External TRG**: the external trigger signal when enabled;
    * **Over Threshold**: digital signal that is 1 when the input signal is over the requested threshold;
    * **Shaped TRG**: logic signal generated by a channel in correspondence with its local self-trigger. It is used to propagate the trigger to the other channels of the board and to other external boards, as well as to feed the coincidence trigger logic (refer to **[Coincidence]**);

  * **TRG Val. Acceptance Win.**: logic signal corresponding to the time window where the coincidence validation is accepted. The validation enables the event dump into the memory (refer to **[Coincidence]**);
  * **Pile Up**: logic pulse set to 1 when a pile up event occurred;
  * **Coincidence**: logic pulse set to 1 when a coincidence occurred (refer to **[Coincidence]**).

(f) Digital Trace 4:
  * **Short Gate**;
  * **Over Threshold**: digital signal that is 1 when the input signal is over the requested threshold;
  * **TRG Validation**: digital signal that is 1 when a coincidence validation signal comes from the mother board FPGA (refer to **[Coincidence]**);
  * **TRG HoldOff**: logic signal generated by a channel in correspondence with its local self-trigger. Other triggers are inhibited for the overall Trigger Hold-Off duration;
  * **Pile Up**: logic pulse set to 1 when a pile up event occurred;
  * **Coincidence**: logic pulse set to 1 when a coincidence occurred (refer to **[Coincidence]**).

- x724/x780/x781 with DPP-PHA legacy

  (a) Analog Trace 1:
  * **Input**: the input signal from pre-amplified detectors;
  * **RC-CR**: first step of the trigger and timing filter;
  * **RC-CR2**: second step of the trigger and timing filter;
  * **Trapezoid**: trapezoid resulting from the energy filter;

  (b) Analog Trace 2:
  * **Input**: the input signal from pre-amplified detectors;
  * **Threshold**: the RC-CR2 threshold value;
  * **Trapezoid-BL**: the trapezoid shape minus its baseline;
  * **Baseline**: displays the trapezoid baseline;

  (c) Digital Trace 1: **Trigger**;

  (d) Digital Trace 2:
  * **TRG Window**: shows the RT Discrimination Width;
  * **Armed**: digital input showing where the RC-CR2 crosses the Threshold;
  * **Peak Run**: starts with the trigger and last for the whole event;
  * **Pile-Up**: shows when there is a pile-up event and corresponds to the time interval when the energy calculation is disabled due to the pile-up event;
  * **Peaking**: shows where the energy is calculated;
  * **Trg Validation Win**: digital input showing the trigger validation acceptance window TVAW (refer to **[Coincidence]**);
  * **BSL Holdoff**: shows the baseline hold-off parameter;
  * **TRG Holdoff**: shows the trigger hold-off parameter;
  * **Trg Validation**: shows the trigger validation signal TRG_VAL (refer to **[Coincidence]**);
  * **Acq Veto**: this is 1 when either the input signal is saturated or the memory board is full.

- x724/x780/x781/V1782 with DPP-PHA

  (a) Analog Trace 1:
  * **Input**: the input signal from pre-amplified detectors;
  * **RC-CR**: first step of the trigger and timing filter;
  * **Fast Filter**: second step of the trigger and timing filter;
  * **Trapezoid**: trapezoid resulting from the energy filter;

  (b) Analog Trace 2:
  * **Input**: the input signal from pre-amplified detectors;
  * **Threshold**: the RC-CR2 threshold value;
  * **Trapezoid-BL**: the trapezoid shape minus its baseline;

* **Baseline**: displays the trapezoid baseline;

(c) Digital Trace 1: **Trigger**

(d) Digital Trace 2:

* **Peaking**: shows where the energy is calculated;
* **Armed**: digital input showing where the RC-CR2 crosses the Threshold;
* **Peak Run**: starts with the trigger and last for the whole event;
* **Pile-Up**: shows when there is a pile-up event and corresponds to the time interval when the energy calculation is disabled due to the pile-up event;
* **Peaking**: shows where the energy is calculated;
* **Trg Validation Win**: digital input showing the trigger validation acceptance window TVAW (refer to **[Coincidence]**);
* **BSL Freeze**: shows the time interval in which the baseline evaluation is freezed;
* **TRG Holdoff**: shows the trigger hold-off parameter;
* **Trg Validation**: shows the trigger validation signal TRG_VAL (refer to **[Coincidence]**);
* **Over Range Protection Time**: this is 1 when the input stage is saturated;
* **TRG Window**: not used;
* **Ext TRG**: shows the external trigger, when available;
* **Busy**: shows when the memory board is full;
* **Peak Ready**: shows after the Peak Mean time.

- x725(S)/x730(S) with DPP-PSD

(a) Analog Trace 1:

* **Input**
* **Smoothed Input** or **CFD** (if enabled);

(b) Analog Trace 2:

* **None**
* **Baseline**
* **Smoothed Input** or **CFD** (if enabled);

(c) Digital Trace 1:

* **Long Gate**;
* **Over Threshold**: digital signal that is 1 when the input signal is over the requested threshold;
* **Shaped TRG**: logic signal generated by a channel in correspondence with its local self-trigger. It is used to propagate the trigger to the other channels of the board and to other external boards, as well as to feed the coincidence trigger logic (refer to **[Coincidence]**);
* **Val. Acceptance Win.**: logic signal corresponding to the time window where the coincidence validation is accepted. The validation enables the event dump into the memory (see **[Coincidence]**);
* **Pile Up**: logic pulse set to 1 when a pile up event occurred;
* **Coincidence**: logic pulse set to 1 when a coincidence occurred (refer to **[Coincidence]**);
* **Trigger**.

(d) Digital Trace 2:

* **Short Gate**;
* **Over Threshold**: digital signal that is 1 when the input signal is over the requested threshold;
* **TRG Validation**:digital signal that is 1 when a coincidence validation signal comes from the motherboard FPGA (refer to **[Coincidence]**);
* **TRG HoldOff**: logic signal generated by a channel in correspondence with its local self-trigger. Other triggers are inhibited for the overall Trigger Hold-Off duration;
* **Pile Up**: logic pulse set to 1 when a pile up event occurred (to be implemented);
* **Coincidence**: logic pulse set to 1 when a coincidence occurred (refer to **[Coincidence]**);

    * **Trigger**.
- x725(S)/x730(S) with DPP-PHA
  (a) Analog Trace 1:
    * **Input**: the input signal from pre-amplified detectors;
    * **RC-CR**: first step of the trigger and timing filter;
    * **RC-CR2**: second step of the trigger and timing filter;
    * **Trapezoid**: trapezoid resulting from the energy filter;
  (b) Analog Trace 2:
    * **Input**: the input signal from pre-amplified detectors;
    * **Threshold**: the RC-CR2 threshold value;
    * **Trapezoid-BL**: the trapezoid shape minus its baseline;
    * **Baseline**: displays the trapezoid baseline;
  (c) Digital Trace 1: **Trigger**;
  (d) Digital Trace 2:
    * **Peaking**: shows where the energy is calculated;
    * **Armed**: digital input showing where the RC-CR2 crosses the Threshold;
    * **Peak Run**: starts with the trigger and last for the whole event;
    * **Pile-Up**: shows when there is a pile-up event and corresponds to the time interval when the energy calculation is disabled due to the pile-up event;
    * **Peaking**: shows where the energy is calculated;
    * **Trg Validation Win**: digital input showing the trigger validation acceptance window TVAW (refer to **[Coincidence]**);
    * **BSL Freeze**: shows where the trapezoid baseline is frozen for the energy calculation;
    * **TRG Holdoff**: shows the trigger hold-off parameter;
    * **Trg Validation**: shows the trigger validation signal TRG_VAL (refer to **[Coincidence]**);
    * **Acq Busy**: this is 1 when the board is busy (saturated input signal or full memory board) or there is a veto;
    * **TRG Window**: shows the RT Discrimination Width;
    * **Ext TRG**: shows the external trigger, when available;
    * **Busy**: shows when the memory board is full.
- x740D with DPP-QDC
  (a) Analog Trace:
    * **Input**;
    * **Smoothed Input**;
    * **Baseline**;
  (b) Digital Trace 1: **Gate**
  (c) Digital Trace 2: **Trigger**
  (d) Digital Trace 3: **Trigger Hold-Off**
  (e) Digital Trace 4: **Over-Threshold**
- x751 with DPP-PSD
  (a) Analog Trace 1:
    * **Input**;
    * **CFD** (only if Dual Trace is enabled);
    * **Baseline** (only if Dual Trace is enabled);
  (b) Analog Trace 2:
    * **CFD**;
    * **Baseline**; (only if Dual Trace is enabled);
  (c) Digital Trace 1:
    * **Long Gate**;

  * **Over Threshold**: digital signal that is 1 when the input signal is over the requested threshold;
  * **Shaped TRG**: logic signal generated by a channel in correspondence with its local self-trigger. It is used to propagate the trigger to the other channels of the board and to other external boards, as well as to feed the coincidence trigger logic (refer to **[Coincidence]**);
  * **TRG Val. Acceptance Win.**: logic signal corresponding to the time window where the coincidence validation is accepted. The validation enables the event dump into the memory (refer to **[Coincidence]**);
  * **Pile Up**: logic pulse set to 1 when a pile up event occurred;
  * **Coincidence**: logic pulse set to 1 when a coincidence occurred (refer to **[Coincidence]**);

  (d) Digital Trace 2:
  * **Short Gate**;
  * **Over Threshold**: digital signal that is 1 when the input signal is over the requested threshold;
  * **TRG Validation**: digital signal that is 1 when a coincidence validation signal comes from the mother board FPGA (refer to **[Coincidence]**);
  * **TRG HoldOff**: logic signal generated by a channel in correspondence with its local self-trigger. Other triggers are inhibited for the overall Trigger Hold-Off duration;
  * **Pile Up**: logic pulse set to 1 when a pile up event occurred;
  * **Coincidence**: logic pulse set to 1 when a coincidence occurred (refer to **[Coincidence]**);

- x2740/x2745/x2730 with DPP-PSD

  (a) Analog Trace 1 and 2:
  * **Input**;
  * **Baseline**;
  * **CFD**;

  (b) Digital Trace 1 to 4:
  * **Baseline Freeze**;
  * **Time Filter Armed**;
  * **ADC Saturation**;
  * **TRG Holdoff**;
  * **Charge ready**;
  * **Charge saturation**;
  * **Negative Overthreshold**;
  * **Over Threshold**;
  * **Pileup**;
  * **Gate**;
  * **Short gate**;
  * **Trigger**.

- x2740/x2745 with DPP-PHA

  (a) Analog Trace 1 and 2:
  * **Input**;
  * **Time Filter**;
  * **Energy Filter**;
  * **Energy Filter Baseline**;
  * **Energy Filter – Baseline**;

  (b) Digital Trace 1 to 4:
  * **Trigger**;
  * **Time Filter Armed**;
  * **ReTrigger Guard**;
  * **Energy Filter Baseline Freeze**;

* **Energy Filter Peaking**;
* **Energy Filter Peak Ready**;
* **Energy Filter Pile Up Guard**;
* **Event Pile Up**;
* **ADC Saturation**;
* **ADC Saturation Protection**;
* **Post Saturation Event**;
* **Energy Filter Saturation**;
* **Acquisition Inhibit**.

5.4.10.4 The Energy Histogram Icon Bar

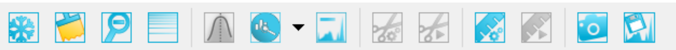
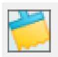
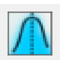
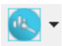
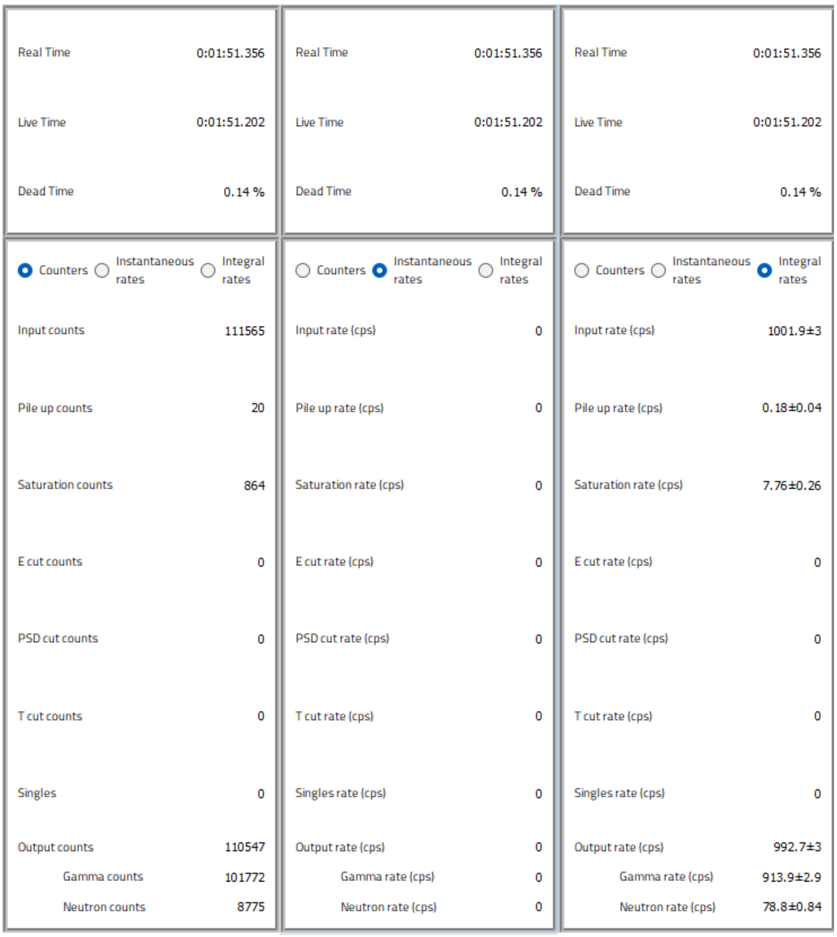


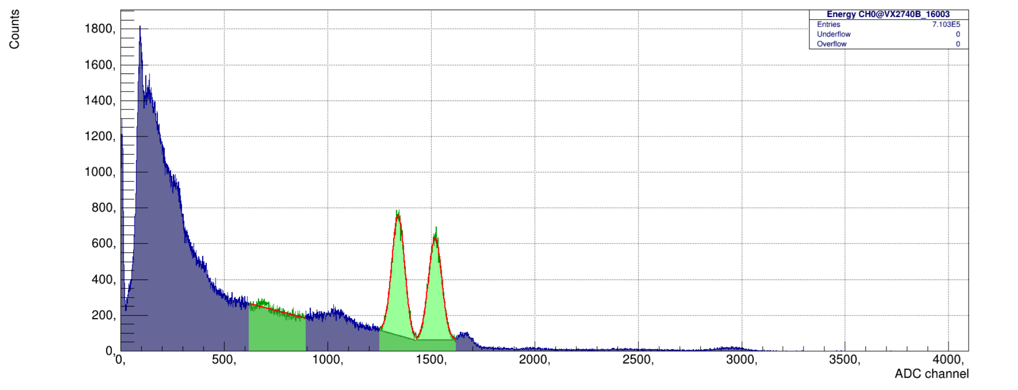
Fig. 5.53: CoMPASS Energy Histogram Icon Bar.

The above icons correspond to the following functions (from left to right):

1. **Freeze Plot**  : disable/enable the automatic refresh of the plot.
2. **Clean Histogram**  : reset the histogram.
3. **Unzoom**  : unzoom the plot. **Note**: to zoom the plot select an interval in the x-axis or in the y-axis.
4. **LogY**  : Set the logarithmic y-scale.
5. **Fit**:  Fit the selected area. **Note**: to enable this button first freeze the plot.
6. **Analysis**:  Allows to open the histogram Statistics or ROIs management subwindows.
   The Statistics windows summarizes:
   - the Real, Live and Dead Time
   - the Counters related to the events included or rejected from the concerned plot
   - the Instantaneous rates (in cps, averaged on the last second of acquisition) of the events included or rejected from the concerned plot
   - the Integral rates (in cps, averaged on the total acquisition time) of the events included or rejected from the concerned plot

   The ROI management windows allows the user to Add/Remove multiple Region of Interests, Load/Save them to a file and Export to other acquisition channels, select the background function to be used when fitting the spectrum and dispaly the ROI fit results (Centroid, Sigma, Reduced χ^2, FWHM, FWTM, Percentage Resolution, Gross Counts, Net Counts, Background Counts). Check **[CompassQS]** for more details.

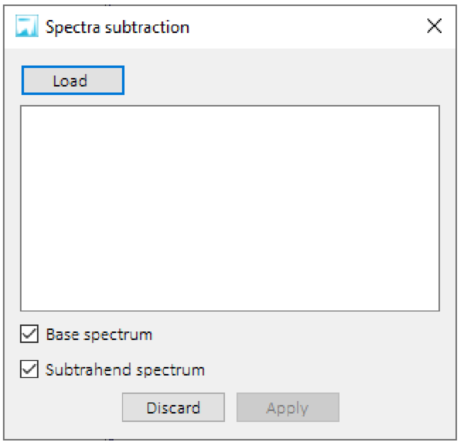




	Begin	End	Begin (keV)	End (keV)	Energy (keV)	Centroid	Sigma	Chi2n	FWHM	FWTM	Resolution	Gross Cnt	Net Cnt	Bkg Cnt
ROI 1	621.197	893.53	621.197	893.53	0	600±170	19±73	1.57951	50±170	80±310	8±29 %	61030±250	0±0.00029	61030±250
ROI 2	1252.01	1427.08	1252.01	1427.08	0	1341.42±0.22	30.72±0.26	0.914339	72.33±0.62	131.8±1.1	5.392±0.046 %	66720±260	51550±230	15180±120
ROI 3	1427.08	1618.83	1427.08	1618.83	0	1519.21±0.23	32.26±0.26	1.16813	75.98±0.61	138.5±1.1	5.001±0.04 %	57660±240	46070±210	11580±110

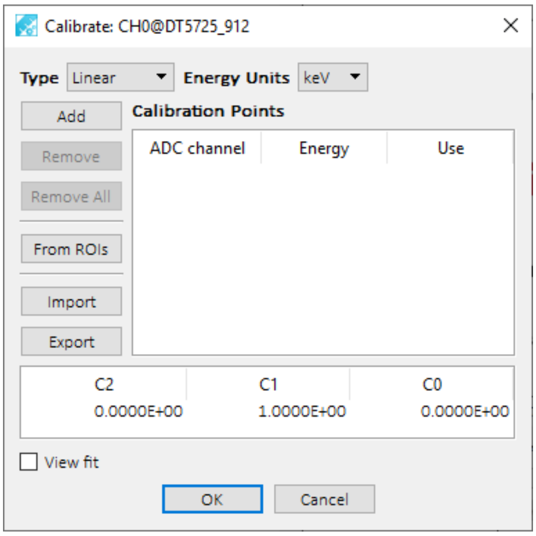
Fig. 5.54: ROI selection and fit (top) and the corresponding results in the table box (bottom).

7. **Energy Spectra Subtraction**: Open the spectra subtraction tool.

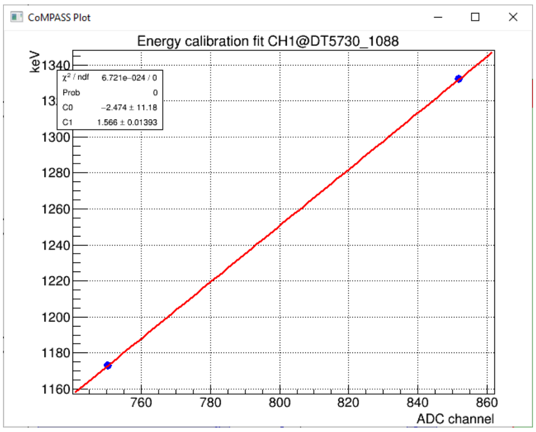


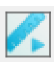
The user can then Load the subtrahend spectrum and see it alone or overlapped to the original one, selecting the corresponding option.

8. **Setup Calibration**:  Opens the calibration window.



The user can select the calibration curve, choosing between ”Linear” and ”Quadratic”, the Energy Units between keV and MeV, and add manually the peaks value in ADC channel and energy. The user can also automatically import the centroid of the peaks to be used for the calibration by pressing the button ”From ROIs”. It is also possible to verify the calibration fit by pressing ”View fit”

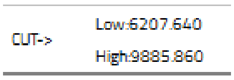


9. **Apply Calibration**:  Apply the set calibration.

10. **Define Cut**:  After pressing this button it is possible to select the low and high cuts directly in

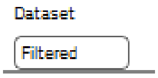
Note: the calibration parameters C0, C1, C2 are saved in the *run.info* file contained in the project folder under the path ”DAQ\run”.

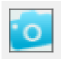
the plot by clicking the two positions in the spectrum. The values of cuts will appear below the icon bar.

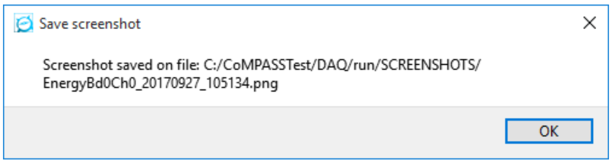


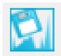
Note: it is also possible to select the cuts from the ”Rejection” tab (see Sec. **The Rejection Tab**).

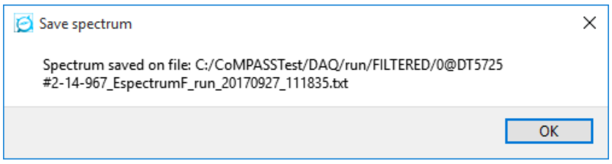
11. **Cut Apply**:  This button apply the selected cut. The dataset will be marked as ”Filtered”.



12. **Snapshot**:  This button takes a screenshot of the current plot.



13. **Save spectrum**:  This button save the spectrum in the format according to the option selected in the Acquisition Tab - Spectra saving section.



The histogram range can be defined in **The Spectra Tab** under ”Settings” (*Energy*).

5.4.10.5 The Time Histogram Icon Bar

Fig. 5.55: CoMPASS Time Histogram Icon Bar.

The Time Histogram shows the distribution of the difference between the timestamps of one event and the previous one occurred in the same digitizer channel.

The icons for the time histogram plot are the same as for **The Energy Histogram Icon Bar**, with the exception of the calibration icons which are not available.

In case of Time histogram it is possible to select the x-axis scale choosing among nano, micro and milli seconds.

The histogram range can be defined in **The Spectra Tab** under ”Settings” (*Time intervals*).

5.4.10.6 The Tof Histogram Icon Bar

The Tof histogram shows the distribution of the differences between the timestamps of two events occurred in two different digitizer channels. Which are the concerned digitizer channels depends on the

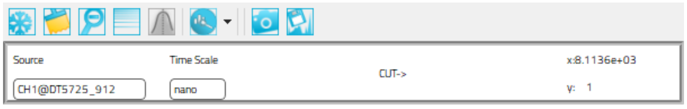


Fig. 5.56: CoMPASS Tof Histogram Icon Bar.

currently selected channel correlation in the ”Time Correlation” tab.

The icons for the Tof histogram plot are the same as for **The Time Histogram Icon Bar**, with the exception of the cuts, which correspond to the ”Correlation Window” under the ”Time Correlations” tab.

In case of Tof histogram it is possible to select the x-axis scale choosing among nano, micro and milli seconds.

The histogram range can be defined in **The Spectra Tab** under ”Settings” (*Start/stop* Δt).

5.4.10.7 The PSD Histogram Icon Bar

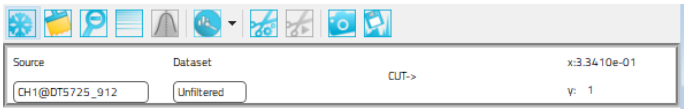


Fig. 5.57: CoMPASS PSD Histogram Icon Bar.

The icons for the PSD histogram plot are the same as for **The Energy Histogram Icon Bar**, with the exception of the calibration icons which are not available.

The histogram range can be defined in **The Spectra Tab** under ”Settings” (*PSD*).

5.4.10.8 The 2D PSD vs E, Evs E and Δt vs E Scatterplot Histogram Icon Bar

Fig. 5.58: CoMPASS ScatterPlot Histogram Icon Bar.

Refer to Sec. **The Energy Histogram Icon Bar** for a description of the Scatterplot histogram icons.

The 2D histogram ranges can be defined in **The Spectra Tab** under ”Settings” (*2D Energy/2D PSD*).

5.4.10.9 The MCS Plot Icon Bar

Fig. 5.59: CoMPASS MCS Graph Icon Bar.

Refer to Sec. **The Energy Histogram Icon Bar** for a description of the Scatterplot histogram icons.

The MCS graph Dwell time (in seconds), MCS X Axis mode (”Time interval (s) or ”Most recent (s)) and MCS view mode (”cps vs time” or ”cps histogram”) can be set by pressing the  button.

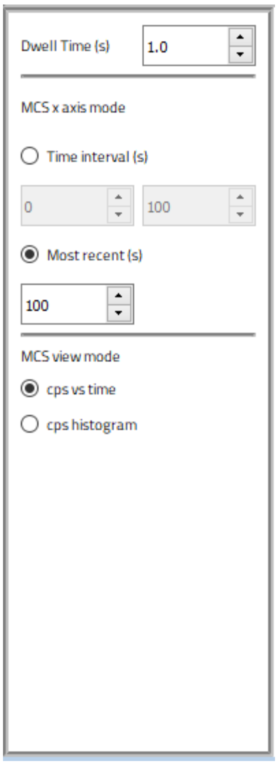


Fig. 5.60: CoMPASS MCS plot settings windows.

In cps vs time mode MCS plot shows the following traces as function of elapsed time:

- Input counts
- Events rejected because of pile-up
- Events rejected because of saturations
- Events rejected because of energy selection
- Events rejected because of PSD selection
- Events rejected because of time selection
- Events rejected because of correlation selection
- Output events
- Events tagged as ”Gamma” particle type (according to Particle ID settings tab)
- Events tagged as ”Neutron” particle type (according to Particle ID settings tab)

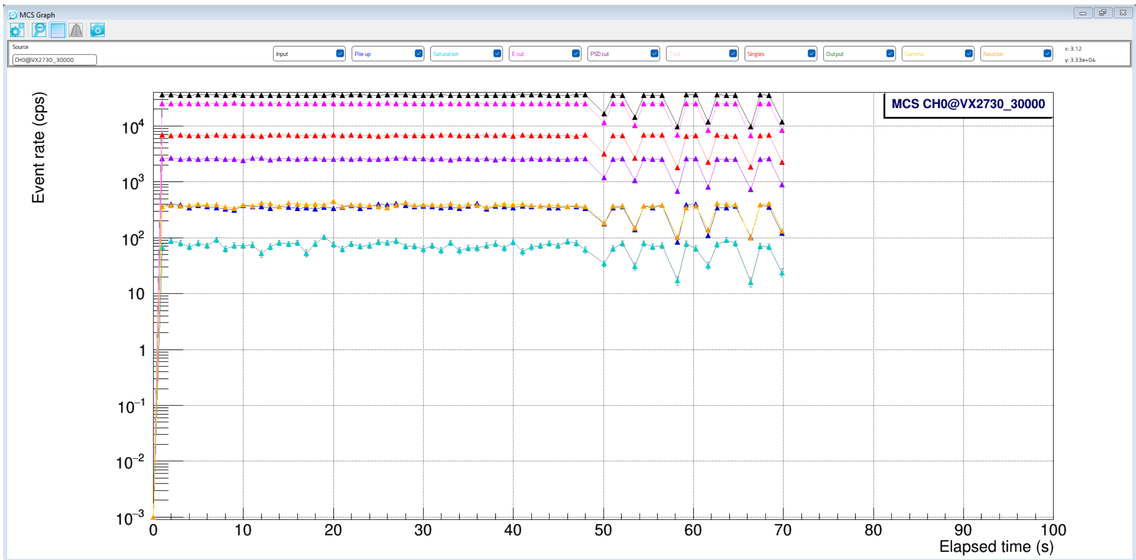


Fig. 5.61: CoMPASS MCS plot settings in cps vs time mode.

In cps histogram mode MCS plot shows the same quantities but in histrogram visualization:

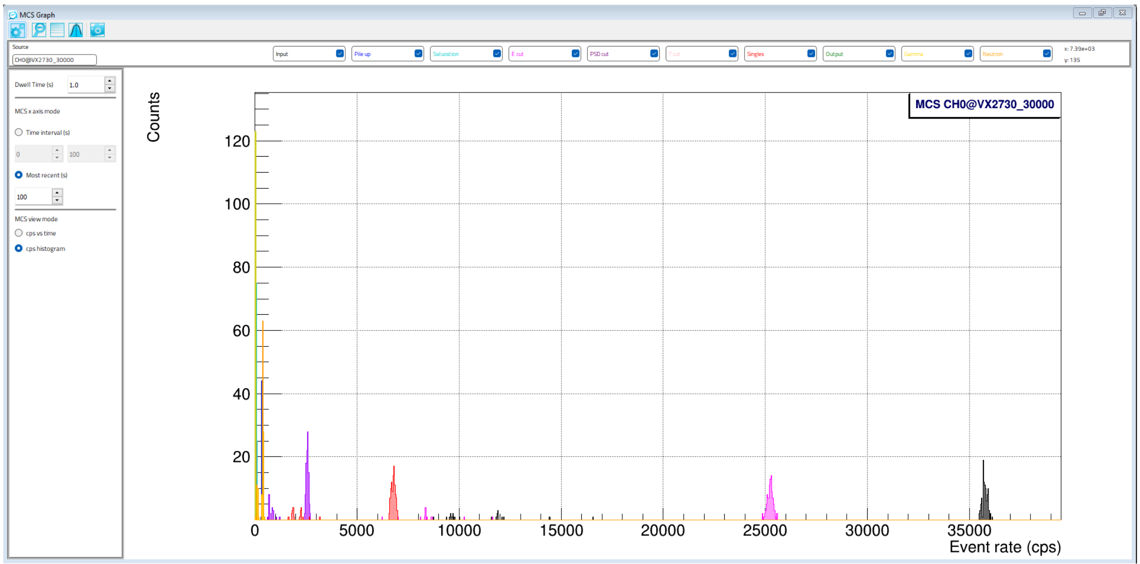


Fig. 5.62: CoMPASS MCS plot settings in histogram mode.

5.4.11 The Statistics Table

The **Statistics Table** is shown in Fig. **5.63**.

The **Statistics Table** allows the user to monitor the acquisition statistics of the current run such as:

- **Real Time** of the acquisition;
- **ICR**, the number/rate of the events coming from the detector to the digitizer input
- **Throughput**, the number/rate of the events coming rate from the board;

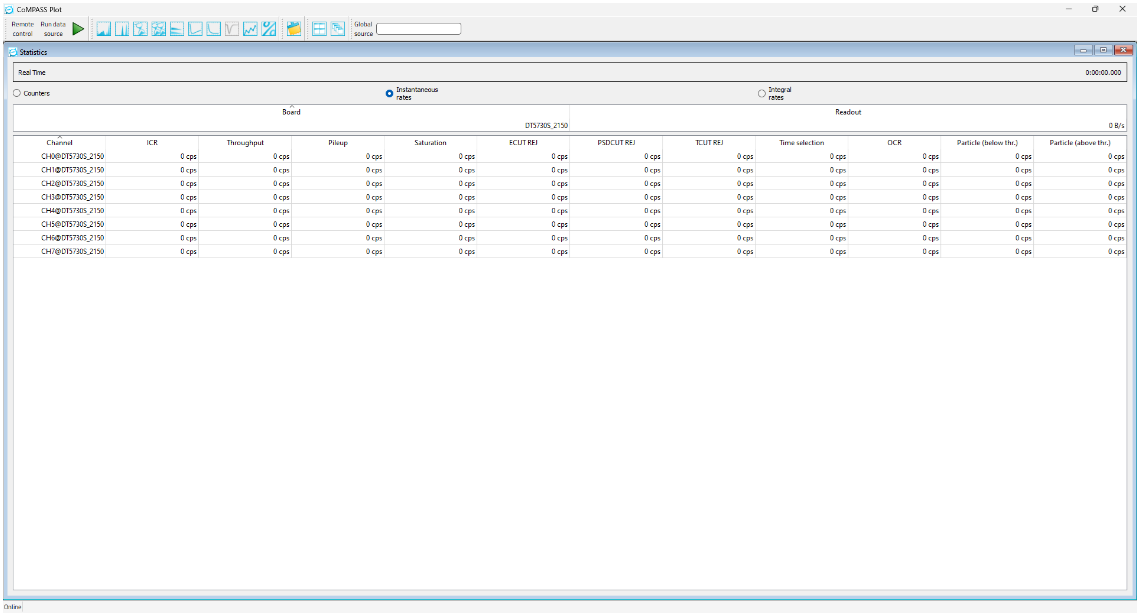


Fig. 5.63: CoMPASS Statistics Table.

- **Saturation**, the number/rate of events that saturate the input dynamics (positive and negative saturation), the long/short gate for DPP-PSD firmware or the trapezoid for the DPP-PHA firmware. Saturation cut must be enabled through **The Rejection Tab**;
- **PUR** (Pile-Up Rejection), the number/rate of events identified as piled-up. Pile-up rejection must be enabled in **The Rejection Tab**;
- **ECUT/PSDCUT/TCUT REJ**, the number/rate of events that have NOT passed the energy/PSD/time cuts. Cuts must be enabled in **The Rejection Tab** or through the plot;
- **SINGLES**, the number/rate of events that have NOT passed the software time correlations (that can be set through **The Time Selection Tab**);
- **OCR**, the number/rate of events passing the cuts and filling the histograms.
- **Particle (below thr.)**, the number/rate of events tagged because their PSD value is below the threshold set in the **The Particle ID Tab (DPP-PSD only)**;
- **Particle (above thr.)**, the number/rate of events tagged because their PSD value is above the threshold set in the **The Particle ID Tab (DPP-PSD only)**;

  NOTE: the sum of the columns from ”Pile Up” to ”OCR” should give the ”Throughput”.

The user can choose to display such information as Counters, Istantaneous rates or Integral rates.

In addition, the user can choose to display the information using the scientific notation in place of the standard one just clicking on the dedicated tick.

6 Digitizer Synchronization Guide

This chapter will guide the user to synchronize two or more CAEN digitizers running a DPP firmware. The first section is focused on the VME boards, the second section on the Desktop and NIM boards, the third section on the new VME27XX and Destop DT57XX boards while the forth section on a mixed system composed by V17XX and V27XX boards. This document is based on **[syncNote]**.

6.1 Synchronization of the VME V17XX digitizers

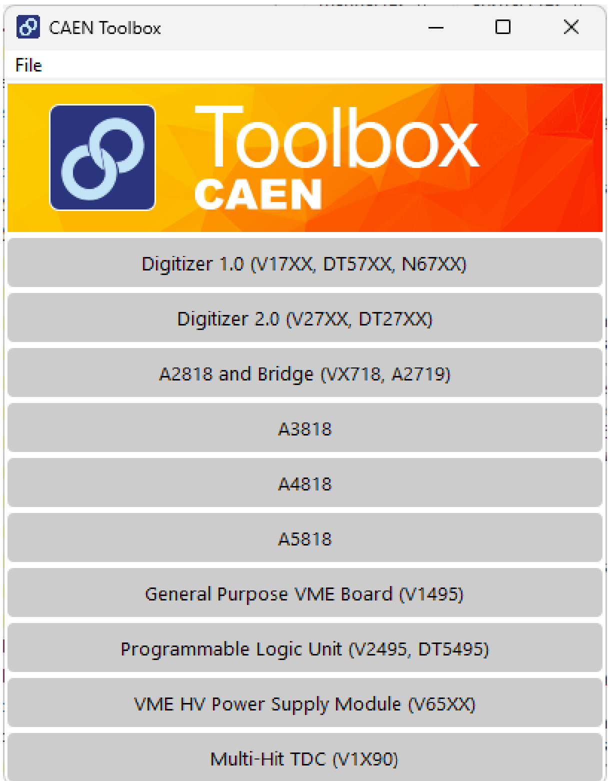
In the following, one V17XX digitizer acts as the master board while the others act as slaves. The idea is to lock the clocks of all the digitizers and to propagate the start of run in a daisy chain configuration.

Required software:

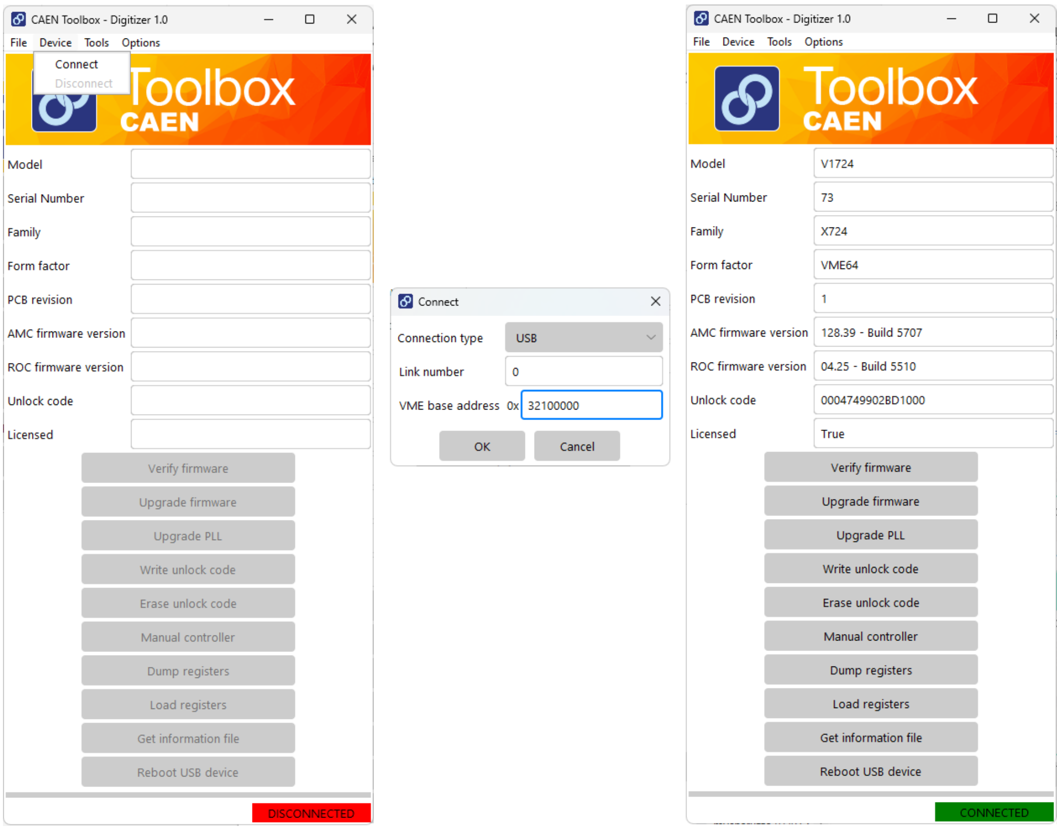
- CAEN Toolbox;
- CoMPASS

Phase 1: the **clock synchronization**:

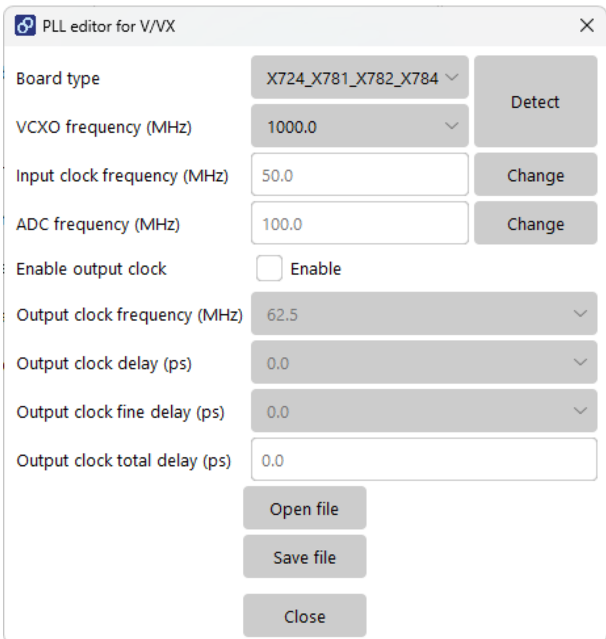
1. The PLL of master must be reprogrammed to provide in the CLOCK OUT the 50 or 62.5 MHz frequency depending on the slave board.
   - Open CAEN Toolbox, select "Digitizer 1.0".



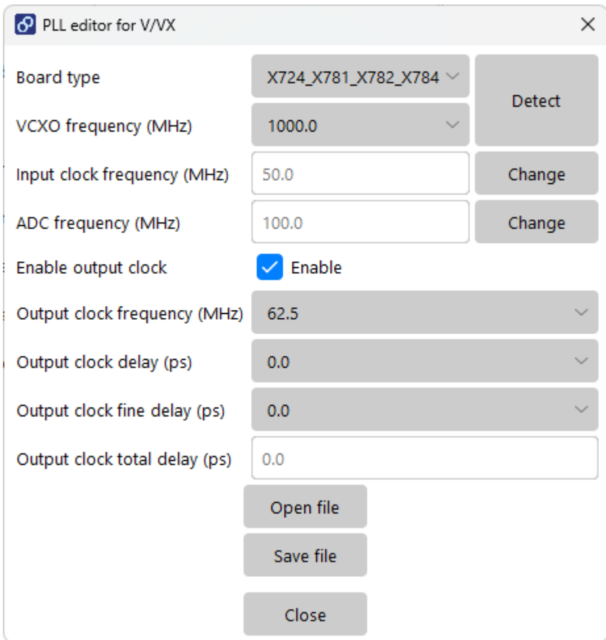
- from the top menu select Device → Connect, insert the digitizer connection parameters and press Connect.



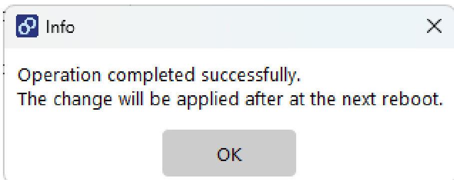
- if the master digitizer is a V1720, V1724, V1740D, V1751 or V1782, select Tools → PLL Editor from the top menu. The PLL Editor will open. Press "Detect" button to detect the currently connected digitizer.



- Tick "Enable clock output" and select the clock output frequency depending on the slave digitizer model. Set the Clock output delay if required.

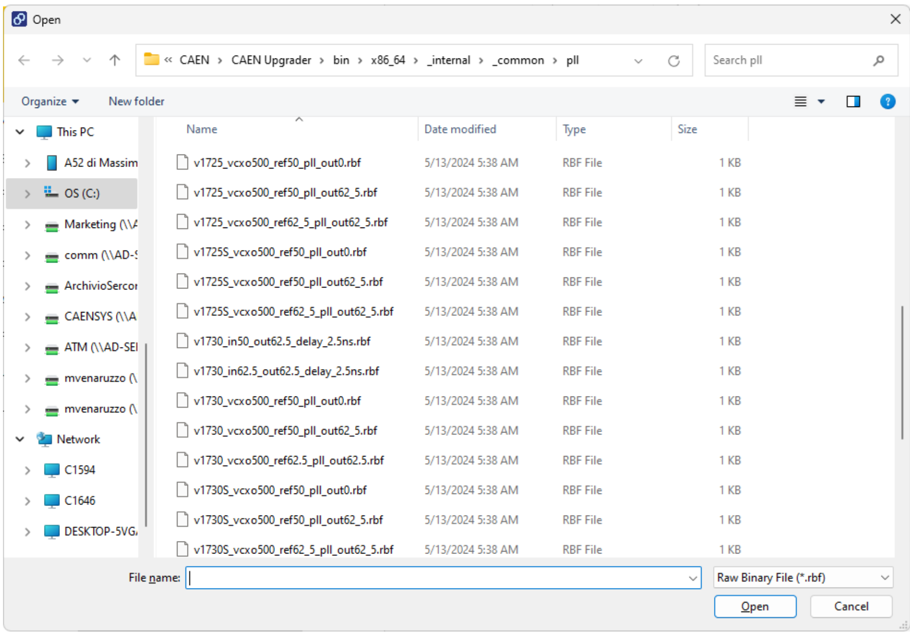


- Press "Save" button to save the PLL .rbf file to the desired location on the pc and close the PLL editor.
- Press the "Upgrade PLL" button and select the PLL .rbf file previously generated. CAEN Toolbox will automatically start the file upload and the PLL programming. Once the file upload is completed the following message appears.



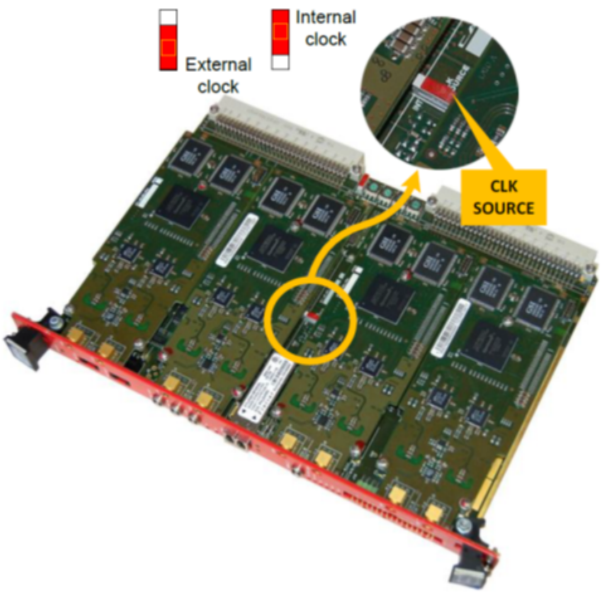
- Power off and on the crate to apply the new PLL configuration.

* if the master digitizer is a V1725(S) or a V1730(S) user can follow the same procedure described here above or press directly the "Upgrade PLL" button.
  - In the browser folder, select the file corresponding to the board model like "v1725_vcxo500_ref50_pll_out62_5.rbf" and press open.

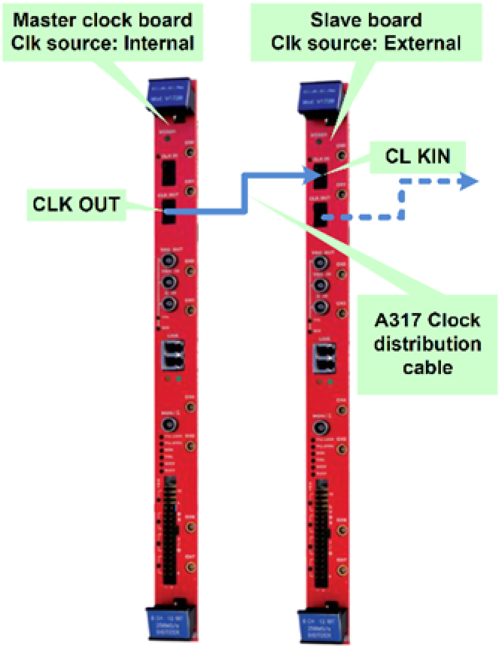


- CAEN Toolbox will automatically start the file upload and the PLL programming. Once the file upload is completed the same previous message appears.

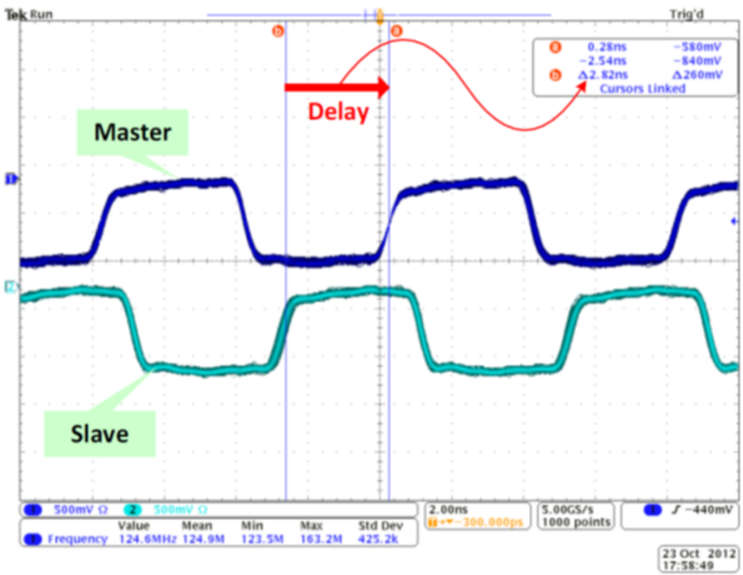
- The PLL of the slave must be reprogrammed to accept in input the 62.5 MHz frequency only if it is a V1725(S) a V1730(S) or a V1740D. All the other digitizer families are indeed already programmed to accept in input the 50 MHz frequency. Other digitizer families have to be programmed to provide in output the 50 MHz only if they are not the last board of the chain.
  - From CAEN Toolbox follow the same procedure above described to connect to the slave board
  - Depending on the digitizer model, proceed with the PLL file generation or selection from the available list files as described in the above paragraphs.
  - Upgrade the PLL firmware into the V17XX.
- Power off the crate.
- Move the DIP switch of the V17XX (slave) from internal to external



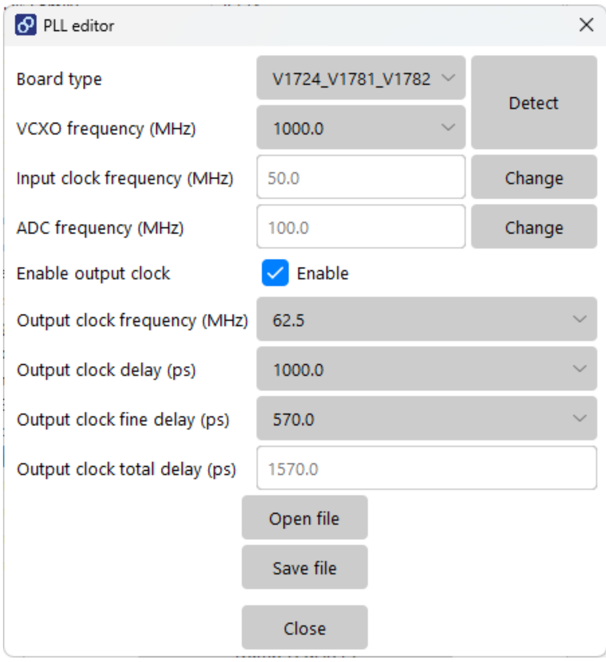
- Connect the A317 cable from the CLOCK OUT connector of master to CLOCK IN connector of slave



- Switch on the crate. The CLOCK IN led of the slave board must be ON; The PLL LOCK led of both boards must be ON.
- To verify that the two clocks are latched and to measure the delay between them, it is possible to provide to the TRG OUT connector the clock and check it from an oscilloscope. In CoMPASS, go into the Sync/Trg tab within **each single board** Settings Tab and select **TRG OUT mode** → **Sampling clock**
- Connect the TRG OUT connector output of each board to an oscilloscope and the check:
  – There is no reciprocal jitter between each other.
  – Measure the delay according to the following scheme



- Reprogram the master board with a PLL file with a delay value as closest as possible to the measured one.

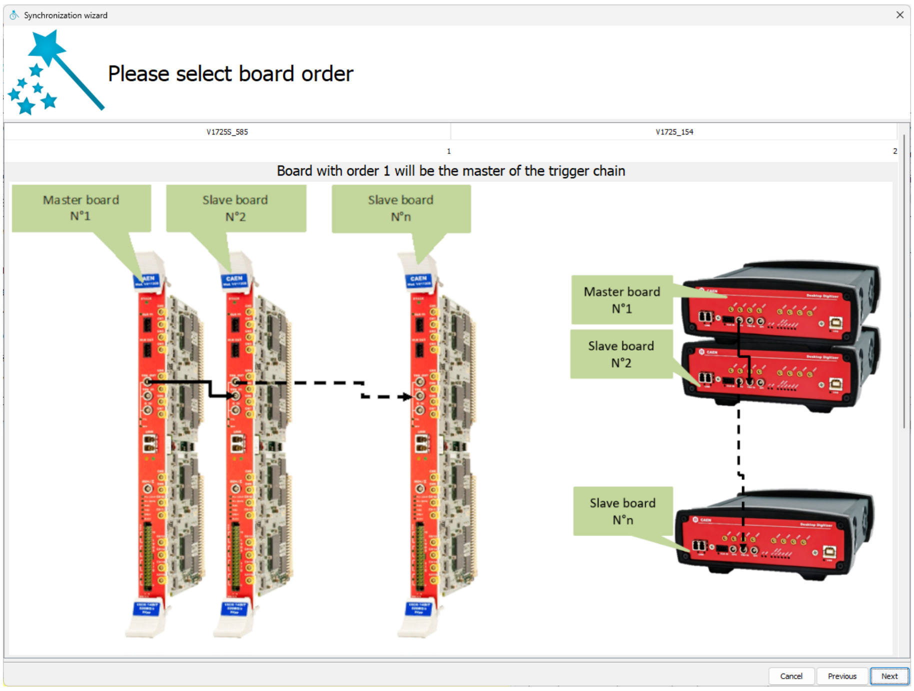


Note: In case of a system composed by digitizer of different families and including V1725(S) and V1730(S) digitizers, it is recommended to put such modules at the end of the chain. They will then receive the 50 MHz reference clock and propagate the 62.5 MHz reference clock to the other V1725(S) and V1730(S).

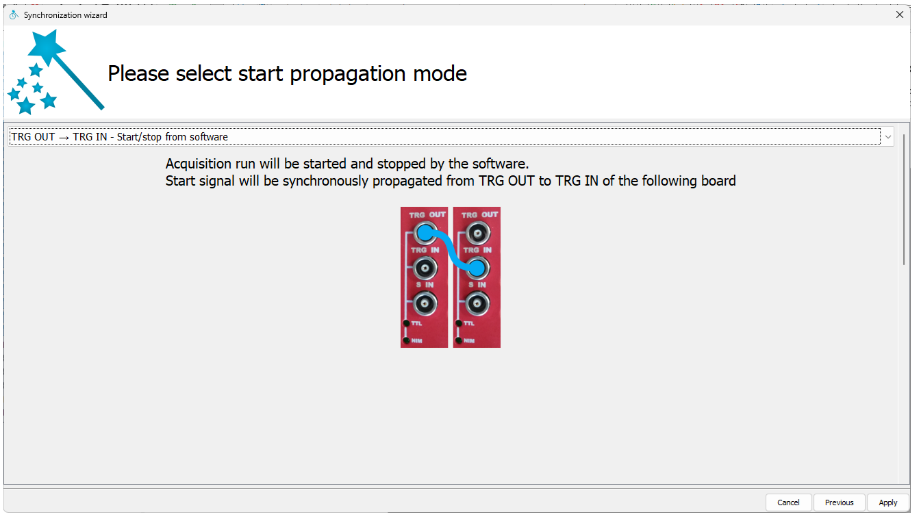
In case the clock of a slave board has been modified to accept an external clock frequency different from 50 MHz, when the clock source it set back to the internal one, before using again the digitizer, the user must remember to program the board PLL again with the default 50 MHz PLL file. Missing such digitizer reprogramming might lead either to the impossibility for the digitizer to lock the PLL or to a digitizer wrong events timestamp information provision.

Phase 2: the ***start_acquisition* propagation**.

1. Connect the TRG OUT connector of master V17XX with TRGIN connector of the first slave V17XX through a LEMO-LEMO cable and proceed this way building a daisy chain with all the digitizer belonging to the system.
2. Open the CoMPASS software and select ”Menu → Synchronization wizard”. In the second tab, set the board order



3. In the third tab, choose one of the available *start_acquisition* propagation option, for example the TRGOUT_TRGIN_OUT option:



4. You can adjust the run delay from master to slave by providing a single pulse into the two boards and check the reported time stamp. This step is not fundamental, the relative delay can be adjusted offline by software.

The two boards are now synchronized and the customer can start the acquisition by pressing the START button in CoMPASS.

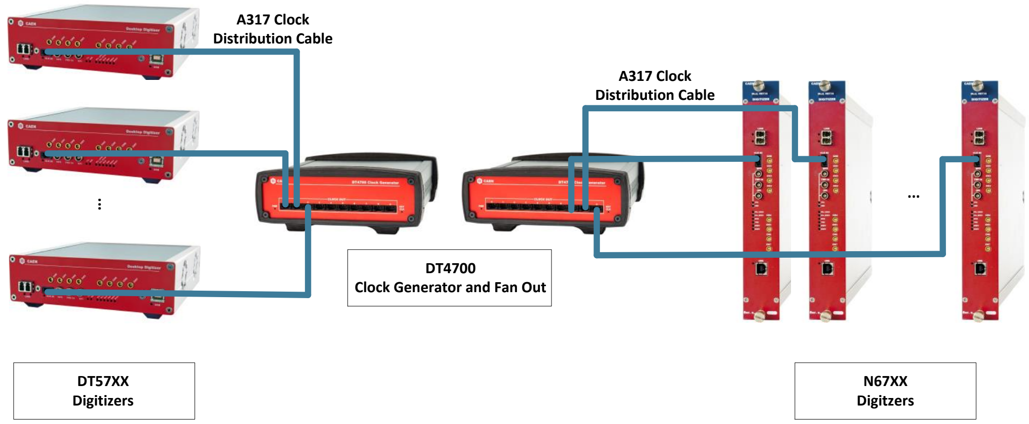
6.2 Synchronization of the Desktop DT57XX and NIM N67XX digitizers

In the following, one DT57XX/N67XX digitizers acts as the master board while the others act as slaves for what concern the *start_acquistion* signal propagation only. The clock signal are, on the contrary distributed in FAN OUT mode because the DT57XX/N67XX digitizers do not feature the CLK OUT connector. A clock generator like the DT4700 model is then required in such a configuration.

Required software: CoMPASS only.

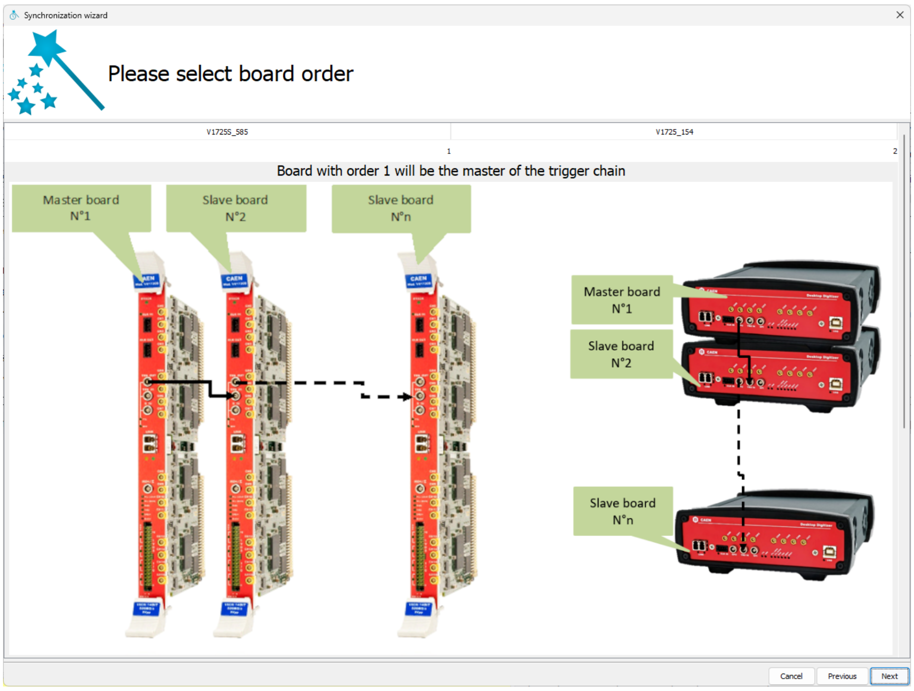
Phase 1: the **clock synchronization**:

1. There is no need to reprogram the digitizer PLL in this case because the DT57XX/N67XX boards are already configured to work with the 50 MHz input clock. It is just required to configure the digitizer so that the reference clock is the external one instead on the internal one. This is done automatically by CoMPASS during the synchronization wizard.
2. There is no need to check the reference clock delay among the boards because the clock is provided to all the digitizers in FAN OUT mode.
3. Connect the A317 cable from the DT4700 CLOCK OUT connector to the DT57XX/N67XX CLOCK IN connector.

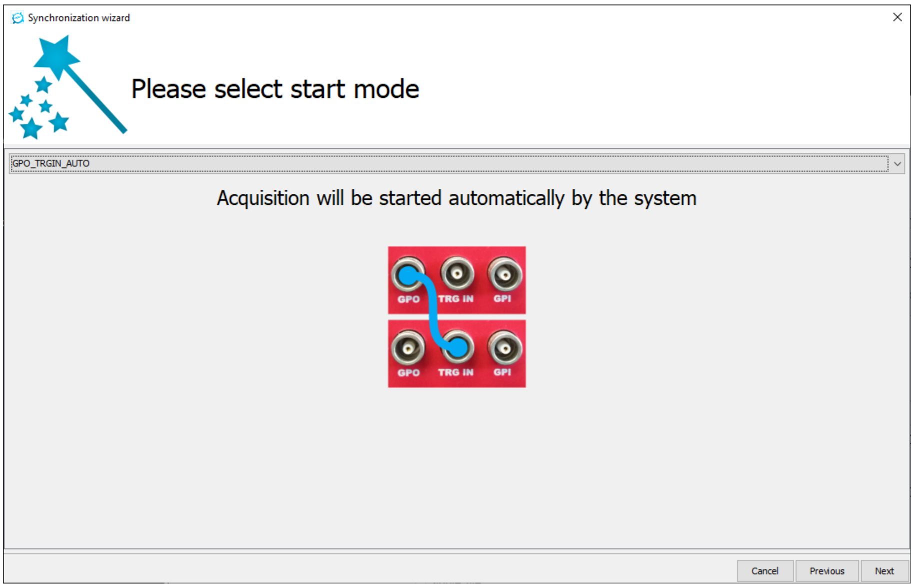


Phase 2: the ***start_acquisition* propagation**.

1. Connect the GPO OUT connector of master DT57XX/N67XX with TRG IN connector of the first slave DT57XX/N67XX through a LEMO-LEMO cable and proceed this way building a daisy chain with all the digitizer belonging to the system.
2. Open the CoMPASS software and select ”Menu → Synchronization wizard”. In the second tab, set the board order



3. In the third tab, choose one of the available *start_acquisition* propagation option, for example the GPO_TRGIN_AUTO option:



4. You can adjust the run delay from master to slave by providing a single pulse into the two boards and check the reported time stamp. This step is not fundamental, the relative delay can be adjusted offline by software.

The two boards are now synchronized and the customer can start the acquisition by pressing the START button in CoMPASS.

6.3 Synchronization of the VME V27XX and desktop DT27XX digitizers

In the following, one V27XX/DT57XX digitizer acts as the master board while the others act as slaves. The idea is to lock the clocks of all the digitizers and to propagate the start of run in a daisy chain configuration.

Required software:

- CoMPASS only

The **clock synchronization** and the ***start_acquisition*** **propagation** are done together through the CoMPASS Synchronization Wizard

1. Connect the A319 cable from the CLOCK OUT connector of the master to CLOCK IN connector of slave

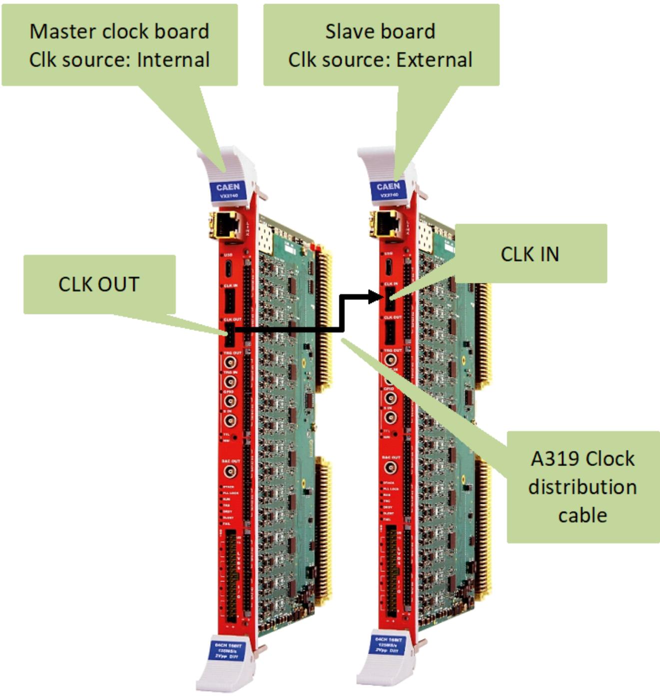


Fig. 6.1: V/VX27xx case.

2. There is no need of additional cable connection because the start_acquisition signal is propagated from the master to the slave(s) by the A319 cable

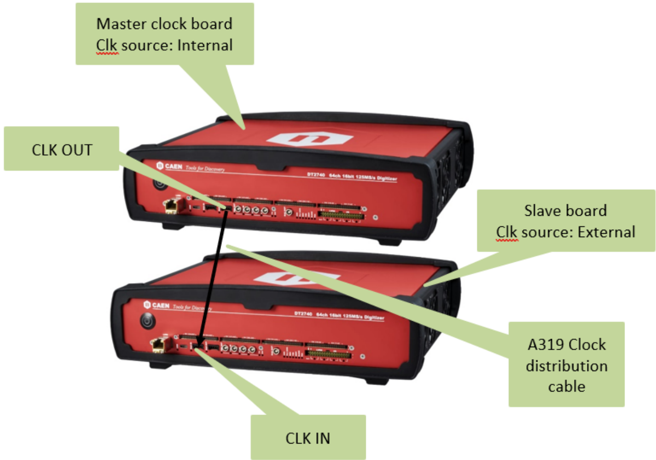
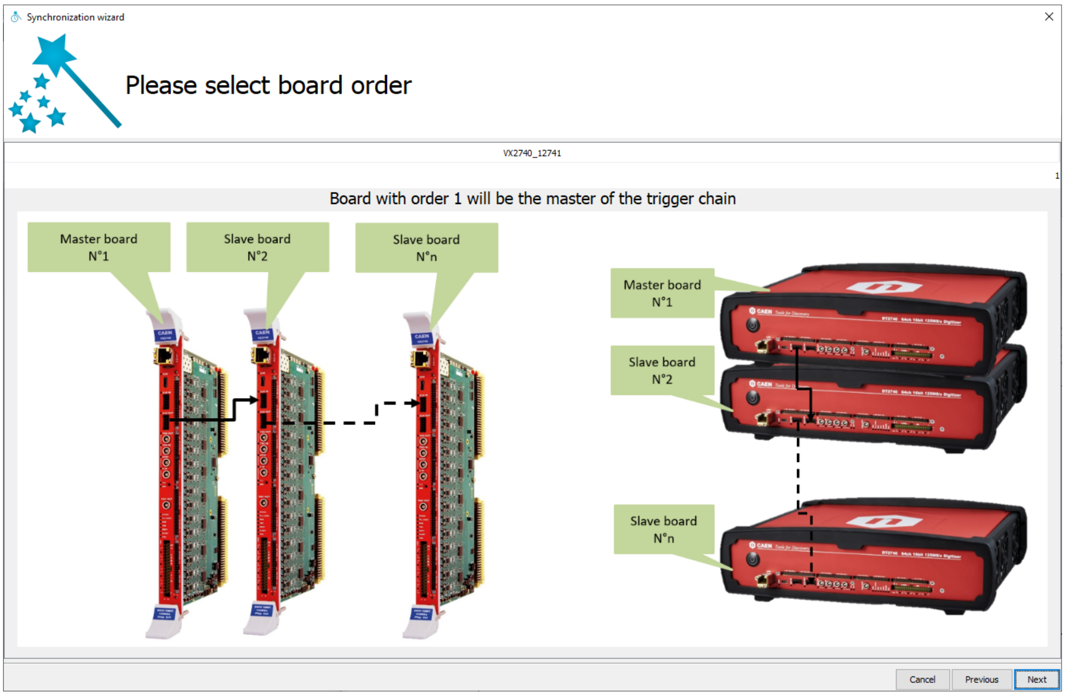
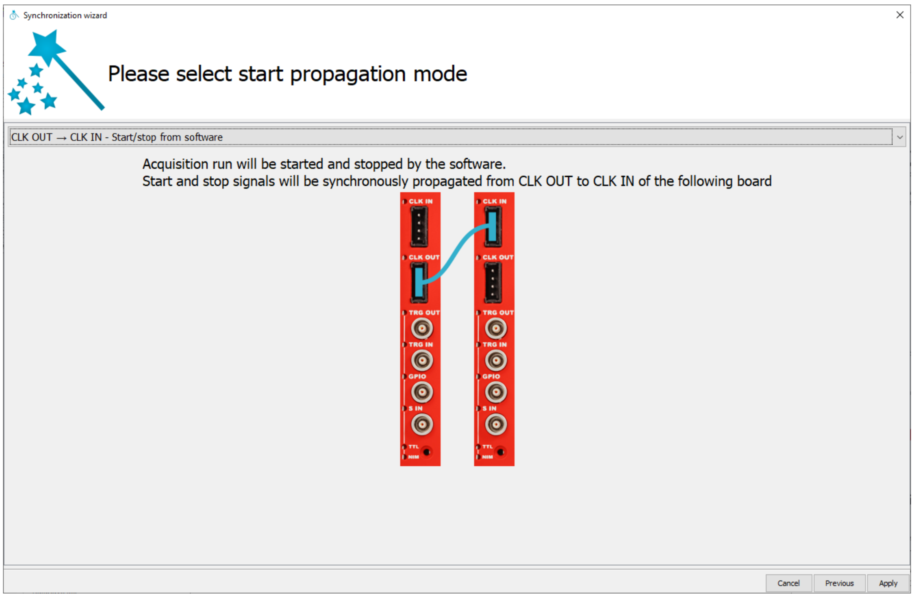


Fig. 6.2: DT27xx case.

3. Open the CoMPASS software and select "Menu → Synchronization wizard". In the second tab, set the board order



4. In the third tab, choose one of the available *start_acquisition* propagation option, for example ”CLK OUT → CLK IN - Start/stop from software” option:



5. Press Apply to have CoMPASS applying the synchronization settings
6. The CLOCK IN led of the slave board must be ON; the PLL LOCK led of both boards must be ON.
7. You can adjust the run delay from master to slave by providing a single pulse into the two boards and check the reported time stamp. This step is not fundamental, the relative delay can be adjusted offline by software.

The two boards are now synchronized and the customer can start the acquisition by pressing the START button in CoMPASS.

6.4 Synchronization of the VME V17XX and V/VX/DT27XX digitizers

When it is required to synchronize a systerm composed by a mixed 17XX and 27XX, the advice is to group the 17XX and the 27XX digitizer together and to setup the system in order to get the 17XX digitizer as the firsts in the chain. In this way there will bi a single discontinuity point between the last 17xx and the first 27xx.

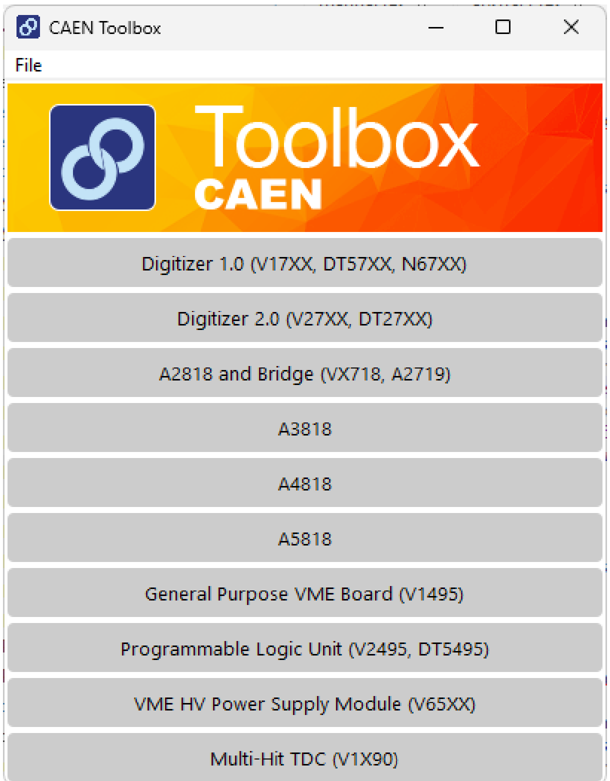
In the following, a V17XX digitizer acts as the master board while a V27XX act as slaves. The idea is to lock the clocks of all the digitizers and to propagate the start of run in a daisy chain configuration.

Required software:

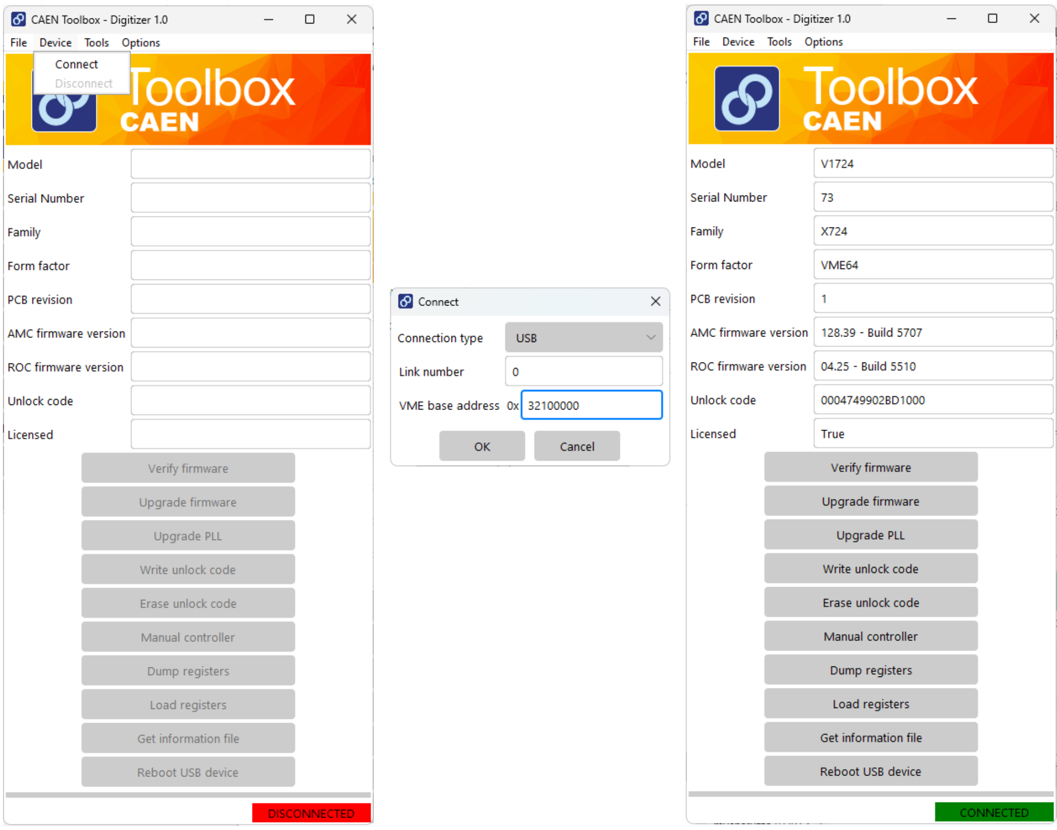
- CAEN Toolbox
- CoMPASS

Phase 1: the **clock synchronization**:

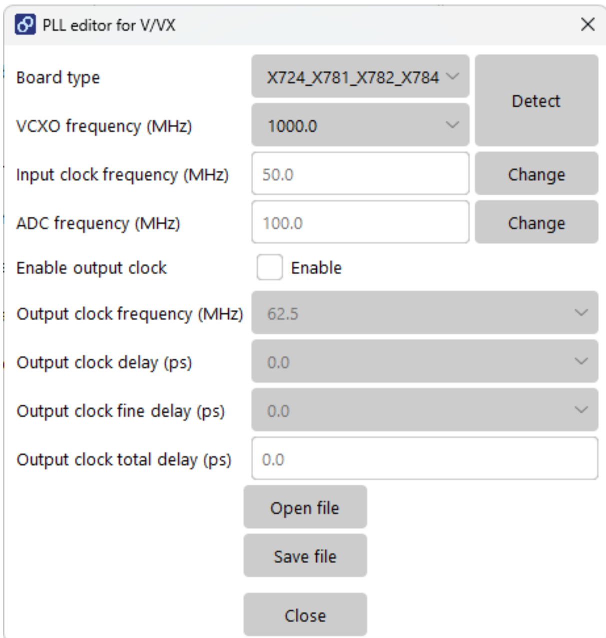
1. The PLL of the V17xx must be reprogrammed to provide on the CLOCK OUT connector the 62.5 MHz frequency.
    - Open CAEN Toolbox, select "Digitizer 1.0".



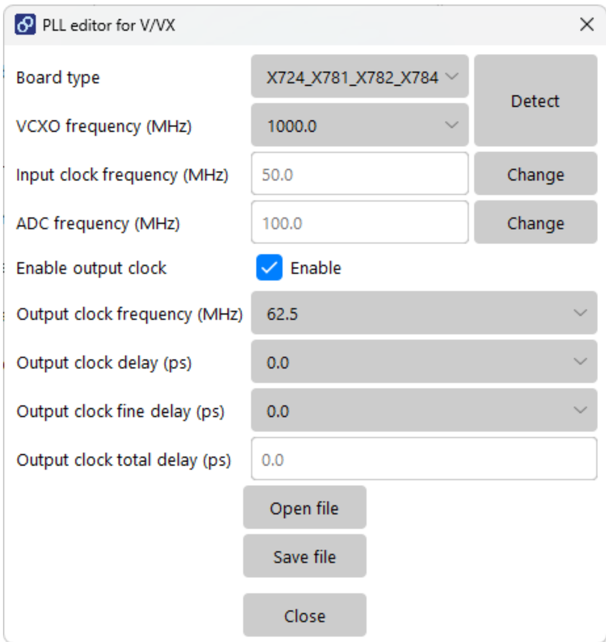
- from the top menu select Device → Connect, insert the digitizer connection parameters and press Connect.



- if the master digitizer is a V1720, V1724, V1740D, V1751 or V1782, select Tools → PLL Editorfor V/VX from the top menu. The PLL Editor will open. Press ”Detect” button to detect the currently connected digitizer.

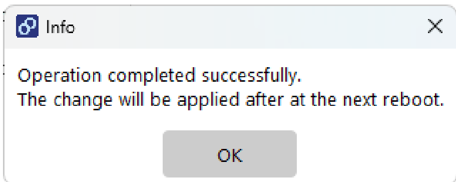


– Tick ”Enable clock output” and select the clock output frequency depending on the slave digitizer model. Set the Clock output delay if required.



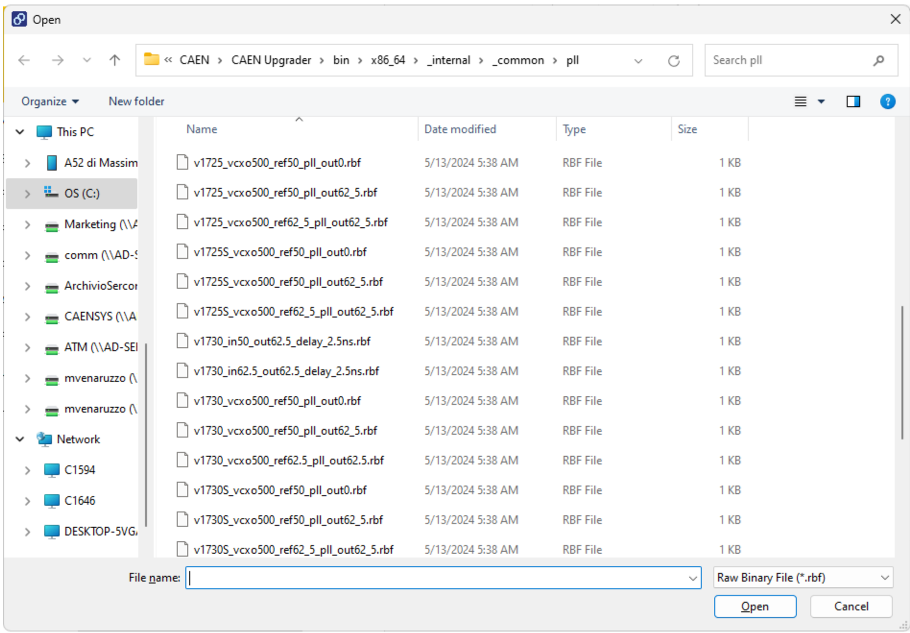
– Press ”Save” button to save the PLL .rbf file to the desired location on the pc and close the PLL editor.

– Press the ”Upgrade PLL” button and select the PLL .rbf file previously generated. CAEN Toolbox will automatically start the file upload and the PLL programming. Once the file upload is completed the following message appears.



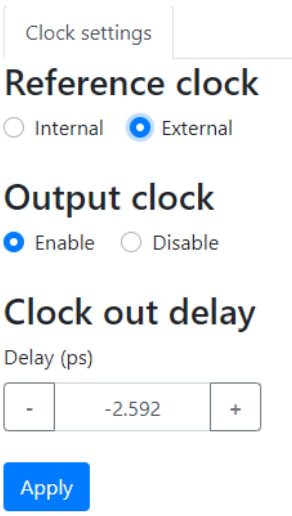
– Power off and on the crate to apply the new PLL configuration.

- if the master digitizer is a V1725(S) or a V1730(S) user can follow the same procedure described here above or press directly the ”Upgrade PLL” button.
  – In the browser folder, select the file corresponding to the board model like ”v1725_vcxo500_ref50_pll_out62_5.rbf” and press open.

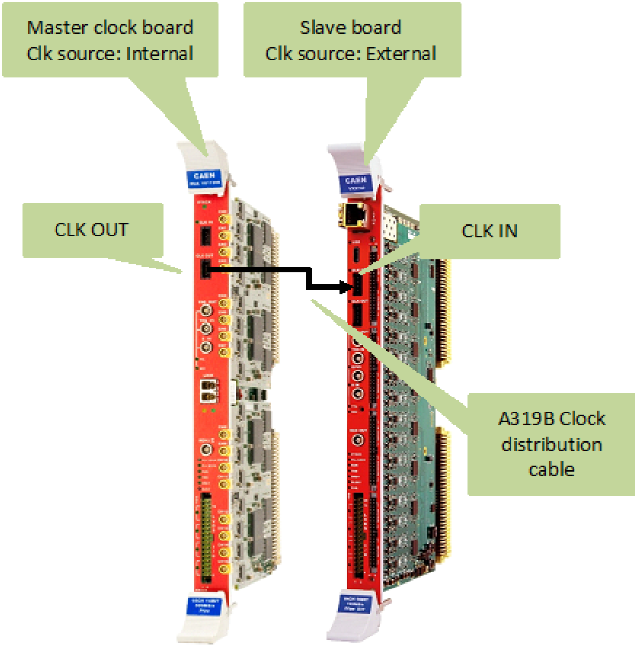


- CAEN Toolbox will automatically start the file upload and the PLL programming. Once the file upload is completed the same previous message appears.

- The PLL of the slave already accept in input the 62.5 MHz clock and it must be programmed to accept the external clock signal.
  - Open the VX27XX/DT27XX Web Interface, select ”Clock Settings”.
  - Select Reference clock ”External”, Output clock ”Enable” and press Apply for the slave board



– Connect the A319B cable from the CLOCK OUT connector of the master to CLOCK IN connector of slave



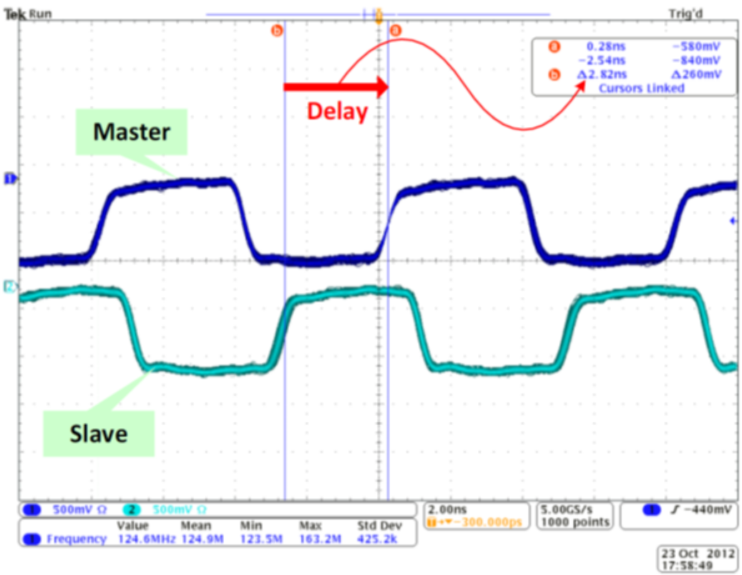
– Switch on the crate. The CLOCK IN led of the slave board must be ON; the PLL LOCK led of both boards must be ON.

– To verify that the two clocks are latched and to measure the delay between them, it is possible to provide to the TRG OUT connector the clock and check it from an oscilloscope. In CoMPASS, go into the Sync/Trg tab within **each single board** Settings Tab and select **TRG OUT mode** $\rightarrow$ **PLL clock**

– Connect the TRG OUT connector output of each board to an oscilloscope and the check:

  ∗ There is no reciprocal jitter between each other.

  ∗ Measure the delay according to the following scheme

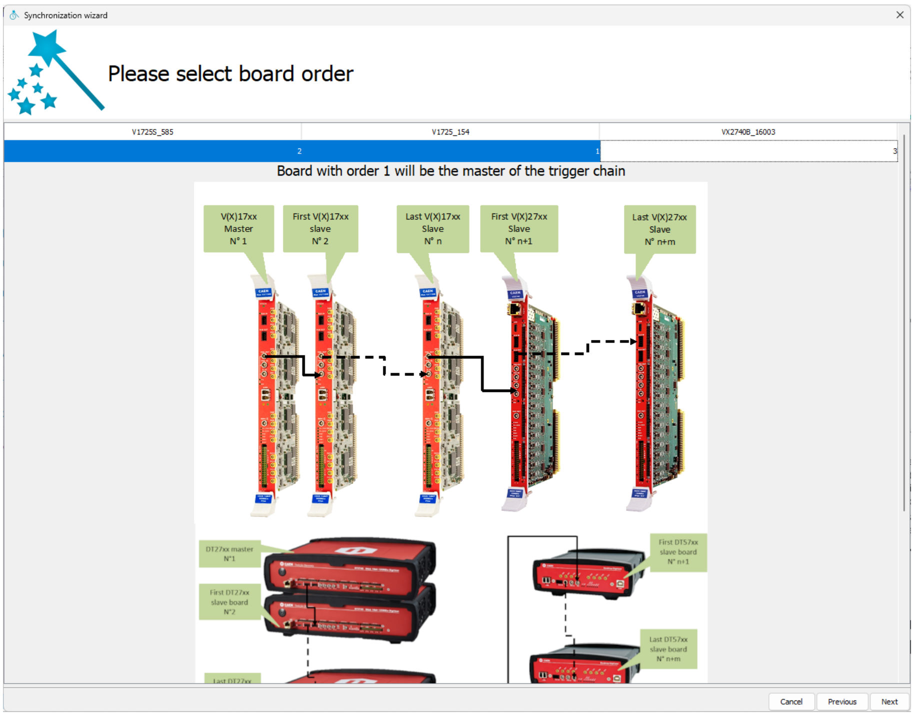


> **In case the clock of a V17XX slave board has been modified to accept an external clock frequency different from 50 MHz, when the clock source it set back to the internal one, before using again the digitizer, the user must remember to program the board PLL again with the default 50 MHz PLL file. Missing such digitizer reprogramming might lead either to the impossibility for the digitizer to lock the PLL or to a digitizer wrong events timestamp information provision.**

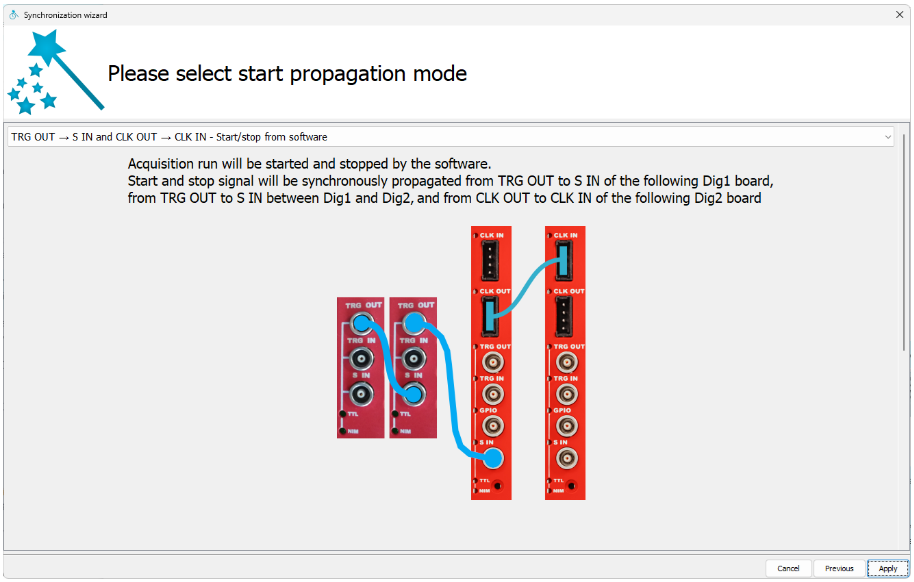
Phase 2: the ***start_acquisition* propagation**.

(a) All the V17XX possibly present in the chain must be daisy chained with the TRG OUT - S IN connection. Connect the TRG OUT connector of master V17XX (or the last V17xx slave) with S-IN connector of the first slave V27XX through a LEMO-LEMO cable. The rest of the slaves 27xx (if any) can be daisy chained simply connectin the CLK-OUT and CLK-IN 4 pin connector as explained in the previous section.

(b) Open the CoMPASS software and select ”Menu → Synchronization wizard”. In the second tab, select the board order



(c) In the third tab, choose one of the available *start_acquisition* propagation option, for example the TRG OUT → S IN and GPO → GPI option:



(d) You can adjust the run delay from master to slave by providing a single pulse into the two boards and check the reported time stamp. This step is not fundamental, the relative delay can be adjusted offline by software.

The two boards are now synchronized and the customer can start the acquisition by pressing the START button in CoMPASS.

6.5 Synchronization of the Desktop DT57XX/NIM N67XX and DT27XX digitizers

This section may include two kind of operative scenarios:

1. one or more DT27XX and one DT57XX (Case A)
2. one or more DT27XX and more DT57XX (Case B)

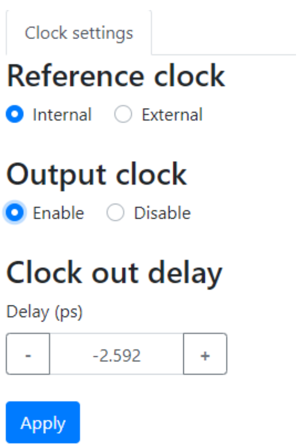
In the first case, no additional hardware is required, and the (last) DT27XX acts as the master board while the DT57XX and the slave one. In the second case a DT4700 Clock Generator is required in order to provide the 62.5 MHz reference clock to all the digitizers; the (last) DT27XX acts as the master board while the DT57XX and the slave one for what concern the propagation of the start_acquisition signal only.

Required software:

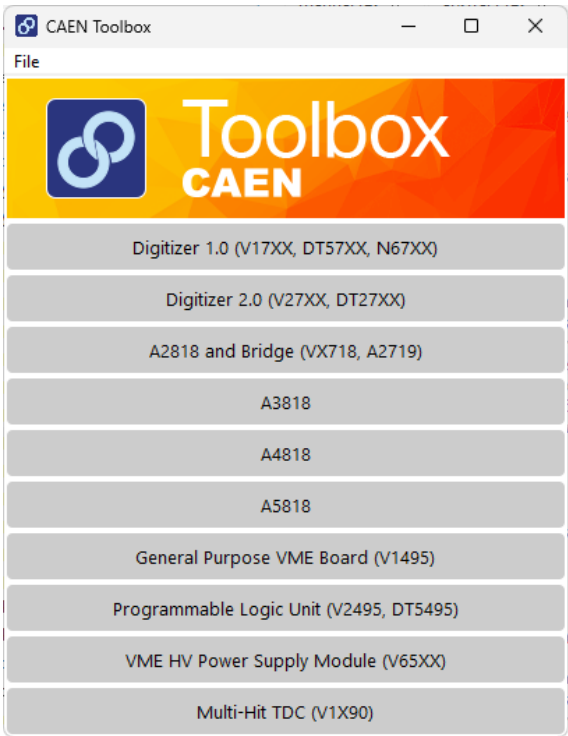
- VX27XX/DT27XX Web Interface;
- CAEN Toolbox
- CoMPASS

Phase 1: the **clock synchronization**:

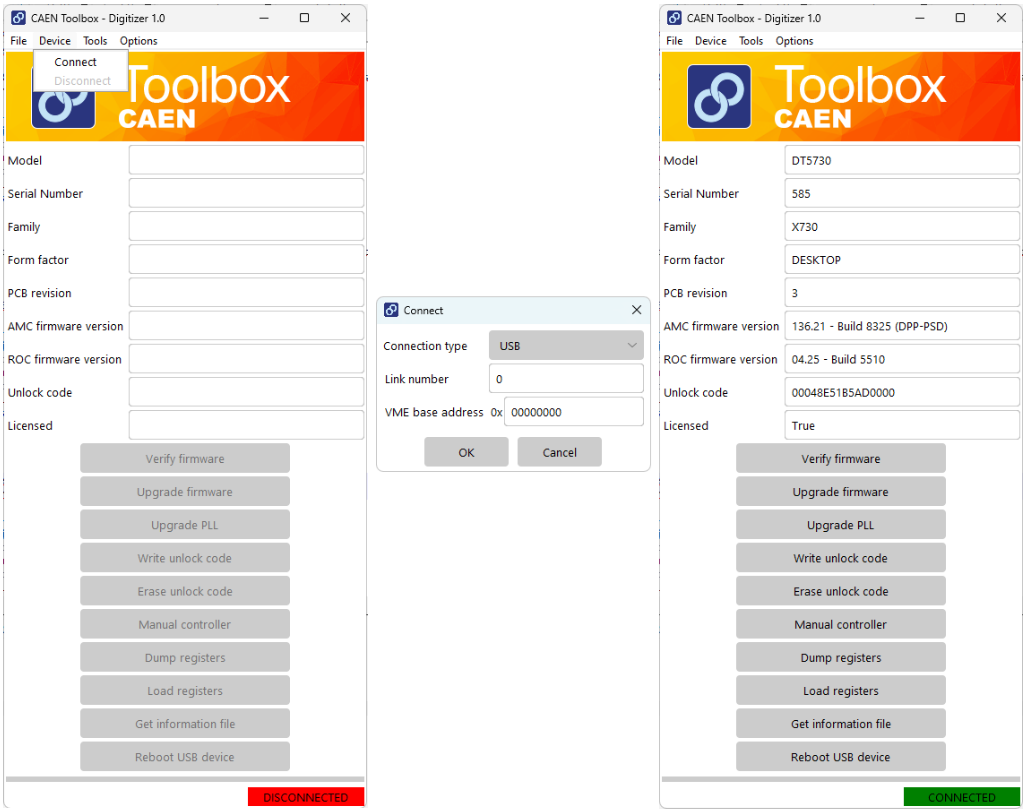
1. **In Case A**, the PLL of the master must be reprogrammed to provide the CLOCK OUT (62.5 MHz).
   - Open the DT27XX Web Interface, select ”Clock Settings”.
   - Select Reference clock ”Internal”, Output clock ”Enable” and press Apply for the master board



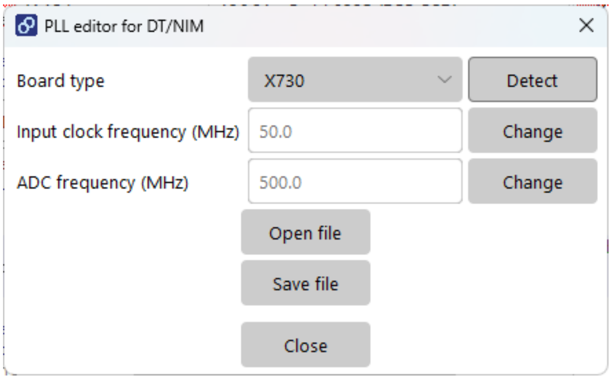
2. The PLL of the slave must to be reprogrammed to accepts the 62.5 MHz clock. This can be done using CAEN Toolbox (TO BE IMPLEMENTED)
   - Open CAEN Toolbox, select ”Digitizer 1.0”.



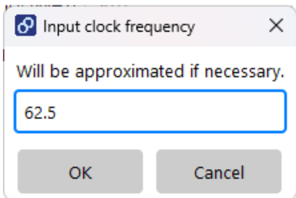
- from the top menu select Device → Connect, insert the digitizer connection parameters and press Connect.

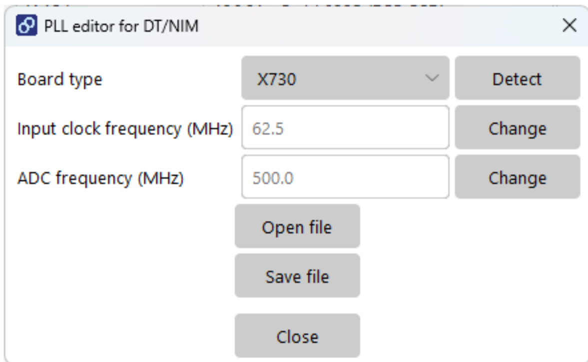


- Select Tools → PLL Editor for DT/NIM from the top menu. The PLL Editor will open. Press ”Detect” button to detect the currently connected digitizer.

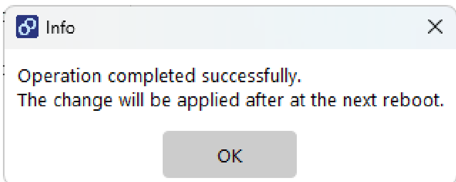


  – Press ”Change” button to modify the accepted Input clock frequency. Then press ”Ok” to confirm





  – Press ”Save” button to save the PLL .rbf file to the desired location on the pc and close the PLL editor.
  – Press the ”Upgrade PLL” button and select the PLL .rbf file previously generated. CAEN Toolbox will automatically start the file upload and the PLL programming. Once the file upload is completed the following message appears.



  – Power off and on the crate to apply the new PLL configuration.

3. Connect the A319B cable from the CLOCK OUT connector of the master to CLOCK IN connector of slave

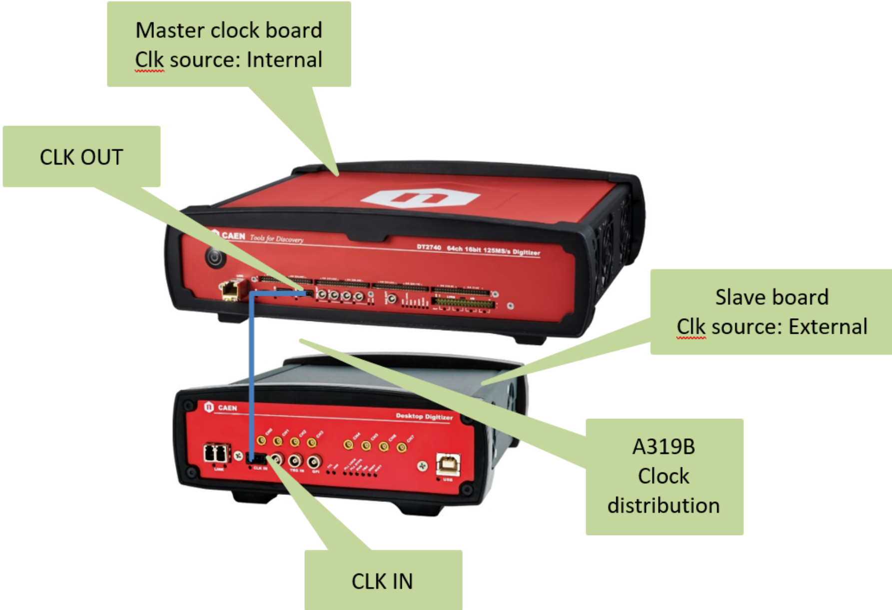


Fig. 6.3: Case A.

4. **In Case B**, it is required to program the PLL of the DT57XX because by default it accept the 50 MHz clock only. To perform this operation, follow the instruction detailed for **Case A**.

5. Connect the A317 cable from the DT4700 CLOCK OUT connector to the DT57XX CLOCK IN connector and the A319B cable from the DT4700 CLOCK OUT connector to the DT27XX CLOCK IN connector.

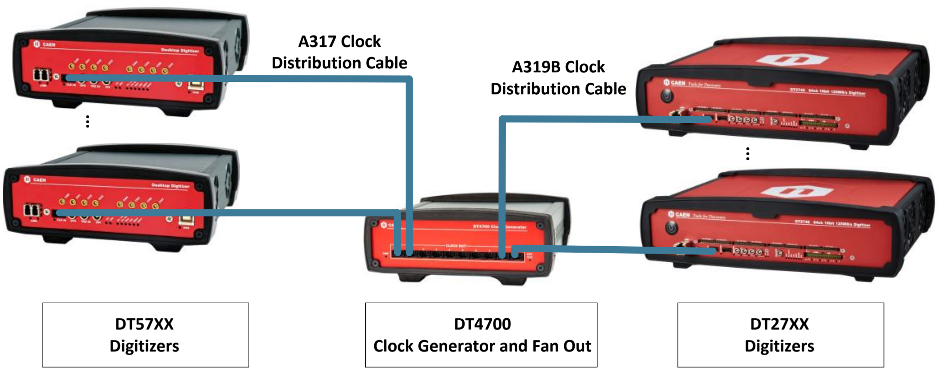


Fig. 6.4: Case B.

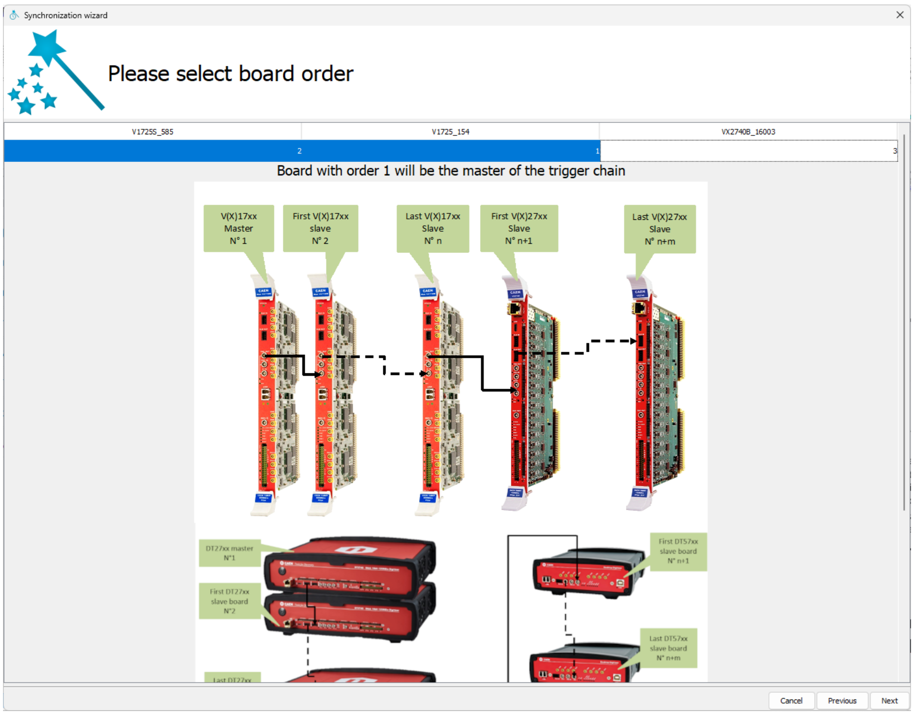
6. The CLOCK IN led of the all the board must be ON; the PLL LOCK led of all the boards must be ON.

7. There is no need to check the reference clock delay among the boards because the clock is provided to all the digitizers in FAN OUT mode.

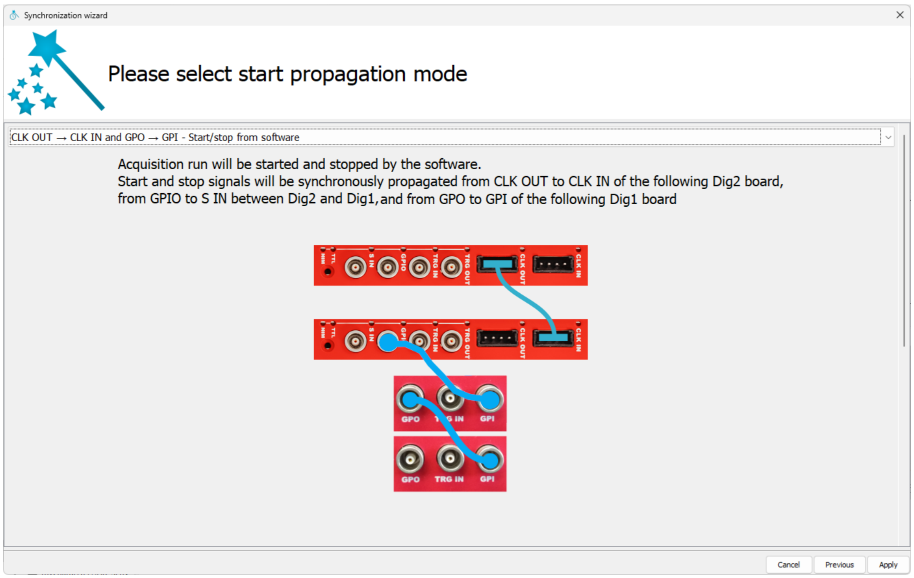
In case the clock of a DT57XX/N67XX slave board has been modified to accept an external clock frequency different from 50 MHz, when the clock source it set back to the internal one, before using again the digitizer, the user must remember to program the board PLL again with the default 50 MHz PLL file. Missing such digitizer reprogramming might lead either to the impossibility for the digitizer to lock the PLL or to a digitizer wrong events timestamp information provision.

Phase 2: the ***start_acquisition* propagation**.

1. In both Cases A and B Connect the GPIO connector of master (or the last) DT27XX either with the GPI of the first slave DT57XX through a LEMO-LEMO cable. The rest of the DT57xx slaves (if any) have to be daisy chained through the GPO-GPI connectors. If more DT27xx are included in the system they can be daisy chained using the CLK OUT - CLK IN connector chain as explained in the dedicated section.
2. Open the CoMPASS software and select ”Menu → Synchronization wizard”. In the second tab, select the board order



3. In the third tab, choose one of the available *start_acquisition* propagation option, for example the CLK OUT → CLK IN and GPO → GPI option.



4. You can adjust the run delay from master to slave by providing a single pulse into the two boards and check the reported time stamp. This step is not fundamental, the relative delay can be adjusted offline by software.

The two boards are now synchronized and the customer can start the acquisition by pressing the START button in CoMPASS.

7 Dead time evaluation in CoMPASS

CoMPASS provides a dead time estimation based on the data coming from the board and allows the user to have access to the same data to evaluate the deadtime by his/her own. CoMPASS indeed allows the user to save the *Raw* acquisition data, i.e. including the saturations and pileup events usually not included in the spectra but required to provide the dead time estimation. The list file includes a column in which additional information about each event is included and coded in a flag (see Sec. **Save the list of Trigger Time Stamp, Energy, PSD and waveforms**).

7.1 Dead time estimation with the DPP-PSD firmware

The deadtime percentage is estimated by CoMPASS as:

$$1 - \frac{(\text{output\_events} + \text{events\_discarded\_by\_user\_selection} + \text{saturation\_events})}{\text{input\_events}} \tag{7.1}$$

The critical point is how to properly estimate the number of input events. In order to do it, CoMPASS sums up the following events:

- output events going into the energy spectrum;
- events rejected by user selection, if any;
- events rejected by the software time sorting algorithm;
- events rejected because of the saturation of the digitizer input stage;
- pile up events counted twice because, in case of two overlapping events within the integration gate, the second one will not have its own trigger and the pile up rejector algorithm will tag only the first one;
- the so called ”poissonian events”.

The last point goes as follows and it is the sum of two kind of events:

- estimated lost events during the Trigger Hold-Off time: using a recursive procedure, a Poisson distribution is generated whose average value λ is the ICR $\times$ Trigger Hold-Off time.

  $$\text{P(n\_events\_lost\_during\_THO)} = \frac{\lambda^n}{n!}e^{-\lambda} \tag{7.2}$$

  where λ = ICR $\times$ Trigger Hold-Off.

  The starting point is the first ICR and then with a recursive procedure improves the estimation at each iteration;
- estimated lost events during a memory full condition: when an event is tagged with the *memory full* flag (0x10) the software does a small Montecarlo simulation in which it emulates a Poisson distribution whose average value is the ICR $\times$ Memory Full time. The time interval used for this simulation is the difference between the timestamp of the events tagged with the *memory full* flag and the last event without this flag.

Note: in the DPP-PSD firmware case, no estimation of lost events during the saturation of the input stage is performed. This is due to the fact that in the DPP-PSD firmware there is no parameter that allows the software to know the decay time of the input signal and because the typical signals used in the DPP-PSD case are fast and so the probability of a signal overlap during an input stage saturation is low unless the input rate is very high. This means that a correction taking into account this effect will be a higher order correction.

7.2 Dead time estimation with the DPP-PHA firmware

The deadtime percentage is estimated by CoMPASS as:

$$1 - \frac{(\mathrm{output\_events} + \mathrm{events\_discarded\_by\_user\_selection} + \mathrm{saturation\_events})}{\mathrm{input\_events}} \tag{7.3}$$

As in the previous case, the critical point is how to properly estimate the number of input events. In order to do it, CoMPASS sums up the following events:

- output events going into the energy spectrum
- events rejected by user selection, if any
- events rejected by the software time sorting algorithm
- events rejected because the saturation of the digitizer input stage
- pile up events
- the so called ”poissonian events”

The last point goes as follows and it is the sum of two kind of events:

- estimated lost events during the Trigger Hold-Off time: using a recursive procedure, a Poisson distribution is generated whose average value λ is the ICR $\times$ Trigger Hold-Off time.

  $$P(\mathrm{n\_events\_lost\_during\_THO}) = \frac{\lambda^n}{n!}e^{-\lambda} \tag{7.4}$$

  where λ = ICR $\times$ Trigger Hold-Off.

  The starting point is the first ICR and then with a recursive procedure improves the estimation at each iteration;
- estimated lost events during a saturation of the input range: if an events is flagged as saturated, the software does a small Montecarlo simulation in which it emulates a Poisson distribution whose average value is the ICR $\times$ Saturation time. The time interval used for this simulation is the signal Trapezoid Decay Time taken as the best estimation of the time required for the digitizer/MCA input stage to come out of the saturation condition.

  $$P(\mathrm{n\_events\_lost\_during\_input\_saturation}) = \frac{\lambda^n}{n!}e^{-\lambda} \tag{7.5}$$

  where λ = ICR $\times$ Trapezoid Decay Time.

  If the first emulated events falls in the time interval that is the minimum value between the trapezoid decay time and the distance between the saturated event and the first following good event then this emulated event is included in the ICR and the emulation proceed. If this events falls outside that time interval or also after a time corresponding to the trapezoid decay time, it is assumed that event would have been detected and so not added to the ICR. When the latter case occurs, the Montecarlo emulation is stopped.

8 Technical Support

To contact CAEN specialists for requests on the software, hardware, and board return and repair, it is necessary a MyCAEN+ account on www.caen.it:

https://www.caen.it/support-services/getting-started-with-mycaen-portal/

All the instructions for use the Support platform are in the document:

A paper copy of the document is delivered with CAEN boards.
The document is downloadable for free in PDF digital format at:

https://www.caen.it/safety-information-product-support

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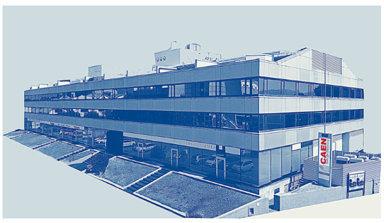

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