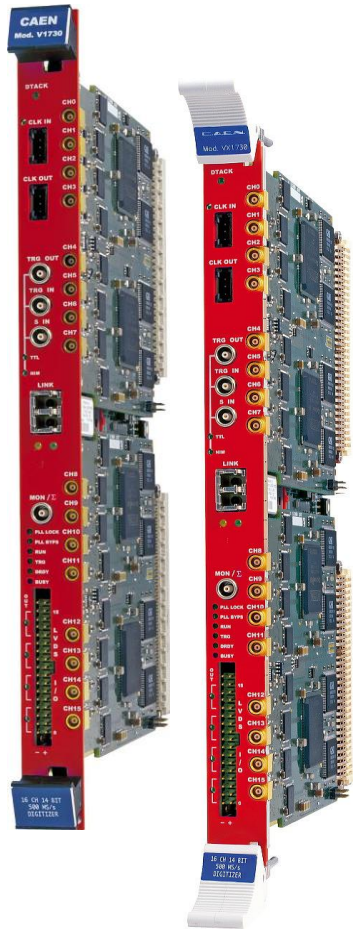
Rev. 9 - February 3rd, 2025

V1730/VX1730 & V1725/VX1725

16/8-channel 14-bit 500/250 MS/s Digitizer



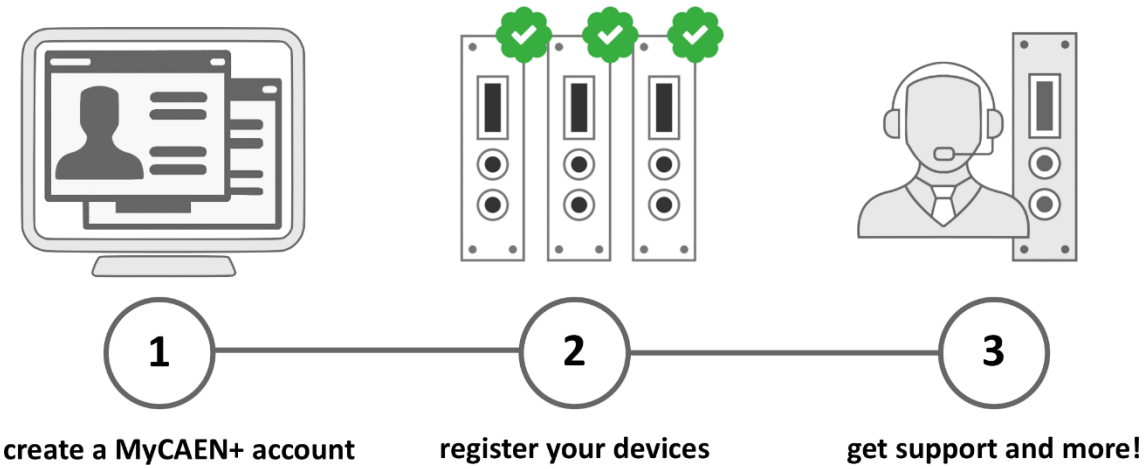
CAEN
Tools for Discovery

User Manual
UM2792

Register your device

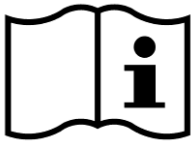
Register your device to your **MyCAEN+** account and get access to our customer services, such as notification for new firmware or software upgrade, tracking service procedures or open a ticket for assistance. **MyCAEN+** accounts have a dedicated support service for their registered products. A set of basic information can be shared with the operator, speeding up the troubleshooting process and improving the efficiency of the support interactions.

MyCAEN+ dashboard is designed to offer you a direct access to all our after sales services. Registration is totally free, to create an account go to https://www.caen.it/become-mycaenplus-user **and fill the registration form with your data.**



https://www.caen.it/become-mycaenplus-user/

Purpose of this Manual



This document contains the full hardware description of the V1730/VX1730 and V1725/VX1725 CAEN digitizers operating as **Waveform Recording Digitizer** (based on the hereafter called *"waveform recording firmware"*).

The reference firmware revision is**: 4.29_0.9** for V1730/VX1730/V1725/VX1725 and **4.29_0.4** for V1730S/VX1730S/V1725S/VX1725S.

For higher releases compatibility, check in the firmware revision history files.

For any reference to registers in this document, please refer to document [RD3] on the digitizer web page.

For any reference to DPP firmware in this document, please refer to [RD9][RD11][RD12] present on the firmware web page.

Change Document Record

Date	Revision	Changes
Feb 3rd, 2014	00	Initial release.
Dec 15th, 2014	01	Added new Chap. **7** on temperature protection. Introduced temperature monitoring safety notices. Updated Sec. **Trigger Management**.
Jun 10th, 2016	02	Fully reviewed to the new V1725 digitizer (250 MS/s). Updated Chap. **Technical Specifications**, **Power Requirements**, **Panels Description**, **Firmware and Upgrades,** Sec. **Clock Distribution**, **PLL Mode, Output Clock**, **Channel Calibration**, **Multi-Event Memory Organization**, **Event Structure**, **Acquisition Synchronization** , Trigger **Management**, **Mode 1: TRIGGER**, **Buffer Occupancy Mode**, DPP-PSD Control Software. Added Sec. CaenScope, Sec. MC²A Analyzer.
Sep 24th, 2019	03	Global review. Added support to the new 730S/725S modules. Added Sec.: **DC Offset Individual Setting**, **TRG-IN as Gate**, **CoMPASS**, **DPP-ZLEplus and DPP-DAW Control Software**, **Troubleshooting**.
May 6th, 2020	04	Updated **Tab. 1.1**, Chap. **7**, Sec. **Acquisition Run/Stop**, CaenScope. Added Sec. **Channel Self-Trigger Rate Meter (725S and 730S only)**.
Sep 2nd, 2020	05	Updated Sec. **DPP-ZLEplus and DPP-DAW Control** Software, and power consumption specifications in Chap. **3**, **6**.
May 4th, 2021	06	Updated Sec. **Troubleshooting**, power consumption values in **Tab. 3.1** and list of LVDS adapters in **Tab. 1.1.** Reviewed Sec. **External Trigger Event Structure**. Reviewed Sec. **Mode 1: TRIGGER** and Sec. **Mode 2: nBUSY/nVETO** for DPP firmware. Added **Tab. 10.5** and **Tab. 10.7**. Added more information on the time stamp reset via the S-IN connector in Sec. **Timer Reset**.
March 31st, 2023	07	Updated **Purpose of this Manual** and **Reference Documents**. Added **Manufacturer Contacts**, **Limitation of Responsibility**, **Disclaimer**, **Made in Italy**. Updated **Tab. 1.1**. Updated power consumptions of V1730SB/VX1730SB models and added Baseline RMS Noise in Chap. **3**. Updated Chap. **4**. Added Chap. **5**. Updated Chap. **6**. Updated Sec. **Trigger** Clock, **Trigger Majority Mode**. Updated **Tab. 10.3**. Updated Chap. **11** and Chap. **Technical Support.** Removed Sec. **MC2 Analyzer.**
July 2nd, 2024	08	Removed all CAEN Upgrader references due to software obsolescence and replaced with CAEN Toolbox.
Feb 3rd, 2025	09	Reviewed Cover and End pages. Replaced references to CAENUpgrader with CAENToolbox. Replaced references to CAENScope with WaveDump 2. Removed all MC² Analyzer references to software obsolescence. Added Chap. **7**, Sec. **12.4**, Chap. **15**, Chap. **16**, Chap. **17**. Update **Safety Notices**, Chap. **1**, Tab. **1.1**, Tab. **3.1**, Chap. **4**, Chap. **5**, Tab. **6.1**, Sec. **9.1**, Sec. **10.2**, Sec. **10.3**, Sec. **10.5**, Sec. **10.6**, Sec. **10.6.3**, Sec. **10.6.4**, Sec. **10.6.5**, Sec. **10.7**, Sec. **10.7.3**, Sec. **10.8**, Sec. **10.9.3**, Sec. **10.8**, Fig. **10.19**, Sec. **10.11**, Sec. **10.15**, Sec. **11.1**, Sec. **11.2**, Chap. **12**, Chap. **13**, Sec. **14.1.2**.

Symbols, Abbreviated Terms, and Notations

ADC	Analog-to-Digital Converter
AMC	ADC & Memory Controller
DAQ	Data Acquisition
DAC	Digital-to-Analog Converter
DC	Direct Current
LVDS	Low-Voltage Differential Signal
ROC	ReadOut Controller
GUI	Graphical User Interface
DPP	Digital Pulse Processing
ETTT	Extended Trigger Time Tag

OS	Operating System
PLL	Phase-Locked Loop
PSD	Pulse Shape Discrimination
TTT	Trigger Time Tag
USB	Universal Serial Bus

Reference Documents

[RD1] UM11111 – CAEN Toolbox User Manual
[RD2] AN2086 – Synchronization of a multi-board acquisition system with CAEN digitizers
[RD3] UM5118 – 730-725 Raw Waveform Registers Description
[RD4] UM1934 - CAENComm User & Reference Manual
[RD5] UM1935 - CAENDigitizer User & Reference Manual
[RD6] UM2091 - CAEN WaveDump User Manual
[RD7] GD2483 - WaveDump QuickStart Guide
[RD8] UM7934 – CAEN WaveDump 2 User Manual
[RD9] UM5960 - CoMPASS User Manual
[RD10] UM3185 – CAENDPP User Manual
[RD11] UM5954 – DPP-DAW User Manual
[RD12] UM6064 – DPP-ZLEPlus User Manual
[RD13] GD2728 – How to make Coincidences with CAEN Digitizers
[RD14] GD9764 – CAEN FELib Library User Guide
[RD15] DS7799 - A4818 USB-3.0 to Optical Link Adapter Datasheet
[RD16] UM10551 – A5818 Technical Information Manual
[RD17] UM7685 - V3718/VX3718 VME to USB-2.0/Optical Link Bridge User Manual
[RD18] UM8305 - V4718/VX4718 VME to USB-3.0/Ethernet/Optical Link Bridge User Manual
[RD19] AN2472 - CONET1 to CONET2 migration

https://www.caen.it/support-services/documentation-area/

Manufacturer Contacts

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Limitation of Responsibility

If the warnings contained in this manual are not followed, CAEN will not be responsible for damage caused by improper use of the device. The manufacturer declines all responsibility for damage resulting from failure to comply with the instructions for use of the product. The equipment must be used as described in the user manual, with particular regard to the intended use, using only accessories as specified by the manufacturer. No modification or repair can be performed.

Disclaimer

No part of this manual may be reproduced in any form or by any means, electronic, mechanical, recording, or otherwise, without the prior written permission of CAEN spa.

The information contained herein has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies. CAEN spa reserves the right to modify its products specifications without giving any notice; for up to date information please visit www.caen.it.

Made in Italy

We remark that all our boards have been designed and assembled in Italy. In a challenging environment where a competitive edge is often obtained at the cost of lower wages and declining working conditions, we proudly acknowledge that all those who participated in the production and distribution process of our devices were reasonably paid and worked in a safe environment (this is true for the boards marked "MADE IN ITALY", while we cannot guarantee for third-party manufactures).

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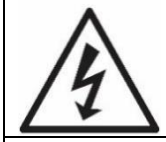
Safety Notices

N.B. Read carefully the "Precautions for Handling, Storage and Installation" document provided with the product before starting any operation.

The following HAZARD SYMBOLS may be reported on the unit:

	Caution, refer to the product manual
	Caution, risk of electrical shock
	Protective conductor terminal
	Earth (Ground) Terminal
	Alternating Current
	Three-Phase Alternating Current

The following symbol may be reported in the present manual:

	General warning statement

The symbol could be followed by the following terms:

- **DANGER**: Indicates a hazardous situation that, if not avoided, will result in serious injury or death.
- **WARNING**: Indicates a hazardous situation that, if not avoided, could result in death or serious injury.
- **CAUTION**: Indicates a situation or condition that, if not avoided, could cause physical injury, or damage the product and/or its environment.

GENERAL NOTICES:

CAUTION: Avoid potential hazards.

USE THE PRODUCT ONLY AS SPECIFIED.

ONLY QUALIFIED PERSONNEL SHOULD PERFORM SERVICE PROCEDURES

CAUTION: Avoid Electric Overload.

TO AVOID ELECTRIC SHOCK OR FIRE HAZARD, DO NOT POWER A LOAD OUTSIDE OF ITS SPECIFIED RANGE

CAUTION: Avoid Electric Shock.

TO AVOID INJURY OR LOSS OF LIFE, DO NOT CONNECT OR DISCONNECT CABLES WHILE THEY ARE CONNECTED TO A VOLTAGE SOURCE

CAUTION: Do Not Operate without Covers.

TO AVOID ELECTRIC SHOCK OR FIRE HAZARD, DO NOT OPERATE THIS PRODUCT WITH COVERS OR PANELS REMOVED

CAUTION: Do Not Operate in Wet/Damp Conditions.

TO AVOID ELECTRIC SHOCK, DO NOT OPERATE THIS PRODUCT IN WET OR DAMP CONDITIONS

CAUTION: Do Not Operate in an Explosive Atmosphere.

TO AVOID INJURY OR FIRE HAZARD, DO NOT OPERATE THIS

PRODUCT IN AN EXPLOSIVE ATMOSPHERE

THIS DEVICE SHOULD BE INSTALLED AND USED BY A SKILLED TECHNICIAN ONLY OR UNDER HIS SUPERVISION

DO NOT OPERATE WITH SUSPECTED FAILURES.
IF YOU SUSPECT THIS PRODUCT TO BE DAMAGED, PLEASE CONTACT THE TECHNICAL SUPPORT

See Chap. **18** for the Technical Support contacts.

VME NOTICES:

CAUTION: This product needs proper cooling.

USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEATING MAY DEGRADE THE MODULE PERFORMANCES!

V1730x/V1730Sx DIGITIZERS CANNOT BE OPERATED WITH CAEN CRATES VME8001/8002/8004/8004A!

CAUTION: This product needs proper handling.

THIS DIGITIZER DOES NOT SUPPORT LIVE INSERTION (HOT-SWAP)!
REMOVE OR INSERT THE BOARD WHEN THE CRATE IS POWERED OFF!

ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE!

1 Introduction

The Mod. V1730 is 1-unit wide VME 6U module housing a 16-channel 14-bit 500 MS/s ADC Waveform Digitizer with software selectable 2 V_{pp} or 0.5 V_{pp} input dynamic range on single ended MCX coaxial connectors. The DC offset is adjustable in the ±1 V (@$2V_{pp}$) or ±0.25 (@$0.5V_{pp}$) range via a 16-bit DAC on each channel (see Sec. **10.1**). A 8-channel version is available by ordering option (see Tab. **1.1**).

Operationally, the mod. V1725 differs from the V1730 for operating at 250 MS/s sampling frequency.

The ADC resolution and the sampling frequency make these digitizers well suited for mid-fast signal detection systems (e.g. liquid or inorganic scintillators coupled to PMTs or Silicon Photomultipliers).

Each channel has a SRAM Multi-Event Buffer divisible into 1 ÷ 1024 buffers of programmable size. Two sizes of the channel digital memory are available by ordering options (see Tab. **1.1**).

V1730 and V1725 digitizers are provided with FPGAs that can run special DPP firmware for Physics Applications (see Chap. **14**).

A common acquisition trigger signal (common to all the channels) can be fed externally via the front panel TRG-IN input connector or via software. Alternatively, each channel is able to generate a self-trigger when the input signal goes under/over a programmable threshold. For each couple of adjacent channels, the relevant self-triggers are then processed to provide out a single trigger request. In the DPP firmware, the trigger requests can be used at channel level for the event acquisition (independent triggering), while in the default firmware they can be processed by the board to generate a common trigger causing all the channels to acquire an event simultaneously. The trigger from one board can be propagated to the other boards through the front panel TRG OUT connector.

During the acquisition, data stream is continuously written in a circular memory buffer. When the trigger occurs, the digitizer writes further samples for the post trigger and freezes the buffer that can be read by one of the provided readout links. The acquisition can continue without any dead time in a new buffer.

V1730 and V1725 feature front panel CLK-IN connector as well as an internal PLL for clock synthesis from internal/external references. Multi-board synchronization is supported, so all V1730 or all V1725 can be synchronized to a common clock source and ensuring Trigger Time Stamps alignment. Once synchronized, all data will be aligned and coherent across the multi-board system. CLK-IN / CLK-OUT connectors allow for a Daisy-chained clock distribution.

16 general purpose LVDS I/Os also FPGA-controlled can be programmed for Busy, Data Ready, Memory Full or Individual Trig-Out management. An Input Pattern (external signal) can be provided on the LVDS I/Os to be latched to each trigger as an event marker (see Sec. **10.9**).

An analog output (MON/Σ) from internal 12-bit 125-MHz DAC controlled by the FPGA allows to provide out four types of information: Trigger Majority, Test Pulses, Memory Occupancy, Voltage Level (see Sec. **10.8**).

The module is equipped with a VME64 interface (VM64X in case of VX1730 and VX1725) where the data readout can be performed in Single Data Transfer (D32), 32/64-bit Block Transfer (BLT, MBLT, 2eVME. 2eSST) and 32/64-bit Chained Block Transfer (CBLT).

The module houses Optical Link interface (CAEN proprietary CONET protocol) supporting transfer rate up to 80 MB/s and offers daisy chain capability. Therefore, it is possible to connect up to 8 ADC modules to a single Optical Link Controller by using the A4818 adapter, or up to 32 using a A5818 (4-link version).

VME and Optical Link accesses take place on independent paths and are handled by the on-board controller; therefore, when accessed through Optical Link, the board can be operated outside the VME Crate.

In addition to the waveform recording firmware, CAEN provides for this digitizer four types of Digital Pulse Processing firmware (DPP):

- Pulse Shape Discrimination (DPP-PSD), which combines the functions of a digital QDC (charge integration) and discriminator of different shapes for particle identification.
- Pulse Height Analysis (DPP-PHA), which is the digital solution equivalent to Shaping Amplifier and Peak Sensing ADC for nuclear physics or other applications requiring radiation detectors.
- Zero Length Encoding (DPP-ZLEplus) for the zero suppression and data reduction.
- Dynamic Acquisition Windows (DPP-DAW) which improves zero suppression for trigger-less acquisition systems.

All these DPP firmware make the digitizer an enhanced system for Physics Applications.

To interface the digitizers, CAEN provides the drivers for the supported communication links, a set of C libraries, LabVIEW VIs and example codes, configuration tools for firmware management (e.g. upgrade, board information, etc.) and direct register access, readout software for the waveform recording firmware (WaveDump, WaveDump 2) and for the DPP firmware (CoMPASS, DPP-ZLE and DPP-DAW Control Software).

Board Models	Description
V1730	16 ch. 14bit 500 MS/s Digitizer:640kS/ch,CE30,SE
V1730B	16 ch. 14bit 500 MS/s Digitizer:5.12MS/ch,CE30,SE
V1730C	8 Ch. 14 bit 500 MS/s Digitizer:640kS/ch,CE30,SE
V1730D	8 Ch. 14 bit 500 MS/s Digitizer:5.12MS/ch,CE30,SE
V1730S	16 ch. 14bit 500 MS/s Digitizer:640kS/ch,Arria V GX,SE
V1730SB	16 ch. 14bit 500 MS/s Digitizer:5.12MS/ch,Arria V GX,SE
V1730SC	8 Ch. 14 bit 500 MS/s Digitizer:640kS/ch,Arria V GX,SE
V1730SD	8 Ch. 14 bit 500 MS/s Digitizer:5.12MS/ch,Arria V GX,SE
VX1730	16 ch. 14bit 500 MS/s Digitizer:640kS/ch,CE30,SE
VX1730B	16 ch. 14bit 500 MS/s Digitizer:5.12MS/ch,CE30,SE
VX1730C	8 Ch. 14 bit 500 MS/s Digitizer:640kS/ch,CE30,SE
VX1730D	8 Ch. 14 bit 500 MS/s Digitizer:5.12MS/ch,CE30,SE
VX1730S	16 ch. 14bit 500 MS/s Digitizer:640kS/ch,Arria V GX,SE
VX1730SB	16 ch. 14bit 500 MS/s Digitizer:5.12MS/ch,Arria V GX,SE
VX1730SC	8 Ch. 14 bit 500 MS/s Digitizer:640kS/ch,Arria V GX,SE
VX1730SD	8 Ch. 14 bit 500 MS/s Digitizer:5.12MS/ch,Arria V GX,SE
V1725	16 Ch. 14 bit 250 MS/s Digitizer:640kS/ch,CE30,SE
V1725B	16 Ch. 14 bit 250 MS/s Digitizer:5.12MS/ch,CE30,SE
V1725C	8 Ch. 14 bit 250 MS/s Digitizer:640kS/ch,CE30,SE
V1725D	8 Ch. 14 bit 250 MS/s Digitizer:5.12MS/ch,CE30,SE
V1725S	16 Ch. 14 bit 250 MS/s Digitizer:640kS/ch,Arria V GX,SE
V1725SB	16 Ch. 14 bit 250 MS/s Digitizer:5.12MS/ch,Arria V GX,SE
V1725SC	8 Ch. 14 bit 250 MS/s Digitizer:640kS/ch,Arria V GX,SE
V1725D	8 Ch. 14 bit 250 MS/s Digitizer:5.12MS/ch,Arria V GX,SE
VX1725	16 Ch. 14 bit 250 MS/s Digitizer:640kS/ch,CE30,SE
VX1725B	16 Ch. 14 bit 250 MS/s Digitizer:5.12MS/ch,CE30,SE
VX1725C	8 Ch. 14 bit 250 MS/s Digitizer:640kS/ch,CE30,SE
VX1725D	8 Ch. 14 bit 250 MS/s Digitizer:5.12MS/ch,CE30,SE
VX1725S	16 Ch. 14 bit 250 MS/s Digitizer:640kS/ch,Arria V GX,SE
VX1725SB	16 Ch. 14 bit 250 MS/s Digitizer:5.12MS/ch,Arria V GX,SE
VX1725SC	8 Ch. 14 bit 250 MS/s Digitizer:640kS/ch,Arria V GX,SE
VX1725SD	8 Ch. 14 bit 250 MS/s Digitizer:5.12MS/ch,Arria V GX,SE
DPP Firmware	**Description**
DPP-PSD (730 family)	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (x730)
DPP-PSD (725 family)	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (x725)
DPP-PHA (730 family)	DPP-PHA - Digital Pulse Processing for Pulse Height Analysis (x730)
DPP-PHA (725 family)	DPP-PHA - Digital Pulse Processing for Pulse Height Analysis(x725)
DPP-ZLE (730 family)	DPP-ZLE – Digital Pulse Processing with Zero Length Encoding (x730)
DPP-ZLE (725 family)	DPP-ZLE – Digital Pulse Processing with Zero Length Encoding (x730)
DPP-DAW (730 family)	DPP-DAW – Digital Pulse Processing with Dynamic Acquisition Window (x730)
DPP-DAW (725 family)	DPP-DAW – Digital Pulse Processing with Dynamic Acquisition Window (x725)
Related Products	**Description**
A2818	A2818 - PCI Optical Link (Obsolete)
A3818A	A3818A - PCIe 1 Optical Link (Obsolete)
A3818B	A3818B - PCIe 2 Optical Link (Obsolete)
A3818C	A3818C - PCIe 4 Optical Link (Obsolete)
A4818	A4818 - USB3 to Conet2 Bridge
A5818	A5818 - PCIe 4 Optical Link, Gen. 3
V3718	V3718 - VME-USB Bridge
VX3718	VX3718 - VME-USB Bridge
V4718	V4718 - VME64-USB 3.0, Ethernet and Optical Link Bridge
VX4718	VX4718 - VME64-USB 3.0, Ethernet and Optical Link Bridge
VME8004B	VME8004B - 2U 4 Slot VME64 Mini Crate
VME8004X	VME8004X - 2U 4 Slot VME64X Mini Crate
VME8008B	VME8008B - 4U 8 Slot VME64 Mini Crate
VME8008X	VME8008X - 4U 8 Slot VME64X Mini Crate
VME8010	VME8010 - 7U 21 Slot VME64 Low Cost Crate
VME8011	VME8011 - 7U 21 Slot VME64 Low Cost Crate, pluggable power supply
VME8100	VME8100 - 8U 21 Slot VME64/64X Enhanced Crate Series
VME8200	VME8200 - 9U 21 Slot VME64X Enhanced Crate series
VME8001	VME8001 - 1U 2 Slot VME64 Mini Crate (compatible only with V/VX1725 and V/VX1725S)
µ-Crate	µ-Crate - Desktop single-slot VME64X Crate

Accessories	Description
DT4700	Clock Generator
A316	Cable assembly 2.54mm 2-pin header female - 5 cm
A317	Cable assembly for Clock distribution 3-pin AMPMODU IV female terminations – 18 / 25 cm
A318	Adapter for Clock signal FISCHER S101A004 male to 3-pin AMPMODU IV female - 10 cm
A319B	A319B - Clock Cable for Digitizer Series 1.0 to 2.0 interconnection (L=20cm)
A654	Cable assembly LEMO 00 male to MCX male - 1 m
A654 KIT4	4 Cable assembly LEMO 00 male to MCX male - 1 m
A654 KIT8	8 Cable assembly LEMO 00 male to MCX male - 1 m
A659	Cable assembly BNC male to MCX male - 1 m
A659 KIT4	4 MCX to BNC Cable Adapter
A659 KIT8	8 MCX to BNC Cable Adapter
A952	Cable assembly 2.54mm 34 pin female to 2.54mm 34 pin female - 50 cm
A953	Cable assembly 2.54mm 34 pin female to two 2.54mm 34 pin female - 50 cm
A954	Cable assembly 2.54mm 34 pin female to two 2.54mm 16 pin female - 50 cm
AI2740	Optical Fibre 40 m simplex
AI2730	Optical Fibre 30 m simplex
AI2720	Optical Fibre 20 m simplex
AI2705	Optical Fibre 5 m simplex
AI2703	Optical Fibre 30 cm simplex
AY2730	Optical Fibre 30 m duplex
AY2720	Optical Fibre 20 m duplex
AY2705	Optical Fibre 5 m duplex

Tab. 1.1: Table of models and related items

2 Block Diagram

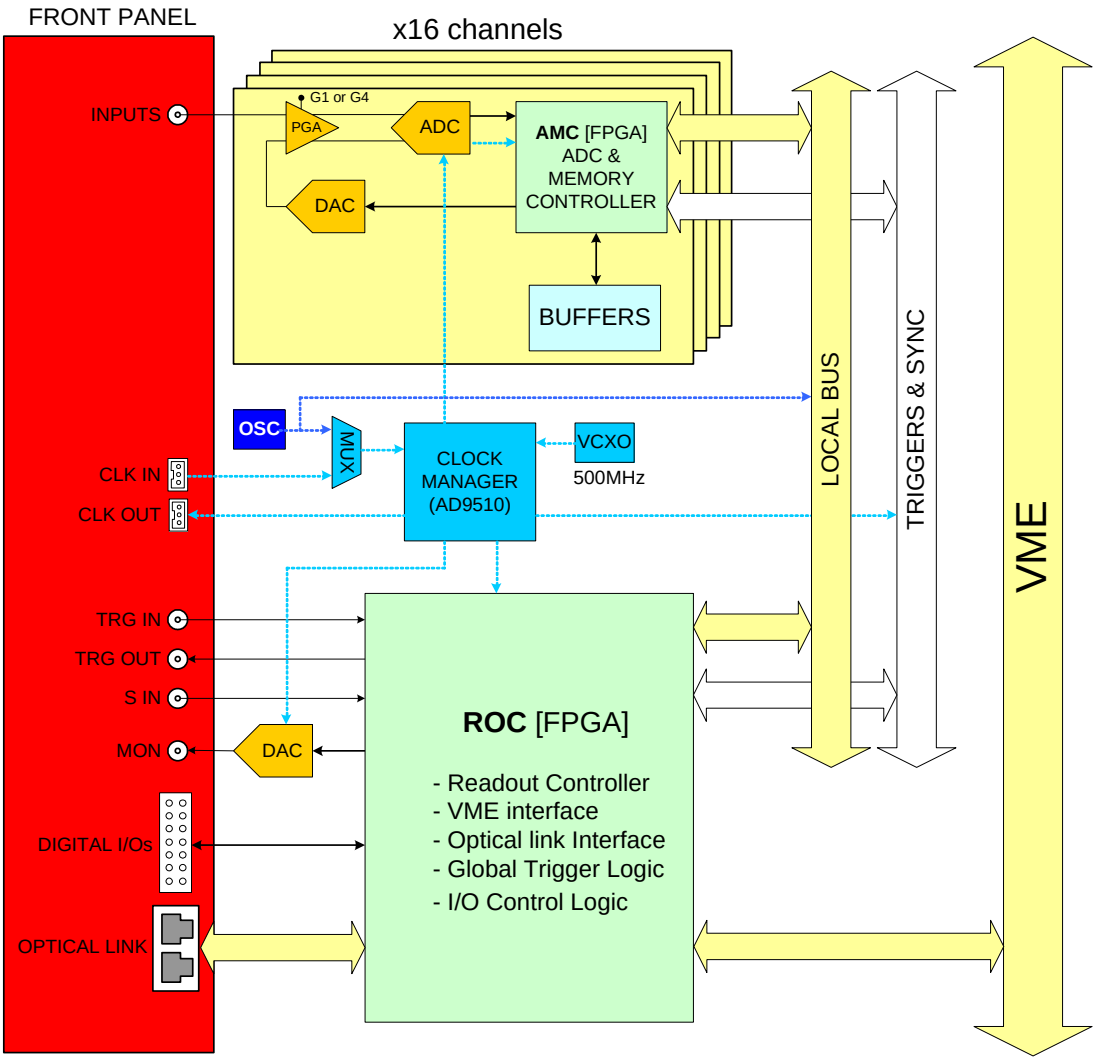


Fig. 2.1: Block Diagram

3 Technical Specifications

ANALOG INPUTS	**Number of Channels** 16 / 8 channels [1] Single ended **Full Scale Range (FSR)** 0.5 V_{pp} / 2 V_{pp} (default) SW selectable [1] *"size1 / size2" denotes different model versions*	**Impedance** Z_{in} = 50 Ω **DC Offset** Programmable 16-bit DAC for DC offset adjustment on each channel in the FSR.	**Connector** MCX **Bandwidth** 250 MHz (V1730) 125 MHz (V1725)
DIGITAL CONVERSION	**Resolution** 14 bits	**Sampling Rate** 500 MS/s (V1730) 250 MS/s (V1725) Simultaneously on each channel	
SYSTEM PERFORMANCES	**V/VX1730S-V/VX1725S Baseline RMS Noise (open inputs)** @ 2 V_{pp}: 2.6 LSB = 312 uV @ 0.5 V_{pp}: 3.4 LSB = 102 uV		
FPGA	**V/VX1730-V/VX1725** Altera Cyclone EP4CE30 (one FPGA serves 4 channels)	**V/VX1730S-V/VX1725S** Intel/Altera Arria V GX (one FPGA serves 4 channels)	
TRIGGER	**Trigger Source** - *Self-trigger*: Channel over/under threshold for either Common or Individual (DPP only) trigger generation - *External-trigger*: Common by TRG-IN connector - *Software-trigger*: Common by software command **Trigger Propagation** TRG-OUT programmable digital output	**Trigger Time Stamp V1730/V1730S** Waveform Recording: 31-bit counter, 16 ns resolution, 17 s range; 48-bit extension by firmware DPP-PSD: 47-bit counter, 2 ns resolution, 78 h range; 10-bit and about 2 ps fine time stamp with digital CFD DPP-PHA: 47-bit counter, 2 ns resolution, 78 h range DPP-DAW: 48-bit counter, 2 ns resolution, 156 h range DPP-ZLEplus: 48-bit counter, 16 ns resolution, 625 h range **Trigger Time Stamp V1725/V1725S** Waveform Recording: 31-bit counter, 16 ns resolution, 17 s range; 48-bit extension by firmware DPP-PSD: 47-bit counter, 4 ns resolution, 156 h range; 10-bit and about 4 ps fine time stamp with digital CFD DPP-PHA: 47-bit counter, 4 ns resolution, 156 h range DPP-DAW: 48-bit counter, 4 ns resolution, 312 h range DPP-ZLEplus: 48-bit counter, 32 ns resolution, 1250 h range	
ACQUISITION MEMORY	640 kS/ch or 5.12 MS/s Multi-event Buffer divisible into 1 ÷ 1024 buffers. Independent read and write access; programmable event size and pre/post-trigger		
ADC CLOCK GENERATION	Clock source: internal/external On-board programmable PLL provides generation of the main board clocks from internal (50 MHz local Oscillator) or external (front panel CLK-IN connector) reference		
DIGITAL I/O	**CLK-IN (AMP Modu II)** AC coupled input clock Differential LVDS, ECL, PECL, LVPECL, CML (single ended NIM/TTL available by A318 adapter) Accuracy<100ppm requested Z_{diff} = 100 Ω **CLK-OUT (AMP Modu II)** DC coupled clock output locked at ADC sampling clock Differential LVDS **TRG-OUT (LEMO)** Trigger digital output NIM/TTL R_t = 50 Ω	**TRG-IN (LEMO)** External trigger digital input Signal Width > 8 ns NIM/TTL Z_{in} = 50 Ω **S-IN (LEMO)** SYNC/START digital input Signal Width > 8 ns NIM/TTL Z_{in} = 50 Ω	**LVDS I/O** 16 general purpose LVDS I/O controlled by the FPGA: Busy, Data Ready, Memory full, Individual Trig-Out and other functions can be programmed. An Input Pattern from the LVDS I/O can be associated to each trigger as an event marker
SYNCHRONIZATION	**Clock Propagation** *Daisy chain*: Through CLK-IN/CLK-OUT connectors *One-to-many*: From an external clock source (DT4700) to CLK-IN connector Clock Cable delay compensation **Trigger Time Stamps Alignment** By S-IN input connector	**Acquisition Synchronization** Sync, Start/Stop by digital I/Os (S-IN or TRG-IN input / TRG-OUT output) **Data Aligment** Busy/Veto management through digital I/Os (TRG-OUT/TRG-IN) or LVDS I/Os	

ANALOG MONITOR	12-bit/125 MHz DAC FPGA controlled output with four operating modes: Test pulses: 1 Vpp ramp generator Majority signal: proportional to the no. of couples of channels under/over the threshold (steps of 125 mV) Memory Occupancy signal: proportional to the Multi-Event Buffer Occupancy (1 buffer ~ 1mV) Voltage level: programmable output voltage level			
COMMUNICATION INTERFACE	**Optical Link** CONET: CAEN proprietary protocol Up to 80 MB/s transfer rate Daisy chain capability	**VME** VME 64X compliant Data transfer mode: BLT32, MBLT64 (70 MB/s by CAEN Bridge), CBLT32/64, 2eVME, 2eSST (up to 200 MB/s)		
FIRMWARE	**Waveform Recording Firmware** Free firmware for waveform recording	**DPP Firmware** Pay firmware for Digital Pulse Processing: DPP-PSD, DPP-PHA, DPP-ZLEplus, DPP-DAW	**Upgrades** Supported via VMEbus/Optical Link	
SOFTWARE	**Readout SW** CAEN software for users and developers: *WaveDump*, *WaveDump2* (Windows®, Linux®)	**Libraries and Tools** General purpose C libraries with readout demos (Windows®, Linux®, LabVIEW™) and configuration tools.		
MECHANICAL	**Form Factor** 1-unit wide VME64/VME64X boards	**Weight** 440 g (8 ch) 540 g (16 ch)	**Dimensions** 6U x 160 mm	
ENVIRONMENTAL	**Environment:** Indoor use **Operating Temperature:** 0°C to +40°C **Storage Temperature:** –10°C to +60°C **Operating Humidity:** 10% to 90% RH non condensing **Storage Humidity:** 5% to 90% RH non condensing **Altitude:** < 2000m **Pollution Degree:** 2 **Overvoltage Category:** II **EMC Environment:** Commercial and light industrial **IP Degree:** IPX0 Enclosure, not for wet location			
REGULATORY COMPLIANCE	**EMC** CE 2014/30/EU Electromagnetic compatibility Directive	**Safety** CE 2014/35/EU Low Voltage Directive		
POWER REQUIREMENTS (TYP.)	**Mod./Supply Voltage**	**+5 V**	**+12 V**	**-12 V**
	V/VX1730	8.2 A	840 mA	*not used*
	V/VX1730B	10.2 A	840 mA	*not used*
	V/VX1730C (ref. PCB rev.0)	5 A	400 mA	400 mA
	V/VX1730D (ref. PCB rev. 0)	6.5 A	400 mA	400 mA
	V/VX1725	5.2 A	750 mA	*not used*
	V/VXV1725B/1725C/1725D	*n.a.*		
	V/VX1730S	9,3 A	900 mA	*not used*
	V/VX1730SB	11.5 A	800 mA	*not used*
	V/VX1730SC	5.3 A	500 mA	*not used*
	V/VX1730SD	6.3 A	400 mA	*not used*
	V/VX1725S	7.5 A	700 mA	*not used*
	V/VX1725SB	8 A	800 mA	*not used*
	V/VX1725SC	5 A	500 mA	*not used*
	V/VX1725SD	6.5 A	500 mA	*not used*

Tab. 3.1: Specifications table

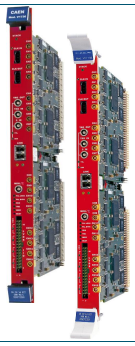
4 Packaging and Compliancy

V1725/VX1725 and V1730/VX1730 modules are 1-unit wide, 6U VME64/VME64X boards.

8-channel versions of the V1730/V1725 and VX1730/VX1725 digitizers (see Tab. **1.1**) differ from 16-channel ones for mounting only the mezzanine managing the analog input channels from 0 to 7. From a functional point of view, what described in this manual applies identically to 8-channels versions.

The device is inspected by CAEN before the shipment, and it is guaranteed to leave the factory free of mechanical or electrical defects.

The content of the delivered package standardly consists of the part list shown in the table below (Tab. **4.1**).

	Part	Description	Qt
	V/VX1730 or V/VX1725	Digitizer device	x1
	Documentation	UM2792 – V1730/VX1730 & V1725/VX1725 User Manual	x1

Tab. 4.1: Delivered kit content

CAUTION: to manage the product, consult the operating instructions provided.

When receiving the unit, the user is strictly recommended to:

- Inspect containers for damage during shipment. Report any damage to the freight carrier for possible insurance claims.
- Check that all the components received match those listed on the enclosed packing list as in Tab. **4.1**. (CAEN cannot accept responsibility for missing items unless we are notified promptly of any discrepancies.)
- Open shipping containers; be careful not to damage contents.
- Inspect contents and report any damage. The inspection should confirm that there is no exterior damage to the unit such as broken knobs or connectors and that the front panel and display face are not scratched or cracked. Keep all packing material until the inspection has been completed.
- If damage is detected, file a claim with the carrier immediately and notify CAEN service.
- If equipment must be returned for any reason, carefully repack equipment in the original shipping container with original packing materials if possible. Please, contact CAEN service (Chap. **18**).
- If equipment is to be installed later, place equipment in the original shipping container and store it in a safe place until ready to install.

DO NOT SUBJECT THE ITEM TO UNDUE SHOCK OF VIBRATIONS

DO NOT BUMP, DROP OR SLIDE SHIPPING CONTAINERS

DO NOT LEAVE ITEMS OR SHIPPING CONTAINERS UNSUPERVISED IN AREAS WHERE UNTRAINED PERSONNEL MAY MISHANDLE THE ITEMS

USE ONLY ACCESSORIES WHICH MEET THE MANUFACTURER'S SPECIFICATIONS

Official documentation, firmware updates, software tools, and accessories are available on the CAEN website *www.caen.it* at the Digitizer web page. MyCAEN+ account needed for download (see Chap. **18**).

For a correct and safe use of the module, refer to Chap. **6** and **7**.

5 PID (Product Identifier)

PID is the CAEN product identifier, an incremental number greater than 10000 that is unique for each product[1]. The PID is on a label affixed to the product (Fig. **5.1**) and it is even stored in an on-board non- volatile memory readable at bit [7:0] of registers 0xF080 or 0xF084 **[RD3]**. The PID information is also available through CAENToolbox Software (for more details refer to **[RD1]**).

Note: The serial number is still valid to identify older boards, where the PID label is not present.

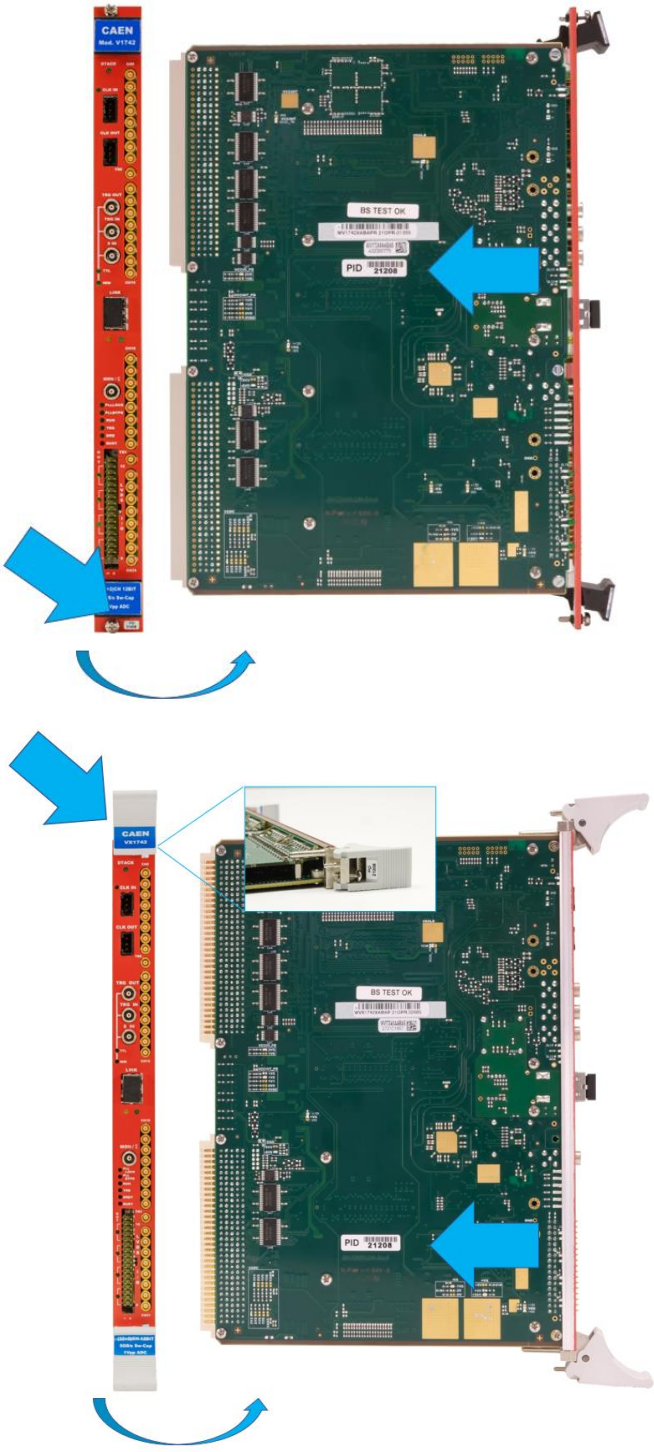


Fig. 5.1: PID location on the VME64 and VME64X device (the number and digitizer model in the pictures are purely indicative)

[1] The PID substitutes the serial number previously identifying the boards.

6 Power Requirements

The table below resumes the typical power consumptions per relevant power supply voltage.

The values in the table can be taken as reference also for VME64X models.

MODULE	SUPPLY VOLTAGE		
	+5 V	+12 V	-12 V
V/VX1730	8.2 A	840 mA	*not used*
V/VX1730B	10.2 A	840 mA	*not used*
V/VX1730C (ref. PCB rev. 0)	5 A	400 mA	400 mA
V/VX1730D (ref. PCB rev. 0)	6.5 A	400 mA	400 mA
V/VX1725	5.2 A	750 mA	*not used*
V/VX1725B - V/VX1725C - V/VX1725D	*n.a.*		
V/VX1730S	9.3 A	900 mA	*not used*
V/VX1730SB	11.5 A	800 mA	*not used*
V/VX1730SC	5.3 A	500 mA	*not used*
V/VX1730SD	6.3 A	400 mA	*not used*
V/VX1725S	7.5 A	700 mA	*not used*
V/VX1725SB	8 A	800 mA	*not used*
V/VX 725SC	5 A	500 mA	*not used*
V/VX1725SD	6.5 A	500 mA	*not used*

Tab. 6.1: Power requirements table

Note.: The declared values are measured in standard operating conditions. In general, they could be subject to slight changes due to the firmware type, the firmware version, and the operating mode.

Note.: The reported power requirements may be different depending on the motherboard revision numbers, which could be read at 0xF04C register. Please, contact CAEN for old power consumption specifications.

7 Cooling Management

The V1725/VX1725 and V1730/VX1730 Digitizers can operate in the temperature range 0° ÷ +40°.

The VME models must be operated in ventilated crates as recommended in the **Safety Notices**.

EXTERNAL FANS MUST BE USED WHEN THE BOARD IS INSTALLED IN A SETUP WITH POOR AIR FLOW

V1730x/V1730Sx DIGITIZERS CANNOT BE OPERATED WITH CAEN CRATES VME8001, VME8002, VME8004, AND VME8004A. OVERHEAT MAY DAMAGE THE MODULE

The Users must take care to provide a proper cooling to the board with external fan if the boards is used in an enclosure or if the board is installed in a setup with poor air flow.
Excessive temperature will, in first instance, reduce the performance and the quality of the measurements and can also damage the board.

If the board is stored in cold environment, please check for water condensation before power on.

The board has not been tested for radiation hardness. High energy particles can be source of errors and can damage the FPGA. If used in strong proton or neutron beams, arrange proper shielding, or remote the sensors with a custom cable.

7.1 Cleaning Air Vents

CAEN recommends to occasionally clean the air vents on all vented sides of the board or crate, if present. Lint, dust, and other foreign matter can block the vents and limit the airflow. Be sure to power off the board and disconnect it from the power by physically detach the power chord before cleaning the air vents and follow the general cleaning safety precautions.

IT IS UNDER THE RESPONSIBILITY OF THE CUSTOMER A NON-COMPLIANT USE OF THE PRODUCT

8 Temperature Protection

TEMPERATURE PROTECTION IS NOT AVAILABLE FOR WAVEFORM RECORDING FIRMWARE RELEASES < 4.5_0.3

To preserve hardware damages, the digitizer implements an automatic turn-off of the board channels in event of internal over-temperature. Internal temperature can be monitored by reading at register address 0x1nA8.

The over-temperature limit is fixed at 85°C for V1730S/V1725S digitizers and 70°C for the V1730/V1725 ones. As soon as the internal temperature exceeds this limit, the board enters the temperature protection condition and the firmware automatically performs the following actions:

- turns off all the channel ADCs;
- stops the acquisition, if running (data possibly stored at that moment can be readout in any case).

This status does not change as long as the internal temperature remains over 75°C for V1730S/V1725S digitizers and 62°C for the V1730/V1725 ones. As soon as the temperature decreases under this limit, the user can turn on the channel ADCs again and restart the acquisition, if necessary.

The temperature protection can be controlled by register addresses 0x8104 and 0x81C0 **[RD3]**.

9 Panels Description

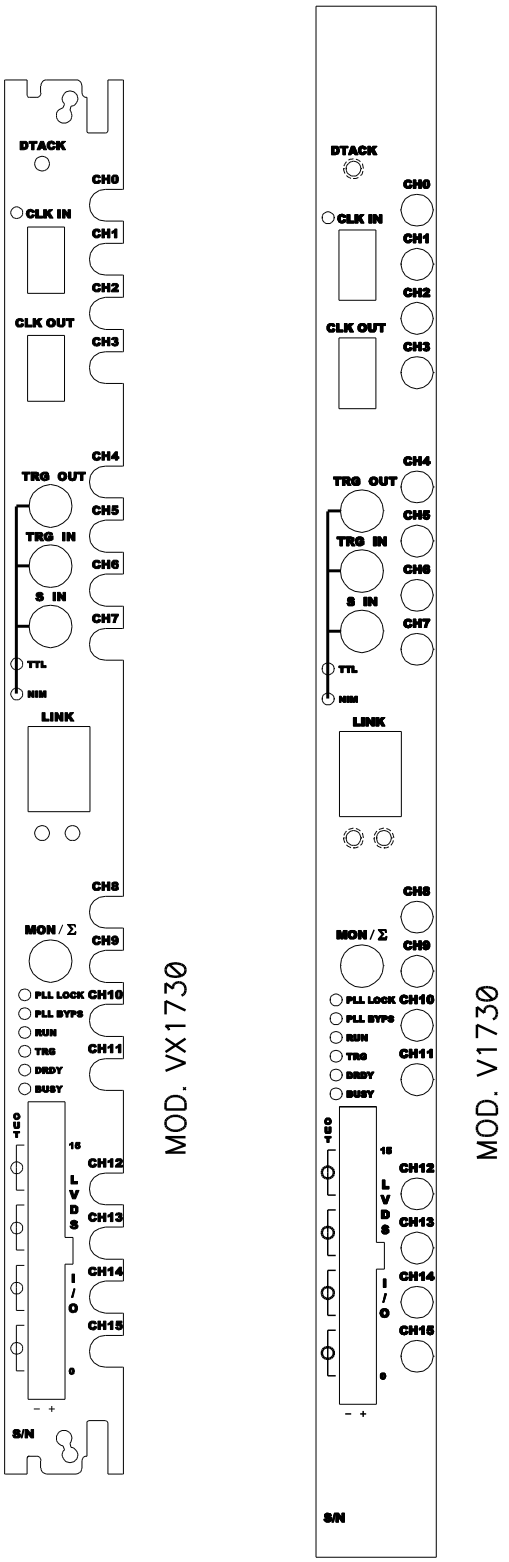


Fig. 9.1: Front panels view: VX1730, V1730

V1725 and V1730 digitizers do have the same front panel, and so it is for VX1725 and VX1730 ones.

9.1 Front Panel

ANALOG INPUT

FUNCTION

Input connectors from CH0 to CH15 receive the input analog signals.

ELECTRICAL SPECS

Input dynamics:

- 2 V_{pp} (default);
- 0.5 V_{pp} SW selectable.

Input impedance (Z_{in}): 50 Ω.

MECHANICAL SPECS

Series: MCX connectors.

Type: CS 85MCX-50-0-16 (jack/female).

Manufacturer: SUHNER

Suggested plug/male: MCX-50-2-16.

Suggested cable: RG174 type.

CLOCK INPUT / CLOCK OUTPUT

FUNCTION

Input and output connectors for the external clock.

ELECTRICAL SPECS

Sign. type:

differential LVDS, ECL, PECL, LVPECL, CML. Single-ended-to-differential A318 cable adapter available (see Tab. **1.1**)

Coupling:

- AC (CLK-IN);
- DC (CLK-OUT).

Z_{diff}: 100 Ω.

Accuracy < 100 ppm

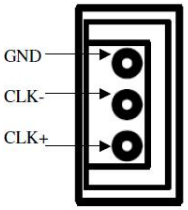
MECHANICAL SPECS

Series: AMPMODU connectors.

Type: 3-102203-4 (3-pin).

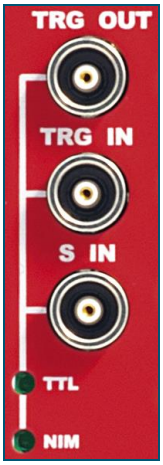
Manufacturer: AMP Inc.

PINOUT



CLK IN LED (GREEN): indicates the external clock is enabled.

TRIGGER INPUT / TRIGGER OUTPUT/ SYNC INPUT



FUNCTION

- TRG-OUT: digital output connector to propagate:
  - the internal trigger sources;
  - probes from the mezzanines;
  - S-IN signal

according to register addresses 0x8110 and 0x811C;

  - probes from the motherboard, like the Run, ClkOut, ClockPhase, PLL_Unlock or Busy signal

according to register address 0x811C.

- TRG-IN: digital input connector for the external trigger.
- S-IN: SYNC/START/STOP digital input connector configurable as reset of the time stamp (see Sec. **10.12.3**)or to start/stop the acquisition (see Sec. **10.6.2**).

ELECTRICAL SPECS

Signal level: NIM or TTL, SW selectable.

TRG-IN/S-IN Input impedance (Z_{in}): 50 Ω.

TRG-OUT requires 50 Ω termination.

MECHANICAL SPECS

Series: 101 A 004 connectors.

Type: DLP 101 A 004-28.

Manufacturer: FISCHER.

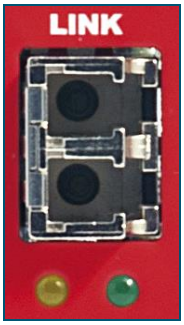
Alternatively:

Type: EPL 00 250 NTN.

Manufacturer: LEMO.

TTL (GREEN), NIM (GREEN): indicate the standard TTL or NIM is set for TRG-OUT, TRG-IN, S-IN.

OPTICAL LINK PORT



FUNCTION

Optical LINK connector for data readout and flow control. Daisy chainable. Compliant to Multimode 62.5/125µm cable featuring LC connectors on both sides.

ELECTRICAL SPECS

Transfer rate: up to 80 MB/s.

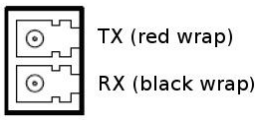
MECHANICAL SPECS

Series: SFF Transceivers.

Type: FTLF8519F-2KNL (LC connectors).

Manufacturer: FINISAR.

PINOUT



LINK LEDs (GREEN/YELOW): right LED (GREEN) indicates the network presence, while left LED (YELLOW) signals the data transfer activity.

ANALOG MONITOR

FUNCTION

Analog Monitor output connector with 4 programmable modes (see Sec. **10.8**):

- Trigger Majority;
- Test Pulses;
- Memory Occupancy;
- Voltage Level.

ELECTRICAL SPECS

12-bit (100 MHz) 1V_{pp} DAC output on R_t=50 Ω.

MECHANICAL SPECS

Series: 101 A 004 connectors.

Type: DLP 101 A 004-28.

Manufacturer: FISCHER.

Alternatively:

Type: EPL 00 250 NTN.

Manufacturer: LEMO.

DIAGNOSTIC LEDs

DTACK (GREEN): indicates there is a VME read/write access to the board;

PLL LOCK (GREEN): indicates the PLL is locked to the reference clock;

PLL BYPS (GREEN): indicates the PLL drives directly the ADCs. PLL circuit is switched off and PLL LOCK LED is turned off;

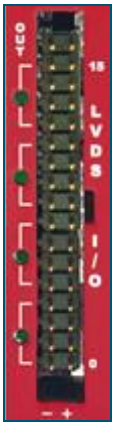
RUN (GREEN): indicates the acquisition is running (data taking, see Sec. **10.6.2**).

TRG (GREEN): indicates the trigger is accepted;

DRDY (GREEN): indicates the event/data is present in the Output Buffer;

BUSY (RED): indicates all the buffers are full for at least one channel.

LVDS I/Os CONNECTOR



FUNCTION

16-pin connector with programmable general purpose LVDS I/O signals organized in 4 independent signal groups:
0÷3; 4÷7; 8÷11; 12÷15.

Input/Out direction is software controlled.

Different selectable modes (see Sec. **10.9**):

- Register;
- Trigger;
- nBusy/nVeto;
- Legacy.

ELECTRICAL SPECS

Level: differential LVDS.

Z_{diff}: 100 Ω.

MECHANICAL SPECS

Series: TE - AMPMODU Mod II Series

Type: 5-826634-0 (lead spacing: 2.54mm; row pitch: 2.54mm)

Manufacturer: AMP Inc.

LVDS I/O LEDs (GREEN): Each LED close to a 4-pin group lights on if the pins are set as outputs.

IDENTIFICATION LABELS	
	**FUNCTION** On top and bottom of insertion/extraction handle: – Manufacturer – Model name – Brief ADC features On bottom (V1725/V1730) or on the HANDLE (VX1725/VX1730): – Product Identifier (PID) **Note:** For older boards, a 4-digit Serial Number (S/N) is reported on a little serigraph on the bottom of the VME board's front panel.

9.2 Internal Components

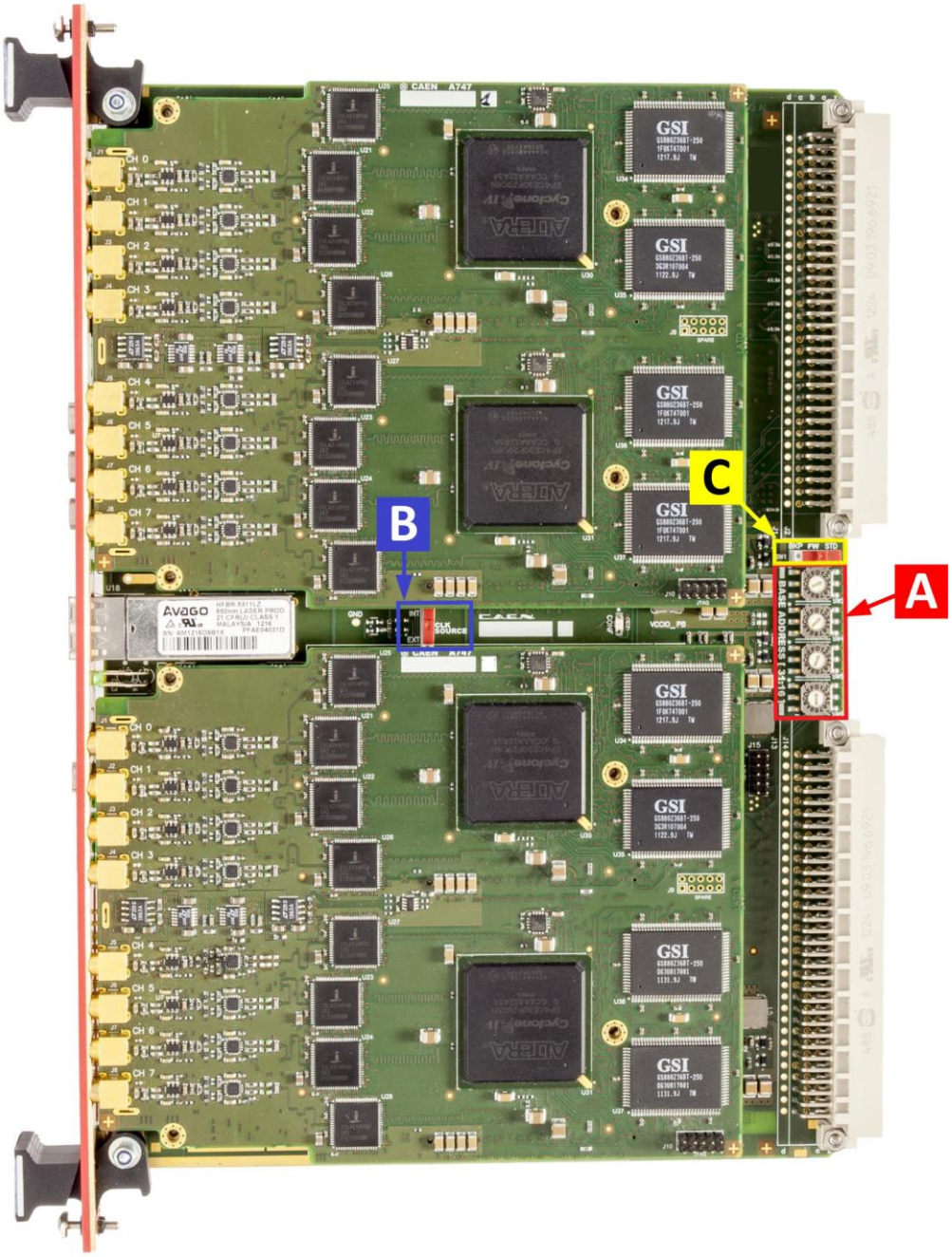


Fig. 9.2: Rotary and dip switches location

A	**SW3,4,5,6:** **"Base Address [31:16]"**	**Type:** Rotary Switches	**Function:** Set the VME Base Address of the module
B	**SW2:** **"CLOCK SOURCE" INT/EXT**	**Type:** Dip Switch	**Function:** Selects the clock source (External or Internal)
C	**SW7:** **"FW" BKP/STD**	**Type:** Dip Switch	**Function:** Selects between the "Standard" (STD) and the "Backup" (BKP) FLASH page as first to be read at power-on to load the FW on the FPGAs (default position is STD); see Chap. **14**

10 Functional Description

10.1 Analog Input Stage

The internal Programmable Gain Amplifier (Fig. **10.1**) allows for dual input range of 2 V_{pp} (default) or 0.5 V_{pp} on the single ended MCX coaxial connectors. In order to preserve the full dynamic range according to the polarity of the input signal (bipolar, positive unipolar, negative unipolar), it is possible to add a DC offset by means of a 16-bit DAC, which is up to ±1 V @ 2 V_{pp} and ±0.25 V @ 0.5 V_{pp}. The input bandwidth ranges from DC to 250 MHz (@3dB) for V1730, to 125 MHz (@3dB) for V17725 (with 2nd order linear phase anti-aliasing low-pass filter).

The input range is software selectable by direct write at register address 0x1n28.

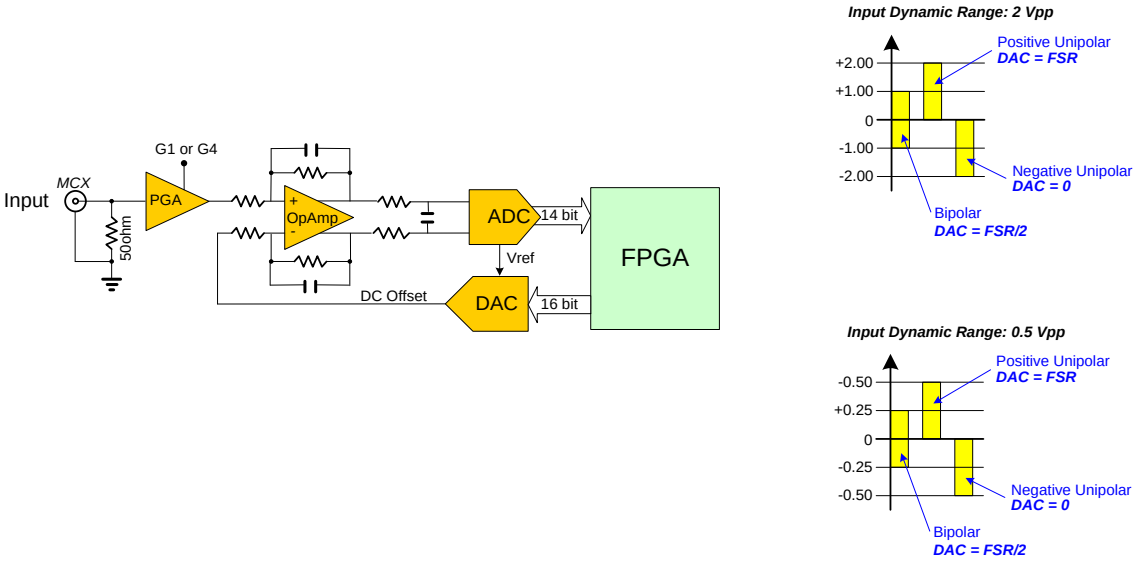


Fig. 10.1: Analog Input Diagram

10.1.1 DC Offset Individual Setting

Setting the DC offset for channel n can be done either by a direct write at register addresses 0x1n98 (or 0x8098 for common setting), or by library function (CAENDigitizerLib -> SetChannelDCOffset), or in the readout software **[RD6][RD8][RD9][RD11][RD12]**.

10.2 Clock Distribution

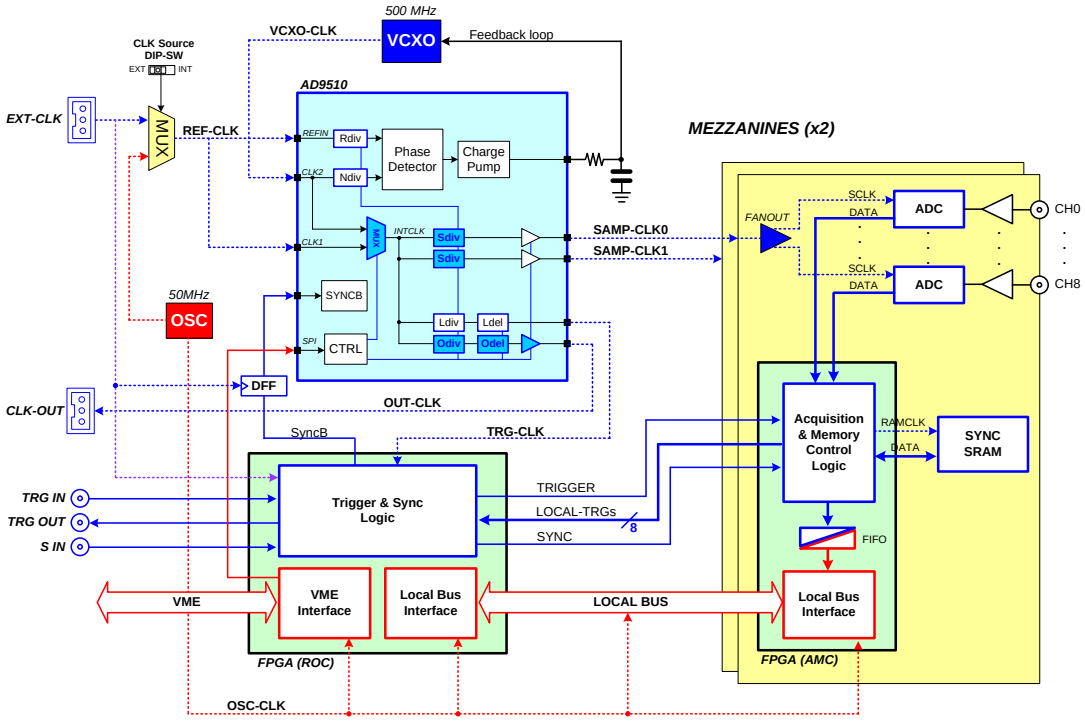


Fig. 10.2: Clock Distribution Diagram

The clock distribution of the module takes place on two domains: OSC-CLK and REF-CLK.

OSC-CLK is a fixed 50-MHz clock coming from a local oscillator which handles VMEbus, Optical Link and Local Bus, that takes care of the communication between motherboard and mezzanines (see red traces in Fig. **10.2**)**.**

REF-CLK handles ADC sampling, trigger logic, acquisition logic (samples storage into RAM, buffer freezing on trigger) through a clock chain. REF-CLK can be either an external (via the front panel CLK-IN connector) or an internal (via the 50-MHz local oscillator) source. In the latter mode, OSC-CLK and REF-CLK will be synchronous (the operation mode remains the same).

REF-CLK clock source selection can be done by SW2 on-board switch (see Fig. **9.2**):

- INT mode (default) means REF-CLK is the 50 MHz of the local oscillator (REF-CLK = OSC-CLK);
- EXT mode means REF-CLK source is the external frequency fed on CLK-IN connector.

CLK-IN signal must be differential (LVDS, ECL, PECL, LVPECL, CML) with a jitter lower than 100 ppm (see Chap. **3**). CAEN provides the A318 cable to adapt single-ended signals coming from an external clock unit into the differential CLK-IN connector (see Tab. **1.1**)

The V1730 and V1725 boards mount a phase-locked-loop (PLL) and clock distribution device, AD9510. It receives the REF-CLK and generates the sampling clock for ADCs and the mezzanine FPGA (SAMP-CLK0 and SAMP-CLK1), as well as the trigger logic synchronization clock (TRG-CLK) and the output clock (CLK-OUT).

The AD9510 configuration can be changed and stored into non-volatile memory. Changing the AD9510 configuration is primarily intended to be used for external PLL reference clock frequency change (see Sec. **10.3**). The digitizer can lock to an external 50 MHz reference clock in the default AD9510 configuration.

Refer to the AD9510 datasheet for more details:

https://www.analog.com/media/en/technical-documentation/data-sheets/AD9510.pdf

(in case the active link above doesn't work, copy and paste it on the internet browser)

10.3 PLL Mode

The Phase Detector within the AD9510 device allows to couple REF-CLK with a VCXO (500 MHz frequency) to provide the nominal ADCs frequency (500 MHz for V1730 and 250 MHz for V1725).

As introduced in Sec. **10.2**, the source of the REF-CLK signal can be external on CLK-IN front panel connector or internal from the 50 MHz local oscillator (see Fig. **10.2**) Programming the REF-CLK source internal or external can be performed by acting on the on-board dip switch SW2 (see Sec. **9.2**).

The following options are allowed:

1. 50 MHz internal clock source – it is the standard operating mode, where the default AD9510 dividers do not require to be reprogrammed (the digitizer works in the AD9510 default configuration). The on-board Clock Source switch (SW2) position must be on INT. REF-CLK = OSC-CLK.
2. 50 MHz external clock source – in this case, the clock source is taken from an external device; the AD9510 dividers do not need to be reprogrammed as the external clock reference is the same as the default one. The on-board Clock Source switch (SW2) position must be on EXT. CLK-IN = OSC-CLK = REF-CLK.
3. External clock source different from 50 MHz – the clock is externally provided as in point 2, but AD9510 dividers must be reprogrammed to lock the VCXO to the new REF-CLK and provide the nominal sampling frequency. The on-board Clock Source switch (SW2) position must be on EXT. CLK-IN = REF-CLK≠ OSC-CLK.

If the digitizer is locked, the PLL-LOCK front panel LED must be on.

Note: the user can configure the clock parameters, generate the PLL programming file and load it on the board by using the CAEN Toolbox software (see Chap. **12**).

10.4 Trigger Clock

The TRG-CLK logic works at 125 MHz (i.e. 1/4 of the SAMP-CLK for V1730, 1/2 for the V1725).

10.5 Output Clock

The AD9510 output can be available on the front panel CLK-OUT connector (see Chap. **9**). This option is particularly useful in case of multi-board synchronization to propagate the clock reference source in Daisy Chain between boards using the A317 clock distributor cable (see Tab. **1.1**).

This option can be enabled by the user while configuring the PLL programming file in the CAEN Toolbox software (see Chap. **12**).

10.6 Acquisition Modes

10.6.1 Channel Calibration

THE 725S/730S DIGITIZER VERSIONS DO NOT NEED CALIBRATION!

The module performs a self-calibration of the ADCs at its power-on. Anyway, in order to achieve the best performance, the calibration procedure is recommended to be executed by the user, on command, after the ADCs have stabilized their operating temperature. The calibration will not need to be repeated at each run unless the operating temperature changes significantly, or clock settings are modified (e.g. switching from internal to external clock).

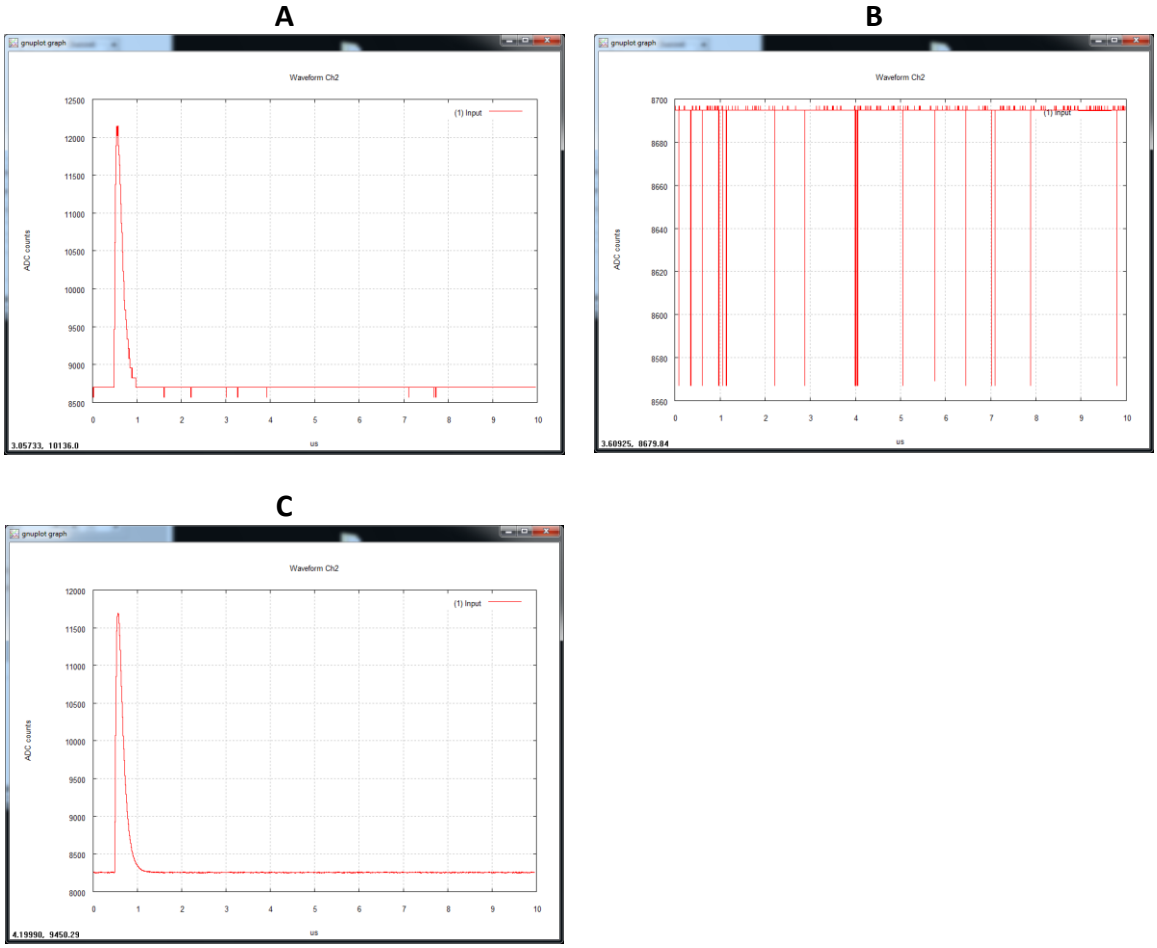
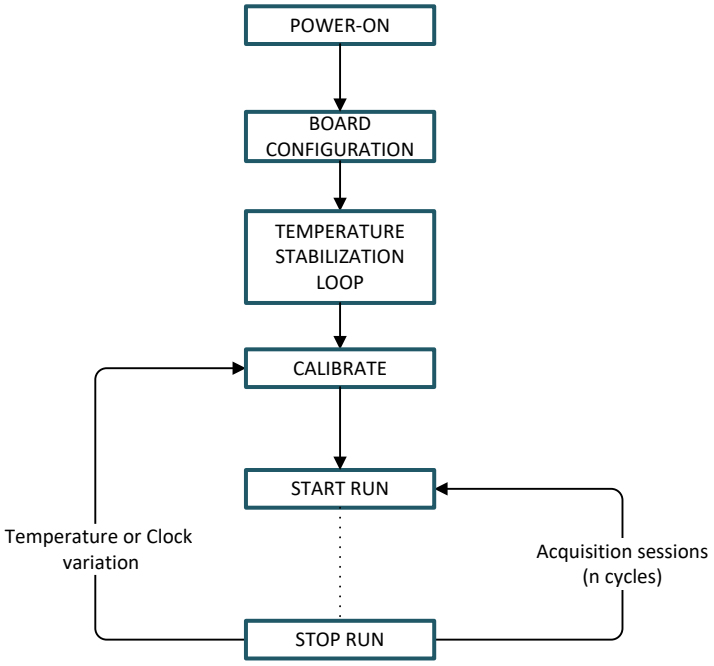


Fig. 10.3: Typical channel before the calibration (A and B) and after the calibration (C)

The diagram below schematizes the flow for a proper calibration:



– At low level, the ADCs temperature can be read at the register address 0x1nA8, while the calibration must be performed through register address 0x809C. The following steps are required:

  - Write whatever value at register address 0x809C: the self-calibration process will start simultaneously on each channel of the board and the "Calibrating bit" flag of register address 0x1n88 will be set to 0.
  - Poll the "Calibrating bit" flag until it returns to 1.

Note: It is normally not required to calibrate after a board reset but, if a Reset command is intentionally issued to the digitizer (write access at register address 0xEF24) to be directly followed by a calibration procedure, it is recommended to wait for the board to reach stable conditions (indicatively 100 ms) before to start the calibration.

Note: At power-on, a Sync command is also issued by the firmware to the ADCs to synchronize all of them to the board's clock. In the standard operating, this command is not required to be repeated by the user. If a Sync command is intentionally issued (write access at register address 0x813C), the user must consider that a new calibration procedure is needed for a correct board operating.

– At the library level, developers can refer to the routines of the CAENDigitizer library (see Chap. **11**): *ReadTemperature* function for temperature readings, *Set/GetChannelDCOffset* function for DC Offset management, *Reset* function to reset the board, and the *Calibrate* function which executes the channel calibration steps above described.

IMPORTANT NOTE: Starting from CAENDigitizer release 2.6.1, the *Reset* function has been modified so that it no longer includes the channel calibration routine implemented in the code. This calibration must be performed on command by the dedicated *Calibrate* function [RD5].

– At software level, CAEN manages the on command channel calibration in different readout software (see the relevant software documentation).

➢ ***WaveDump***

1. Lauch WaveDump. This software performs an automatic ADC calibration and displays a message when it is completed (see Fig. **10.4**).

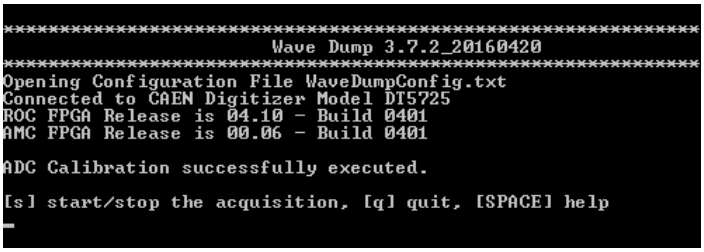


Fig. 10.4: Automatic calibration at WaveDump first run

This allows the user to start an acquisition being sure that the digitizer has been calibrated at least once.

NOTE THAT: If SKIP_STARTUP_CALIBRATION parameter is set to YES in WaveDump configuration file, the automatic start-up calibration is not performed, and no message is displayed.

2. At any time, once the acquisition is stopped (“s” command by keyboard), the channel temperature can be read out for monitoring (“m” command).

3. In case of significant variations, a manual channel calibration can be forced (“c” command) as in **Fig. 10.5**

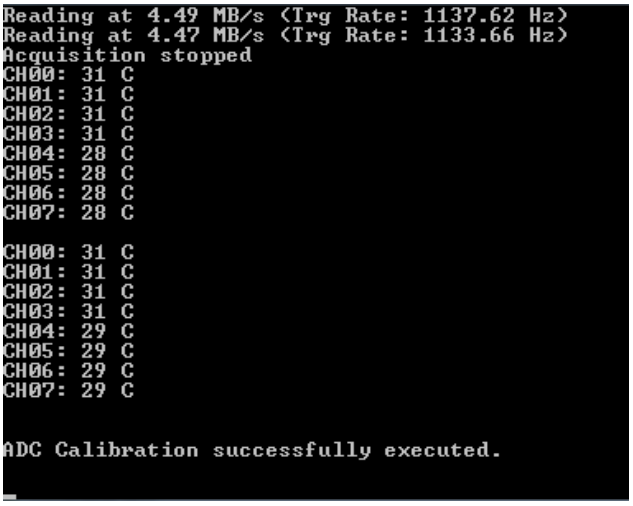


Fig. 10.5: Temperature monitoring with manual calibration in **WaveDump software**

4. The acquisition can then start again (“s” command)

Please, refer to WaveDump User Manual for complete software description (**[RD6]**).

- ***CoMPASS***

  1.Launch CoMPASS software.

  2.Connect to the digitizer.

  3.Before to start the acquisition, go to the "Input" tab and enable the "Calib. ADC" checkcell.

  4.Start the acquisition: the calibration of the channel ADCs is performed at every start acquisition.

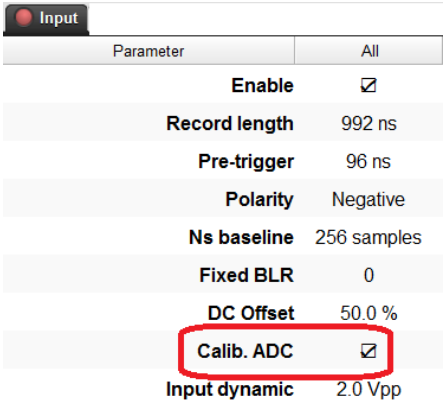


Fig. 10.6: Channel calibration in CoMPASS software

10.6.2 Acquisition Run/Stop

The acquisition can be started and stopped in different ways, according to bits[1:0] setting at register address 0x8100 and bit[2] of the same register:

- SW CONTROLLED (bits[1:0] = 00): Start and Stop take place by software command. Bit[2] = 0 means stopped, while bit[2] = 1 means running.

- S-IN CONTROLLED (bit[1:0] = 01): acquisition is armed by setting bit[2] = 1, then two options are selectable through bit [11]:
  - START/STOP ON LEVEL - If bit[11] = 0, then acquisition starts when the S-IN signal is high and stops when it is low; if bit[2] = 0 (disarmed), the acquisition is always off.
  - START ON EDGE - If bit[11] = 1, then acquisition starts on the rising edge of the S-IN signal and must be stopped by software command (bit[2] = 0).

Note: the START ON EDGE option is implemented from ROC FPGA fw revision 4.22 on.

- FIRST TRIGGER CONTROLLED (bits[1:0] = 10): bit[2] = 1 arms the acquisition and the Start is issued on the rising edge of the first trigger pulse arriving at the TRG-IN connector. This pulse is not used as a trigger while actual triggers start from the second pulse on TRG-IN. The Stop acquisition must be SW controlled (resetting bit[2]).

- LVDS I/Os CONTROLLED (bits[1:0] = 11): this mode acts like the S-IN CONTROLLED, but using the configurable features of the signals on the LVDS I/Os connector (see Sec. **10.9**).

10.6.3 Acquisition Triggering: Samples & Events

In the waveform recording firmware, the arrival of the trigger signal during the acquisition provokes:

- The storage of the Trigger Time Tag (TTT), that is the time reference related to the start of the run. It is a 31-bit counter plus an overflow bit (see Sec. **10.6.5.1**). The value of the counter is updated at the same frequency as the Trigger Logic Unit (see Fig. **10.2**), that is 125 MHz (8 ns) or every 4 ADC clock cycles of the DT5730 and 2 of the DT5725. As the acquired data are written into the board internal memory in 4-sample bunches, the TTT counter value is read at half the Trigger Logic frequency (i.e. 62.5 MHz), fixing the Trigger Time Tag resolution at 16 ns for both DT5730 and DT5725 (i.e. the LSB of the TTT is always “0”).
- The Increment the EVENT COUNTER.
- The filling of the active buffer with the pre/post-trigger samples, whose number is programmable via register address 0x8114 **[RD3]**; the acquisition window width (also referred to as record length) is determined via register addresses 0x800C and 0x8020; then, the buffer is frozen for readout purposes, while acquisition goes on in another buffer.

An event is therefore composed by the trigger time tag, pre- and post-trigger samples and the event counter.

Overlap between “acquisition windows” may occur (a new trigger occurs while the board is still storing the samples related to the previous trigger); this overlap can be either rejected or accepted (programmable via register address 0x8000).

If the board is programmed to accept the overlapped triggers, as the “overlapping” trigger arrives, the current active buffer is filled up, then the samples storage continues in the subsequent one. In this case, not all events will have the same size (see Fig. **10.7** below).

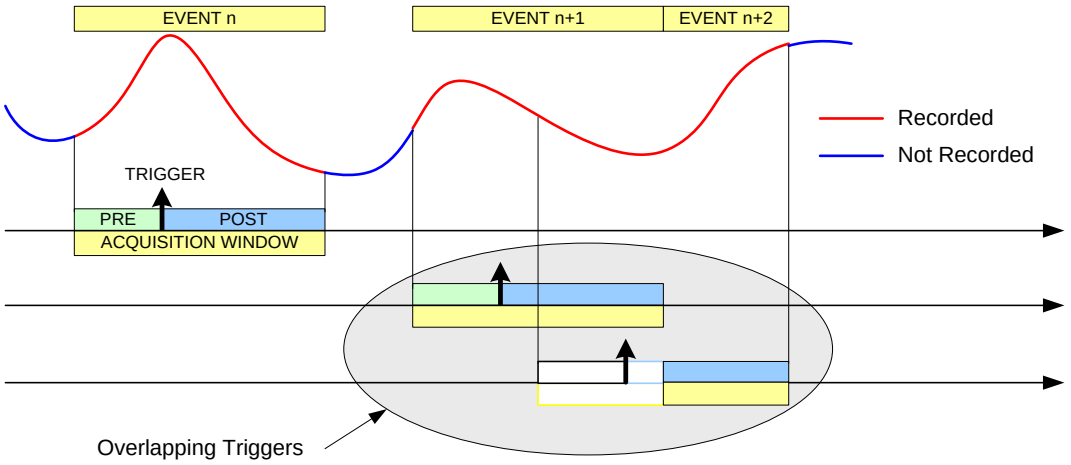


Fig. 10.7: Trigger overlap

A trigger can be refused for the following causes:

- Acquisition is not active.
- Memory is FULL and therefore there are no available buffers.
- The required number of samples for building the pre-trigger of the event is not reached yet; typically, this happens when the trigger occurs too early either with respect to the *RUN Acquisition* command (see Sec. **10.6.2**) or with respect to a buffer emptying after a *Memory FULL* status (see Sec. **10.6.6**).
- The trigger overlaps the previous one and the board is not enabled for accepting overlapped triggers.

As a trigger is refused, the current buffer is not frozen, and the acquisition continues writing on it. The EVENT COUNTER can be programmed in order to be either incremented or not. If this function is enabled, the EVENT COUNTER value identifies the number of the triggers sent (but the event number sequence is lost); if the function is not enabled, the EVENT COUNTER value coincides with the sequence of buffers saved and read out.

10.6.4 Multi-Event Memory Organization

Each channel of the V1730/V1725 features a SRAM memory to store the acquired events. The memory size for the event storage is 640 kS/ch or 5.12 MS/s, according to the board version (see Tab. **1.1)**. The channel memory can be divided in a programmable number of buffers, N_b (N_b from 1 up to 1024), by the register address 0x800C **[RD3]**, as described in Tab. **10.1** below.

Register Value 0x800C	Buffer Number (N_b)	Size of one Buffer / channel (*)	
		SRAM 1.25 MB (640 kS)/ch	SRAM 10.24 MB (5.12 MS)/ch
0x0	1	1.25 MB – 20 B (640 kS – 10 S)	10.24 MB – 20 B (5.12 MS – 10 S)
0x1	2	640 kB – 20 B (320 kS – 10 S)	5.12 MB – 20 B (2.56 MS – 10 S)
0x2	4	320 kB – 20 B (160 kS – 10 S)	2.56 MB -20 B (1.28 MS – 10 S)
0x3	8	160 kB – 20 B (80 kS – 10 S)	1.28 MB – 20 B (0.64 MS – 10 S)
0x4	16	80 kB – 20 B (40 kS – 10 S)	0.64 MB – 20 B (0.32 MS – 10 S)
0x5	32	40 kB -20 B (20 kS – 10 S)	0.32 MB – 20 B (0.16 MS – 10 S)
0x6	64	20 kB – 20 B (10 kS – 10 S)	0.16 MB – 20 B (0.08 MS – 10 S)
0x7	128	10 kB – 20 B (5 kS – 10 S)	0.08 MB – 20 B (0.04 MS – 10 S)
0x8	256	5 kB – 20 B (2.5 kS – 10 S)	0.04 MB – 20 B (0.02 MS – 10 S)
0x9	512	2.5 kB – 20 B (1.25 kS – 10 S)	0.02 MB – 20 B (0.01 MS – 10 S)
0xA	1024	1.25 kB – 20 B (640 S – 10 S)	0.01 MB – 20 B (5.12 kS – 10 S)

Tab. 10.1: Buffer organization

Having 640 kS memory size as reference, this means that each buffer contains 640k/N_b samples (e.g. N_b = 1024 means 640 samples in each buffer).

(*)IMPORTANT: For AMC FPGA firmware release < **0.2**, the Size of one Buffer related to each Buffer Number must be intended as the number of the samples in Tab. **10.1** without decreasing by 10 samples (20 bytes).

10.6.4.1 Custom-sized Events

In case an event size less than the buffer size is needed, the user can set the N_LOC value at register address 0x8020 **[RD3]**, where N_LOC is the number of memory locations. The size of the event is so forced to be according to the formula:

$$N_{sample} = 10 * N\_LOC$$

When N_LOC = 0, the custom size is disabled.

Note: The value of N_LOC must be set in order that the relevant number of samples does not exceed the buffer size and it must not be modified while the acquisition is running. Even using the custom size setting, the number of buffers and the buffer size are not affected by N_LOC, but they are still determined by N_b.

The concepts of buffer organization and custom size directly affect the width of the acquisition window (i.e. number of the digitized waveform samples per event). The Record Length parameter defined in CAEN software (such as WaveDump and WaveDump2 introduced in Chap. **12**) and the *Set/GetRecordLength* function of the CAENDigitizer library (see Sec. **11.2**) rely on these concepts **[RD5]**.

Note: In the case of DPP firmware, refer to the specific documentation **[RD9][RD11][RD12]**.

10.6.5 Event Structure

The event can be read out via VMEbus or Optical Link; data format is 32-bit long word (see Tab. **10.3**).

An event is structured as:

- **Header** (four 32-bit words)
- **Data** (variable size and format)

10.6.5.1 Header

The header consists of four words carrying the following information:

- **EVENT SIZE** (bit[27:0] of 1st header word) is the size of the event, that is the number of 32-bit long words to be read.
- **BOARD ID** (bit[31:27] of 2nd header word) is the GEO address, meaningful for VME64X modules.
- **BOARD FAIL FLAG** (bit[26] of 2nd header word), implemented from ROC FPGA firmware revision **4.5** on (*reserved* otherwise), is set to "1" as consequence of a hardware problem (e.g. PLL unlocking or over-temperature condition); the user can collect more information about the cause by reading at register address 0x8178 and contact CAEN Support Service if necessary (see Chap. **18**);
- **Bit[24]** (2nd header word) identifies the event format; it is reserved and must be 0;
- **PATTERN/TRG OPTIONS** (bit[23:8] of 2nd header word) is the 16-bit PATTERN latched on the LVDS I/Os as the trigger arrives.

Note: Starting from revision **4.6** of the ROC FPGA firmware, these 16 bits can be programmed to provide trigger information according to the setting of the bits [22:21] at register address 0x811C (see Tab**. 10.2**)

0x811C REGISTER Bits[22:21]	FUNCTIONAL DESCRIPTION	PATTERN/TRG OPTIONS INFORMATION (bit[23:8] of 2nd header word)
00 (default)	PATTERN	Pattern of the 16 LVDS signals
01	Event Trigger Source	Indicates the trigger source causing the event acquisition: Bit[23:19] = 0000 Bit[18] = Software Trigger Bit[17] = External Trigger Bit[16] = Trigger from LVDS connector Bit[15:8] = Channel Trigger requests (refer to Sec. **10.7.3**)
10	Extended Trigger Time Tag (ETTT)	A 48-bit Trigger Time Tag (ETTT) information is configured, where bit[23:8] contribute as the 16 most significant bits together with the 32-bit TTT field of 4th header word **Note:** in the ETTT option, the overflow bit is not provided
11	Not used	If configured, it acts the same as the "00" setting

Tab. 10.2: PATTERN/TRG OPTIONS configuration table

- **CHANNEL MASK** (bit[7:0] of the 2nd and bit[31:24] of the 3rd header word) is the mask of the channels participating in the event (e.g. CH0 and CH12 participating → Channel Mask = 0001 0000 0000 0001). This information must be used by the software to acknowledge which channel the samples are coming from (the first event contains the samples from the channel with the lowest number).

- **EVENT COUNTER** (bit[23:0] of 3rd header word) is the trigger counter; it can count either accepted triggers only, or all triggers (according to bit[3] of register address 0x8100).
- **TRIGGER TIME TAG** (bit[31:0] of 4th header word) is the 31-bit Trigger Time Tag (TTT) information (31 bit counter and 32nd bit as roll-over flag), which is the trigger time reference. The word is composed of the value of the 31-bit counter of the Trigger Time Tag (bit[30:0]) plus the overflow bit (bit[31]) indicating that the timestamp counter has overflowed at least once (Fig. **10.8**). If the ETTT option is enabled, then this field becomes the 32 less significant bits of the 48-bit Extended Trigger Time Tag information in addition to the 16 bits (MSB) of the TRG OPTIONS field (2nd event word). Note that, in the ETTT case, the roll-over flag is no more provided (Fig. **10.9**). The trigger time tag is reset either after each start of acquisition or via front panel signal on S-IN or LVDS I/O connectors, and increments at 125MHz frequency for both V1730 and V1725, which is every 4 ADC clock cycles for V1730 and 2 ADC clock cycles for V1725. The TTT value is read at half this frequency (i.e. 62.5 MHz), so the TTT specifications result in 16 ns resolution and 17 s range (i.e. 8 ns*(2^{31}-1)), which can be extended to 625 h (i.e. 8 ns*(2^{48}-1)) by the Extended Trigger Time Tag option.

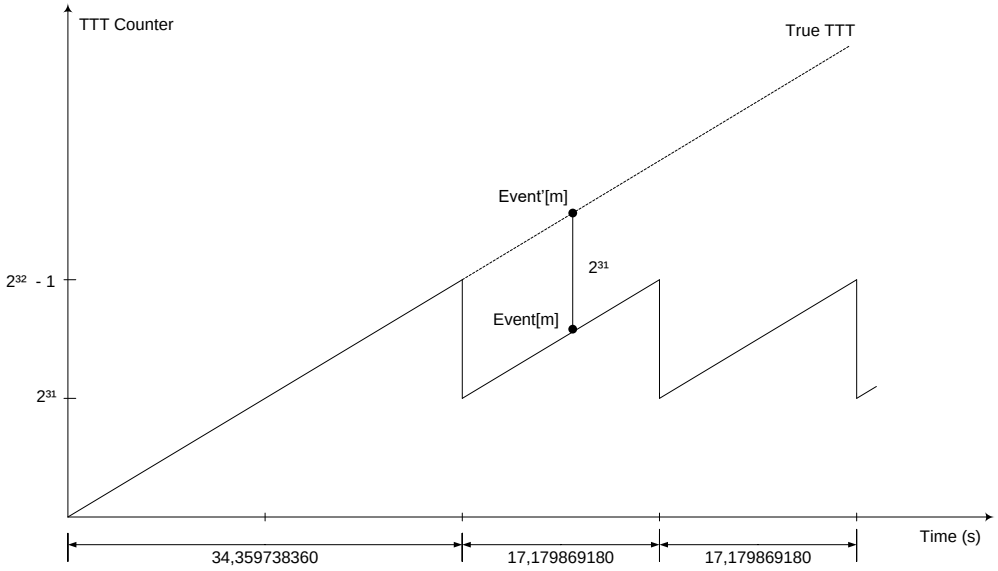


Fig. 10.8: TTT description in case of V1730

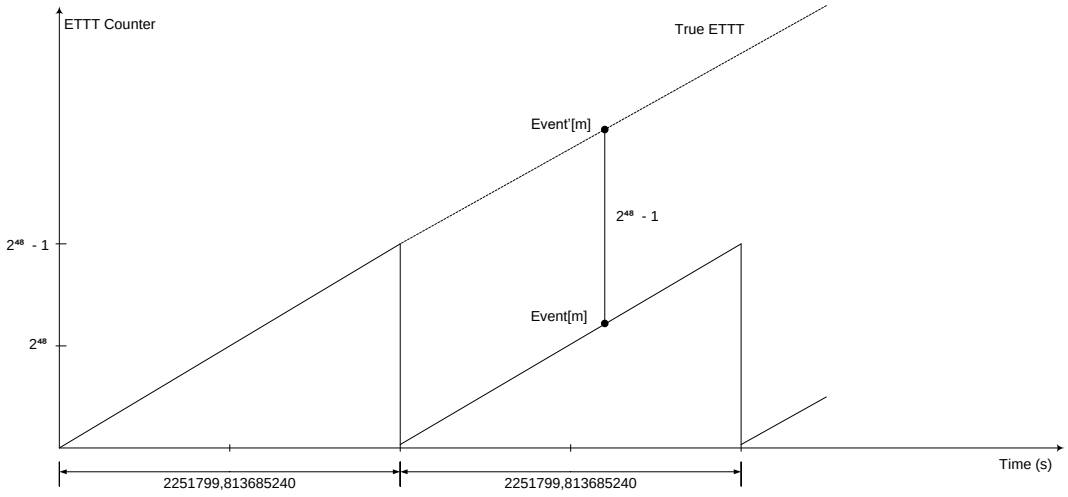


Fig. 10.9: ETTT description in case of V1730

10.6.5.2 Data

Data are the samples from the enabled channels. Data from masked channels are not read.

10.6.5.3 Event Format Example

The event format is shown in the following figure (case of 16 channels enabled).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1	0	1	0	EVENT SIZE																												HEADER
BOARD ID							BF	RES	0	PATTERN / TRG OPTIONS															CHANNEL MASK [7:0]							
CHANNEL MASK [15:8]										EVENT COUNTER																						
TRIGGER TIME TAG																																
0	0	SAMPLE [1] – CH[0]														0	0	SAMPLE [0] – CH[0]														DATA CH0
0	0	SAMPLE [3] – CH[0]														0	0	SAMPLE [2] – CH[0]														
• • •																																
0	0	SAMPLE [N-1] – CH[0]														0	0	SAMPLE [N-2] – CH[0]														
0	0	SAMPLE [1] – CH[1]														0	0	SAMPLE [0] – CH[1]														DATA CH1
0	0	SAMPLE [3] – CH[1]														0	0	SAMPLE [2] – CH[1]														
• • •																																
0	0	SAMPLE [N-1] – CH[1]														0	0	SAMPLE [N-2] – CH[1]														
• • •																																• • •
0	0	SAMPLE [1] – CH[15]														0	0	SAMPLE [0] – CH[15]														DATA CH15
0	0	SAMPLE [3] – CH[15]														0	0	SAMPLE [2] – CH[15]														
• • •																																
0	0	SAMPLE [N-1] – CH[15]														0	0	SAMPLE [N-2] – CH[15]														

Tab. 10.3: Event format example

Note: Data transfer starts from Channel 0; once all the data from one Channel are transferred, data transfer from the subsequent Channel begins.

Note: The firmware saves the waveforms in the memory of the digitizer with a granularity of n (i.e. in group of n samples). This way of writing the waveforms in memory allows for a potential ΔT between the instant when the trigger physically arrives and when it is sensed by the digitizer. The resulting effect is a jitter in the acquisition window between one event and the next. This jitter can be observed by graphing the waveforms of the enabled channels using an acquisition software. The channels may jitter together between one event and the next, but not among themselves.

10.6.6 Acquisition Synchronization

Each channel of the digitizer is provided with a SRAM memory that can be organized in a programmable number N_b of circular buffers (see Sec. **10.6.4**). When the trigger occurs, the FPGA writes further a programmable number of samples for the post-trigger and freezes the buffer, so that the stored data can be read via VMEbus or Optical Link, while the acquisition can continue in a new buffer.

When all buffers are filled, the board is considered FULL: no trigger is accepted and the acquisition stops (i.e. the samples coming from the ADC are not written into the memory, so they are lost). As soon as at least one buffer is read out, the board exits the FULL condition and acquisition restarts.

> ***IMPORTANT:*** *When the acquisition restarts, no trigger is accepted until at least the entire buffer is written. This means that the dead time is extended for a certain time (depending on the size of the acquisition window) after the board exits the FULL condition.*

A way to eliminate this extra dead time is by setting bit[5] = 1 at register address 0x8100. The board is so programmed to enter the FULL condition when N_b-1 buffers are written: no trigger is then accepted, but samples writing continues in the last available buffer. As soon as one buffer is readout and becomes free, the boards exit the FULL condition and can immediately accept a new trigger. This way, the FULL reflects the BUSY condition of the board (i.e. inability to accept triggers).

Note: when bit[5] = 1, the minimum number of circular buffers to be programmed is N_b = 2.

In some cases, the BUSY propagation from the digitizer to other parts of the system has some latency and it can happen that one or more triggers occur while the digitizer is already FULL and unable to accept those triggers. This condition causes event loss and it is particularly unsuitable when there are multiple digitizers running synchronously, because the triggers accepted by one board and not by other boards cause event misalignment.

In these cases, it is possible to program the BUSY signal to be asserted when the digitizer is close to FULL condition, but it has still some free buffers (Almost FULL condition). In this mode, the digitizer remains able to accept some more triggers even after the BUSY assertion and the system can tolerate a delay in the inhibit of the trigger generation. When the Almost FULL condition is enabled by setting the Almost FULL level (register address 0x816C) to X, the BUSY signal is asserted as soon as X buffers are filled, although the board still goes FULL (and rejects triggers) when the number of filled buffers is N_b or N_b-1, depending on bit[5] at register address 0x8100 as described above.

It is possible to provide the BUSY signal on the digitizer front panel TRG-OUT output by bit[20], bit[19:18] and bit[17:16] at register address 0x811C. In case of multi-board setup, the BUSY signal can be propagated among boards through the front panel LVDS I/O connectors (see Sec. **10.9**).

10.6.7 Channel Self-Trigger Rate Meter (725S and 730S only)

Each channel of the digitizer is equipped with a digital discriminator with a programmable threshold (see Sec. **10.7.3**). The discriminator activity can be monitored through a special counter. The 32-bit value of this counter (register address 0x1nEC) indicates how many times per second the input pulse crossed the discriminator threshold on channel n.

Note: the counter is available for 725S and 730S models only and implemented from ROC FPGA fw revision **4.22** on.

10.7 Trigger Management

When operating the waveform recording firmware, all board channels share the same trigger (board common trigger), so they acquire an event simultaneously and in the same way (determined number of samples according to buffer organization and custom size settings, as well as position with respect to the trigger defined by the post-trigger).

Note: For the trigger management in the DPP firmware operating, please refer to the DPP documentation **[RD9] [RD11][RD12]**.

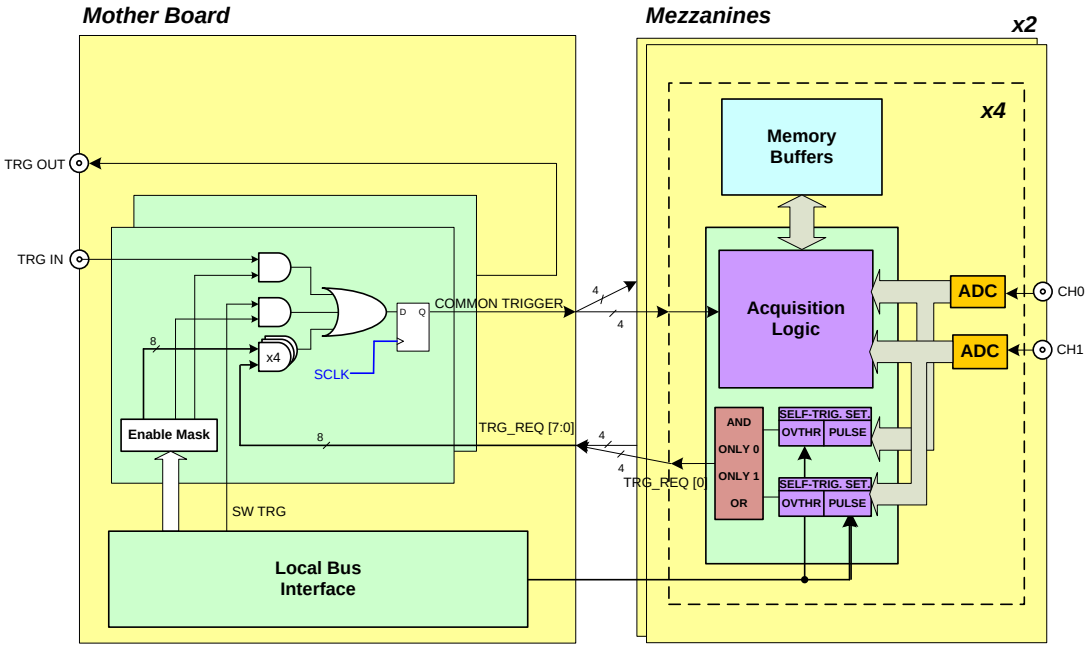


Fig. 10.10: Block Diagram of the trigger management

The digitizer supports different sources for the generation of the board common trigger (configurable at register address 0x810C):

- Software trigger
- External trigger
- Self-trigger
- Coincidences
- TRG-IN as Gate
- LVDS I/O trigger

10.7.1 Software Trigger

Software triggers are internally produced via a software command (write access at register address 0x8108) through VMEbus or Optical Link.

10.7.2 External Trigger

A TTL or NIM external signal can be provided in the front panel TRG-IN connector (configurable at register address 0x811C). When setting up a system of multiple digitizers (see Sec**. 10.8**), there could be a random jitter of 1 TRG-CLK hit (see Sec. **10.4**) if the external signal is provided asynchronously with the internal clock of the boards (e.g. from external trigger FAN-IN on TRG-IN). One board could then sense the trigger at clock_hit[N], while another board at clock_hit[N+1] and the same jitter is then present between the pulse acquired by one board and that acquired by the other board.

10.7.3 Self-Trigger

The digitizer is equipped with a digital discriminator for each channel. Each channel is so able to generate a self-trigger signal when the digitized input pulse crosses the configurable threshold of its discriminator (register address 0x1n80). The self-triggers of each couple of adjacent channels are then processed to output a single trigger request. The trigger requests are propagated to the central trigger logic on the motherboard (see Fig. **10.10**) where they are ORed to produce the board common trigger, which is finally distributed back to all channels causing the event acquisition (see Sec. **10.7.7**). An example of self-trigger and trigger request logic for channel 0 and channel 1 couple is schematized in Fig. **10.11**.

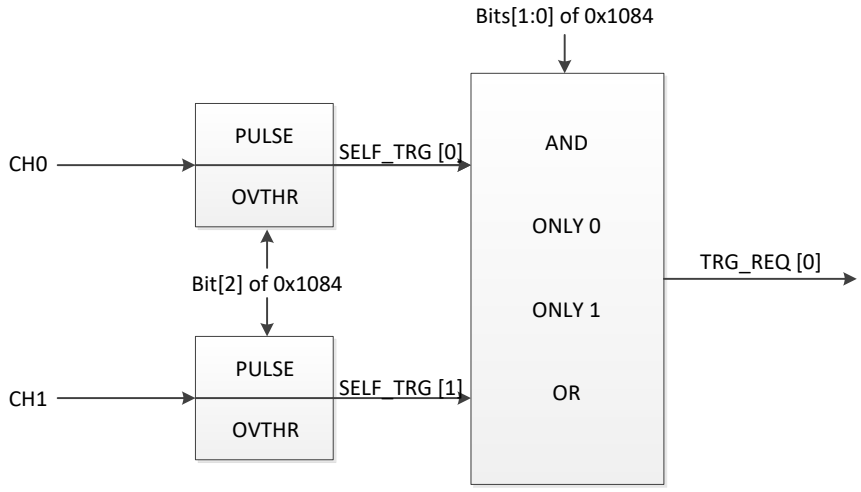


Fig. 10.11: Self Trigger and Trigger Request logic for Ch0 and Ch1 couple. A single trigger request signal is generated.

The FPGA, by register address 0x1n84, can be programmed in order the self-trigger to be:

- an *over/under-threshold signal* (see Fig. **10.12**). This signal can be programmed to be active (i.e. "1") as long as the input pulse stays over the threshold or under the threshold (depending on the trigger polarity bit at register address 0x8000).

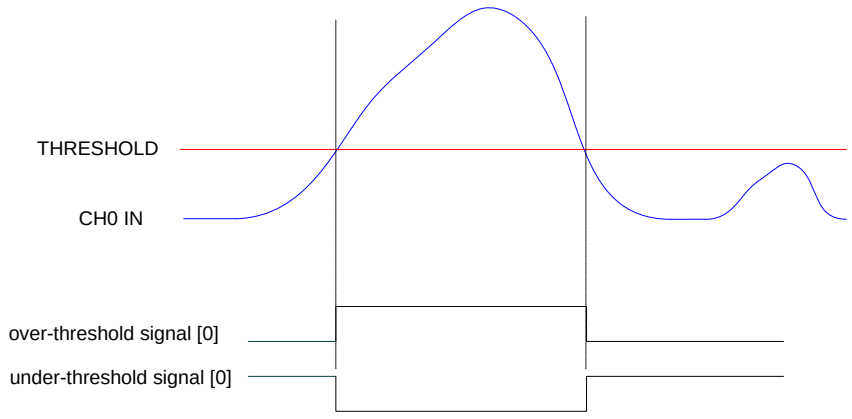


Fig. 10.12: Channel over/under threshold signal

- a *pulse of configurable width* (see Fig. **10.13**); the width parameter can be set at register address 0x1n70.

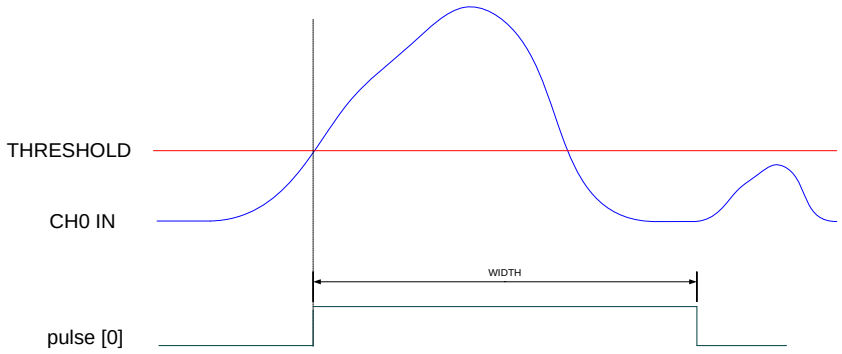


Fig. 10.13: Channel pulse signal

The FPGA, by register address 0x1n84, can be programmed in order the trigger request for a couple of adjacent channels to be the

AND,

ONLY CH(n),

ONLY CH(n+1),

OR

of the relevant self-trigger signals (see Fig. **10.11**).

Default Conditions: by default, the FPGA is programmed so that the trigger request is the OR of two pulses of 16ns-width.

Note: the above described configurability of both the self-trigger logic and the trigger request logic are supported only by AMC FPGA firmware releases > **0.1**.
Previous revisions of the firmware do not implement the register address 0x1n84 as well as the 0x1n70, the self-trigger is intended only as the over/under threshold signal and a trigger request is intended only as the OR of the self-triggers couple.

When operating in self-trigger mode, the firmware includes a feature that allows programming the number of pulse samples required to remain above or below the threshold (depending on signal polarity) to generate a self-trigger. This option can be adjusted in steps of 4 samples within a single trigger clock cycle, by writing at the channel register address 0x1n40. By default, the register value is set to "0," which disables this feature. In this case, a single sample crossing the threshold is enough to generate the trigger pulse.

This new feature is particularly useful to avoid spurious triggers occurring with very noisy signals at low thresholds or signals with a very slow and noisy falling time. For more details refers to document **[RD3]**.

Note: This feature is supported for revision of Waveform Recording firmware >= **4.29_0.9** for V1730/VX1730/V1725/VX1725 and **4.29_0.4** for V1730S/VX1730S/V1725S/VX1725S.

10.7.4 LVDS I/O Trigger

LVDS I/O specific pins on the front panel dedicated connector can be programmed as trigger inputs and enabled to participate in the common trigger generation with other trigger sources. See Fig. **10.18** and refer to Sec. **10.9** for details.

10.7.5 Trigger Coincidence Level

Operating the waveform recording firmware, the acquisition trigger is common to the whole board. This common trigger allows the coincidence acquisition mode to be performed through the Majority operation.

Note: From AMC FPGA firmware release > **0.1**, it is possible to program the self-trigger logic as described in Sec. **10.7.3**.

Enabling the coincidences is possible by writing at register address 0x810C:

- Bit[7:0] enable the trigger request signals to participate in the coincidence;
- Bit[23:20] set the coincidence window (T_{TVAW}) linearly in steps of the Trigger clock;
- Bit[26:24] set the Majority (i.e. Coincidence) level.

The coincidence takes place when:

Number of enabled trigger requests > Majority level

Supposing bit[7:0] = 0xFF (i.e. all the 8 trigger requests are enabled) and bit[26:24] = 01 (i.e. Majority level = 1), a common trigger is issued whenever at least two of the enabled trigger requests are in coincidence within the programmed T_{TVAW}.

The Majority level must be smaller than the number of trigger request signals enabled via bits[7:0] mask. The default setting is bit[26:24] = 00 (i.e. Majority level = 0), which means the coincidence acquisition mode is disabled and the T_{TVAW} is meaningless. In this case, the board common trigger is simple OR of the signals from the enabled channels pairs.

Note: In the following pictures CH4 up to CH15 are considered disabled in order not to overload the plots.

Fig. **10.14** and Fig. **10.15** show the trigger management in case the coincidences are disabled.

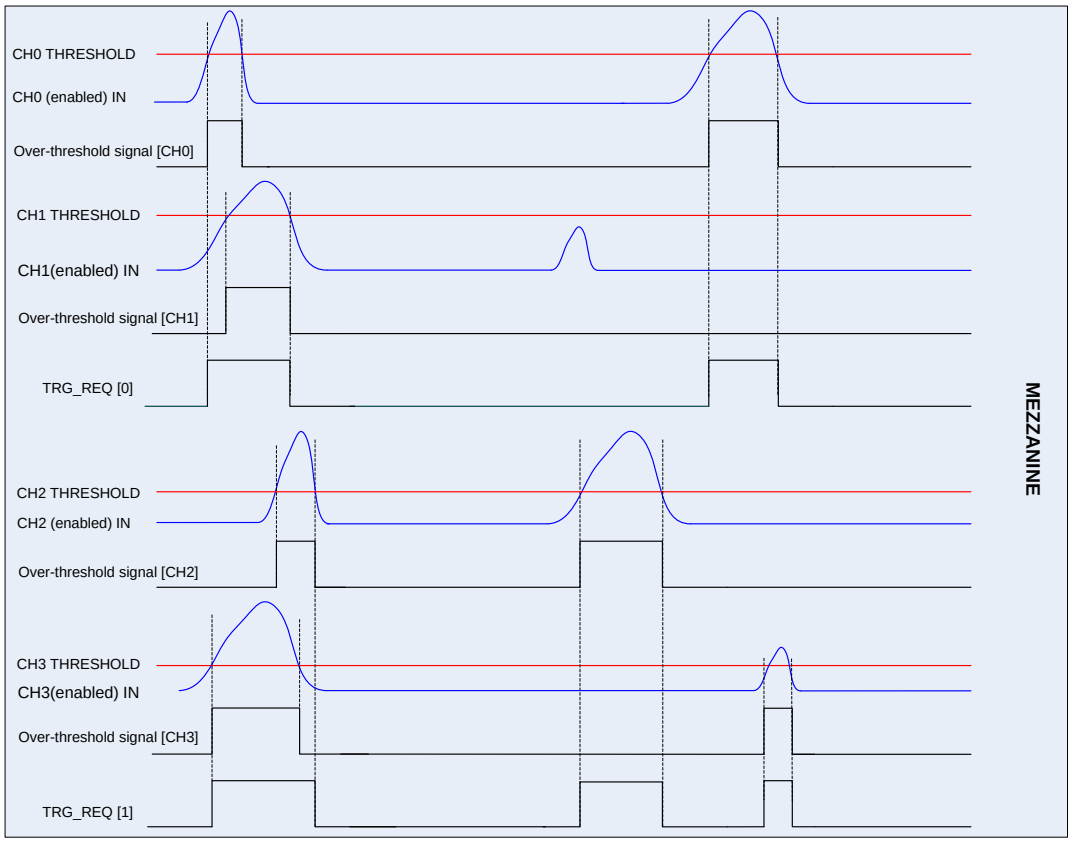


Fig. 10.14: Trigger request management at mezzanine level with Majority level = 0

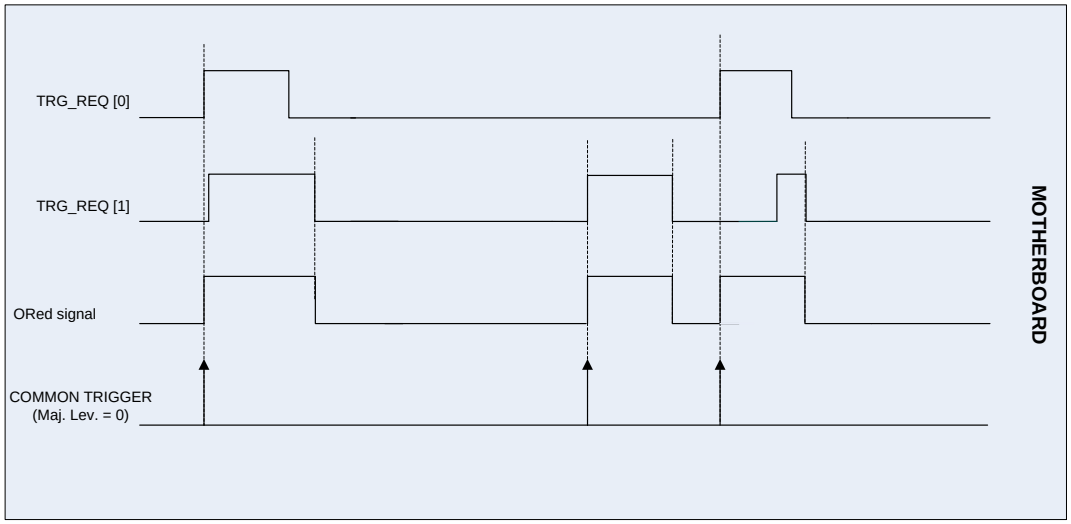


Fig. 10.15: Trigger request management at motherboard level with Majority level = 0

Fig. **10.16** shows the trigger management in case the coincidences are enabled with Majority level = 1 and T_{TVAW} is a value different from 0. In order to simplify the description, CH1 and CH3 channels are considered disabled, so that the relevant trigger requests are the over-threshold signals from CH0 and CH2.

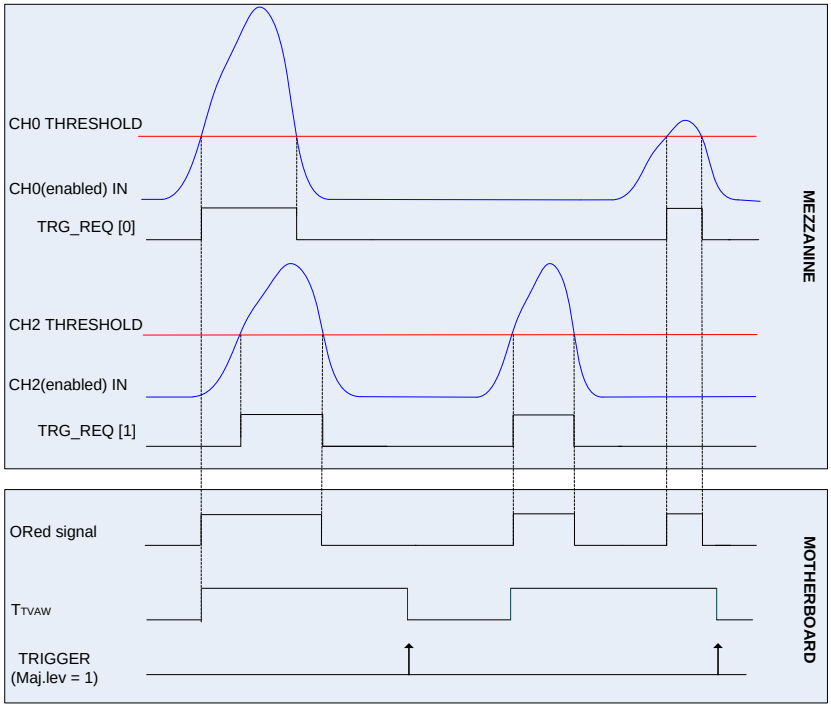


Fig. 10.16: Trigger request relationship with Majority level = 1 and $T_{TVAW} \neq 0$

Note: with respect to the position where the common trigger is generated, the portion of input signal stored depends on the programmed length of the acquisition window and on the post trigger setting.

Fig. **10.17** shows the trigger management in case the coincidences are enabled with Majority level = 1 and T_{TVAW} = 0 (i.e. 1 clock cycle). In order to simplify the description, CH1 and CH3 channels are considered disabled, so that the relevant trigger requests are the over-threshold signals from CH0 and CH2.

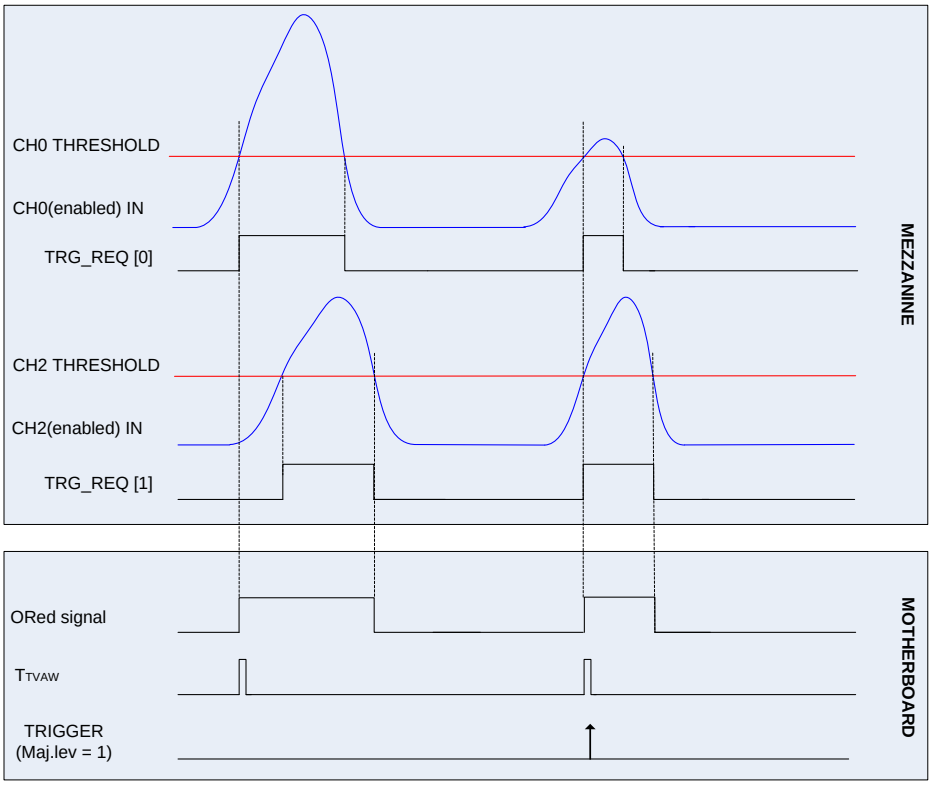


Fig. 10.17: Trigger request relationship with Majority level = 1 and T_{TVAW} = 0

In this case, the common trigger is issued if at least two of the enabled trigger requests are instantaneously in coincidence (no T_{TVAW} is waited).

Note: CAEN provides a guide to coincidences including a practical example of making coincidences with the waveform recording firmware **[RD13]**.

10.7.6 TRG-IN as Gate

It is possible to configure TRG-IN as a gate for trigger anti-veto function. The common acquisition trigger is then issued upon the AND between the external signal on TRG-IN and the other trigger sources but the software trigger (i.e. the software trigger cannot participate in the Trigger as Gate mode).

This mode is enabled by setting bit[27] = 1 of register 0x810C and bit[10] = 1 of register 0x811C. The trigger sources participating in AND with TRG-IN are configurable through register 0x810C as well.

10.7.7 Trigger Distribution

As described in Sec. **10.7**, the OR of all the enabled trigger sources, synchronized with the internal clock, becomes the common trigger of the board that is fed in parallel to all channels, consequently provoking the capture of an event. By default, only the Software Trigger and the External Trigger participate in the common acquisition trigger (refer to the red path on top of Fig. **10.18**).

A Trigger Out signal is also generated on the relevant front panel TRG-OUT connector (NIM or TTL) and allows to extend the trigger signal to other boards.

Thanks to its configurability (see Fig. **10.18**), TRG-OUT can propagate:

- the OR of all the enabled trigger sources (only the Software Trigger is provided by default, as in the red path of Fig. **10.18**);
- the OR, AND or MAJORITY exclusively of the channel trigger requests.

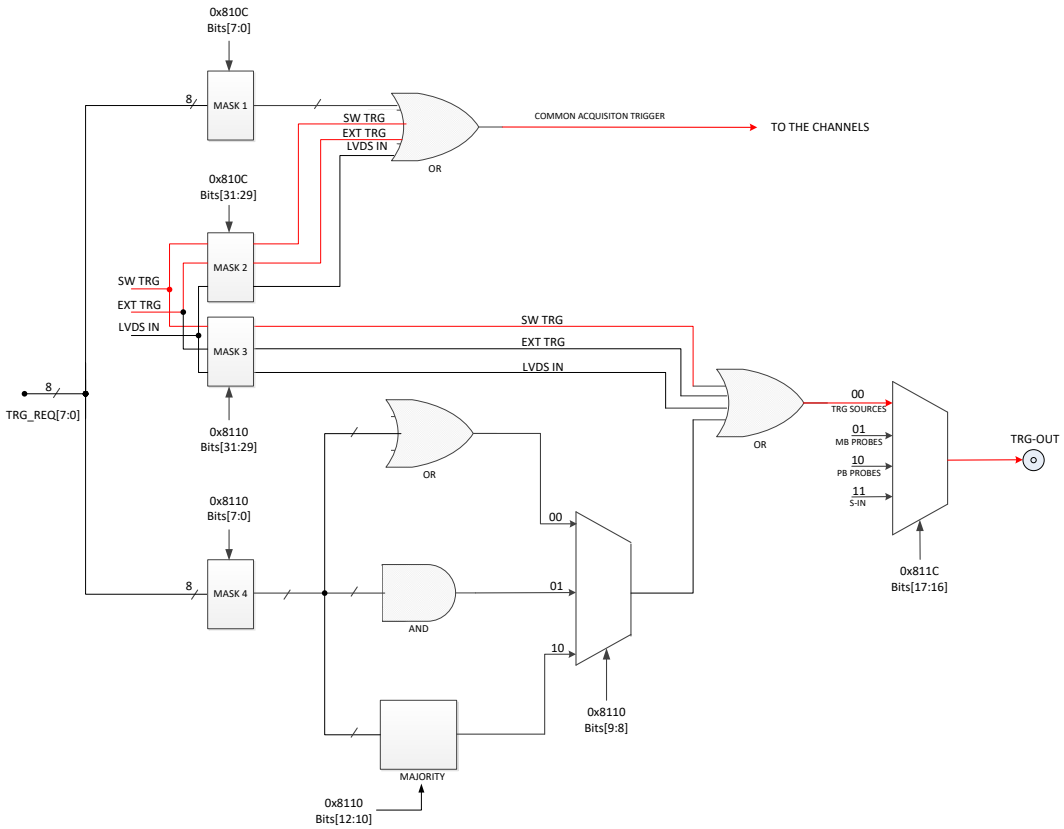


Fig. 10.18: Trigger configuration of TRG-OUT front panel connector

The registers involved in the TRG-OUT programming are:

- 0x8110;
- 0x811C.

Note: for the 8-channel VME versions (C/CS/D/DS), trigger requests and the relevant masks are over 4 bits instead of 8.

10.7.7.1 Example

For instance, it could be required to start the acquisition on all the channels of a multi-board system as soon as one of the channels of a board (board "n") crosses its threshold. Trigger Out signal is then fed to an external Fan Out logic unit (e.g. CAEN V2495 board); the obtained signal has then to be provided to the external trigger input TRG-IN of all the boards in the system (including the board which generated the Trigger Out signal). In this case, the programming steps to perform are following described.

1. Register 0x8110 on board "n":
   - Enable the desired trigger request as Trigger Out signal on board "n" (by bit[7:0] mask).
   - Disable Software Trigger, External Trigger and LVDS I/O Trigger as Trigger Out signal on board "n" (bit[31:29] = 000).
   - Set Trigger Out signal as the OR of the enabled trigger requests on board "n" (bit[9:8] = 00).
2. Register 0x811C on board "n":
   - Configure the digitizer to propagates on TRG-OUT the internal trigger sources according to the 0x8110 settings (i.e. the enabled trigger request, in the specific case) on board "n" (bit[17:16] = 00).
3. Register 0x810C on all the boards in the system (including board "n"):
   - Enable External Trigger to participate in the board common acquisition trigger, disable Software Trigger, LVDS I/O Trigger and the Trigger Requests from the channels (bit[31:29] = 010; bits[7:0] = 00000000).

10.8 Multi-board Synchronization Overview

When multi-board systems are involved in an experiment, it is necessary to synchronize different boards. In this way, the user will be able to acquire from a system of N boards with Y channels each like if they were just one board with (N * Y) channels.

Synchronizing CAEN digitizers mainly means:

- **Clock synchronization:** the goal is to have the same sampling clock in all the channels. There are two possible modes:
  - Clock Fan-Out. The reference clock signal from an external source is split and provided to all the boards in parallel (for example by using CAEN DT4700 unit).
  - Clock Daisy chain**.** The first board acts as clock master; it can use internal 50 MHz or an external clock, then generates a clock-out that is provided to the first slave board that propagates it to the second one, and so on. If a board uses the external clock or must generate the clock-out, it is required to reconfigure the PLL (see Sec. **10.3**);
- **Time Stamp synchronization**: the goal is to have the same start/stop of the acquisition and same zero for the time stamp on all the boards at the start of run.
- **Trigger synchronization:** the goal is to propagate and combine the triggers from all the boards to have the same global trigger for the event acquisition.
- **Event data synchronization:** the goal is to keep the event data aligned across boards (same trigger => same data). Each board asserts the Busy signal when its memory buffer is almost full (see Sec. **10.6.6**); the principle is to have a system Busy (global) to veto the acquisition of all the boards as soon as at least one board goes busy, and as long as the system Busy is asserted.

For details about multi-board synchronization, on how to implement the points above and configure the board accordingly, please refer to the dedicated Application Note **[RD2]** or contact CAEN for support (see Chap. **18**).

10.9 Front Panel LVDS I/Os

The V1730 is provided with 16 general purpose programmable LVDS I/O signals (see Chap. **9**). From the ROC FPGA firmware revision 3.8 on, a more flexible configuration management has been introduced, which allows these signals to be programmed in terms of direction (INPUT/OUTPUT) and function by groups of 4.

THE USER MUST SET BIT[8] = 1 AT 0x811C IN ORDER TO ENABLE THE NEW LVDS I/Os CONFIGURATION MODES

NOTE ABOUT LVDS I/Os CONFIGURATIONS IMPLEMENTED IN ROC FW RELEASES <3.8

*THE DEFAULT FIRMWARE OF V1730 MAKES ALSO AVAILABLE THE OLD CONFIGURATIONS (bit[8] = 0). USERS WHOSE SOFTWARE BASES ON THE OLD LVDS I/Os CONFIGURATION MANAGEMENT CAN REFER TO THE USER MANUAL OF THE RELEVANT DIGITIZER OR CAN CONTACT CAEN (SEE CHAP. **18**) FOR INFORMATION.*

SINCE THIS COULD BE NO LONGER GUARANTEED IN THE FUTURE, THE USER IS HEARTLY RECOMMENDED TO TAKE THE NEW CONFIGURATION MANAGEMENT AS REFERENCE!

The direction of the signals are set by bit[5:2] at register address 0x811C:

Bit[2] → LVDS I/O[3:0]

Bit[3] → LVDS I/O[7:4]

Bit[4] → LVDS I/O[11:8]

Bit[5] → LVDS I/O[15:12]

Where setting the bit to 0 enables the relevant signals in the group as INPUT, while 1 enables them as OUTPUT.

When enabled (i.e. bit[8] = 1), the new management allows each group of 4 signals of the LVDS I/O 16-pin connector to be configured in one of the 4 following modes (according to bits[15:0] at register address 0x81A0):

- Mode 0 (bit[n+3:n] = 0000): REGISTER
- Mode 1 (bit[n+3:n] = 0001): TRIGGER
- Mode 2 (bit[n+3:n] = 0010): nBUSY/nVETO
- Mode 3 (bit[n+3:n] = 0011): LEGACY

where n = 0, 4, 8, 12.

Note: Whatever option is set, the LVDS I/Os are always latched with the trigger and the relevant status of the 16 signals is always written into the Pattern field of the header (see Sec. **10.6.5**) the user can then choose to read it out or not.

WAVE REC. FW	REGISTER	TRIGGER	nBUSY/nVETO	LEGACY
LVDS IN [15:12]	Reg[15:12]	*Not available*	15: nRunIn 14: nTriggerIn 13: nVetoIn 12: nBusyIn	15: reserved 14: reserved 13: reserved 12: nClear_TTT
LVDS IN [11:8]	Reg[11:8]	*Not available*	11: nRunIn 10: nTriggerIn 9: nVetoIn 8: nBusyIn	11: reserved 10: reserved 9: reserved 8: nClear_TTT
LVDS IN [7:4]	Reg[7:4]	*Not available*	7: nRunIn 6: nTriggerIn 5: nVetoIn 4: nBusyIn	7: reserved 6: reserved 5: reserved 4: nClear_TTT
LVDS IN [3:0]	Reg[3:0]	*Not available*	3: nRunIn 2: nTriggerIn 1: nVetoIn 0: nBusyIn	3: reserved 2: reserved 1: reserved 0: nClear_TTT

Tab. 10.4: Features description when LVDS group is configured as INPUT (waveform recording firmware)

DPP FW	REGISTER	TRIGGER	nBUSY/nVETO	LEGACY
LVDS IN [15:12]	Reg[15:12]	TrigIn_Couple[7:4]	15: nRunIn 14: reserved 13: reserved 12: reserved	15: reserved 14: reserved 13: reserved 12: reserved
LVDS IN [11:8]	Reg[11:8]	TrigIn_Couple[3:0]	11: nRunIn 10: reserved 9: reserved 8: reserved	11: reserved 10: reserved 9: reserved 8: reserved
LVDS IN [7:4]	Reg[7:4]	TrigIn_Couple[7:4]	7: nRunIn 6: reserved 5: reserved 4: reserved	7: reserved 6: reserved 5: reserved 4: reserved
LVDS IN [3:0]	Reg[3:0]	TrigIn_Couple[3:0]	3: nRunIn 2: reserved 1: reserved 0: reserved	3: reserved 2: reserved 1: reserved 0: reserved

Tab. 10.5: Features description when LVDS group is configured as INPUT (DPP firmware)

WAVE REC. FW	REGISTER	TRIGGER	nBUSY/nVETO	LEGACY
LVDS OUT [15:12]	Reg[15:12]	TrigOut_Couple[7:4]	15: nRun 14: nTrigger 13: nVeto 12: nBusy	15: Run 14: Trigger 13: DataReady 12: Busy
LVDS OUT [11:8]	Reg[11:8]	TrigOut_Couple[3:0]	11: nRun 10: nTrigger 9: nVeto 8: nBusy	11: Run 10: Trigger 9: DataReady 8: Busy
LVDS OUT [7:4]	Reg[7:4]	TrigOut_Couple[7:4]	7: nRun 6: nTrigger 5: nVeto 4: nBusy	7: Run 6: Trigger 5: DataReady 4: Busy
LVDS OUT [3:0]	Reg[3:0]	TrigOut_Couple[3:0]	3: nRun 2: nTrigger 1: nVeto 0: nBusy	3: Run 2: Trigger 1: DataReady 0: Busy

Tab. 10.6: Features description when LVDS group is configured as OUTPUT (waveform recording firmware)

DPP FW	REGISTER	TRIGGER	nBUSY/nVETO	LEGACY
LVDS OUT [15:12]	Reg[15:12]	TrigOut_Couple[7:4]	15: nRun 14: reserved 13: reserved 12: reserved	15: Run 14: reserved 13: reserved 12: reserved
LVDS OUT [11:8]	Reg[11:8]	TrigOut_ Couple[3:0]	11: nRun 10: reserved 9: reserved 8: reserved	11: Run 10: reserved 9: reserved 8: reserved
LVDS OUT [7:4]	Reg[7:4]	TrigOut_ Couple[7:4]	7: nRun 6: reserved 5: reserved 4: reserved	7: Run 6: reserved 5: reserved 4: reserved
LVDS OUT [3:0]	Reg[3:0]	TrigOut_ Couple[3:0]	3: nRun 2: reserved 1: reserved 0: reserved	3: Run 2: reserved 1: reserved 0: reserved

Tab. 10.7: Features description when LVDS group is configured as OUTPUT (DPP firmware)

10.9.1 Mode 0: REGISTER

Direction is INPUT: the logic level of the LVDS I/O signals can be read at register address 0x8118.

Direction is OUTPUT: the logic level of the LVDS I/O signals can be written at register address 0x8118.

10.9.2 Mode 1: TRIGGER

Note: Each pin of the LVDS I/O connector handles a couple of channels (e.g. 8 pins may be used to transmit 8 different trigger signals, each one propagated to a particular couple of channels).

Direction is INPUT: Available only in case of DPP firmware loaded on the FLASH page (see Tab. **10.5**).

Direction is OUTPUT: the TrgOut_Couple[(n + 3) : n] signals (n = 0, 4) consist of the trigger requests coming directly from the channel couples on the mezzanines.

Note: trigger requests are limited to 4 In case of 8-channel VME versions (C/CS/D/DS).

10.9.3 Mode 2: nBUSY/nVETO

Note: In case a DPP firmware is loaded on the FLASH page, only the nRun signal (among those described below) is available in the nBusy/nVETO mode (see Tab. **10.5** and Tab. **10.7**).

nBusy Signal

nBusyIn (INPUT) is an active low signal which, if enabled, is used to generate the nBusy signal (OUTPUT) as below.

The Busy signal (fed out on LVDS I/Os or TRG-OUT LEMO connector) is:

Almost_Full OR (**LVDS_BusyIn** AND **BusyIn_enable**)

where

- **Almost_Full** indicates the filling of the Buffer Memory up to a programmable level (12-bit range) set at register address 0x816C;
- **LVDS_BusyIn** is available in nBUSY/nVETO configuration (see Tab. **10.4**);
- **BusyIn_enable** is enabled by bit[8] = 1 at register address 0x8100.

nVETO Signal

Direction is INPUT: nVETOIn is an active low signal which, if enabled (bit[9] = 1 at register address 0x8100), it is used to veto the generation of the common trigger propagated to the channels for the event acquisition.

NVetoIn can optionally be used to disable the TRG-OUT generation (TRG-OUT VETO). The TRG-OUT VETO is enabled by setting bit[12] = 1 a register address 0x8100, while the TRG-OUT VETO duration can be extended by the register 0x81C4.

Direction is OUTPUT: the nVETO signal is the copy of nVETOIn.

nTrigger Signal

Direction is INPUT: nTriggerIn is an active low signal which, if enabled, is a real trigger able to cause the event acquisition. It can be propagated to TRG-OUT LEMO connector or to the individual triggers.

Direction is OUTPUT: nTrigger signal is configurable as copy either of the trigger signal propagated to the TRG-OUT LEMO connector or of the acquisition common trigger (bit[16] at the 0x81A0 register from ROC FPGA firmware rev. 4.9 on).

nRun Signal

Direction is INPUT: nRunIn is an active low signal which can be used as Start for the digitizer (bit[1:0] = 11 at register address 0x8100). It is possible to program the Start on the level or on the edge of the nRunIn signal (bit[11] at register address 0x8100).

Direction is OUTPUT: nRun signal is the inverse of the internal Run of the board.

10.9.4 Mode 3: LEGACY

Note: In case a DPP firmware is loaded on the FLASH page, no signal is available if the direction is INPUT, while only the Run signal is available if the direction is OUTPUT in the Legacy mode (see Tab. **10.5** and Tab. **10.7**).

Legacy Mode has been introduced in order the LVDS connector (properly programmed) to be able to feature the same I/O signals available in the ROC FPGA firmware revisions lower than 3.8.

nClear_TTT signal

Direction is INPUT: It is the Trigger Time Tag (TTT) reset, like in the old configuration.

Direction is OUTPUT: not implemented.

Busy Signal

Direction is INPUT: not used.

Direction is OUTPUT: the Busy signal is active high and it is exactly the inverse of the nBusy signal (see Sec. **10.9.3**). In case register address 0x816C is set to 0x0 and the BusyIn signal is disabled, the Busy is the FULL signal present in the old configuration.

DataReady Signal

Direction is INPUT: not used.

Direction is OUTPUT: the DataReady is an active high signal indicating that the board has data available for readout (the same as the DataReady front panel LED does).

Trigger Signal

Direction is INPUT: not used.

Direction is OUTPUT: the active high Trigger signal is the copy of the acquisition trigger (common trigger) sent from the motherboard to the mezzanines (it is neither the signal provided out on the TRG-OUT LEMO connector nor the inverse of the signal sent to the LVDS connector).

Run Signal

Direction is INPUT: not used.

Direction is OUTPUT: the Run signal is active high and represents the inverse of the nRun signal (see Sec. **10.9.3**).

10.10 Analog Monitor

The board houses a 12-bit, 125MHz DAC with a dynamic of 0÷1 V on a 50 Ω load, whose input is controlled by the ROC FPGA and the signal output (driving 50 Ω) is available on the MON/Σ output connector (see Sec. **9.1**). MON output of more boards can be summed by an external Linear Fan In.

The DAC control logic implements four operating modes according to the value of bit[2:0] at register address 0x8144:

MODE	0x8144 VALUE
Trigger Majority	0x0
Test	0x1
Not used	0x2
Buffer Occupancy	0x3
Voltage Level	0x4

10.10.1 Trigger Majority Mode

It is possible to generate a Majority signal with the DAC: a voltage signal whose amplitude is proportional to the number of channels under-/over-threshold (1 step = 125 mV); this allows, via an external discriminator, to produce a common trigger signal when the number of triggering channels has exceeded a particular threshold.

Note that the step is driven by the output signal coming from the channel logic (see Sec. **10.7.3**), so it can be retrieved the overthreshold information of a maximum of 8 different channels or all the 8 couples.

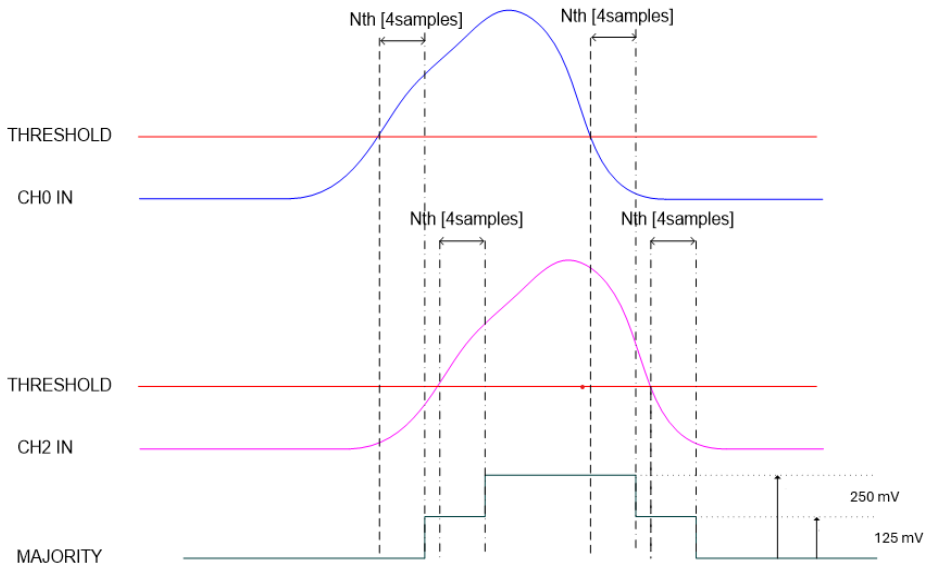


Fig. 10.19: Majority logic (2 channels over threshold; bit[6]= 0 at register address 0x8000)

In the example depicted in Fig. **10.19**, the MON output provides a signal whose amplitude is proportional to the number of channels over the trigger threshold.

10.10.2 Test Mode

In this mode, the MON output provides a saw-tooth signal with 1V amplitude and 24.41kHz frequency.

10.10.3 Buffer Occupancy Mode

In this mode, MON output connector provides a voltage value increasing proportionally with the number of buffers filled with events, in fixed steps of 0.976 mV given by:

$$\frac{V_{max}}{N_{bmax}}$$

where $V_{max} \approx 1$ V and $N_{bmax} = 1024$ is the Maximum_Number_of_Buffers (i.e. the value of register address 0x800C, as introduced in Sec. **10.6.4**).

Example: if 0x800C = 0x4 (i.e. 16 buffers), the maximum Buffer Occupancy output voltage level is given by 0.976 mV * 16.

This mode allows to test the readout efficiency: in fact, if the average event readout throughput is as fast as trigger rate, then MON out value remains constant; otherwise, if MON out value grows in time, this means that readout rate is slower than trigger rate.

Starting from revision **4.9** of the ROC FPGA firmware, it is possible to apply a digital gain to the fixed step, particularly when the memory is organized in a small number of buffers. The gain can be set as powers of two ranging between $2^0 = 1$ (no gain, which is the default setting) and 2^A, where the exponent is the value to write at register address 0x81B4.

10.10.4 Voltage Level Mode

In this mode, MON out provides a voltage value programmable via the 12-bit 'N' parameter written at register address 0x8138, with: $V_{mon} = 1/4096*N$ (Volt).

10.11 Test Pattern Generator

The AMC FPGA can emulate the ADC and write into memory a triangular signal sweeping the entire ADC dynamics for test purposes. It can be enabled via register address 0x8000.

10.12 Reset, Clear and Default Configuration

10.12.1 Global Reset

Global Reset is performed at Power-ON of the module or via software by write access at register address 0xEF24 (whatever 32-bit value can be written). It allows to clear the data off the Output Buffer, the event counter and performs a FPGAs global reset, which restores the FPGAs to the default configuration. It initializes all counters to their initial state and clears all detected error conditions.

10.12.2 Memory Reset

The Memory Reset clears the data off the Output Buffer.

The Memory Reset can be forwarded via a write access at register address 0xEF28 **[RD3]** (whatever 32-bit value can be written).

10.12.3 Timer Reset

The timer reset initializes the time tag counters (Event Time Tag and Group Trigger Time Tag). The timer reset can be issued either via software by a software clear command at 0xEF28 register address, or via hardware by sending a pulse to the front panel Trigger Time Tag Reset input of LVDS I/Os (see Sec. **10.9**), or to the S-IN input (leading edge sensitive). In case the S-IN connector needs to be used to reset the trigger time stamps, no configurations or access to registers are necessary. The user only has to transmit a NIM or TTL signal to the input, depending on the software selected logic level for the S-IN connector. The time stamps reset occurs at every leading edge of the logic signal sent to the S-IN connector.

10.13 VMEBus Interface

The module is provided with a fully compliant VME64/VME64X interface, whose main features are:

- EUROCARD 9U Format
- J1/P1 and J2/P2 with either 160 pins (5 rows) or 96 (3 rows) connectors
- A24, A32 and CR-CSR address modes
- D32, BLT/MBLT, 2eVME, 2eSST data modes
- MCST write capability
- CBLT data transfers
- RORA interrupter
- Configuration ROM

10.13.1 Addressing Capabilities

- Base address: the module works in A24/A32 mode The Base Address of the module is selected through four rotary switches (see Fig. **9.2**), then it is validated only with either a Power-ON cycle or a System Reset (see Sec. **10.12.1**).

ADDRESS MODE	ADDRESS RANGE	NOTES
A24	[0x000000:0xFF0000]	SW2 and SW3 ignored

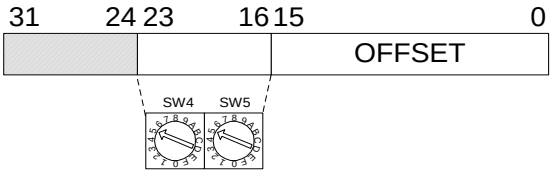


Fig. 10.20: A24 addressing

ADDRESS MODE	ADDRESS RANGE	NOTES
A32	[0x00000000:0xFFFF0000]	-

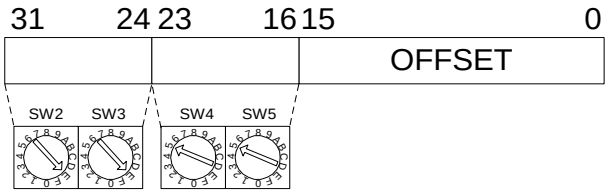


Fig. 10.21: A32 addressing

- CR/CSR address: the addressing is based on the slot number taken from the relevant backplane lines. The recognised Address Modifier for this cycle is 2F. This feature is implemented only on versions with 160-pin connectors.

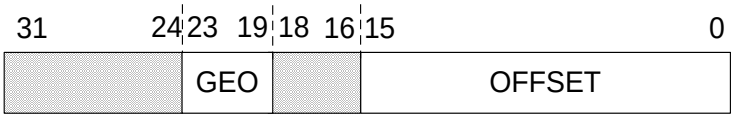


Fig. 10.22: CR/CSR addressing

10.13.2 Address Relocation

Bit[15:0] at register address 0xEF10 allow to set via software the board Base Address (valid values ≠ 0). Such register allows to overwrite the rotary switches settings; its setting is enabled via register address 0xEF00 (bit[6]). The used addresses are:

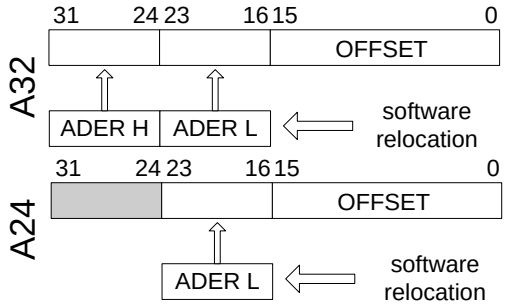


Fig. 10.23: Software relocation of base address

10.14 Data Transfer Capabilities and Events Readout

The board features a Multi-Event digital memory per channel, configurable by the user to be divided into 1 up to 1024 buffers, as detailed in Sec. **10.6.4**. Once they are written in the memory, the events become available for readout via VMEbus or Optical Link. During the memory readout, the board can store other events (independently from the readout) on the available free buffers.

The events are read out sequentially and completely, starting from the header of the first available event, followed by the samples of the enabled channels (from 0 to 15) as reported in **Tab. 10.3**. Once an event is completed, the relevant memory buffer becomes free and ready to be written again (old data are lost). After the last word in an event, the first word (Header) of the subsequent event is readout. It is not possible to read out an event partially.

The size of the event (EVENT SIZE) is configurable and depends on register addresses 0x8020 and 0x800C, as well as on the number of enabled channels.

The board supports D32 single data readout, Block Transfer BLT32, MBLT64 (70 MB/s by CAEN Bridge), CBLT32/64, 2eVME, 2eSST (up to 200 MB/s).

10.14.1 Block Transfer D32/D64, 2eVME and 2eSST

The Block Transfer readout mode allows to read N complete events sequentially, where N is set at register address 0xEF1C, or by using the SetMaxNumEventsBLT function of the CAENDigitizer library **[RD5]**.

When developing programs, the readout process can be implemented on different basis:

- Using **Interrupts**: as soon as the programmed number of events is available for readout, the board sends an interrupt to the PC over the optical communication link **(not supported by USB)**.
- Using **Polling** (interrupts disabled): by performing periodic read accesses to a specific register of the board it is possible to know the number of events present in the board and perform a BLT read of the specific size to read them out.
- Using **Continuous Read** (interrupts disabled): continuous data read of the maximum allowed size (e.g. total memory size) is performed by the software without polling the board. The actual size of the block read is determined by the board that terminates the BLT access at the end of the data, according to the configuration of register address 0xEF1C, or the library function SetMaxNumEventsBLT mentioned above. If the board is empty, the BLT access is immediately terminated and the “Read Block” function will return 0 bytes (it is the ReadData function in the CAENDigitizer Library **[RD5]**).

The event is configurable as indicated in the introduction of the paragraph, namely:

[Event Size] = [8*(Buffer Size)] + [16 bytes]

Then, it is necessary to perform as many cycles as required in order to readout the programmed number of events.

It is suggested to enable BERR signal during BLT32 cycles, in order to end the cycle avoiding filler readout. The last BLT32 cycle will not be completed, it will be ended by BERR after the #N event in memory is transferred (see example in the figure below).

Since some 64-bit CPU cut off the last 32- bit word of a transferred block, if the number of words composing such block is odd, it is necessary to add a dummy word (which has then to be removed via software) in order to avoid data loss. This can be achieved by setting the ALIGN64 bit (bit[5]) at register address 0xEF00.

MBLT64 cycle is similar to the BLT32 cycle, except that the address and data lines are multiplexed to form 64 bit address and data buses.

The 2eVME allows to achieve higher transfer rates thanks to the requirement of only two edges of the two control signals (DS and DTACK) to complete a data cycle.

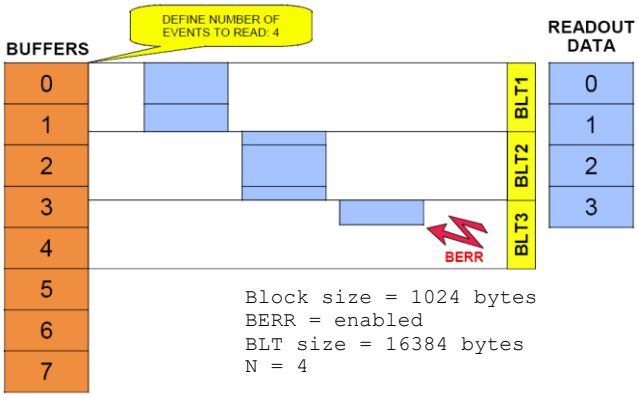


Fig. 10.24: Example of BLT readout

10.14.2 Chained Block Transfer D32/D64

The board allows to read out events from more daisy chained boards (Chained Block Transfer mode).

The technique which handles the CBLT is based on the passing of a token between the boards; it is necessary to verify that the used VME crate supports such cycles.

Several contiguous boards, in order to be Daisy chained, must be configured as “first”, “intermediate” or “last” via register address 0xEF0C. A common Base Address is then defined via the same register; when a BLT cycle is executed at the address CBLT_Base + 0x0000 ÷ 0x0FFC, the “first” board starts to transfer its data, driving DTACK properly; once the transfer is completed, the token is passed to the second board via the IACKIN-IACKOUT lines of the crate, and so on until the “last” board, which completes the data transfer and asserts BERR (which has to be enabled): the Master then ends the cycle and the slave boards are rearmed for a new acquisition.

If the size of the BLT cycle is smaller than the events size, the board which has the token waits for another BLT cycle to begin (from the point where the previous cycle has ended).

10.14.3 Single D32 Transfer

This mode allows to read out a word per time, from the header (actually 4 words) of the first available event, followed by all the words until the end of the event, then the second event is transferred. The exact sequence of the transferred words is shown in Sec. **10.6.5**.

After the 1st word is transferred, it is suggested to check the EVENT SIZE information and then do as many cycles as necessary (actually EVENT SIZE -1) to read completely the event.

10.15 Optical Link Access

The digitizer houses an interface for optical link communication which uses optical fiber cables as physical transmission line, with a maximum transfer data rate of 80 MB/s.

CONET is the proprietary serial protocol designed by CAEN to enable optical link communication between digitizers (acting as CONET slaves) and the host PC. This communication needs CONET master such as the A5818 controllers, or the A4818 adapter.

CONET2 is the latest protocol version, implemented at the firmware level on digitizers and controllers, that improves the data transfer rate efficiency by 50% compared to the earlier CONET1 version.

Note: CONET1 and CONET2 protocol versions are incompatible; communication will fail in any optical chain containing both CONET1 and CONET2 boards.

To update your system from CONET1 to CONET2, it is recommended to follow the instructions provided by CAEN in the dedicated Application Note **[RD19]**.

The optical link interface has Daisy-chain capability. Therefore, it is possible to connect up to eight digitizers to a single Optical Link Controller by using the A4818 adapter, while up to thirty-two digitizers with the A5818 PCIe card. Detailed information can be found at the relevant controller web page on CAEN website.

The parameters for read/write accesses via Optical Link are the same used by VME cycles (Address Modifier, Base Address, data Width, etc…); wrong parameter settings cause Bus Error.

Setting bit[3] at register address 0XEF00 enables the module to broadcast an interrupt request on the Optical Link; the enabled Optical Link Controllers propagate the interrupt on the PCI bus when a request from the Optical Link is sensed. Interrupts can also be managed at the CAENDigitizer library level **[RD5]**.

VME and Optical Link accesses take place on independent paths and are handled by board internal controller, with VME having higher priority; anyway it is better to avoid accessing the board via VME and Optical Link simultaneously.

11 Drivers & Libraries

11.1 Drivers

In order to interface with the board, CAEN provides the drivers for the supported physical communication channels and compliant with Windows® and Linux® OS:

- **CONET Optical Link**, managed by the A5818 PCIe cards. The driver installation package is available on CAEN website in the "Software/Firmware" tab at the A5818 page (**login required**).

Note: For the installation of the Optical Link driver, refer to the User Manual of the specific card **[RD16]**.

- **USB-2.0 Link**, managed by the CAEN (USB-to-VME) Bridges V3718. The driver installation package is downloadable for free on CAEN website at the V3718 page (**login required**).
- **USB-3.0 Link**, managed by the V4718 (USB3-to-VME) Bridge and by the A4818 (USB3-to-CONET) Adapter. The driver installation packages are downloadable for free on CAEN website at the V4718 and A4818 page respectively (**login required**).

Note: To install the USB Link driver, follow the instructions inside the ReadMe file included in the packet, or refer to the V3718, V4718 User Manuals **[RD17][RD18]**, or A4818 Data Sheet **[RD15]**.

11.2 Libraries

CAEN libraries are a set of middleware software required by CAEN software tools for a correct functioning. These libraries, including also demo and example programs, represent a powerful base for users who want to develop customized applications for the digitizer control (communication, configuration, readout, etc.):

- **CAENDPP (DPP-PHA firmware only) [RD10]** is a high-level library of C functions designed to completely control exclusively CAEN digitizers running DPP-PHA firmware and Digital MCAs. The library manages all the relevant board settings, DPP parameters configuration, data acquisition storage. Configuration of synchronized start/stop acquisition is supported in multi-board hardware setup, as well as the single board can be configured for coincidences or anticoincidences among channels. Histograms are built at the library level and managed through specific library functions; other advanced histogram functionalities are provided (e.g. histogram recovery). Lists of data can be automatically saved to output files. HV management is also handled by the library, if supported by the target board.
- **CAENDigitizer [RD5]** is a library of C functions designed specifically for the Digitizer families and it supports both waveform recording and DPP firmware. The CAENDigitizer library is based on the CAENComm which, in turn, is based on CAENVMELib. For this reason, **the CAENVMELib and CAENComm libraries must be already installed on the host PC before installing the CAENDigitizer**.
- **CAENComm** library **[RD4]** manages the communication at low level (read and write access). The purpose of this library is to implement a common interface to the higher software layers, masking the details of the physical channel and its protocol, thus making the libraries and applications that rely on the CAENComm independent from the physical layer. **The CAENComm requires the CAENVMELib library (access to the VME bus) even in the cases where the VME is not used.**

Installation packages are available for free download on CAEN web site (*www.caen.it*) at the relevant library product page (**login required**).

As an alternative to the libraries mentioned above, a more recent set of libraries can be used:

- **CAEN_FE_lib [RD14]** is a library that can be used to control and acquire data from CAEN digitizers. This library is just an interface and does not include support to any digitizer family. In order to use a digitizer, you must install first the respective underlying CAEN_Digx library.
- **CAEN_DIG1_lib [RD14]** is the high level library of functions designed specifically for CAEN V/VX17xx, DT57xx, N67xx first generation digitizers. The CAEN_FE_Lib library must be already installed on the host PC before installing the CAEN_Dig1.
- **CAEN_DIG2_lib [RD14]** is the high level library of functions designed specifically for CAEN 27xx second generation digitizers. The CAEN_FE_Lib library must be already installed on the host PC before installing the CAEN_Dig2.

Installation packages are available for free download on CAEN web site ((*www.caen.it*) at CAEN_FELib page (**login required**.

THE 725S/730S DIGITIZER VERSIONS ARE SUPPORTED FROM CAENDIGITIZER REL. 2.15.0 ON

WINDOWS® and LINUX® compliant customized software. *The user must install the required libraries apart.* ***LINUX® compliant non-stand alone CAEN software.*** *The user must install the required libraries apart to run the software.*

The CAENComm (and so the CAENDigitizer) library supports the following communication channels (see Fig. **11.1**).

PC → USB3 → A4818 → CONET → VME64/VME64X Digitizer

PC → USB → V3718/VX3718 → VMEbus → VME64/VME64X Digitizer

PC → USB3 → V4718/VX4718 → VMEbus → VME64/VME64X Digitizer

PC → USB3 → A4818 → CONET → V3718/VX3718 → VMEbus → VME64/VME64X Digitizer

PC → USB3 → A4818 → CONET → V4718/VX4718 → VMEbus → VME64/VME64X Digitizer

PC → PCI/PCIe → A2818/A3818/A5818 → CONET → VME64/VME64X Digitizer

PC → PCI/PCIe → A2818/A3818/A5818 → CONET → V3718/VX3718 → VMEbus → VME64/VME64X Digitizer

PC → PCI/PCIe → A2818/A3818/A5818 → CONET → V4718/VX4718 → VMEbus → VME64/VME64X Digitizer

PC → ETHERNET → V4718/VX4718 → VMEbus → VME64/VME64X Digitizer

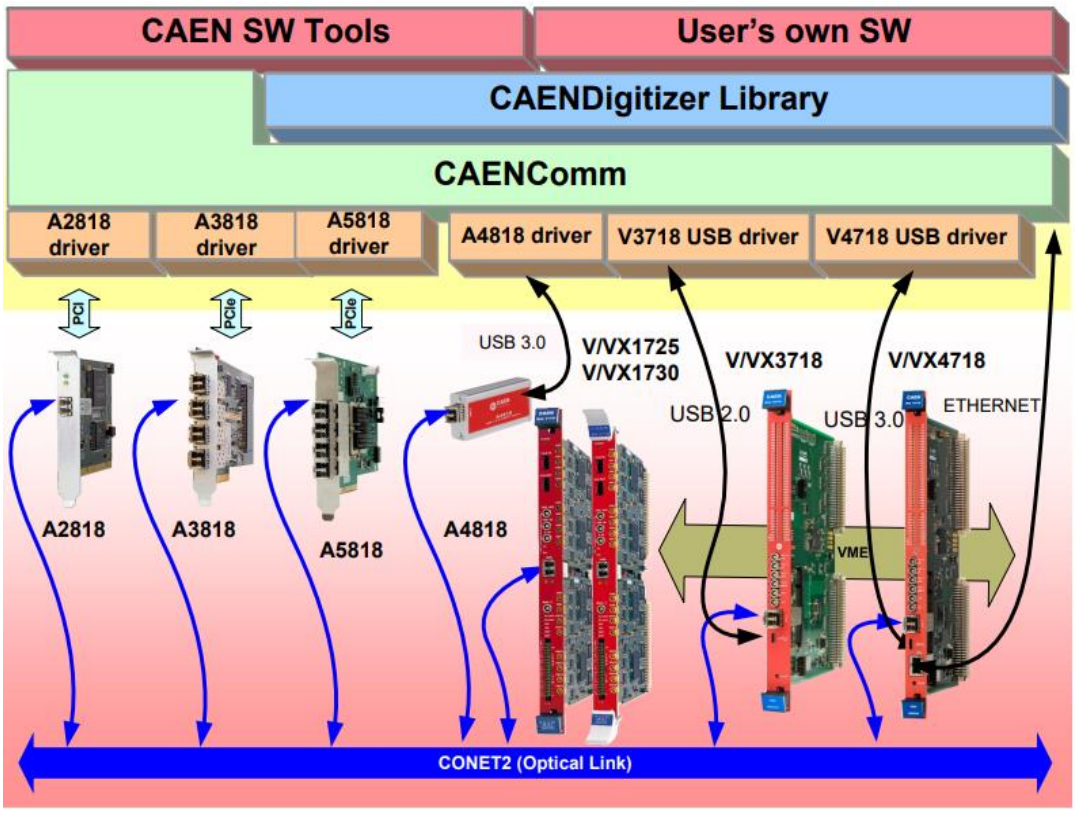


Fig. 11.1: Drivers and software layers based on CAENComm and CAENDigitizer libraries.

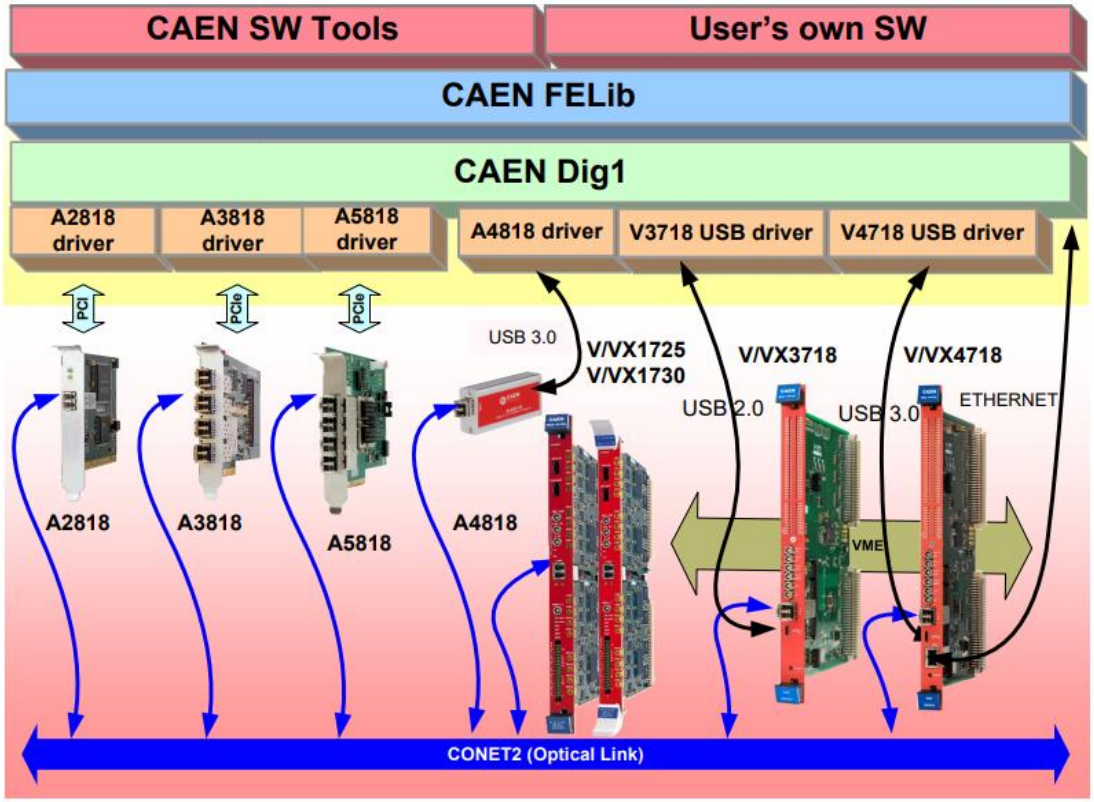


Fig. 11.2: Drivers and software layers based on CAEN_FELib and CAEN_Dig1 libraries.

12 Software Tools

CAEN provides software tools to interface the 730 and 725 digitizer families, which are available for free download on CAEN web site (www.caen.it) in the relevant software and firmware product pages (**login required**).

12.1 CAEN Toolbox

CAEN Toolbox is the comprehensive software suite designed for CAEN Front-End boards.

With V1730/V1725, CAEN Toolbox simplifies various tasks into a few easy steps, including:

- Uploading different FPGA firmware versions to the digitizer
- Reading the firmware release of the digitizer
- Managing firmware licenses, particularly for DPP firmware
- Upgrading the internal PLL
- Obtaining the Board Info file, useful for support
- Managing the reboot of the FPGA firmware from either the Backup or the Standard FLASH page
- Debugging your setup using the Manual Controller

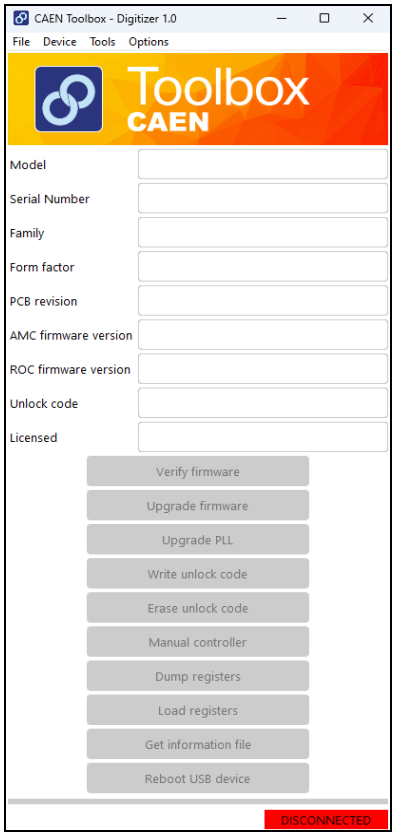


Fig. 12.1: CAEN Toolbox Graphical User Interface

Related to V1725/VX1725 and V1730/VX1730, CAEN Toolbox is based on the CAENComm library (see Sec. **11.2**). The software is compatible with both Windows® and Linux® platforms, operating as a standalone application on each available version. For installation instructions and a detailed description of tis features, refer to the CAEN Toolbox documentation **[RD1]**. Both documentation and software packages can be downloaded directly from the dedicated webpage on the CAEN website (**login required**).

12.2 CAENComm Demo

CAENComm Demo is a simple software developed in C/C++ source code and provided both with Java™ and LabVIEW™ GUI interface. The demo mainly allows for a full board configuration at low level by direct read/write access to the registers and may be used as a debug instrument.

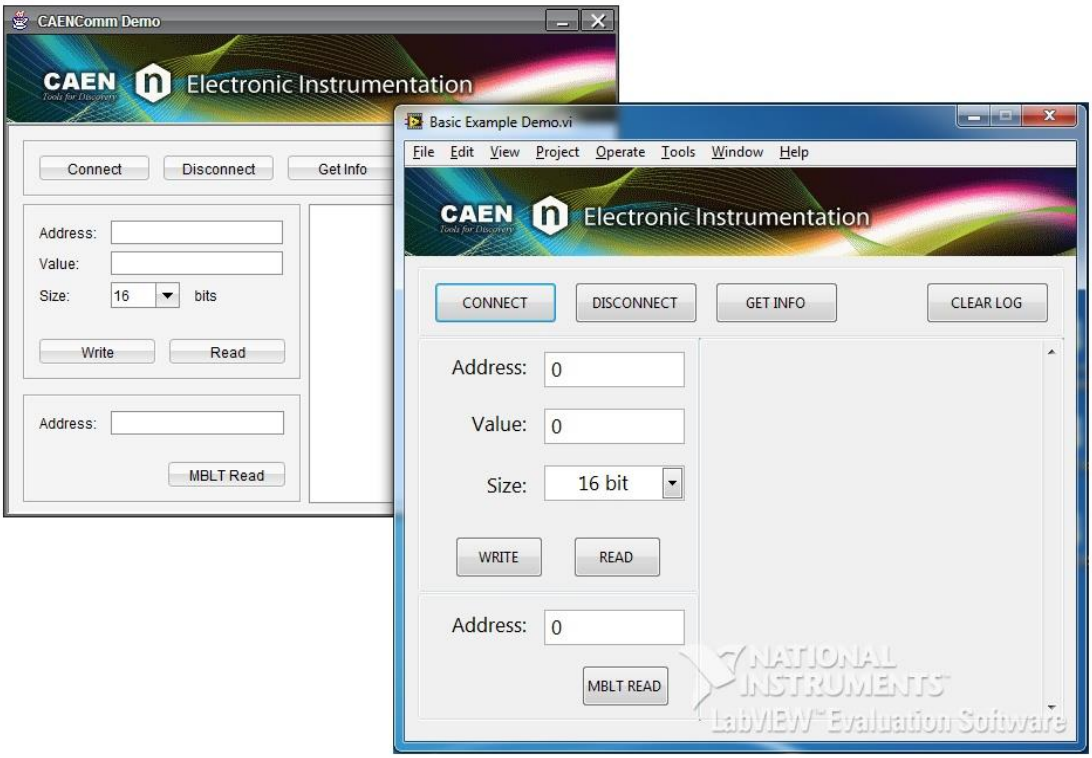


Fig. 12.2: CAENComm Demo Java and LabVIEW graphical interface

CAENComm Demo is based on the CAENComm library (see Sec. **11.2**) and it is included in the installation package of the library. Th software is available only for Windows® platform.

The software installation package and the documentation **[RD4]** can be downloaded from the CAEN website (**login required**).

12.3 CAEN WaveDump

THIS SOFTWARE DOES NOT WORK WITH DPP FIRMWARE

THE 725S/730S DIGITIZER VERSIONS ARE SUPPORTED FROM SOFTWARE REL. 3.10.0 ON

WaveDump is a basic console application, with no graphics, supporting only CAEN digitizers running the waveform recording firmware. It allows the user to program a single board (according to a text configuration file containing a list of parameters and instructions), to start/stop the acquisition, read the data, display the readout and trigger rate, apply some post-processing (e.g. FFT and amplitude histogram), save data to a file and also plot the waveforms using Gnuplot (third-party graphing utility: www.gnuplot.info).

WaveDump is a very helpful example of C code demonstrating the use of libraries and methods for an efficient readout and data analysis. Thanks to the included source files and the VS project, starting with this demo is strongly recommended to all those users willing to write the software on their own.

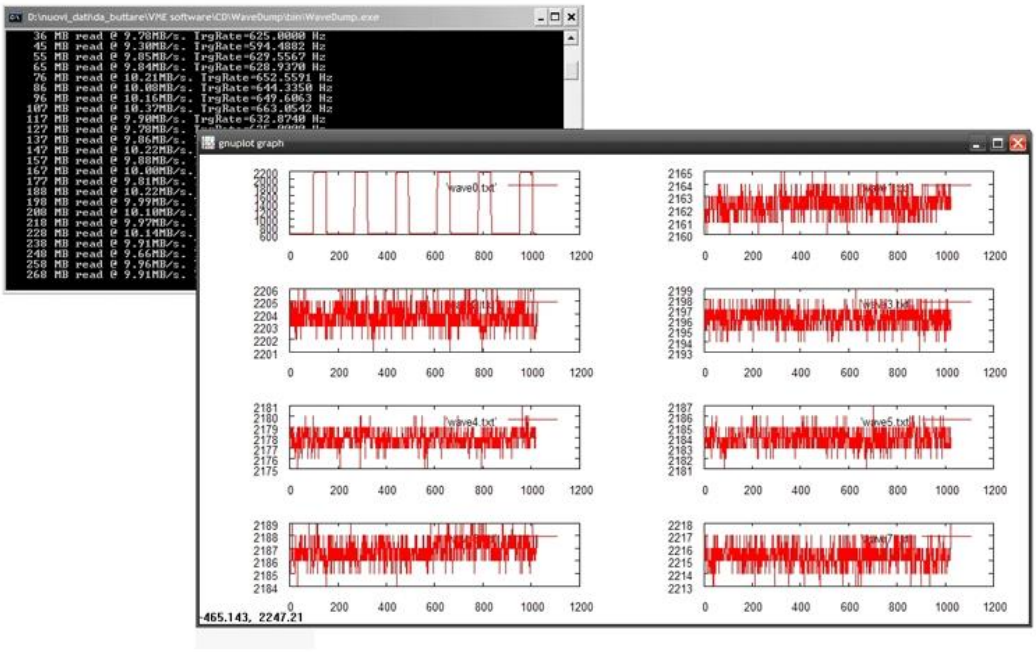


Fig. 12.3: CAEN WaveDump

CAEN WaveDump relies on the CAENDigitizer library (see Sec. **11.2**) and it can run on Windows® and Linux® platforms. Windows® versions of WaveDump are stand-alone (all required libraries are present within the software package), while the Linux® versions need the required libraries to be previously installed by the user. Moreover Linux® users are required to install the third-party Gnuplot.

The installation packages, the software User Manual **[RD7]** and a guide for getting started with it can be downloaded from CAEN website (**login required**).

12.4 CAEN WaveDump 2

WaveDump2 has been developed to support the Digitizer 2.0 new generation of CAEN digitizers, including the 2740, 2745, 2730, and future series, running the waveform recording firmware (D-Wave).

Starting from **revision 2.0.0**, support has been extended to pre-existing CAEN Digitizer 1.0 series: DT57xx, N67xx, V17xx, VX17xx.

WaveDump2 is a C++ software developed upon Qt cross-platform application development framework. Through an advanced and user-friendly configuration GUI, it provides all the necessary tools and functionalities for managing any hardware parameters. The settings can be conveniently stored into or loaded from a configuration file, or a sequence of operations can be recorded to script files and then loaded to be re-executed. From a single board to multiple boards and multi-board synchronized systems, data acquisition is managed through a dedicated toolbar and upon different start/stop criteria. Live monitoring of the acquisition statistics can be enabled.

Waveforms are lived plotted in a dedicated section emulating an 8-channel digital oscilloscope, which also provides cursors to make on-screen measurements, as well as marker lines to indicate the trigger position and the trigger threshold level. Traces can be individually enabled/disabled, and a zooming control in both vertical and horizontal directions is possible. Basic processing like FFT and samples histogram is provided runtime. The collected waveform data can be saved to ASCII or binary files for offline analysis.

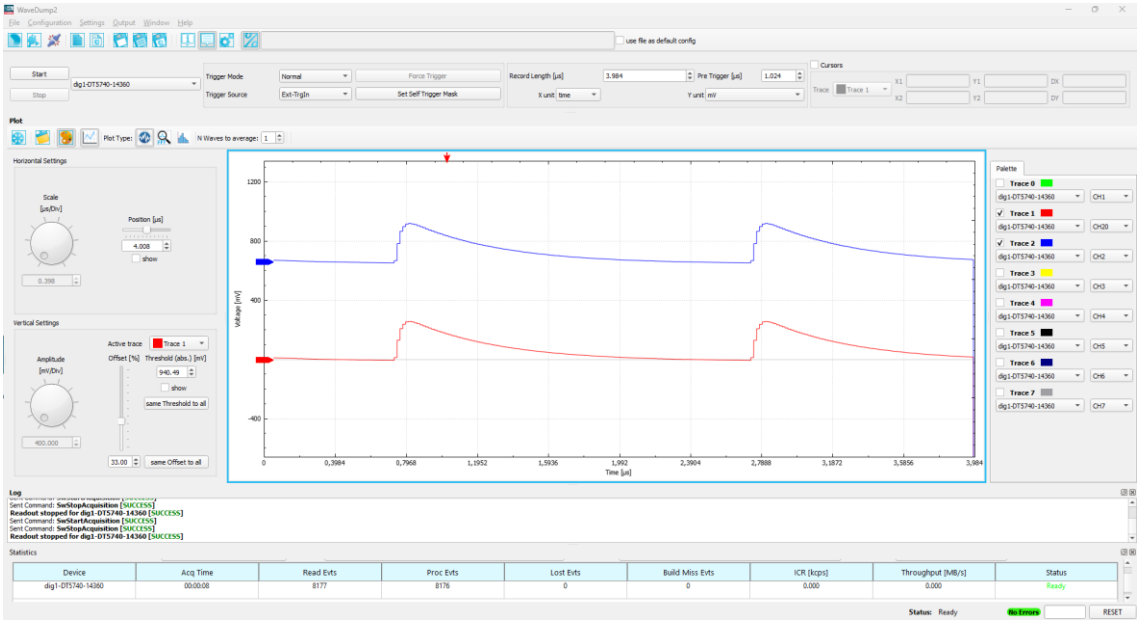


Fig. 12.4: CAEN WaveDump2

Related to Digitizer 1.0, WaveDump2 is based on the CAEN FELib and Dig1 libraries (see Sec. **11.2**). The software can run on 64-bit Windows® and Linux® operating systems. Regardless of the platform, the CAEN FELib is automatically installed along with the software, while the Dig1 library must be manually installed by the user.

The installation packages, the required libraries and the software User Manual **[RD8]** can be downloaded on CAEN website (**login required**).

12.5 CoMPASS

THIS SOFTWARE DOES NOT WORK WITH WAVEFORM RECORDING FIRMWARE

CoMPASS (CAEN Muti-PArameter Spectroscopy Software) is the new software from CAEN able to implement a Multi-parametric DAQ for Physics Applications, where the detectors can be connected directly to the digitizer inputs and the software acquires energy, timing, and PSD spectra.

CoMPASS software has been designed as a user-friendly interface to manage the acquisition with all the CAEN DPP algorithms. CoMPASS can manage multiple boards, even in synchronized mode, and the event correlation between different channels (hardware and/or software), apply energy and PSD cuts, calculate and show the statistics (trigger rates, data throughput, etc...), save the output data files (raw data, lists, waveforms, spectra) and use the saved files to run off-line with different processing parameters.

CoMPASS Software supports CAEN first generation digitizers x720, x724, x725, x730, x740D, x751 digitizer families running the DPP-PSD, rd12-PHA and DPP-QDC firmware, the x780, x781 and x782 MCA family, the DT5790 Pulse Processor and the second generation digitizer x2740, x2745 and x2730 running the DPP-PSD and DPP-PHA firmware.

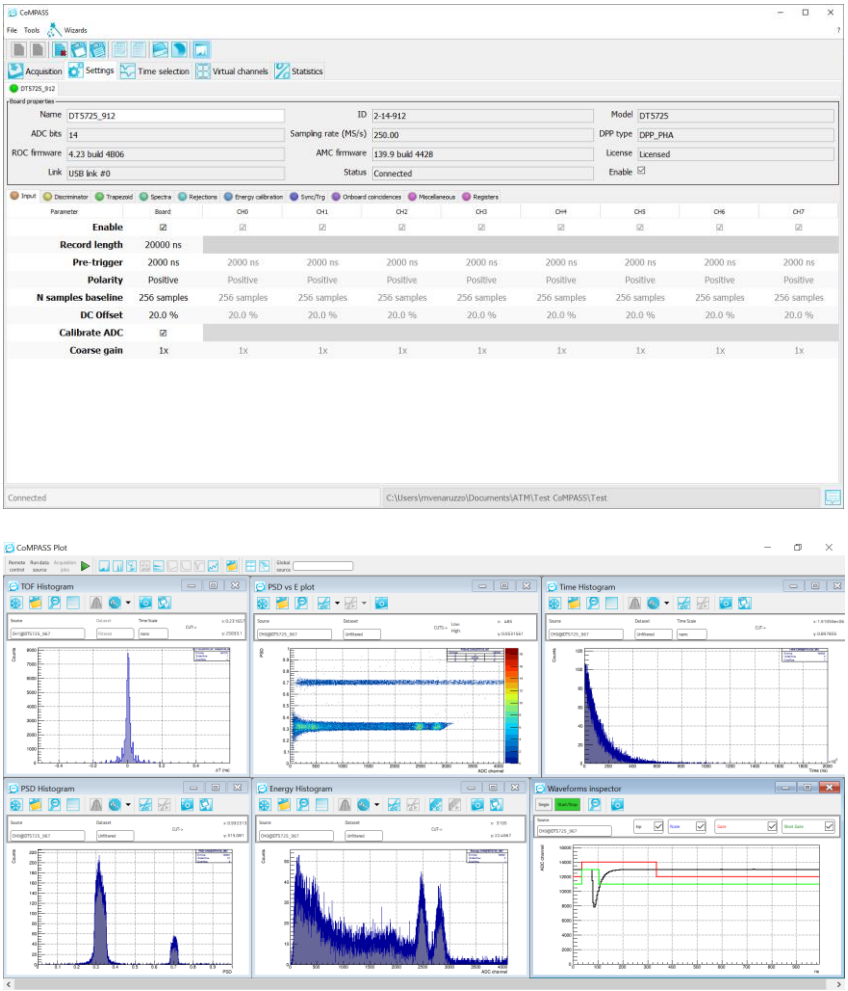


Fig. 12.5: CoMPASS software tool

CoMPASS relies on the CAENDigitizer library (see Sec. **11.2**). The software is compatible with both Windows® and Linux® platforms, operating as a standalone application on each available version. The installation packages, the required libraries and the software User Manual **[RD9]** can be downloaded from CAEN website (**login required**).

12.6 DPP-ZLEplus and DPP-DAW Control Software

THIS SOFTWARE DOES NOT WORK WITH WAVEFORM RECORDING FIRMWARE

These two C software applications are provided respectively for the DPP-ZLEplus and DPP-DAW firmware. As is, each one allows to configure the parameters of the relevant DPP algorithm and control the data acquisition, or the user can take the included C source code as an example to access the underlying library functions and develop customized readout software. The package includes the source files, the Visual Studio project, and a Makefile for Linux users.

The software run on Windows® and Linux® platforms.

The software rely on the CAENDigitizer and CAENComm libraries (see Sec. **11.2**).

Note: Windows® and Linux® versions of the software are stand-alone, the user needs to install only the driver for the communication link, while the software locally installs the DLLs of the required libraries.

Refer to the software documentation for installation instructions and a detailed description **[RD11][RD12]**.

13 HW Installation

To power on the board, preform the following steps:

1. Insert the V1725/V1730 into the crate;
2. Power up the crate

ONLY QUALIFIED PERSONNEL SHOULD PERFORM INSTALLATION OPERATIONS

DO NOT INSTALL THE EQUIPMENT IN A SETUP WHERE IT IS DIFFICULT TO ACCESS THE BACK PANEL FOR DISCONNECTING THE DEVICE

IT IS RECOMMENDED THAT THE SWITCH OR CIRCUIT-BREAKER IS NEAR THE EQUIPMENT

THE SAFETY OF ANY SYSTEM THAT INCORPORATES THE DEVICE IS UNDER THE REPONSIBILITY OF THE ASSEMBLER OF THE SYSTEM

13.1 Power-on Status

At power-on, the module is in the following status:

- the Output Buffer is cleared;
- registers are set to their default configuration.

After the power-on, only the NIM and PLL LOCK LEDs must stay on (see Fig. **13.1**).

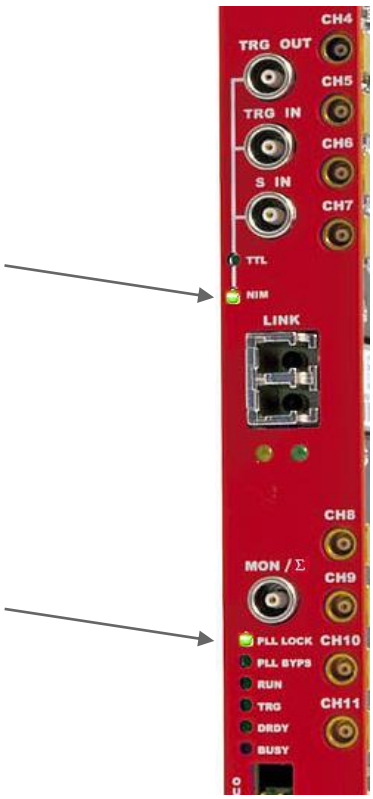


Fig. 13.1: Front panel LEDs status at power -on

EXCEPT FOR THE 725S/730S VERSIONS, AFTER POWER-ON, CAEN RECOMMENDS PERFORMING THE CHANNEL CALIBRATION AS DESCRIBED AT PAGE 33 IN ORDER TO ACHIEVE THE BEST DEVICE PERFORMANCE

14 Firmware and Upgrades

The board hosts one FPGA on the mainboard and two FPGAs per mezzanine (i.e. one FPGA per 4 channels). The channel FPGAs firmware is identical. A unique file is provided that will update all the FPGAs at the same time.

ROC FPGA MAINBOARD FPGA (Readout Controller + VME interface):

FPGA Altera Cyclone EP1C20.

AMC FPGA MEZZANINE FPGA (ADC readout/Memory Controller):

FPGA Altera Cyclone EP4CE30

or

FPGA INTEL/ALTERA ARRIA V GX

(725S and 730S versions only)

The firmware is stored onto the on-board FLASH memory. Two copies of the firmware are stored in two different pages of the FLASH, referred to as Standard (STD) and Backup (BKP). In case of waveform recording firmware, the board is factory equipped with the same firmware version on both pages.
At power-on, a microcontroller reads the FLASH memory and programs the module automatically loading the first working firmware copy, that is the STD one in normal operating.

The on-board dedicated SW7 dip switch (see Sec. **9.2**) allows to select the first FLASH page to be read at power-on (STD by default).

It is possible to upgrade the board firmware via VMEbus or Optical Link by writing the FLASH with the CAEN Toolbox software (see Chap. **12**).

IT IS STRONGLY SUGGESTED TO OPERATE THE DIGITIZER UPON THE STD COPY OF THE FIRMWARE. UPGRADES ARE SO RECOMMENDED ONLY ON THE STD PAGE OF THE FLASH. THE BKP COPY IS TO BE INTENDED ONLY FOR RECOVERY USAGE. IF BOTH PAGES RESULT CORRUPTED, THE USER WILL NO LONGER BE ABLE TO UPLOAD THE FIRMWARE VIA VMEbus OR OPTICAL LINK AGAIN AND THE BOARD NEEDS TO BE SENT TO CAEN IN REPAIR!

14.1 Firmware Upgrade

Firmware updates are available for download on CAEN website (www.caen.it) at the digitizer page (login required).

Different firmware updates are available for the 725/730 digitizer families:

- The waveform recording firmware;
- The DPP firmware implementing different algorithms for Physics Applications:
  - DPP-PSD firmware for the Pulse Shape Discrimination
  - DPP-PHA firmware for the Pulse Height Analysis
  - DPP-ZLEplus firmware with Zero Length Encoding
  - DPP-DAW firmware with Dynamic Acquisition Window

The waveform recording is free firmware and updates are free downloadable.

The DPP firmware are paid firmware: the trial version can be free downloaded and is fully functional for a 30-minute per power cycle operation. The user must then purchase a license and store the provided unlock code onto the digitizer to run the firmware and its updates without time limitation. The licence is managed by CAEN Toolbox tool **[RD1]**.

14.1.1 DPP Firmware File Description

The programming file is a CFA file (CAEN Firmware Archive). It is an archiving file format that aggregates all the programming files of the same firmware kind which are compatible with the same digitizer family.

The name of the CFA file follows a general convention:

- *<DIGITIZER>*_rev_X.Y_W.Z.CFA for the waveform recording firmware
- *<DIGITIZER>_<DPP_ALGORITHM>*_rev_X.Y_W.Z.CFA for the DPP firmware

where:

<DIGITIZER> are all the boards that can be updated by the CFA file;

options are:

- x730 (includes x730, x730B, x730C, x730D module versions);
- x730S (includes x730S, x730SB, x730SC, x730SD module versions);
- x725 (includes x725, x725B, x725C, x725D module versions);
- x725S (includes x725S, x725SB, x725SC, x725SD module versions);

where x = DT5 for desktop, x = N6 for NIM, x = V1/VX1 for VME64/VME64x format);

<DPP_ALGORITHM> is the kind of DPP firmware (options are DPP-PSD, DPP-PHA, DPP-ZLEplus, DPP-DAW);

X.Y is the major/minor revision number of the ROC FPGA;

W.Z is the major/minor revision number of the AMC FPGA.

To discriminate between the waveform recording firmware and the DPP ones by the firmware version, the reference is the major revision number of the AMC FPGA (W):

W < 128 means a waveform recording firmware

W ≥ 128 means a DPP firmware, and it is a fixed number specific for each algorithm and digitizer family.

For the 730 and 725 digitizer families:

W = 136 means DPP-PSD firmware

W = 139 means DPP-PHA firmware

W = 140 means DPP-ZLEplus firmware

14.1.2 Troubleshooting

In case of upgrade failure (e.g. STD FLASH page is corrupted), the user can try to reboot the board: after a power cycle, the system programs the board automatically from the alternative FLASH page (e.g. BKP FLASH page), if this is not corrupted as well (see Sec. **13.1**). The user can so perform a further upgrade attempt on the STD page to restore the firmware copy.

BECAUSE OF AN UPGRADE FAILURE, THE SW7 DIP SWITCH POSITION MAY NOT CORRESPOND TO THE FLASH PAGE FIRMWARE COPY LOADED ON THE BOARD FPGAs

Note: old versions of the digitizer motherboard have a slightly different FLASH management and the firmware selection switch is SW7. To obtain information about the FLASH type of the digitizer, the user can download the BoardInfoFile (text file) through the “Get information file” tab in CAEN Toolbox software (see. Chap. **12**) and check the value of the FLASH_TYPE parameter: FLASH_TYPE=0 indicates an older version. Alternatively, the user can use CAENComm software or the “Manual Controller” available in CAEN Toolbox to directly access register 0xF050 and check the status of bit[7]. If so, it means that, at power on, the microcontroller loads exactly the firmware copy from the FLASH page.

When a failure occurs during the upgrade of the STD page of the FLASH, which compromises the communication with the V1730/725, the user can perform the following recovering procedure as first attempt:

- force the board to reboot loading the copy of the firmware stored on the BKP page of the FLASH. For this purpose, power off the crate, switch the dedicated SW7 switch to BKP position and power on the crate;
- use CAEN Toolbox to read the firmware revision (in this case the one of the BKP copy). If this succeeds, it is so possible to communicate again with the board;
- use CAEN Toolbox to load the proper firmware file on the STD page, then power off the crate, switch SW7 back to STD position and power on the crate.

If neither of the procedures here described succeeds, it is recommended to send the board back to CAEN in repair (see Chap. **18**).

15 Instructions for Cleaning

The equipment may be cleaned with isopropyl alcohol or deionized water and air dried. Clean the exterior of the product only.
Do not apply cleaner directly to the items or allow liquids to enter or spill on the product.

15.1 Cleaning the Touchscreen

To clean the touchscreen (if present), wipe the screen with a towelette designed for cleaning monitors or with a clean cloth moistened with water.
Do not use sprays or aerosols directly on the screen; the liquid may seep into the housing and damage a component. Never use solvents or flammable liquids on the screen.

15.2 Cleaning the air vents

It is recommended to occasionally clean the air vents (if present) on all vented sides of the board. Lint, dust, and other foreign matter can block the vents and limit the airflow. Be sure to unplug the board before cleaning the air vents and follow the general cleaning safety precautions.

15.3 General cleaning safety precautions

CAEN recommends cleaning the device using the following precautions:

- Never use solvents or flammable solutions to clean the board.
- Never immerse any parts in water or cleaning solutions; apply any liquids to a clean cloth and then use the cloth on the component.
- Always unplug the board when cleaning with liquids or damp cloths.
- Always unplug the board before cleaning the air vents.
- Wear safety glasses equipped with side shields when cleaning the board.

16 Device Decommissioning

After its intended service, it is recommended to perform the following actions:

- Detach all the signal/input/output cable
- Wrap the device in its protective packaging
- Insert the device in its packaging (if present)

THE DEVICE SHALL BE STORED ONLY AT THE ENVIRONMENT CONDITIONS SPECIFIED IN THE MANUAL, OTHERWISE PERFORMANCES AND SAFETY WILL NOT BE GUARANTEED

17 Disposal

The disposal of the equipment must be managed in accordance with Directive 2012/19 / EU on waste electrical and electronic equipment (WEEE).

The crossed bin symbol indicates that the device shall not be disposed with regular residual waste.

18 Technical Support

To contact CAEN specialists for requests on the software, hardware, and board return and repair, it is necessary a MyCAEN+ account on www.caen.it:

https://www.caen.it/support-services/getting-started-with-mycaen-portal/

All the instructions for use the Support platform are in the document:

A paper copy of the document is delivered with CAEN boards.

The document is downloadable for free in PDF digital format at:

https://www.caen.it/safety-information-product-support

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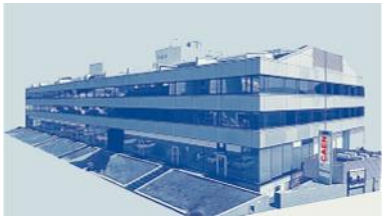

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