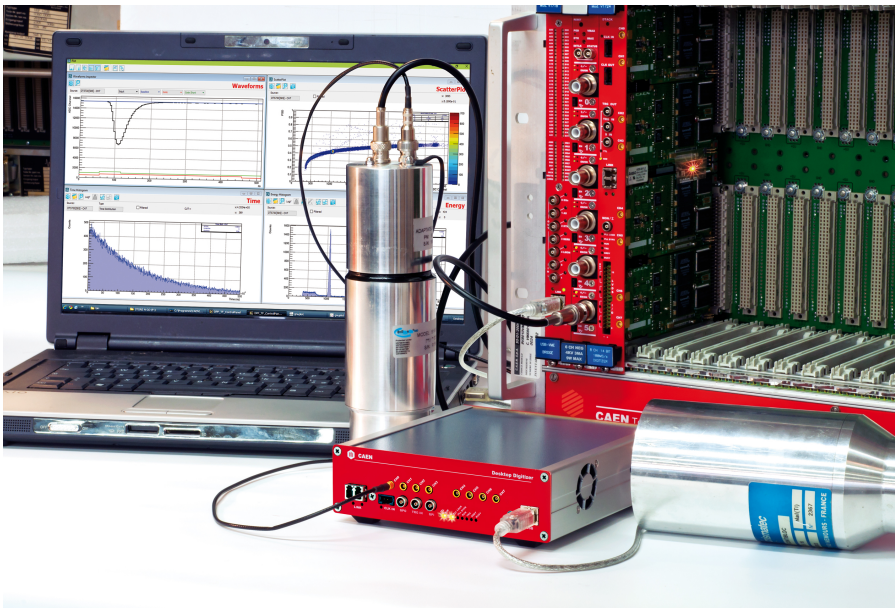
CAEN
Tools for Discovery

Electronic Instrumentation



User Manual WP2081

Digital Pulse Processing in Nuclear Physics

Overview of CAEN DPP algorithms

Rev. 4 - June 12th, 2017

Purpose of this Manual

This White Paper describes many of the potential advantages and benefits afforded by the utilization of Digital Pulse Processing algorithms for Nuclear Physics applications.

Change Document Record

Date	Revision	Changes
August 26th, 2011	03	Revised all chapters, new document format
June 12th, 2017	04	Revised all chapters. Revised supported boards. Removed support to DPP-CI (discontinued). Added sections for DPP-QDC, DPP-ZLEplus and DPP-DAW firmware. Revised Software Interface Chapter.

Symbols, Abbreviated Terms and Notation

DPP	Digital Pulse Processing
PHA	Pulse Height Analysis
PSD	Pulse Shape Discrimination
MCA	Multi-Channel Analyzer
FPGA	Field Programmable Gate Array
CFD	Constant Fraction Discriminator
ADC	Analog to Digital Converter
QDC	Charge to Digital Converter
TDC	Time to Digital Converter
ZLE	Zero Length Encoding
DAW	Dynamic Acquisition Window

Reference Documents

[RD1] W. R. Leo. *Techniques for Nuclear and Particle Physics Experiments*. Ed. by Springer. II ed.

[RD2] V.T. Jordanov and G.F. Knoll. "Digital Synthesis of pulse shapes in real time for high resolution radiation spectroscopy". In: *NIM A* 345 (1994), p. 337.

[RD3] UM3182 – MC2Analyzer User Manual.

[RD4] AN2503 – Charge Integration: Analog Vs. Digital.

[RD5] UM2088 – DPP-PSD User Manual.

[RD6] UM4874 – DPP-QDC User Manual.

[RD7] G. F. Knoll. *Radiation detection and measurement*. Ed. by J. Wiley and sons. III ed.

[RD8] AN2506 – Digital Gamma Neutron discrimination with Liquid Scintillators.

[RD9] AN3251 – Timing Measurements with CAEN Waveform Digitizers.

[RD10] AN5111 – BaF2 and LaBr3 Time Measurements with a 500 MS/s Digitizers.

[RD11] UM2764 – DPP-ZLEplus User Manual.

[RD12] UM5954 – DPP-DAW User Manual.

All CAEN documents can be downloaded at: *http://www.caen.it/csite/LibrarySearch.jsp*

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MADE IN ITALY: We stress the fact that all the boards are made in Italy because in this globalized world, where getting the lowest possible price for products sometimes translates into poor pay and working conditions for the people who make them, at least you know that who made your board was reasonably paid and worked in a safe environment. (this obviously applies only to the boards marked ”MADE IN ITALY”, we cannot attest to the manufacturing process of ”third party” boards).

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1 Measurements in Nuclear Physics

Introduction

The function of Front-End electronics in nuclear physics applications is to acquire the electrical charge pulses generated by a detector, to extract quantities of interest from these pulses, and to convert the pulses into a digital format. The information is subsequently acquired, saved, and analyzed by a computer. In most applications, relevant quantities include the particle charge (proportional to the charge released by the particle in the detector) and time of arrival. In some cases the acquisition is restricted to pulse counting, or more specifically ”selective” counting; meaning that one or more energy interval, or other criteria, are used to select which particles are selected to be counted. In other cases it is necessary to discriminate the type of particle by means of the shape of the pulse. For example, γ-n discrimination is based on a detector response variation when stimulated by either a photon or a neutron. This variation leads to a different rise and/or decay time of the pulse.

An acquisition system is typically comprised of digital logic units. The purpose of this system is to perform coincidence/anti-coincidence, generate triggers, vetoes, gates, and other signals which take into account correlations between different channels and may provide further information such as particle position or trajectory.

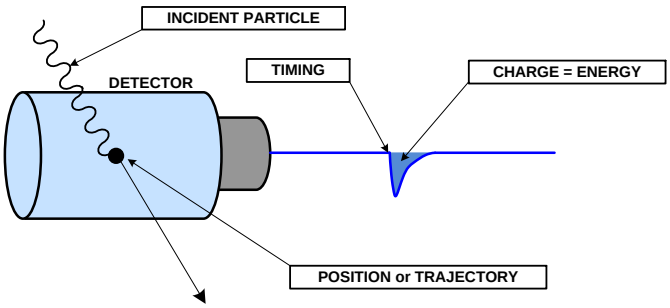

Fig. 1.1: Electrical charge pulse generated by a particle interacting with a detector.

Traditional Analog Chains

Traditionally, electronic readout systems for particle detection were composed almost completely of an analog chain similar to those represented in **Fig. 1.2** and **Fig. 1.4**. Each block of the chain has a specific function, which forces the user to manage several individual blocks for the system to successfully extract all relevant quantities. In the traditional electronics approach the Analog to Digital conversion is performed at the end of the acquisition chain, just before readout to the host computer.

In most cases the first stage of the chain includes a preamplifier, typically located close to the detector. A preamplifier is a very low noise analog circuit that receives the signal (generally weak) generated by the detector and produces an output signal with a S/N ratio suitable for transmission via cable to the readout electronics. Readout electronics are normally housed in a crate or rack, and can be located as far as tens or even hundreds of meters from the detector. There are many types of preamplifiers, but for the purposes

of this document we've divided them into two basic families: **charge sensitive preamplifier** and **current sensitive preamplifier** (or **fast amplifier** or **wideband amplifier**).

A **charge sensitive preamplifier (CSP)** integrates the signal coming from the detector, thus converting the charge into voltage amplitude. Ideally, a CSP is composed of a simple capacitor. However, in order to avoid saturation the integrating capacitor is put in parallel with a discharging resistor, resulting in an output pulse from the preamplifier composed of a fast rise time and an exponential decay (see **Fig. 1.3**). The charge information (energy) is now represented by the pulse height.

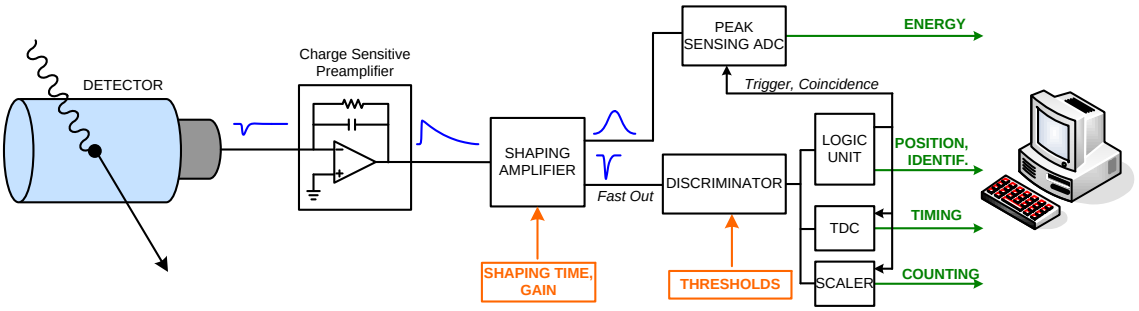

Fig. 1.2: Block diagram of a traditional acquisition system for spectroscopy.

In an effort to preserve the timing information the fast component of the signal (rising edge) is typically treated by a **fast amplifier** (or **timing amplifier**), which derives the signal. The output of the timing amplifier typically feeds an electronics chain composed of a discriminator, a Time to Digital Converter (TDC) for timing acquisition, and sometimes a Scaler for counting acquisition. Additional electronics components may be included to facilitate the implementation of logic operations, perform coincidence (providing trajectory and positional information of the particles), generate triggers, and provide specific information about the target pulse shape (e.g. time over threshold, zero crossing, etc...) which may be utilized for particle identification. Typically the fast amplifier is integrated in the shaping amplifier module and the relevant signal is provided as a separate fast output (sometimes referred to as timing output).

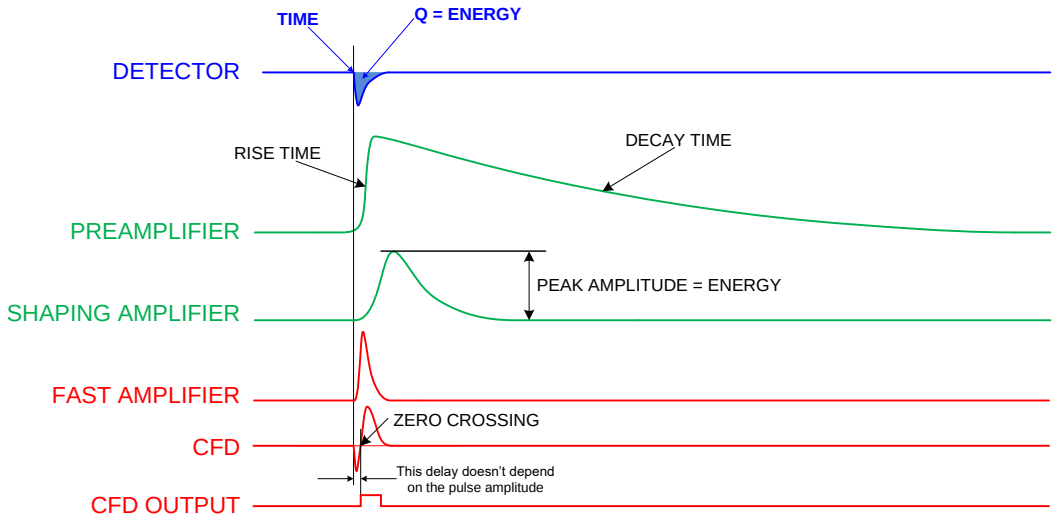

Fig. 1.3: Signals in the traditional analog chain.

Unlike a charge sensitive preamplifier, a **current sensitive preamplifier** is a linear fast amplifier which does not change the shape of the signal. The output from a current sensitive preamplifier is typically a very short pulse (range of tens of nanoseconds to sub-nanosecond) which is particularly useful for applications in which very precise timing information is required. An important advantage of a current sensitive preamplifier is that it reduces the potential for pile-up. For some applications a preamplifier is not required, such as in the case of many PMTs which provide a signal of sufficient amplitude to be fed directly into the readout electronics. In situations in which the shape of the detector signal is unchanged the energy information

is represented by the area below the pulses. This value is typically measured by a Charge Integrating ADC (e.g. QDC), as shown in **Fig. 1.4**. A QDC is a pure integrator which requires a gate signal to define the integrating window. In some applications (generally in beam experiments) this gate signal is provided by a system which knows in advance when the signals are to be integrated. Unfortunately, when this timing component is unknown it is necessary to generate the gate from the detector signal. To do this requires that the signal be split, with one branch being sent to a discriminator to be used in coincidence logic. It is also necessary to add a delay line (typically a length of cable) along the signal path to the QDC input in order to match the pulses with the gate, which arrives with some latency with respect to the analog pulses that produced it.

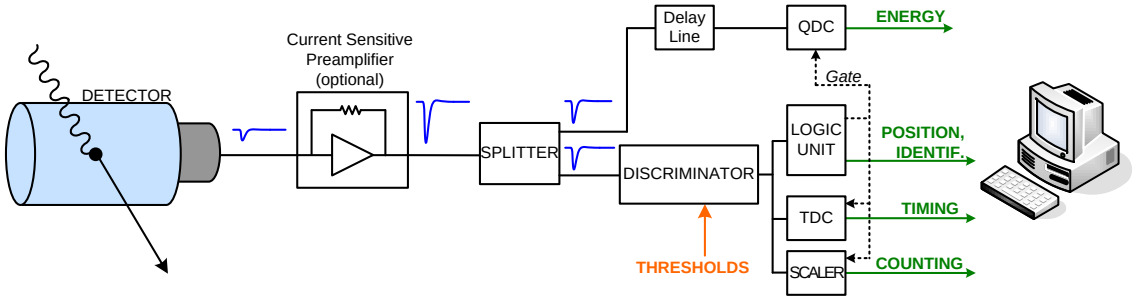

Fig. 1.4: Block diagram of an acquisition system based on the QDC.

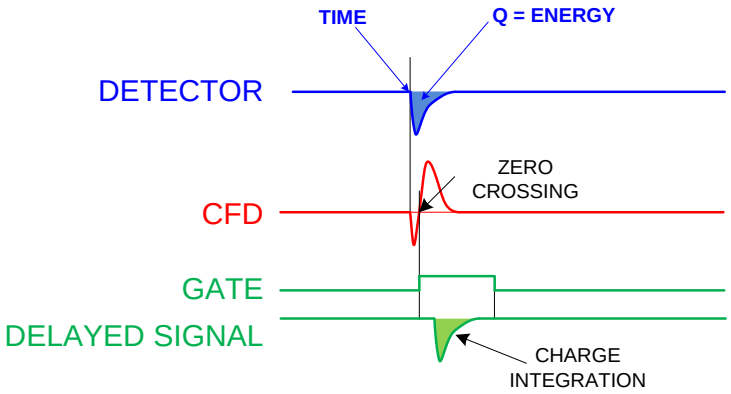

Fig. 1.5: Signals in the QDC based chain.

Digital Pulse Processing: all-in-one, multi-parametric digital DAQ for physics applications

In recent years the availability of very fast, high precision flash ADCs have opened the door to design acquisition systems in which the Analog to Digital conversion occurs very close to the detector. In principle, these acquisition systems afford minimal information loss. However, the acquisition can be negatively impacted by uncertainties due to quantization noise and other sources of electronic noise. In general, applications which require precise timing measurements are a better fit for high sample frequency digitizers (500MS/s or more), while the 12 to 14bit digitizers are well suited for acquisitions in which high energy resolution is critical.

The principle operation of a Waveform Digitizer (also known as a Transient Recorder or Flash ADC) is similar to that of a digital oscilloscope; when the trigger occurs a certain number of samples (i.e. the acquisition window) are recorded into a memory buffer.

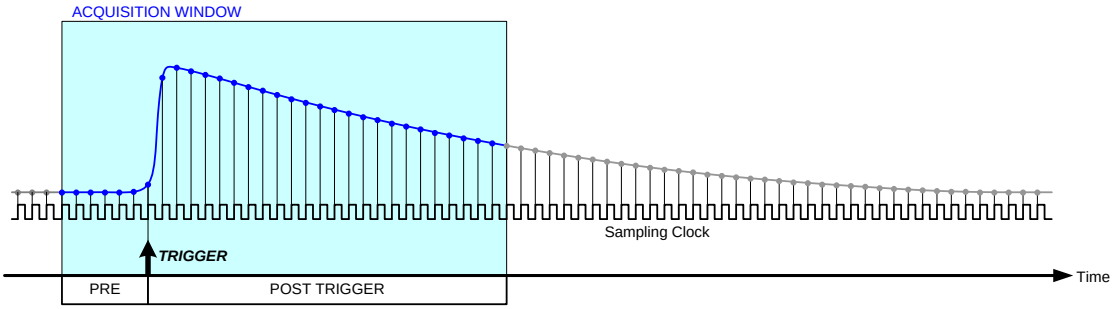

Fig. 1.6: Signal digitization and acquisition window defined by the trigger.

However, digitizers can be designed in such a way as to offer significant advantages over a traditional electronic chain solution:

- The utilization of a Multi Event Memory makes it possible to independently and simultaneously read and write events in the memory buffer.
- They can manage Multi-board synchronization and system scalability. Scaling up from a very small number of channels to thousands of channels is possible by means of clock, trigger and sync distribution features.
- Typically, very high bandwidth data readout links are utilized (VME, optical links, Ethernet)
- They feature FPGAs for on-line data processing and data reduction.

In recent years the utilization of **waveform digitizers** for readout of radiation detectors has become popular for many different physics applications. The conventional analog electronics chain is steadily being replaced by a full digital approach where the detector output (with or without preamp, depending on the detector type) is directly connected to the digitizer input. This approach is especially beneficial in **multi-parametric** acquisition systems wherein the analysis includes multiple quantities and parameters such as energy, pulse shape, and timing. In fact, with the advances in **Digital Pulse Processing** (DPP) it is now possible to apply dedicated algorithms on-line (typically within an FPGA), allowing the user to to extract information of interest from the raw waveform. DPP algorithms can modify the digitizer into a ”single box” solution, capable of performing all traditional functionalities of the outdated TDC, QDC, Peak Sensing ADC, Discriminator, electronics chain and associated analog and logic modules**[RD1]**. Furthermore, DPP permits the digital readout to be sustainable in terms of data throughput by allowing the user to select and read out specific data quantities and parameters. This results in an **“all-in-one, multi-parametric digital DAQ for physics applications”**.

CAEN has developed a complete family of waveform digitizers, each of which is ideally suited for distinct physics, medical, homeland security, and industrial applications. These digitizers are available in different form factors (VME, Desktop, NIM), as depicted in **Tab. 1.1**. CAEN has also developed several Digital Pulse

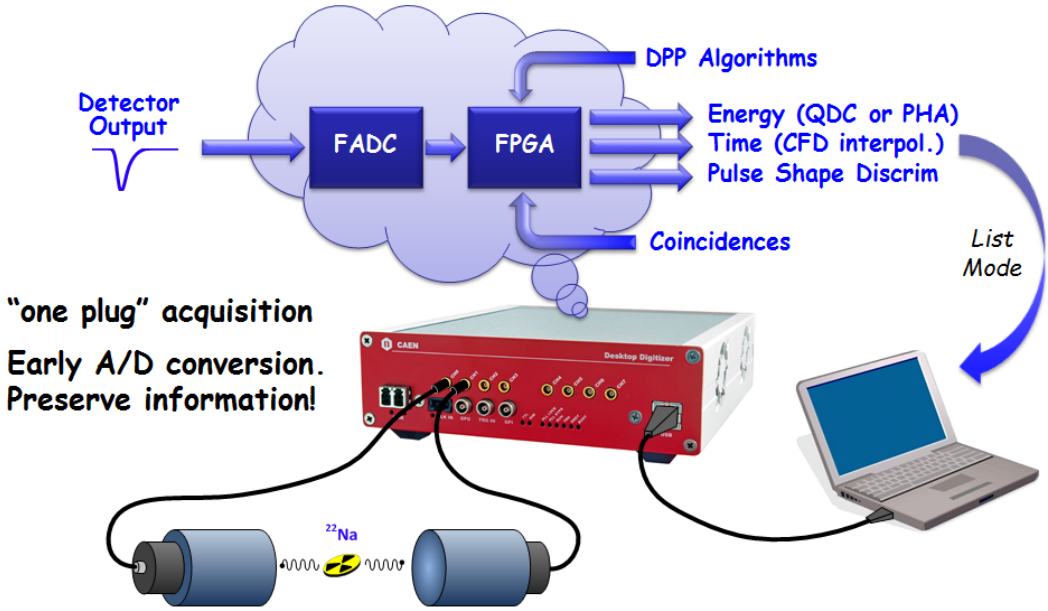

Fig. 1.7: All-in-one Spectroscopy DAQ.

Processing algorithms which permit the user to extract from the detector pulse specific information such as energy, precise timing, PSD, and so on **[RD1]**. **Tab. 1.2** depicts the available functionalities of CAEN DPP Firmware relative to the each digitizer versions. These functionalities will be further described in the following sections.

MODEL(1)	Form Factor	# channels	Sampling Frequency (MS/s)	# Bits	Input Dynamic Range (Vpp)	Bandwidth (MHz)	Memory (Msample/ch) *Record Lenght*	
							small	big
x724	VME	8	100	14	0.5 - 2.25 - 10	40	0.5 *500µs*	4 *4ms*
	Desktop/NIM	4						
x720	VME	8	250	12	2	125	1.25 *5ms*	10 *40ms*
	Desktop/NIM	4						
x730	VME	16	500	14	0.5 and 2	250	1.25 *250µs*	10 *2ms*
	Desktop/NIM	8						
x725	VME	16	250	14	0.5 and 2	125	1.25 *500µs*	10 *4ms*
	Desktop/NIM	8						
x731	VME	8/4	500/1000	8	2	250/500	2/4 *2ms*	
	Desktop/NIM	4/2						
x751	VME	8	1000/2000	10	1	500	1.8/3.6 *1.8ms*	14.4/28.8 *14.4ms*
	Desktop/NIM	4						
x761	VME	2	4000	10	1	1000	7.2 *1.8ms*	57.6 *14.4ms*
	Desktop/NIM	1						
x740	VME	64	62.5	12	2 - 10	30	0.19 *3ms*	1.5 *24ms*
	Desktop/NIM	32						
x742	VME	32+2	5000(2)	12	1	600	0.128 *200ns*	
	Desktop/NIM	16+1						
x743	VME	16	3200(2)	12	2.5	500	0.003 *640ns*	
	Desktop/NIM	8						

(1) The *x* in the model name is ***V1*** for VME, ***VX1*** for VME64X, ***DT5*** for Desktop and ***N6*** for NIM
(2) Sampling frequency of the analog memory (switched capacitor array); A/D conversion takes place at lower speed (dead-time)

Tab. 1.1: CAEN Waveform Digitizers selection table.

One of the most critical components of a fully digital approach is readout bandwidth, especially in regards to applications in which it is necessary to dump the entire waveform from the input channel. In such cases, the

Model	Waveform Recording	Zero Suppression	PHA	PSD	CFD	QDC
x730	√	√	√	√	√	√
x725	√	√	√	√	√	√
x751	√	√		√	√	√
x724	√	√	√			
x720	√	√		√		√
x740	√					√
x761	√					
x742	√					
x743	√					√

Tab. 1.2: Functionalities implemented in the CAEN digital algorithms and supported by the digitizers. The Zero Suppression functionality for the x725 and x730 families is COMING SOON.

amount of data to be read out is often extremely high. Therefore, it may be beneficial or even mandatory to implement on-line digital pulse processing which performs various levels of Zero Suppression and/or Data Reduction. Such data processing must have the ability to transform the raw sequences of samples into a compressed data packet, while simultaneously preserving information relevant to the physics and minimizing the data size. **Fig. 1.8** shows the data flow for a digital readout system.

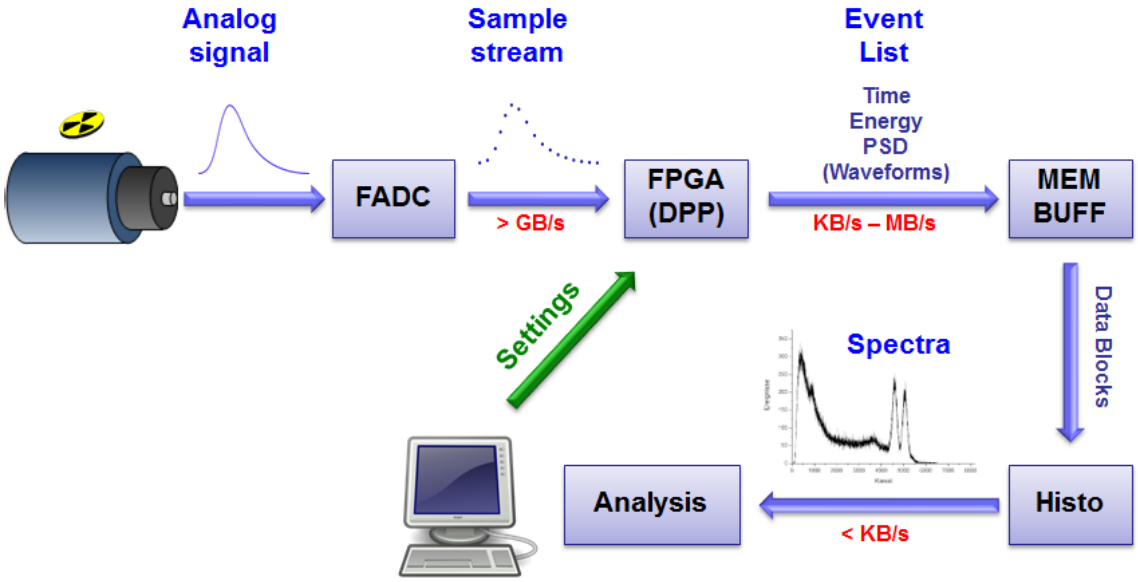

Fig. 1.8: Data flow of a digital readout system.

CAEN digitizers are equipped with several interface options, which are utilized for both module control and for streaming data from the digitizer to the acquisition computer:

1. **CONET**: Optical Readout and Control Link that transfers data from/to the front panel of the digitizers

directly into the computer via a PCI Express card at a maximum possible rate of 80 MB/s per link. The physical user interface is standard, performant, and widely utilized 8 lane PCI Express. One link can manage up to 8 digitizers via front panel daisy chain.

2. **USB 2.0**: A straightforward, plug & play, easy to use standard USB interface. The digitizer can be directly connected to the computer USB port without the need for any additional hardware. The maximum data throughput rate is about 30 MB/s.
3. **VME backplane**: Legacy access via the VME backplane is retained, allowing a data throughput of up to 160 MB/s utilizing the **2eSST** protocol. Please note, a Single Board Computer is required.

Tab. 1.3 shows the maximum bandwidth available for the CAEN digitizers with the different interfaces.

Interface	Bandwidth	VME board	NIM / Desktop board
VME with 2eSST	160 MB/s	✓	
VME with MBLT	60 MB/s	✓	
Optical Link	80 MB/s	✓	✓
USB 2.0	30 MB/s		✓

Tab. 1.3: Readout bandwidth of CAEN digitizer.

Fig. 1.9 depicting a CONET-based readout strategy:

1. 16 digitizers in one VME crate read out by 1 computer at about 320 MB/s.
2. One 4 link A3818 PCIe card. Each link reads 4 digitizers in daisy chain.
3. 20 MB/s per digitizer, however max transfer can be 4 times higher with dedicated links.
4. VME crate is simply utilized for power and mechanics (no backplane communication)

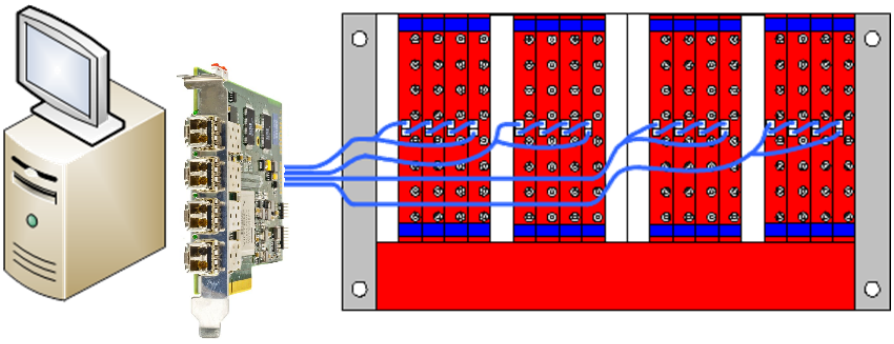

Fig. 1.9: CAEN Digitizer CONET readout example.

Comparison between analog and digital signal treatment

With respect to a traditional analog solution, a fully digital approach offers many advantages and benefits which typically far outweigh the limited drawbacks. Among the undeniable advantages are the multi-parametric capabilities of the digitizer (i.e. a single digitizer board can replace multiple components in a comparable analog chain), the potential to preserve the pulse information, a higher sustainable counting rate, multi-board synchronization and channel correlation capabilities, enormous flexibility thanks to the ability to load several DPP algorithms on the same hardware, a compact spatial solution, and last but not least cost effectiveness.

Harnessing the full capabilities of a digital system, however, is not always a simple matter for new users due to the required understanding of the algorithms and associated control parameters. Additionally, customization of these algorithms implemented in the FPGA is not always a possibility due to various factors. For instance, user customization requires an understanding of the associated programming language which, if improperly applied, may cause failure not only to the algorithms in the firmware but to the hardware itself. Such failures inevitably lead to not negligible demand for support from CAEN. Furthermore, advanced software tools are almost always required to facilitate algorithm customization and to take advantage of all possible algorithm capabilities.

Acquisition modes with Waveform Digitizers

Experiments in nuclear and particle physics can typically be divided into two main categories:

1. experiments with trigger
2. trigger-less experiments

In the case of ”experiments with trigger”, the trigger to an experimental setup is either given from an external source (e.g. beam) or from a predefined combination of signals coming from the detectors which are selected and combined in order to provide a global trigger. This global trigger then allows the data acquisition system to record or reject data matching the predetermined configurations. On the other hand, with a ”trigger-less experiment” each detector is independent from the others. All data coming from a ”trigger-less” setup is saved and the data selection is performed in post-process via offline analysis.

Typically, experiments which include a trigger are interested in retrieving the full waveform while at the same time ignoring or eliminating non-essential data; the goal being to reduce as much as possible the streaming bandwidth by discarding data which does not include useful information. In such cases, the acquisition mode used is the:

- **Waveform Inspector Mode**.

  In this modality, for each trigger the digitizer saves the sequence of samples (e.g. waveform) which fits within the acquisition window into one local memory buffer.

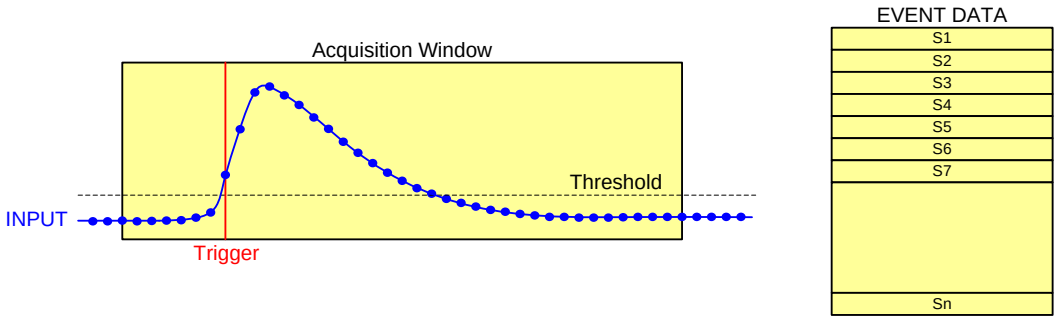

Fig. 1.10: Data acquisition using the Waveform Inspector mode.

Effective zero suppression algorithms are an excellent tool for reducing the data streaming bandwidth and eliminating non-essential data.

Alternatively, ”Trigger-less experiments” are interested in saving all data coming from the acquisition, including the data which might typically fall to the wayside utilizing a zero-suppression algorithm. The goal being to save all data process the information at a later date. As a result, the ideal solution will result in keeping all data, or at minimum reduce the amount of information lost as much as possible. The typical intent is not be to retrieve the full waveform, but to retrieve the quantities of interest (e.g. energy, time stamp, PSD, etc...) already provided by the digitizers. The acquisitions for this case will typically be:

- **List Mode**: In this case, the DPP algorithms are applied on-line by the FPGA, which is operating on a continuous data stream. Whenever a pulse goes over threshold the relevant energy (or other quantities) is calculated and recorded in the memory buffers; thus creating a list of energies (or other relevant quantities). As soon as this list reaches a certain size the data buffer becomes available to read out, while at the same time the acquisition continues in another buffer. Thanks to the greatly reduced amount of data to save and transfer, in most cases this mode is capable of sustaining continuous acquisition even in situations where the pulse rate is very high.
- **Mixed Mode**: In the mode the digitizer stores a list of pulse parameters (energy and/or time stamp information) as well as a subset of the waveform samples. Typically, the number of saved samples of the waveform is low because the purpose of mixed mode is to accurately read a small part of the signal which is critical to pulse characterization. For example, the user may be most interested in reading samples before and after the crossing of the threshold (e.g. zero crossing), intending to perform interpolation on these samples in an effort to increase timing resolution. In other cases, the user may require a fragment of the pulse, upon which an off-line pulse shape analysis will be applied.

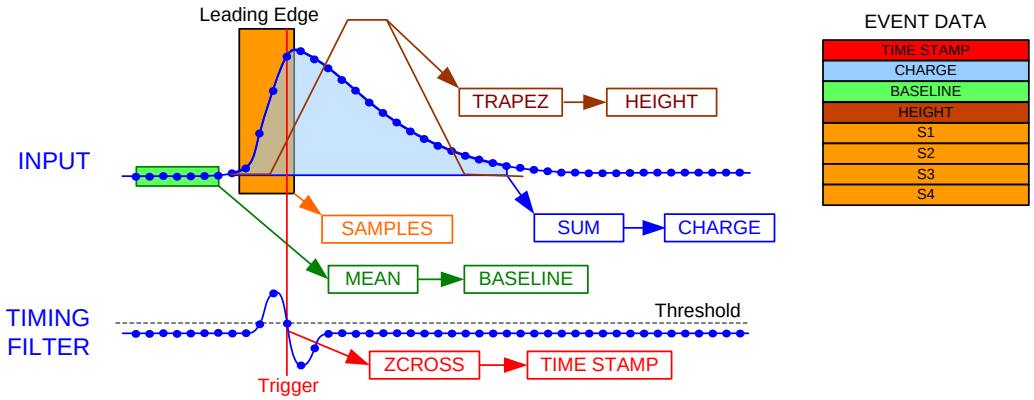

Fig. 1.11: Data acquisition using the Mixed mode.

Trigger-less experiments are generally interested in using the Waveform Inspector Mode in the earliest stages of development for testing the processing algorithms and during the first stage of data acquisition to monitor the signals (including the internal signals at the output of the digital filter stages). The Waveform Inspector Mode can also be beneficial for testing different parameters and their effects on the output filters and for tuning and debugging the acquisition system.

2 Digital Pulse Processing algorithms

Pulse Triggering and Timing Filters

As with oscilloscopes, digitizers typically feature a self-trigger based on a programmable voltage threshold. This trigger is generated when the input signal crosses the threshold. Unfortunately, this technique is not suitable for most physics applications due to baseline fluctuation, pulse pile-up, noise, etc... However, the ability to identify and discriminate pulses of interest out of the noise is critical. In fact, missing pulses or false triggers can result in the loss of important event data, bad pile-up rejection, statistical errors, and other undesirable effects. The digital filters implemented in CAEN digitizers are designed to reject the noise, subtract the baseline, and perform shaping and timing analysis.

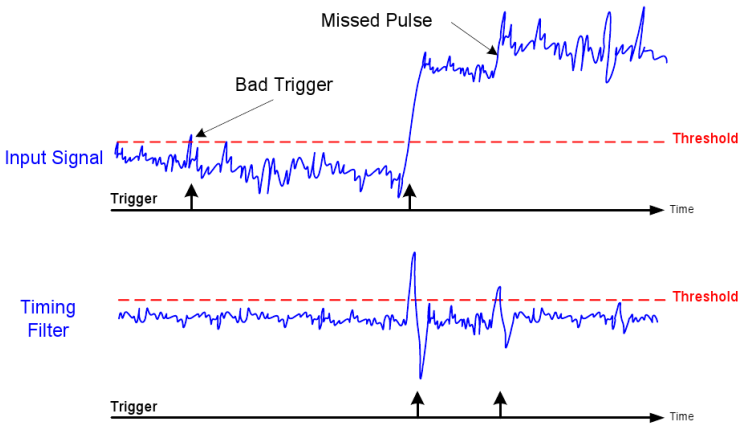

Fig. 2.1: Triggering before and after the timing filter.

While there are many types of timing and triggering filters, CAEN engineers have developed an **RC-(CR)^N** filter which has the capacity to reject high frequency noise (RC filter = mean filter), restore the baseline, cancel low frequency fluctuations (CR^N Filter = derivative), and transform the pulse into a bipolar signal to whose zero crossing (pulse amplitude independent) can be used to determine ”the” or ”a fine” Time Stamp. A more detailed explanation of the fine timing capability of this filter is included in the Section **High Resolution Timing measurements: digital Constant Fraction Discriminator**, which may be found beginning on page 21 of this document.

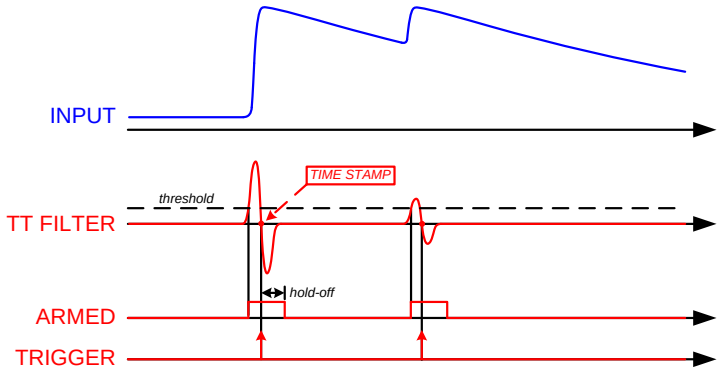

Fig. 2.2: Pulse triggering with Timing Filters.

In some MCA models, CAEN has introduced what is referred to as a **Fast Trapezoid** filter as alternative to the **RC-(CR)^N** (see **Fig. 2.3**).

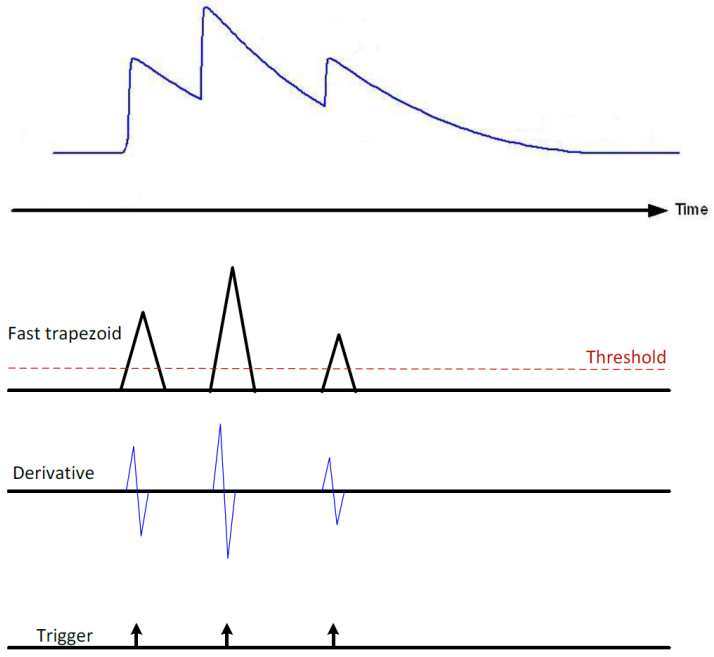

Fig. 2.3: Triggering on the fast trapezoid signal.

In cases wherein the Fast Trapezoid filter is applied the threshold is referred to the fast trapezoid itself and the threshold crossing arms the trigger. To achieve higher precision in the trigger position a subsequent derivative of the fast trapezoid is created. The trigger fires at the zero crossing of the derivative signal itself.

Besides the RC-(CR)^N and the fast trapezoidal filters, CAEN has also developed a digital implementation of the **Constant Fraction Discriminator**, which applies a linear interpolation of the samples adjacent to the zero crossing. This Constant Fraction Discriminator functionality is specific digitizer models running DPP-PSD firmware. More details will be given in the Section **High Resolution Timing measurements: digital Constant Fraction Discriminator**.

Pulse Height Analysis (DPP-PHA): Digital MCA

The purpose of DPP-PHA (Pulse Height Analysis) is to implement a digital version of the analog chain composed of a Shaping Amplifier + Peak Sensing ADC (e.g. Multi-Channel Analyzer). The DPP-PHA is implemented in the following digitizer models; Mod. **x724** (14 bit, 100 MS/s), Mod. **x725** (14 bit, 250 MS/s), Mod. **x730** (14 bit 500 MS/s) and in Digital MCA Models Mod. **DT5780**, **DT5781**, **DT5770**, **Hexagon**, as well as in the Tube-based portable MCA **ɣstream**. DPP-PHA is primarily used for high resolution spectroscopy utilizing Germanium and Silicon detectors. However, it is also well suited for inorganic scintillators such as NaI and CsI. The output of the charge sensitive preamplifier or photomultiplier is connected directly to the input of the digitizer or MCA, eliminating the need for a Shaping Amplifier.

The energy evaluation (or pulse height analysis) is performed by means of a Trapezoidal Filter. There exist many articles and papers which describe the principle of operation for Trapezoidal Filters, as well as relevant equations and implementation techniques for this filter [RD2]. For the purposes of this document the trapezoidal filter can be briefly described as a filter which has the capability to transform a signal generated by a charge sensitive preamplifier (and thus exhibiting typical exponential decay) into a trapezoid which presents a flat top whose height is proportional to the amplitude of the input pulse. In other words, the height of the trapezoid is proportional to the energy released by the particle in the detector.

The function of the trapezoid is analogous to the role played by a Shaping Amplifier in a traditional analog acquisition system. We'd like to highlight the analogous characteristics of the two systems; both utilize a constant "shaping time" and both must be calibrated for pole-zero cancellation. For both systems a long shaping time results in better resolution, which results in a higher probability of pile-up. Both systems are AC coupled with respect to the output of the preamplifier who's baseline is hence removed. Finally, both have their own output DC offset, which constitutes another baseline for peak detection.

Setting the parameters of the trapezoidal filter is similar to operating the potentiometer of a shaping amplifier. This analogy makes the understanding of DPP parameters easier for physicists who may be familiar with the traditional spectroscopy chain.

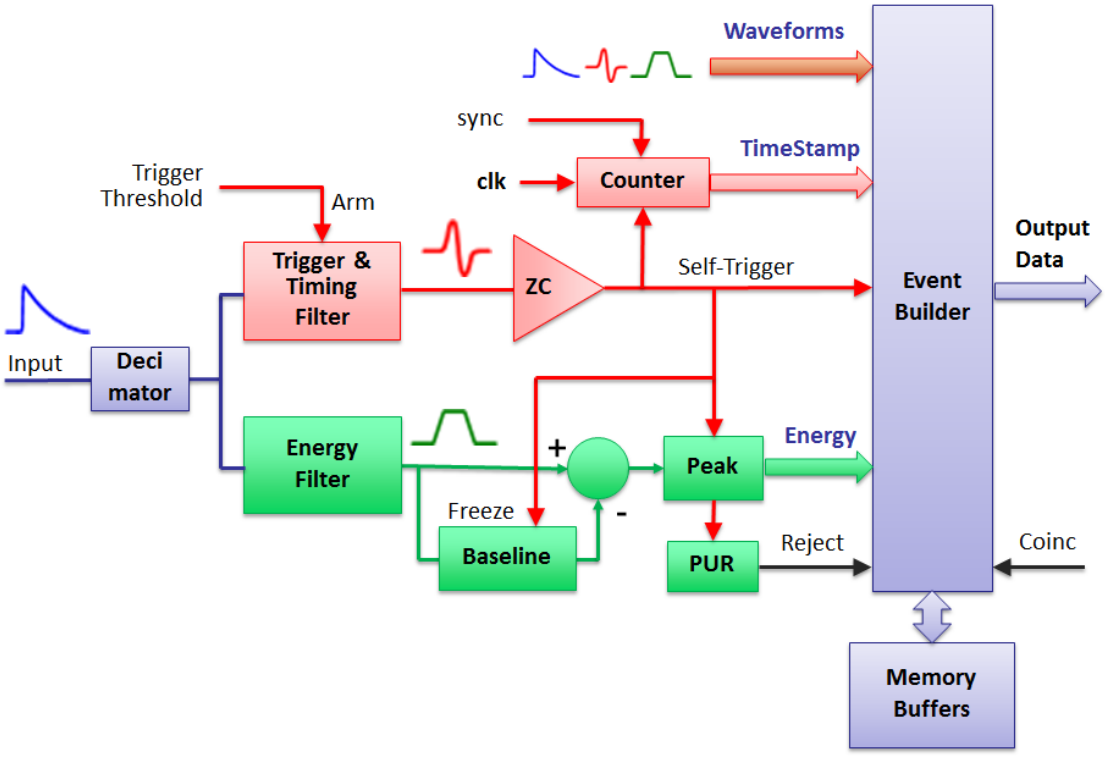

Fig. 2.4: Block Diagram of the DPP-PHA firmware.

The Pulse Height Analysis algorithm is able to perform online baseline restoration, ballistic effect corrections, and manage the pile-up of on-line data acquisition. The following picture is a simplified schematic depicting how the timing and trapezoidal filter is implemented in the DPP-PHA firmware.

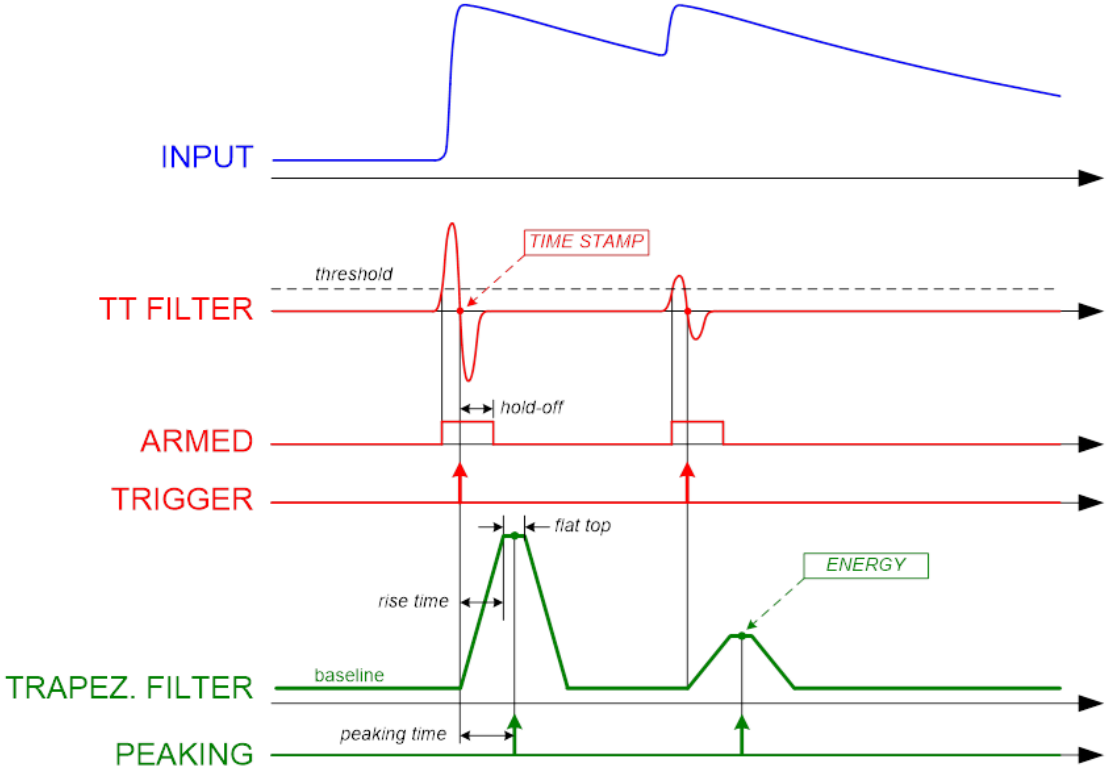

Fig. 2.5: Simplified signal scheme depicting the Trigger and Timing Filter (red) and the Trapezoidal Filter (green). The blue trace represents the input pulses coming from the Preamplifier.

Note: More details about the DPP-PHA firmware can be found in **[RD3]**.

Charge Integration (DPP-PSD and DPP-QDC): Digital QDC

CAEN DPP-PSD and DPP-QDC Firmwares comprise the digital versions of the analog chain composed of a Charge Integrating ADC (QDC), a Discriminator, and a Gate Generator. The DPP-PSD firmware is available for the following digitizer models; **x720** (12bit, 250 MS/s), Mod. **x725** (14bit, 250 MS/s), Mod. **x730** (14bit, 500 MS/s), Mod. **x751** (10bit, 1 GS/s), while the DPP-QDC firmware is available for digitizer model **x740D** (12 bit, 62.5 MS/s). The primary advantage of the digital solution lies in the fact that it is very easy for the user to implement and modify delay lines by simply adjusting the associated parameter in the control software. Thus, developing an integration gate and adjusting it's position to match the position of the pulse is as simple as changing a number. Additionally, the DPP can calculate the baseline of the signal and subtract it, essentially functioning as a pedestal cancellation. The extremely high dynamic range is another critical advantage of the digital approach. Unlike an analog ADC, in which the integrating capacitor can become saturated, with a DPP-based digital solution the charge is represented by the sum of a set of samples (e.g. accumulator). The charge parameter is fully adjustable and may be set as high as is required by simply changing the number of bits in the accumulator.

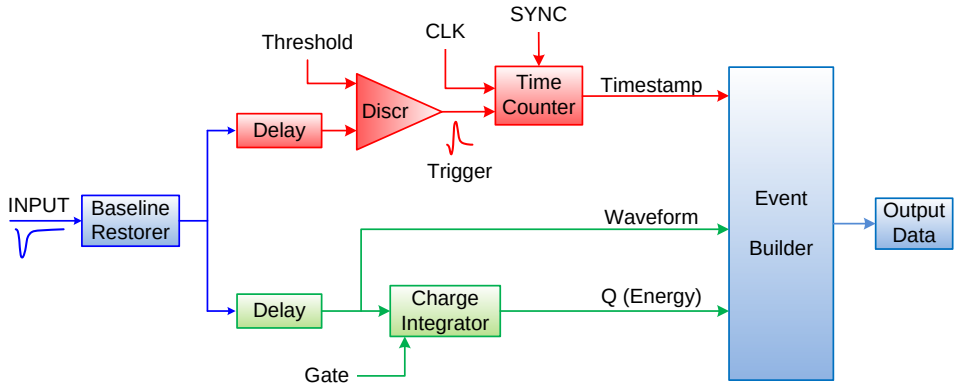

Fig. 2.6: Block Diagram of the charge integration section of the DPP-PSD and of the DPP-QDC.

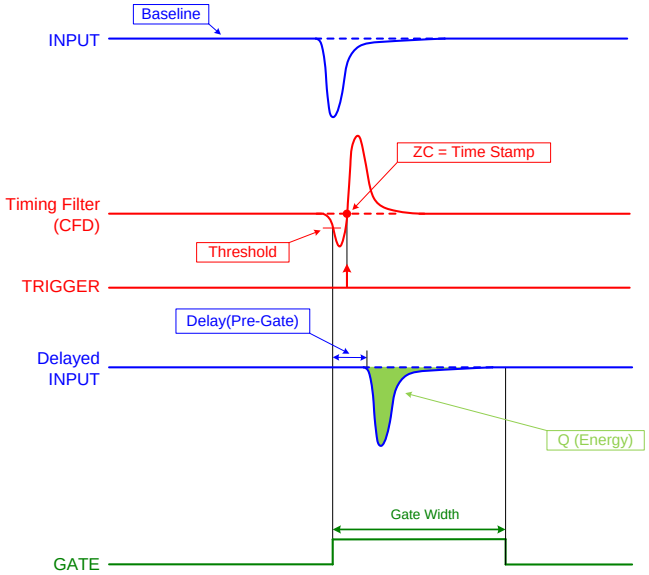

Fig. 2.7: Signals and parameters of the charge integration section of the DPP-PSD and of the DPP-QDC.

Note: More details about the DPP-PSD and DPP-QDC firmware can be found in **[RD4]**, **[RD5]**, and **[RD6]**.

Pulse Shape Discrimination (DPP-PSD): N–γ Discrimination

A very typical example of particle identification is neutron-gamma discrimination utilizing organic liquid scintillators for acquisition. Extending beyond Charge Integration, DPP-PSD firmware has been designed to allow the user perform neutron-gamma discrimination. The DPP-PSD is implemented in the Mod. **x720** (12bit, 250 MS/s), Mod. **x725** (14bit, 250 MS/s), Mod. **x730** (14bit, 500 MS/s), and in the Mod. **x751** (10bit, 1 GS/s).

The shape of the signal is composed by two exponential decays having two different time constants. The ratio between the fast and the slow components provides information with regards to particle typology. In both analog and digital acquisition systems there are two primary approaches: rise-time (or zero crossing) versus energy correlation, or ΔE/E correlation (double gate charge integration) **[RD7]**.

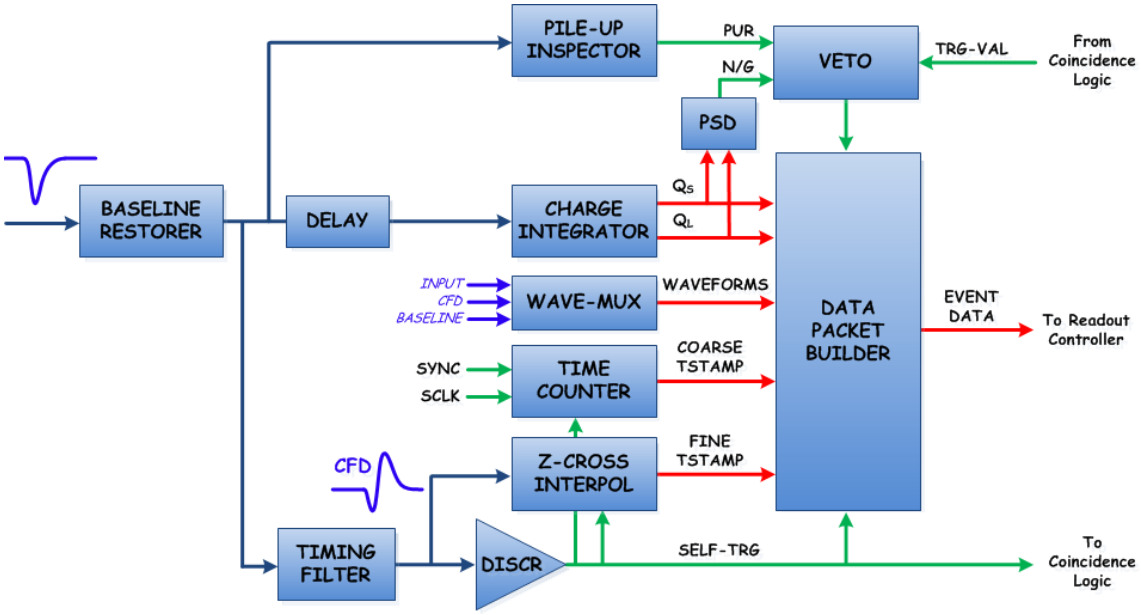

Fig. 2.8: Block Diagram of the parameters of the DPP-PSD.

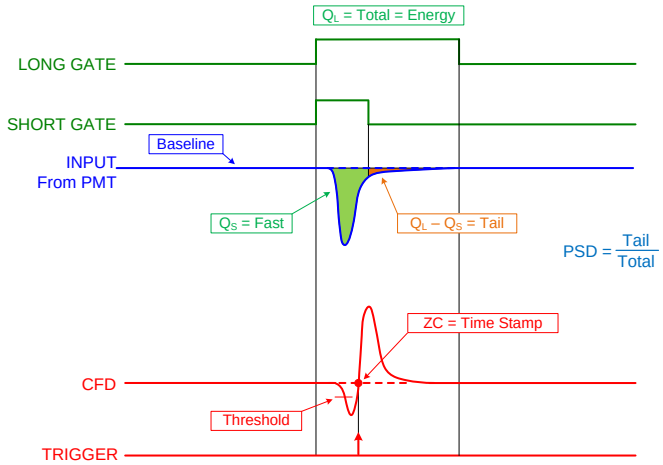

Fig. 2.9: Signals and parameters of the DPP-PSD.

Note: More details about the DPP-PSD and DPP-QDC firmware can be found in **[RD5]** and **[RD8]**.

High Resolution Timing measurements: digital Constant Fraction Discriminator

Traditionally, time measurements in physics (typically defined as the measurement of the arrival time of the pulses with respect to a common time reference) are done utilizing a discriminator which receives the analog pulses and generates a a digital signal followed by a Time-to-Digital Converter (TDC). Conventional TDCs may have quite high resolution (up to 25ps), high channel density (128), multi-hit capability, and other power features. However, there are applications for which conventional TDCs may be poorly suited. For example, in some beam experiments it is necessary to acquire the arrival times associated with a burst of pulses. With multi-hit TDCs the maximum number of hits which may be recorded before readout is required is typically quite low. Another potential problem associated with the traditional chain, the discriminator can sometimes introduce walk or jitter, thus reducing time measurement resolution. Finally, there are applications for which the time information must be correlated to some other quantity of interest, such as charge, pulse height, or pulse shape. In all of these cases a digitizer-based solution may be suitable or even preferable. Another important point to consider; the recent development of ultra-fast A/D converters have resulted in digitizer-based solutions which offer superior timing resolution to the traditional TDC. In fact, applications which require 10ps or better timing resolution are typically based on digitizers.

As with other DPP algorithms, when it comes to digital Constant Fraction Discriminator (CFD) algorithms there is an analogy between a traditional analog chain and digital filters: the input pulse (typically unipolar) is transformed into a bipolar signal, wherein the zero crossing determines the arrival time. This results in timing information which is independent from pulse amplitude, which is the whole point of the timing filters (see Section **Pulse Triggering and Timing Filters**).

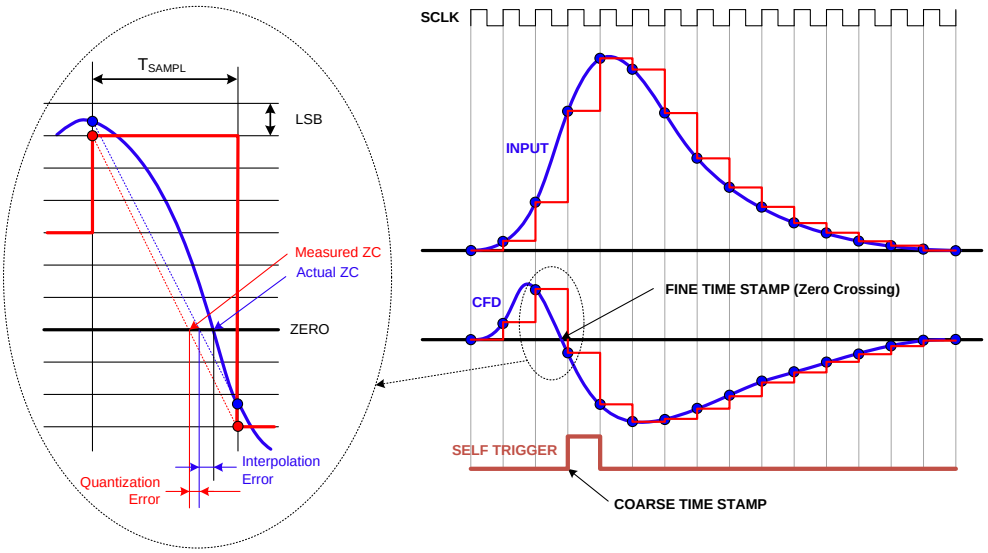

Fig. 2.10: Timing filter and zero crossing with interpolation.

It is possible to increase timing resolution beyond the granularity given by the sampling period of the ADC. To do so it is necessary to perform an interpolation utilizing two or more sample points adjacent to the zero crossing. The result is a line segment between two points, otherwise referred to as a linear interpolation.

If we consider an ideal signal without any electronic noise the precision in determining the zero crossing is dependent upon two factors:

1. The **Interpolation Error E_i** (geometric error) due to deviation of the straight line from the actual pulse curve.
2. The **A/D Quantization Error E_q** that affects the value of the two points used for the linear fit.

In Fig. **Fig. 2.10** the analog signal is depicted by the blue line, and the digital values are depicted in red. Please note, the CFD curve does not exist in analog, it is created digitally in the FPGA of the digitizer. The

self-trigger is issued on the first sample after the zero crossing with the relevant Coarse Time Stamp. The interpolator calculates the Fine Time Stamp by means of the dashed red line, depicted within the oval. The two errors, E_i and E_q, are shown in the picture. The resolution of the fine time stamp is affected by the rising edge of the input signal, by the sampling rate of the digitizer, and by the pulse amplitude when compared to the least significant bit of the ADC (and therefore the number of bits in the ADC).

Both experimental tests and simulations indicate that the rise time of the signal will significantly impact the results in the following manner. If the rise time is greater than than 5*Ts (Ts = sampling period), the error in the calculation of the zero crossing is mainly due to the A/D quantization error, thus the number of bits of the digitizer has a dominant effect on the timing resolution. However, if the rise time is smaller than 5*Ts then the approximation of the curve to a linear segment is too coarse. In such a case the most important contribution to timing error is due to inaccuracy in determining the zero crossing.

Typically the sampling clock and the input signal are not correlated and their resultant phase is completely random. The interpolation error is a function of this phase, as shown in Fig. **Fig. 2.11** where the same analog signal (blue) is sampled by two clocks with disparate phases (green and orange).

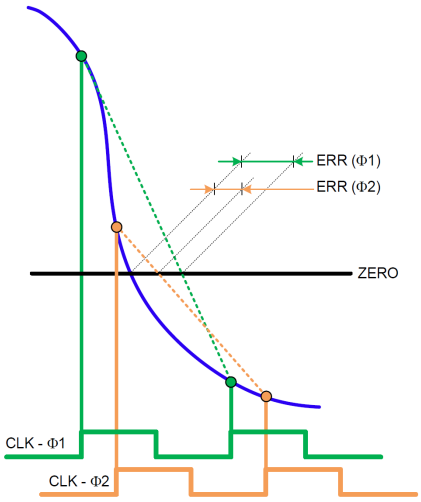

Fig. 2.11: Interpolation error affected by the clock phase.

In a start-stop measurement (time difference between two channels), we have:

$$\Delta T_{MEASURED} = [T_{STOP} + ERR(\Phi_{STOP})] - [T_{START} + ERR(\Phi_{START})] = (T_{STOP} - T_{START}) + [ERR(\Phi_{STOP}) - ERR(\Phi_{START})]$$

being Φ the relative phase between sampling clock and signal. If the start-stop delay (ΔT) is a multiple of the sampling clock period, then $\Phi_{START} = \Phi_{STOP}$, the two errors are perfectly subtracted and the total interpolation error is zero (again we are not considering here the random electronic noise). The worst case is instead when the start-stop delay is (N+0.5)*T_{SAMP} (being N any integer number) and the error difference swings between two symmetrical values depending on the uncorrelated phase of the sampling clock with respect to the signals.

The resultant effect appears on the timing spectrum as a characteristic double peak, the shape of which is attributable to the oscillating disturbances. Additionally, the timing resolution is a function of the measured delay with periodical repetition, being very good at the multiple of T_{SAMP} and assuming the worst value in the middle. **Fig. 2.12** shows the periodicity of the timing resolution while incrementally increasing the start to stop delay.

The associated **Fig. 2.12** is the result of test measurements performed with a 500 MS/s digitizer. The peaks in the curve (e.g. lowest resolution) correspond to 1ns and 3ns, which is the maximum phase shift for the stop relative to the start. The figure also illustrates an artifact in the timing spectrum due to the random rotation of the clock phase.

The interpolation error becomes the dominant source of noise when the input signal has a leading edge (measured from 10% to 90% of the amplitude) close to the sampling period. As a rule of thumb, this

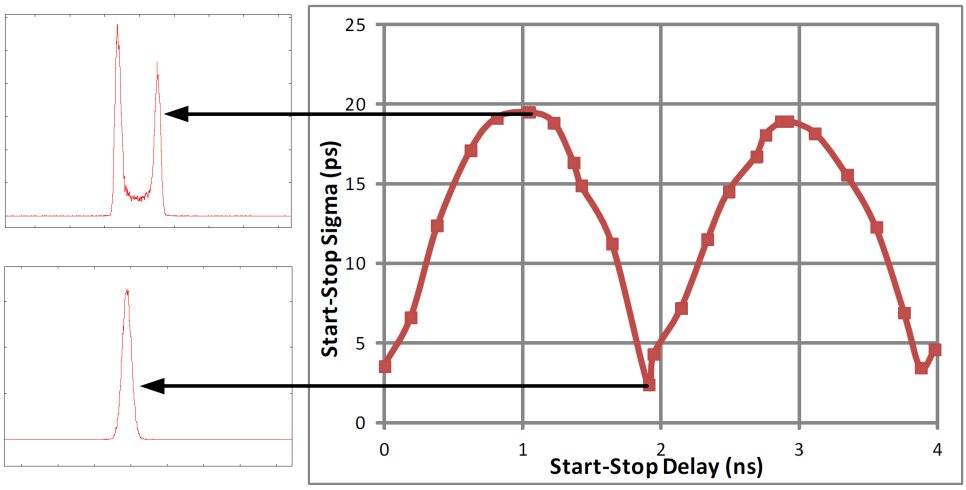

Fig. 2.12: Timing resolution as a function of the Start-Stop delay for a 2 ns rising edge pulse.

interpolation error becomes negligible when the rising edge of the signal is at least 3-5 times the sampling period. For slower signals the noise is dominated by the quantization error or by the electronic noise. Thus, the resolution is no longer dependent on the measured delay. Improvement in timing resolution may be achieved by adding a fast shaper or low pass filter between the detector and the digitizer. This analog filter reduces the high frequency noise and slows down the incoming analog pulses, making them more suitable for the given sampling rate of the digitizer. Increasing timing resolution by slowing down the signal may appear counter-intuitive to users familiar with traditional analog discriminators, where the highest rising edge corresponds to the best timing resolution. However, our tests indicate that slowing down the signal can be a very effective approach for digital CFD.

CAEN engineers have also developed advanced techniques which allow the DPP user to compensate and correct for the interpolation error. These techniques rely on the premise that the interpolated zero crossing is affected by a predictable geometrical error which is dependent upon the known position of the two points being utilized for the interpolation.

Several measurements have been performed with the x730, x751, x761, x742, and x743 digitizer families, and are detailed in **[RD9]** and in **[RD10]**. In the case of the x730, the time measurement has been performed online taking full advantage of the processing capabilities of the algorithms implemented in the FPGA. With regards to the other digitizer families the full waveforms were recorded and the processing was performed in an offline analysis.

Zero Length Encoding (DPP-ZLE): Zero Suppression

In many experimental conditions it is beneficial to retrieve full waveform information from the digitizer without wasting valuable bandwidth and disk space resources by transferring and storing useless information. For exactly such cases the DPP-ZLEplus algorithm has been developed. ZLEplus is based on a zero suppression algorithm and is designed to remove ”useless data” (zeros) from the acquisition. This approach is greatly advantageous for compressing the data and reducing the data throughput requirement from the digitizer to the computer. The DPP-ZLEplus firmware is implemented in digitizer models Mod. **x751** (10bit, 1 GS/s)., Mod. **x725** (14bit, 250 MS/s), Mod. **x730** (14bit, 500 MS/s). The DPP-ZLEplus algorithm is primarily intended for those experiments where the amount of ”interesting” information is quite low with respect to the total information available. For example, when there are large acquisition windows with respect to the length of a single event, or when the input signal rate is quite low. Transmitting the whole acquisition window results in an abundance of information which includes samples containing no critical event data. Those samples correspond to what we refer to as the ”signal baseline” The DPP-ZLEplus firmware dynamically evaluates the signal baseline and freezes it’s value at the beginning of the acquisition window. This dramatically improves memory efficiency and readout throughput.

The following picture illustrates the working principle of the DPP-ZLEplus firmware, including some of the more critical control parameters.

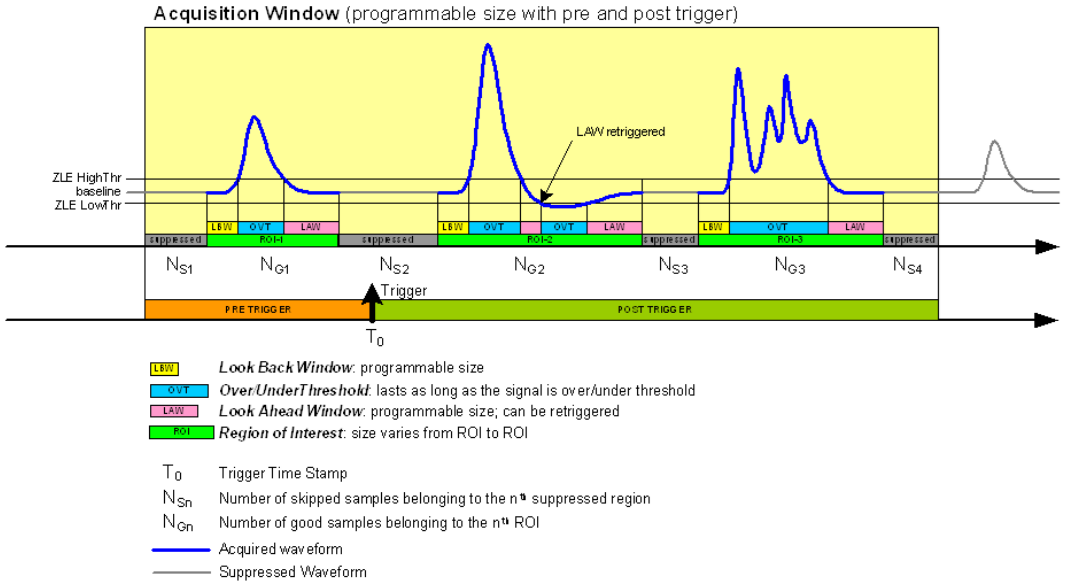

Fig. 2.13: Signals and parameters of the DPP-ZLEplus firmware.

One important feature of DPP-ZLEplus to consider; an external trigger is required to start the acquisition window. The trigger must be sent to the digitizer via the front panel TRG IN connector. The user can then define the ”Pre-Trigger” and the ”Record Length” values, which are thereafter referred to the external trigger. With regards to the above **Fig. 2.13**: within the acquisition window, the algorithm searches for a signal either exceeding the High Threshold (ZLE High Thr) or falling below the Low Threshold (ZLE Low Thr). The user may set two windows, the Look Back Window (LBW) and the Look Ahead Window (LAW). Signal recording begins NLBW samples (N = programmable number) before the threshold crossing (LBW in the above-figure), and stops NLAW samples after the crossing in the opposite direction (LAW in the above-figure). The recording regions define the Region of Interest (ROI) within the algorithm. Outside of the ROI the algorithm records the fixed value of the baseline.

Note: More details about the DPP-ZLEplus firmware can be found in **[RD11]**.

Note: The DPP-ZLEplus is COMING SOON for the Mod. x725 and Mod. x730.

Dynamic Acquisition Window (DPP-DAW): Dynamic Zero Suppression

A second zero suppression firmware, Dynamic Acquisition Window (DPP-DAW), has been developed to improve the zero suppression capabilities of CAEN digitizer models Mod. **x724**, Mod. **x725** and Mod. **x730**. DPP-DAW is based on the same concept of DPP-ZLEplus with one critical difference. DPP-DAW firmware allows each digitizer channel to self-trigger and acquire data independently from the other channels. The firmware can dynamically adjust the record length of every triggered event to fit the actual duration of the input pulses. This feature is implemented via the Time Over Threshold parameter. This feature is advantageous as it prevents accidental cutoff and data loss associated with a fixed acquisition window should the pulse be longer than expected. The DPP-DAW algorithm is capable of continuously evaluating the signal baseline and reference a trigger threshold to the baseline value. As a result, the threshold can follow baseline drift of the input signal without changing trigger conditions of the data acquisition system. The user can set parameters such as minimum record length and pre-trigger as well as define the minimum number of samples under threshold so as to avoid losing samples of interest before and after the Time Over Threshold condition is met. The function of these parameters are illustrated in the Figure below (**Fig. 2.14**).

Another advantageous feature to consider; DPP-DAW can accept an external veto, allowing the user to define an inhibit of data acquisition. A programmable input delay is available to compensate for latency associated with veto generation which is managed by an external logic unit. Additionally, the user may store not only over-threshold sections of the significant pulses but also the samples before and after the threshold crossing points by means of setting the number of samples for the Pre-Trigger and Minimum Under Threshold parameters.

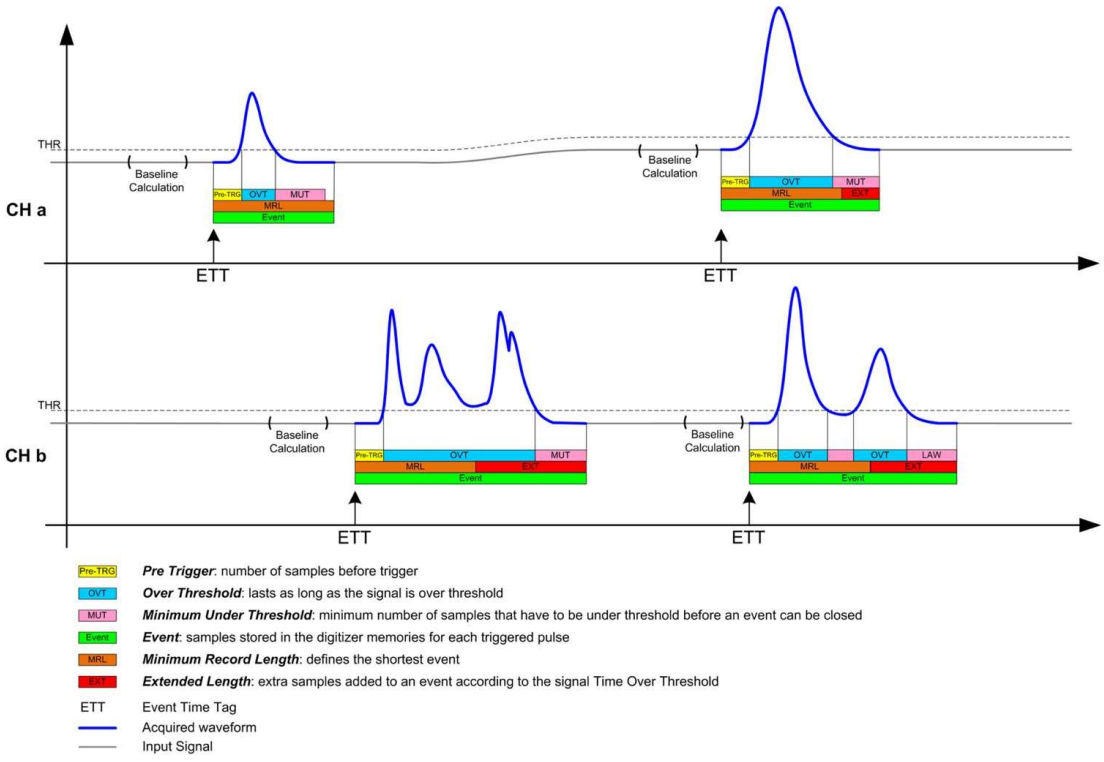

Fig. 2.14: Signals and parameters of the DPP-DAW firmware.

Note: More details about the DPP-DAW firmware can be found in **[RD12]**.

Note: The DPP-DAW is COMING SOON for the Mod. x725 and Mod. x730.

3 Software Interfaces

For the control of each DPP algorithm CAEN provides specific control and acquisition software:

Program Name	DPP Algorithm	Waveform Digitizers / MCA supported
MC²Analyzer	DPP-PHA	**x724 series (14 bit 100 MS/s):** • **V1724/VX1724 (VME)** • **DT5724 (Desktop)** • **N6724 (NIM)** **x725 series (14 bit 250 MS/s):** • **V1725/VX1725 (VME)** • **DT5725 (Desktop)** • **N6725 (NIM)** **x730 series (14 bit 500 MS/s):** • **V1730/VX1730 (VME)** • **DT5730 (Desktop)** • **N6730 (NIM)** **x780 series (14 bit 100 MS/s):** • **DT5780 (Desktop)** • **N6780 (NIM)** **x781 series (14 bit 100 MS/s):** • **DT5781 (Desktop)** • **N6781 (NIM)** **DT5770** *γstream* **Hexagon**
CoMPASS	**DPP-PSD** **DPP-PHA** **DPP-QDC** **(COMING SOON)**	**x720 series (12 bit 250 MS/s):** • **V1720/VX1720 (VME)** • **DT5720 (Desktop)** • **N6720 (NIM)** **x740D series (12 bit 62.5 MS/s) – COMING SOON :** • **V1740D/VX1740D (VME)** • **DT5740D (Desktop)** • **N6740D (NIM)** **x724 series (14 bit 100 MS/s):** • **V1724/VX1724 (VME)** • **DT5724 (Desktop)** • **N6724 (NIM)** **x725 series (14 bit 250 MS/s):** • **V1725/VX1725 (VME)** • **DT5725 (Desktop)** • **N6725 (NIM)** **x730 series (14 bit 500 MS/s):** • **V1730/VX1730 (VME)** • **DT5730 (Desktop)** • **N6730 (NIM)** **x751 series (10 bit 1 GS/s):** • **V1751/VX1751 (VME)** • **DT5751 (Desktop)** • **N6751 (NIM)**

DPP-QDC Demo Software	**DPP-QDC**	**x740D series (12 bit 62.5 MS/s)** • **V1740D/VX1740D (VME)** • **DT5740D (Desktop)** • **N6740D (NIM)**
DPP-ZLEplus Control Software	**DPP-ZLEplus**	**x725 series (14 bit 250 MS/s) – COMING SOON:** • **V1725/VX1725 (VME)** • **DT5725 (Desktop)** • **N6725 (NIM)** **x730 series (14 bit 500 MS/s) – COMING SOON:** • **V1730/VX1730 (VME)** • **DT5730 (Desktop)** • **N6730 (NIM)** **x751 series (10 bit 1 GS/s):** • **V1751/VX1751 (VME)** • **DT5751 (Desktop)** • **N6751 (NIM)**
DPP-DAW Demo Control Software	**DPP-DAW**	**x724 series (14 bit 100 MS/s):** • **V1724/VX1724 (VME)** • **DT5724 (Desktop)** • **N6724 (NIM)** **x725 series (14 bit 250 MS/s) – COMING SOON:** • **V1725/VX1725 (VME)** • **DT5725 (Desktop)** • **N6725 (NIM)** **x730 series (14 bit 500 MS/s) – COMING SOON:** • **V1730/VX1730 (VME)** • **DT5730 (Desktop)** • **N6730 (NIM)**

Tab. 3.1: Software Programs for DPP algorithms.

MC^{2}Analyzer

MC^{2}Analyzer is software which has been specifically designed for the 780/781 Digital MCA families, the DT5770 and Hexagon Digital MCAs, Digitizers which support the DPP-PHA (Digital Pulse Processing for Pulse Height Analysis) Firmware, and the Gamma Stream Tube Base Digital MCA. MC^{2}Analyzer software provides the user with the ability to manage, control, and simultaneously acquire data from multiple supported boards, allowing for the development of a "Multichannel Analyzer System". MC^{2}Analyzer allows the user to set relevant DPP-PHA parameters such as trigger threshold and shaping parameters independently for each acquisition channel, while simultaneously manage communication with the boards, acquire data, and plot histograms as well as waveforms for on-line monitoring of the acquisition. MC^{2}Analyzer also provides control of the HV power supplies which are included in several CAEN MCA products (DT5780, Gamma Stream, and Hexagon). Additionally, MC^{2}Analyzer is able to perform advanced mathematical analysis (e.g. peak search, background subtraction, peak fitting, energy calibration, ROI selection, dead time compensation, histogram rebin, etc...) on both the on-line histograms as well as the collected spectra. The software outputs data from each enable channel in the form of energy and time stamp lists as 1-column ASCII or ANSI N42.42 compliant files; thus allowing for off-line analysis via the implementation of other commercial or user-defined software for quantitative analysis. More information may be found in **[RD3]**.

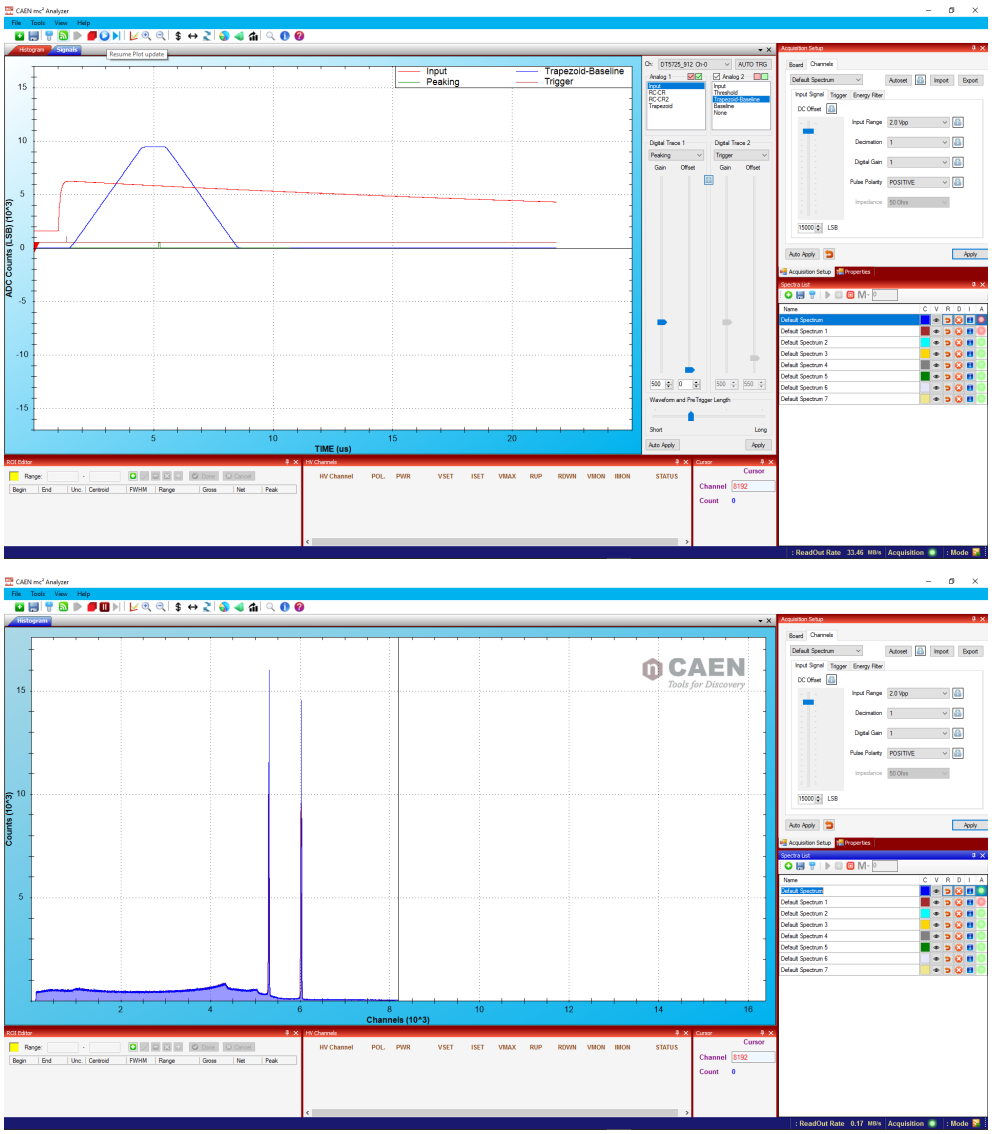

Fig. 3.1: Screen-shots of MC^{2}Analyzer software.

CoMPASS

CAEN Multi-PArameter Spectroscopy Software (CoMPASS) is the newest CAEN software offering, capable of implementing Multi-Parametric DAQ for Physics Applications in which the detectors can be connected directly to the digitizer inputs and the software acquires energy, timing, and PSD spectra. CoMPASS allows the user to manage multiple boards simultaneously while managing time synchronization and event correlation between different channels (via either hardware or software). CoMPASS also allows the user to apply energy and PSD cuts, calculate and depict statistics (e.g. trigger rates, data throughput, etc...), save output data files (raw data, lists, waveforms, spectra), and utilize the saved files to run off-line analysis with different processing parameters.

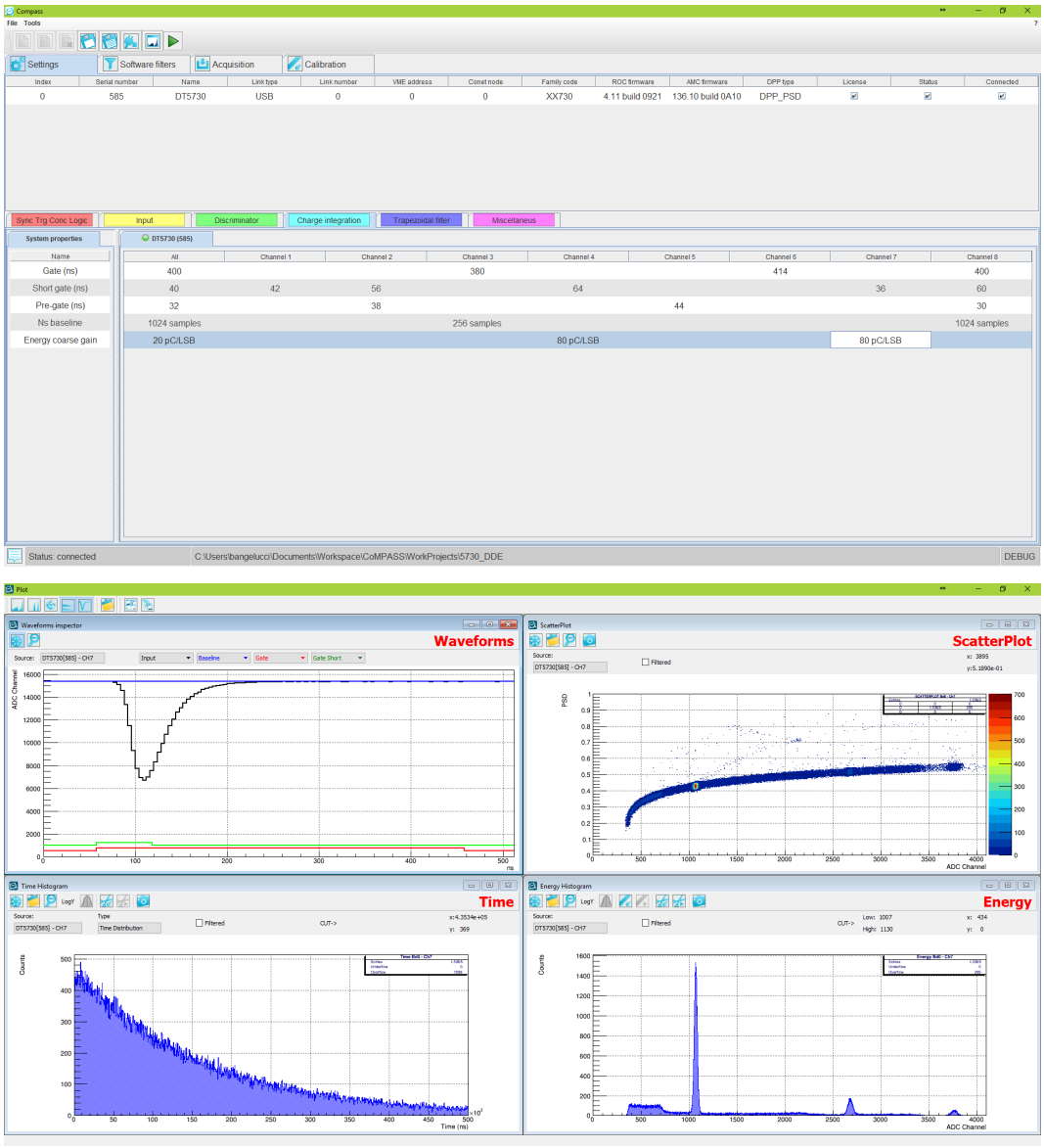

Fig. 3.2: Screen-shots of CoMPASS software.

DPP-QDC Demo Software

DPP-QDC Demo Software is a C demo application which manages communication and data acquisition for the 740D (12bit, 62.5 MS/s) digitizer series. DPP-QDC software allows the user to set up communication parameters and DPP settings. Waveforms and histograms may be plotted for a single channel at a time, and both waveforms and lists of time stamp and energy information can be saved for later analysis. DPP-QDC Demo Software also includes C source files for developers. More information can be found in **[RD6]**.

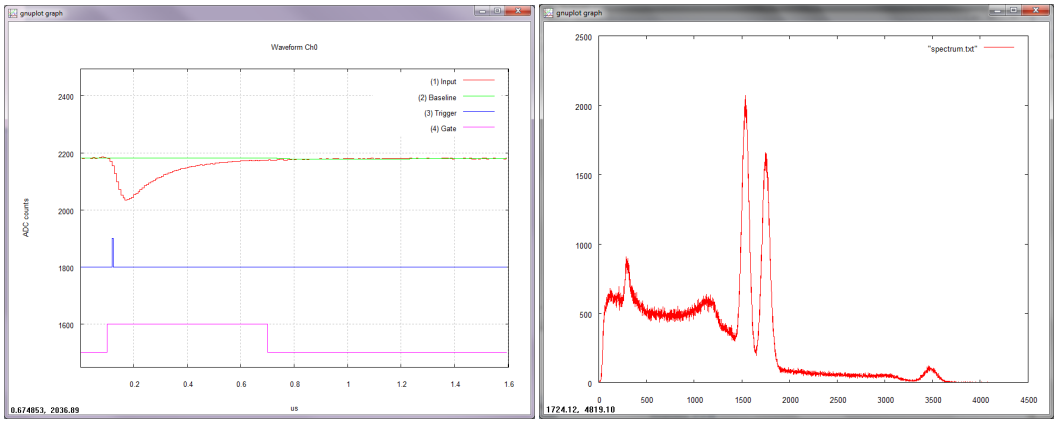

Fig. 3.3: Screen-shots of DPP-QDC Demo Control Software plotter.

DPP-ZLEplus and DPP-DAW Control Software

DPP-ZLEplus Control Software and **DPP-DAW Demo Control Software** are demo applications which are designed to introduce the user to the principles of operation of both DPP-Zero Length Encoding plus (DPP-ZLEplus) and DPP-Dynamic Acquisition Window (DPP-DAW) firmware. The user can perform entire data acquisition utilizing these softwares. The user may also use the source code to develop his or her own customized readout program. The packages include the C source files and Visual Studio project (compliant with Visual Studio Professional 2010). The Control Software is a C-based application that programs the Digitizer according to a set of parameters in the configuration text file, starts/stops the acquisition, and manges data readout. The waveforms elaborated by the ZLEplus and DAW algorithms may be either plotted utilizing gnuplot (an external plotting tool) or they may be saved to output text files. More information can be found in **[RD11]** and **[RD12]**.

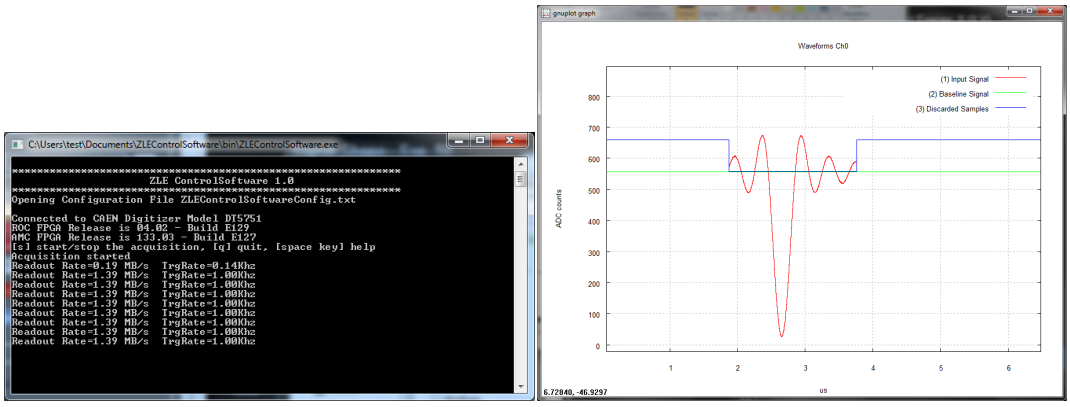

Fig. 3.4: Screen-shots of DPP-ZLEplus Control Software.

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CAEN SpA is acknowledged as the only company in the world providing a complete range of High/Low Voltage Power Supply systems and Front-End/Data Acquisition modules which meet IEEE Standards for Nuclear and Particle Physics. Extensive Research and Development capabilities have allowed CAEN SpA to play an important, long term role in this field. Our activities have always been at the forefront of technology, thanks to years of intensive collaborations with the most important Research Centres of the world. Our products appeal to a wide range of customers including engineers, scientists and technical professionals who all trust them to help achieve their goals faster and more effectively.

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