Rev. 0 - 26/07/1993

# V419

4 Channel Peak-Sensing ADC

CAEN
*Tools for Discovery*

**User Manual**
UM4940

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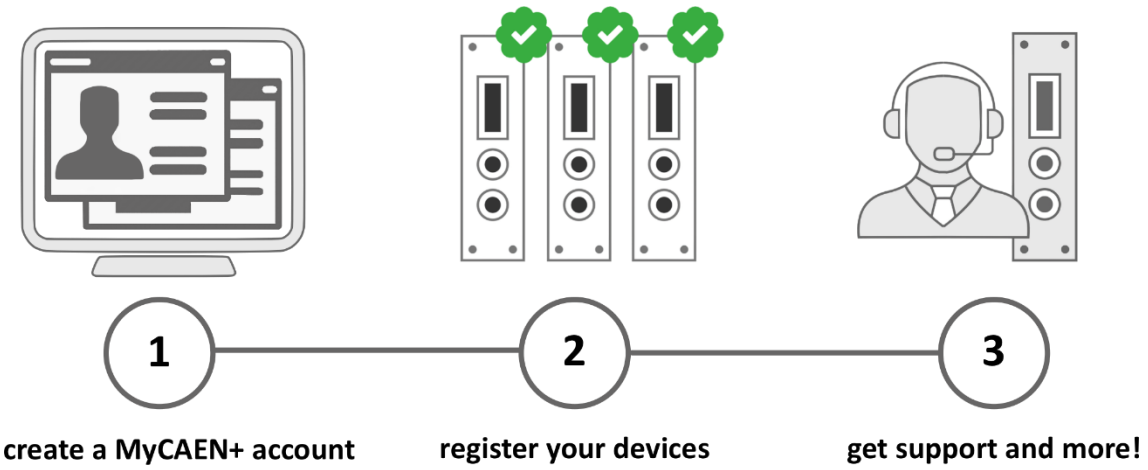


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# Technical Information Manual

**MOD. V 419**

*4 CHANNEL PEAK-SENSING ADC*

*26th July 1993*


CAEN
Mod. V419
DRDY
IN
CH0
TRG
DRDY
IN
CH1
TRG
DRDY
IN
CH2
TRG
DRDY
IN
CH3
TRG
0
1
2
3
TRG SEL
4 CH PEAK
SENSING
ADC

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# Contents

# 1. DESCRIPTION

The increasing complexity of nuclear physics experiments, in particular the use of array of detectors, has brought to light the need for analog to digital conversion systems with a high number of channels, good linearity and resolution characteristics and fast conversion time. Furthermore, a standard read-out interface and software control capability are mandatory requirements .

## 1.1 FUNCTIONAL DESCRIPTION

The model V 419 4 CHANNEL PEAK-SENSING 12 BIT ADC is an A24-D16 single width VME Slave module housing 4 independent channels able to detect and convert the peak value of the analog signals fed to the relevant input connectors .

The basic structure of the circuit is a multi-stretcher configuration built around a high speed conversion module: this means that the board can store up to four simultaneous

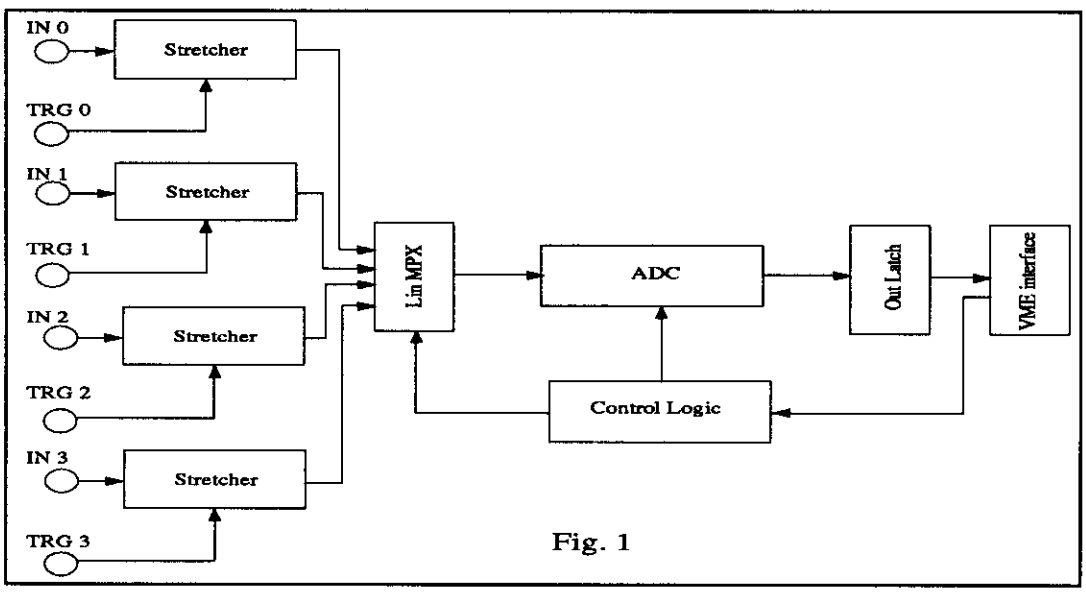

Fig. 1

pulses that will be converted in a fast sequence controlled by a microprogrammed logic ( see fig. 1).

For each channel the relevant linear-gate stretcher detects the peak-value of the input signal during the programmed gate width ( Rise Time Protection) and keeps that value till the end of the conversion phase.

The beginning of the linear gate-stretcher Rise Time Protection can be triggered in two different modes:

• auto-trigger: the Rise Time Protection starts when the signal on the analog input is higher than a fixed pre-threshold of a few millivolts;
• sampling mode : the Rise Time Protection is triggered either by an external pulse (TTL level) or by a software command that can be issued at the same time to all the channels.

When the sampling mode by external pulse is enabled, a front panel dip-switch selector allows the triggering of several channels by the same pulse ( see fig 2 ).

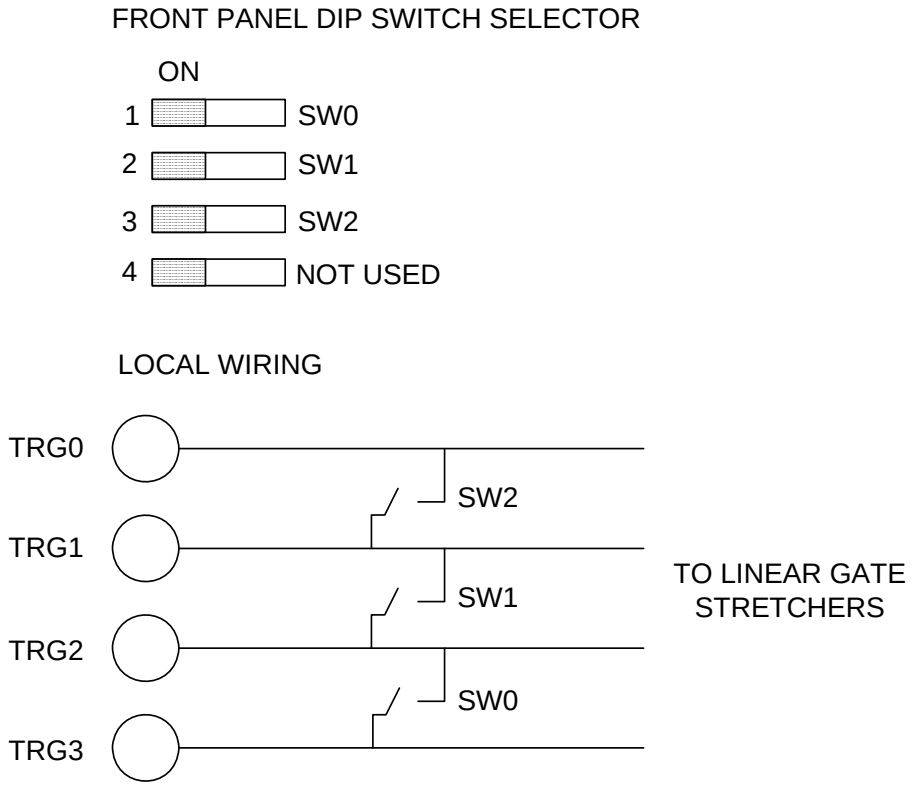


**fig.2**

Each channel has a window discriminator whose thresholds, low and high, can be programmed via VME. The conversion of a signal is possible only if its level is higher than the low threshold and lower than the high one, otherwise the stretcher is cleared to zero immediately at the end of the programmed Rise Time Protection.

The microprogrammed logic sequencer continuously checks the status of the stretchers and when it finds one free, this means after the end of the relevant programmed Rise Time Protection, it selects its signal through the analog multiplexer and enables the ADC block to start its conversion.

The converted data is stored into a memory buffer that can be accessed by the VME and the relevant LED on the front panel lights on. If the output memory buffer of a channel is busy the corresponding opening of the Rise Time Protection is disabled till the user reads the datum via VME.

The unit can accept either square wave, gaussian or semigaussian pulses. It can also convert constant or very slow signals working in sampling mode: for this purpose a sampling input connector is associated with each analog input on the front panel.

All the unit features are completely controllable via software through the VME bus, amongst them there are the following:

- enabling and disabling the acquisition for a given channel;
- linear gate stretcher trigger mode selection;
- output buffer reset : this can be accomplished automatically after a data read operation or by a write command into a register associated to the channel;
- setting of the linear gate aperture time (rise time protection);
- setting of the low and high thresholds of the window discriminator (8 bit values);
- selection of the self-test mode: by means of an analog switch, the linear gate input can be driven by a signal generated by an internal DAC; this makes a full functionality test of the board possible.

From the point of view of the VME interface (that is a slave-only type) the board can be seen as 16 consecutive registers. Each channel is described by means of 4 registers. A DATA REGISTER, a CONTROL/STATUS REGISTER and two registers holding the low and high threshold values of the window discriminator.
Two additional Auxiliary registers, mapped independently from the 16 base registers, are also addressable; their function, when accessed by a write operation, is to generate a software trigger and a reset to all the channels respectively . As these Auxiliary registers can be mapped on the same address in different boards, they can be used to provide the simultaneous trigger or reset a group of multiple ADC boards.

# 2. SPECIFICATIONS

## 2.1 PACKAGING

1-unit wide VME unit.

## 2.2 EXTERNAL COMPONENTS

**CONNECTORS:**

-No 4 LEMO 00 type " IN "; input signals connectors from CH0 to CH3 .

-No 4 LEMO 00 type " TRG "; external trigger signals connectors (std. TTL level) from CH 0 to CH 3.

**LEDs:**

-No 4 red LEDs "DRDY"; each one lights up when the channel's data register contains a valid data.

**DIP-SWITCHES:**

-No 1 " TRG SEL ". If the sampling mode by external trigger is selected, it is possible to send the same trigger pulse to each channel that has been enabled by the relevant switch (only 3 switches are used, refer to fig. 2).

## 2.3 INTERNAL COMPONENTS

**JUMPERS**

-No 33 located on the printed circuit board, to set the Base Address of the module ( see the description on paragraph 3.1).

## 2.4 CHARACTERISTIC OF THE SIGNALS

-signals to be converted (IN from CH0 to CH3) :
the module accepts both positive square wave pulses (min. width 1 μs) and positive gaussian or semigaussian shaped pulses with rise-time variable from 2 μs to 32 μs.
Input impedance : 1 KΩ.

-TRG ( from CH0 to CH3): std. TTL level, 1 KΩ impedance.

## 2.5 GENERAL

The following characteristics have been measured in a VME crate equipped with a linear power supply with 10 $mV_{pp}$ and 3 $mV_{pp}$ ripple on the +5 V and ±12 V respectively.

| | |
|---|---|
| No. of channels | 4 |
| Maximum input voltage | 4.096 V (1 mV/count) |
| Differential Non-linearity Error | < ±1% |
| Integral Non-linearity Error | < 1/2 LSB (±0.023%) |
| Resolution | 12 bits |
| Conversion Time | < 1.2 μs |
| Input Impedance | 1 KΩ |
| Dead Time | Rise-Time Protection + 500 ns |

## 2.6 POWER REQUIREMENTS

| | |
|---|---|
| -12 V | 400 mA |
| 12 V | 350 mA |
| 5 V | 2.3 A |

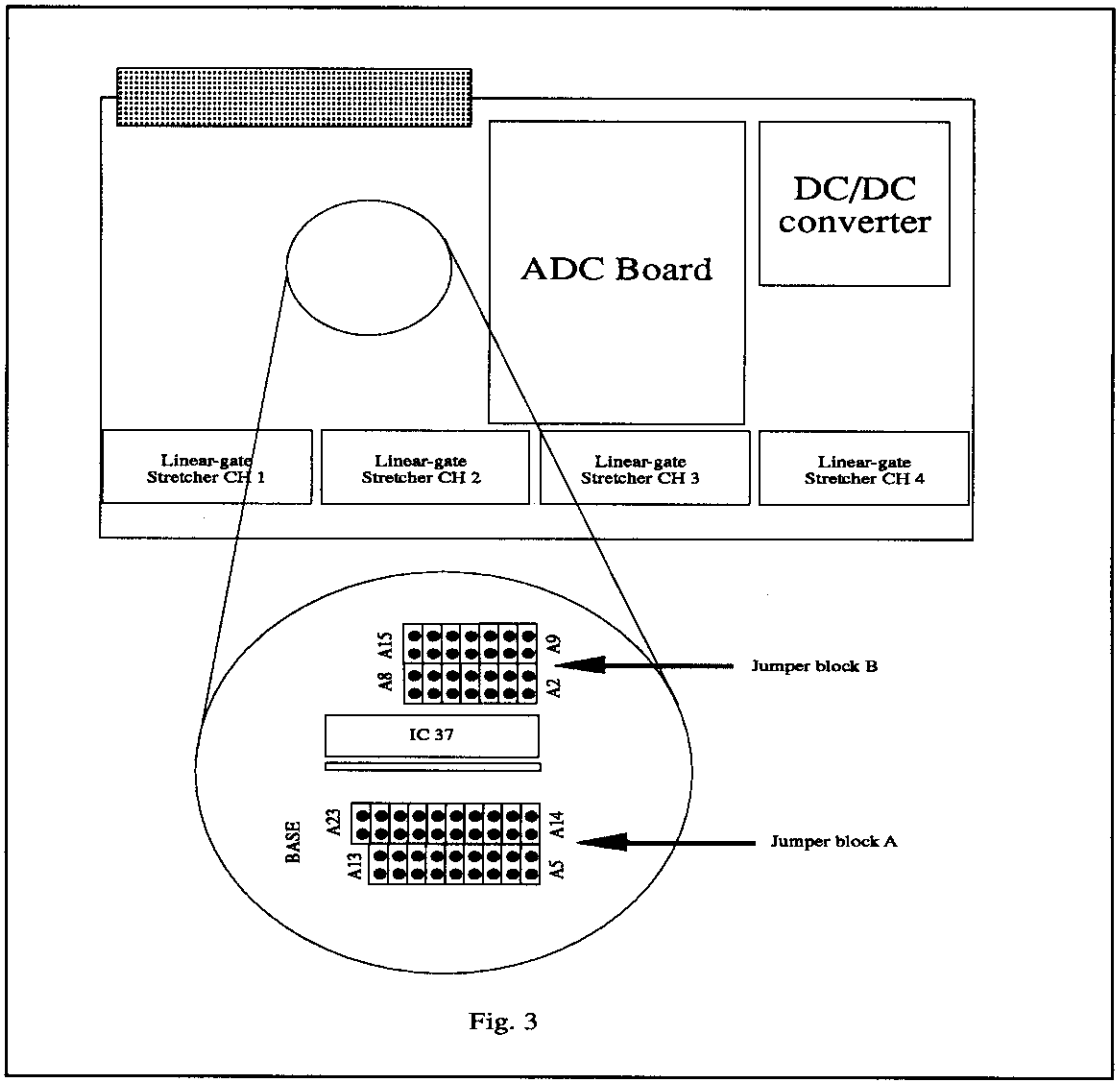


Fig. 3

# 3. OPERATING MODE

## 3.1 ADDRESSING SELECTION

The model V 419 is an A24-D16 VME slave and can be operated in Data Space. In the following description the H at the end of the numbers like E8H means that the numbers are expressed in hexadecimal base.

Before using the unit it is necessary to select the module's Base Address via the relevant jumpers housed inside the unit and shown in fig. 3.
The module's Base Address is composed of a Unit Address, a Registers' Base Address and an Auxiliary Registers' Base Address.
The Unit Address, selectable via the jumpers from A23 to A16 ( from 00H to FFH ) in the jumper block A ( see fig. 3), sets the address of the Unit inside the memory space of the single VME crate and corresponds to the most significant byte of the module's address.

The same Unit Address can be used for several V 419 in the same VME crate.

The Registers' Base Address from A15 to A5, selectable via the jumpers from A15 to A5 ( from 000H to FFEH ) in the jumper block A ( see fig. 3), sets the Base Address of the 16 registers of the single unit and corresponds to the less significant byte of the module's

| ADDRESS<br>xxxx = Base Address | FUNCTION | TYPE |
|---|---|---|
| xxxx 00 | CH0 DATA REGISTER | READ ONLY |
| xxxx 02 | CH0 CONTROL/STATUS REGISTER | READ/WRITE |
| xxxx 04 | CH1 DATA REGISTER | READ ONLY |
| xxxx 06 | CH1 CONTROL/STATUS REGISTER | READ/WRITE |
| xxxx 08 | CH2 DATA REGISTER | READ ONLY |
| xxxx 0A | CH2 CONTROL/STATUS REGISTER | READ/WRITE |
| xxxx 0C | CH3 DATA REGISTER | READ ONLY |
| xxxx 0E | CH3 CONTROL/STATUS REGISTER | READ/WRITE |
| xxxx 10 | CH0 LOW THRESHOLD | WRITE ONLY |
| xxxx 12 | CH0 HIGH THRESHOLD | WRITE ONLY |
| xxxx 14 | CH1 LOW THRESHOLD | WRITE ONLY |
| xxxx 16 | CH1 HIGH THRESHOLD | WRITE ONLY |
| xxxx 18 | CH2 LOW THRESHOLD | WRITE ONLY |
| xxxx 1A | CH2 HIGH THRESHOLD | WRITE ONLY |
| xxxx 1C | CH3 LOW THRESHOLD | WRITE ONLY |
| xxxx 1E | CH3 HIGH THRESHOLD | WRITE ONLY |

*Table 1*

address. The single register is then selected by the addresses from A1 to A4 as reported in table 1.

The Auxiliary Registers' Base Address, selectable via the jumpers from A15 to A2 ( from 0000H to FFFCH ) in the jumper block B ( see fig. 3), sets the Base Address of the 2 Auxiliary registers of the single unit. The single Auxiliary register is then selected by the addresses from A1 as reported in table 2.
In this way if in a single VME crate all the V 419 modules have been programmed with the same Unit Address and Auxiliary Registers' Base Address, all the units at the same time can be accessed in the Auxiliary registers with the same VME cycle to be reset or triggered ( see page. 2 ).

N.B. If the jumper is open the corresponding bit is a logic 0.

## Example:

Two units in the same crate have the following Base Address:

Unit A = FFE00xH
Unit B = FFEF0xH

The same units have the following Auxiliary Registers' Base Address:

Unit A =Unit B = C000H

The two units can be independently controlled having the relevant Registers' Base Address starting at the physical addresses:

Unit A = FFE000H  Unit B = FFEF00H

That means that for example the address of the CH1 CONTROL/STATUS REGISTER of the two units are located at the addresses:

Unit A = FFE002H  Unit B = FFEF02H

At the same time the Auxiliary Registers' Base Address and the Unit Address of the two units is the same; it means that the Auxiliary RESET REGISTER physical address of the two unit is

Unit A = Unit B = FFC000H

and performing a write cycle at this address both the units are reset at the same time.

N.B. This means that the Registers' Base Address and the Auxiliary Registers' Base Address must be set at different memory pages.

The 8 bits from A23 to A16 are used with the bits from A15 to A5 as to define the module Base Address and reserve a page of 32 bytes for each module. The bits from A0 to A4 are decoded in a demultiplexer which generates 16 signals defining the 16 bit Module Registers. In the same way, the same 8 bits from A23 to A16 are used with the bits from A15 to A2 to define a page of 4 bytes for each module. The bit A1 is decoded in a demultiplexer which generates 2 signals defining the two 16 bit auxiliary registers. The organization of the address decoding subsystem is shown in fig. 4

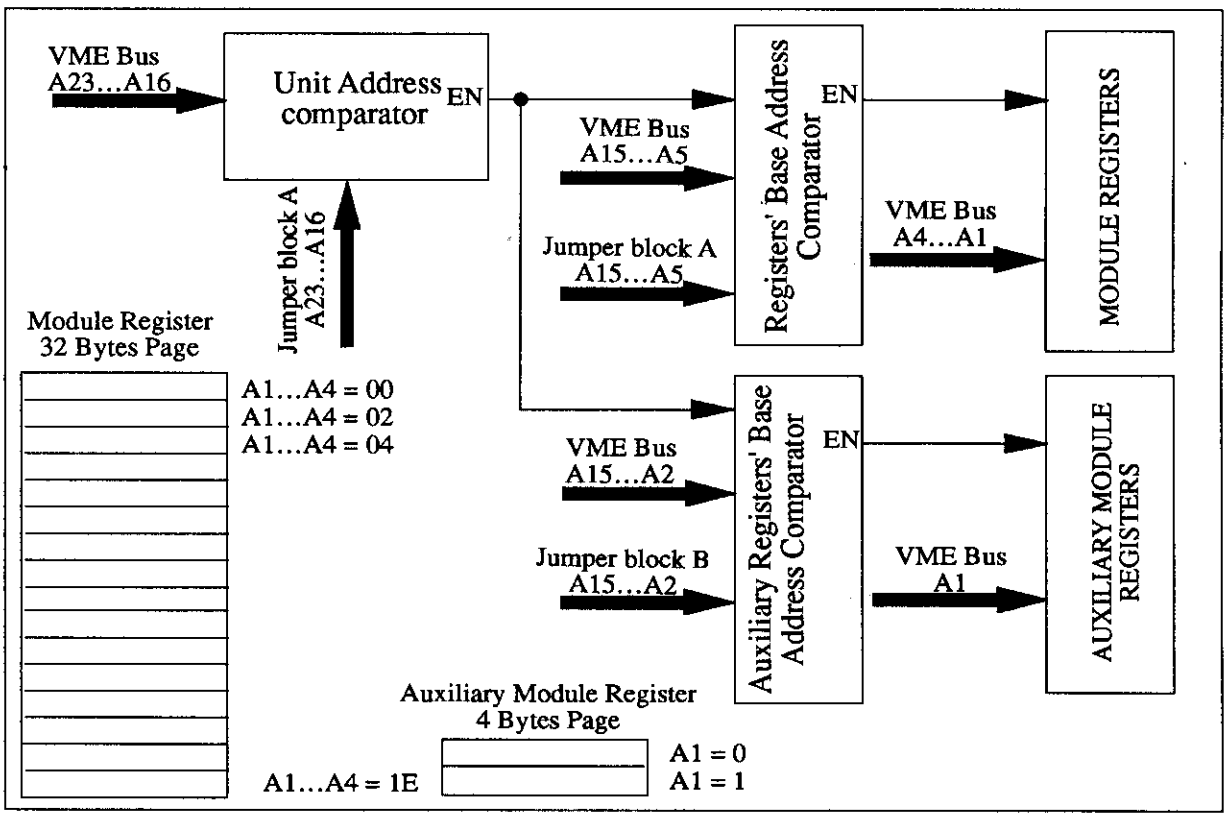


*Fig. 4*

## 3.2 MODULE REGISTERS

Each channel of the unit is described by 4 independent 16 bit Registers:
No 1 DATA REGISTER;
No 1 CONTROL/STATUS REGISTER;
No 1 LOW THRESHOLD REGISTER;
No 1 HIGH THRESHOLD REGISTER.

The offset of the registers referred to the Base Address is reported in table 1.

### 3.2.1 DATA REGISTER

The DATA REGISTER is a read-only register and keeps the converted data relative to the channel on the bits from 0 to 11. Any attempt to perform a WRITE operation on this register gives the automatic reset of the register itself as a result.
The DATA REGISTER can also be automatically reset after any READ of the data if this feature is enabled by the dedicated bit in the CONTROL/STATUS REGISTER.

### 3.2.2 CONTROL/STATUS REGISTER

The bits from 8 to 14 are not used.

| Bit No | MEANING | | |
|---|---|---|---|
| 0...3 | Rise Time Protection value. The programmed time is 2(n+1) µsec where n is the binary number corresponding to the bits | | |
| 4, 5 | Select the linear-gate mode as follows: | | |
| | bit5 | bit4 | |
| | 0 | 0 | Auto trigger |
| | 0 | 1 | Sampling by external TTL signal |
| | 1 | 0 | Sampling by software command |
| | 1 | 1 | Self test |
| 6 | RESET. If 0, the DATA REGISTER is automatically cleared after a read operation. | | |
| 7 | ENABLE/DISABLE. When 0, the conversion of the signal is disabled | | |
| 15 | DATA READY. When this bit is set the relevant DATA REGISTER has a valid datum | | |

### 3.2.3 LOW/HIGH THRESHOLD REGISTERS

These are two 8 bit registers keeping the window discriminator threshold values. The threshold values are the bits from 0 to 7 of the data bus. The value that can be programmed can range from 0 to 4.096. When the module is in Self Test mode, the High Threshold Registers contain the internal DAC setting value for each channel.

## 3.3 AUXILIARY REGISTERS

Two Auxiliary registers per unit are provided to enable the user to manage blocks of conversion channel greater than 4. These Auxiliary registers can be mapped via the Unit Address and the Auxiliary Registers' Base Address at the same physical address for several unit housed in the same VME crate. The meaning of these registers is in the following table.

| A1 | MEANING | TYPE |
|---|---|---|
| 1 | Software Trigger | Write Only |
| 0 | RESET | Write Only |

*Table 2*

In this way all the units in the same crate can be reset or triggered by the same software command.

## 3.4 SELF TEST MODE

The unit can operate in a Self Test mode. By setting bits 4 and 5 of the Control/Status Register to 1, it is possible to send the output of an internal DAC to the channels inputs. The DAC value for each channel can be set on 8 bit, up to 4096 mV, via the relevant High Threshold Register. The Rise Time protection must be triggered via Software. This operating mode allows to test the module's response on known internally generated levels.

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