Rev. 3 - Dec 21st, 2021

V1782

Octal Digital MCA

CAEN
Tools for Discovery

User Manual

Purpose of this Manual

This User Manual contains the main description of the V1782, Octal Digital MCA.

Any information about the registers mentioned in this document is detailed in the *724-781-782 DPP-PHA Registers User Manual* **[RD1]**.

For a deeper comprehension of topics like the principle of operation, the memory organization, the data format, and the readout software, please refer to the *MC²Analyzer User Manual* **[RD7]**.

Change Document Record

Date	Revision	Changes
January 28th, 2019	00	Initial release
May 30th, 2019	01	Global review to adapt to the product new name from V1781 to V1782. Added disclaimer in Chap. **6**.
September 9th, 2019	02	Updated cover picture and **Fig. 3.1**. Removed the "Product Code" column from **Tab. 1.1**. Removed website paths in the text. General text review on CoMPASS software new support.
December 21st, 2021	03	Removed "Preliminary" label from the cover page. Updated CAEN Technologies Inc. address on the back page.

Symbols, abbreviated terms and notation

ACS	Anti-Compton Shields
CSP	Charge Sensitive Preamplifier
DPP	Digital Pulse Processing
ICR	Input Count Rate
MCA	Multi-Channel Analyzer
PHA	Pulse Height Analysis
PMT	Photo Multiplier Tube
TR	Transistor Reset

Reference Documents

[RD1] UM5407 – 724-781-782 DPP-PHA Registers User Manual

[RD2] UM1934 - CAENComm User & Reference Manual

[RD3] UM1935 - CAENDigitizer User & Reference Manual

[RD4] GD2512 – CAENUpgrader QuickStart Guide

[RD5] UM2088 – Digital Pulse Height Analyzer User Manual

[RD6] GD2827 – How to make coincidences with CAEN digitizers

[RD7] UM3182 – MC²Analyzer User Manual

[RD8] UM5960 – CoMPASS User Manual

[RD9] GD6300 – CoMPASS Quick Start Guide

All documents can be downloaded at: https://www.caen.it/support-services/documentation-area/

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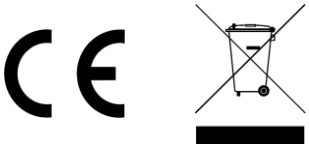

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1 Introduction

The V1782 is a 8-input 32k Digital MCA in 2U wide VME form factor. Each input is on a BNC connector (1 kΩ) with a 4-step software programmable coarse gain, a x0.2 attenuator by jumper selection, and a digital fine gain (1 to 2.2 in steps of 0.0001). When the hadware attenuator is disabled, the possible coarse gains are x1, x2, x4, x8, where x1 is 1 V_{pp} FSR; by enabling the hardware attenuator, the coarse gain options become x0.2, x0.4, x0.8, x1.6, where x0.2 is 5 V_{pp} FSR. An on-board jumper is available to match detectors equipped with RC (DC option) or TR (AC option) preamplifiers. The V1782 accepts signals directly from PMT anodes coupled with most scintillators (e.g. NaI, $LaBr_3$, BGO). Both positive and negative signals are managed by software selection.

The V1782 is principally suited for arrays of multi-segmented HPGe detectors, Clover gamma-ray detectors, and for Silicon strip detectors, but can actually cover a wide range of applications with multi-channel detectors (e.g CZT, scintillators). The 8 available inputs make this MCA ideal to make coicidences/anticoincidences **[RD7]** with ACS systems, low-background measurements with active shield. A practical example is a clover detector, where the channels from the four coaxial N-type HPGe crystals are read out by inputs 0-3 of the V1782, and the ACS is read out by input 4 configured as veto for inputs 0-3 (see Chap **18**).

The digital pulse processing combines Pulse Height Analysis (PHA) and waveform digitizing. The amplitude of the pulse is calculated on-board independently on each input, and the energy spectra are generated by the software. Portions of waveforms can be stored for on-line signal inspection during the card configuration, or saved for off-line analysis.

Front panel digital and analog I/O connectors (3 single-ended NIM/TTL LEMOs, 16 differential LVDS I/Os, 3-pin differential clock input and clock output) extend the standard functions of the V1782 allowing for board-to-board correlation among the inputs, for the implementation of a common veto/gate, for the time stamp synchronization of multiple boards in system building (see Chap. **5**).

Front Panel LED indicators make the user advised on the status of the board, acquisition, I/Os, and communication.

The V1782 is equipped with a VME64 interface supporting Single Data Transfer (D32), 32/64-bit Block Transfer (BLT, MBLT, 2eVME. 2eSST) and 32/64-bit Chained Block Transfer (CBLT) modes.

The card houses an optical link interface (CAEN proprietary CONET protocol) supporting transfer rates up to 80 MB/s and offering daisy chain capability: it is possible to connect up to 8 V1782 modules to a single CAEN A2818 Optical Link Controller, or up to 32 using a 4-link A3818 version. VME and optical link accesses take place on independent paths and are handled by the on-board controller; therefore, when accessed through the optical link, the board can be operated outside the VME Crate.

The V1782 is fully supported by CAEN MC^2 Analyzer and CoMPASS software. MC^2 Analyzer can manage the configuration, the acquisition, and the data plotting and saving of lists and spectra simultaneously from multiple boards, further featuring basic mathematical analysis tools. CoMPASS is a multi-parameter spectroscopy software enhanced with a wide selection of plots and histograms, supporting also ROOT TTree output file format for an easy post processing with user made analysis code. A dedicated software utility is provided for the firmware upgrade and to retrieve board information. Registers and C libraries, which may include example codes or demos, are then available to users who want to develop customized software applications for Windows® and Linux® OS (see Chap. **15**).

Board Model	Description
V1782	Octal Digital Multi Channel Analyzer
DPP Firmware	**Description**
DPP-PHA(*)	Digital Pulse Processing for Pulse Height Analysis
Related Products	**Description**
A1422A005F2	1 Ch. Charge Preamplifier, 5mV/MeVgain
A1422B005F2	4 Ch. Charge Preamplifier, 5mV/MeVgain
A1422C005F2	8 Ch. Charge Preamplifier, 5mV/MeVgain
A1422A045F2	1 Ch. Charge Preamplifier, 45mV/MeVgain
A1422B045F2	4 Ch. Charge Preamplifier, 45mV/MeVgain
A1422C045F2	8 Ch. Charge Preamplifier, 45mV/MeVgain
A1422A090F2	1 Ch. Charge Preamplifier, 90mV/MeVgain
A1422B090F2	4 Ch. Charge Preamplifier, 90mV/MeVgain
A1422C090F2	8 Ch. Charge Preamplifier, 90mV/MeVgain
A1422A400F2	1 Ch. Charge Preamplifier, 400mV/MeVgain
A1422B400F2	4 Ch. Charge Preamplifier, 400mV/MeVgain
A1422A005F3	1 Ch. Charge Preamplifier, 5mV/MeVgain
A1422B005F3	4 Ch. Charge Preamplifier, 5mV/MeVgain
A1422C005F3	8 Ch. Charge Preamplifier, 5mV/MeVgain
A1422A045F3	1 Ch. Charge Preamplifier, 45mV/MeVgain
A1422B045F3	4 Ch. Charge Preamplifier, 45mV/MeVgain
A1422C045F3	8 Ch. Charge Preamplifier, 45mV/MeVgain
A1422A090F3	1 Ch. Charge Preamplifier, 90mV/MeVgain
A1422B090F3	4 Ch. Charge Preamplifier, 90mV/MeVgain
A1422C090F3	8 Ch. Charge Preamplifier, 90mV/MeVgain
A1424	Scintillation Preamplifier
DT4700	Clock Generator
A317	Clock Distribution Cable
A317L	Clock Distribution Cable L 25 cm
A318	Single-Ended-to-Differential Cable Adapter
V1718	VME-to-USB 2.0 Bridge
V2718	VME-to-PCI Bridge
A2818	PCI Optical Link
A3818A	PCIe 1 Optical Link
A3818B	PCIe 2 Optical Link
A3818C	PCIe 4 Optical Link
AI2730	Optical Fibre 30 m simplex
AI2720	Optical Fibre 20 m simplex
AI2705	Optical Fibre 5 m simplex
AI2703	Optical Fibre 30 cm simplex
AY2730	Optical Fibre 30 m duplex
AY2720	Optical Fibre 20 m duplex
AY2705	Optical Fibre 5 m duplex

Tab. 1.1: Table of the related CAEN products and ordering options

(*) The V1782 is factory equipped with a licensed version of the DPP-PHA firmware.

2 Technical Specifications

MECHANICAL	**From Factor** 2-unit wide VME 6U module		**Weight** 800 g
ENVIRONMENTAL	**Operational Conditions** 0 to 50°C Temperature Range		**Compliance** EMC compliant
ANALOG INPUT	**Input Features** ▪ BNC connector ▪ Single ended, DC and 10 µs AC coupling hardware selectable ▪ Impedance: 1 kΩ ▪ Positive and negative signals accepted ▪ Analog Coarse Gain: x1, x2, x4, x8 software selectable (Gain 1 = 1 V_{pp}); gain attenuation x0.2 by on-board jumper ▪ Programmable DC offset adjustment on each input in the full-scale range		**Number of Inputs** 8
ADC	**Resolution** 14 bits		**Sampling Rate** 100 MS/s (simultaneously on each input)
DIGITAL SIGNAL PROCESSING	▪ Trapezoidal filter for the energy calculation: adjustable rise time 0.02 to 40 µs; flat top 0.02 to 40 µs ▪ Trigger and Timing filter based on integrative-derivative component (30-bit time stamp, 10 ns resolution, 10 s range, 64-bit extension by software, roll-over tracking event) ▪ Trigger threshold adjustment ▪ Digital fine gain: 1 to 2.2 in steps of 0.0001 ▪ Trapezoid tail correction; decay time 0.1 to 650 µs ▪ Trigger time tag discrimination by RC-CR^2 filter; shaping time 0.01 to 2.4 µs ▪ Trigger hold-off (imposed dead-time) to prevent after pulses: 0 to 40 µs ▪ Programmable Pile-up Guard duration: 0 to 80 µs beyond the end of the flat top ▪ Baseline restorer: fast, medium, slow		
OPERATING MODES	▪ Pulse Height Analysis (PHA): 1k-2k-4k-8k-16k-32k pulse height histogram built at software level ▪ List mode: pulse height and time stamp for each event ▪ Oscilloscope mode: signal inspection of input pulses and internal filters outputs		
TRIGGER MODES	▪ Uncorrelated: each channel operates independently (based on channel self-trigger) ▪ Correlated: coincidence/anticoincidence among channels and/or an external trigger (TRG-IN) ▪ External: channels are triggered by external trigger only (TRG-IN)		
FRONT PANEL I/Os	**CLK-IN** **(3-pin AMPMODU II)** AC-coupled differential clock input LVDS, ECL, PECL, LVPECL, CML (single-ended NIM/TTL adaptor orderable) Jitter<100ppm requested **CLK-OUT** **(3-pin AMPMODU II)** AC-coupled differential clock output	**TRG-IN (LEMO)** General purpose single-ended digital input Software programmable functions NIM/TTL, Z_{in} = 50 Ω **TRG-OUT (LEMO)** General Purpose Digital output Software programmable functions NIM/ TTL, Zin = 50 Ω	**S-IN (LEMO)** TTTReset/AcqStartStop digital Input NIM/TTL, Z_{in} = 50 Ω **LVDS I/O** **(32-pin AMPMODU II)** 16 general purpose differential LVDS I/O An input pattern from the LVDS I/O can be associated to each trigger as an event marker Multiple functions configurable by register
ANALOG MONITOR OUPTUT	12-bit / 100MHz DAC FPGA controlled 1 V_{pp} dynamics, 50 Ω termination Configurable for test signals		
COMMUNICATION INTERFACE	**Optical Link** CAEN CONET proprietary protocol Up to 80 MB/s transfer rate Daisy chain capability by connecting up to 8 or 32 ADC modules to a single Optical Link Controller (A2818 or A3818 respectively)	**VME** VME 64X compliant interface Data transfer mode: BLT32, MBLT64 (70 MB/s using CAEN Bridge) CBLT32/64, 2eVME, 2eSST (up to 200 MB/s)	
FIRMWARE	DPP-PHA firmware can be upgraded via VMEbus/Optical Link		
SOFTWARE	Fully controlled by MC² Analyzer and CoMPASS spectroscopy software (up to 16k PHA histogram supported) General purpose C libraries with demo samples available for developers Windows® and Linux® OS supported		
CONSUMPTIONS	5.6 A @ +5V; 0.320 A @ +12 V; 0.180 A @ -12V		

Tab. 2.1: Specifications Table

3 Packaging and Compliancy

V1782 module is 2-unit wide, 6U VME64 board, EMC compliant.

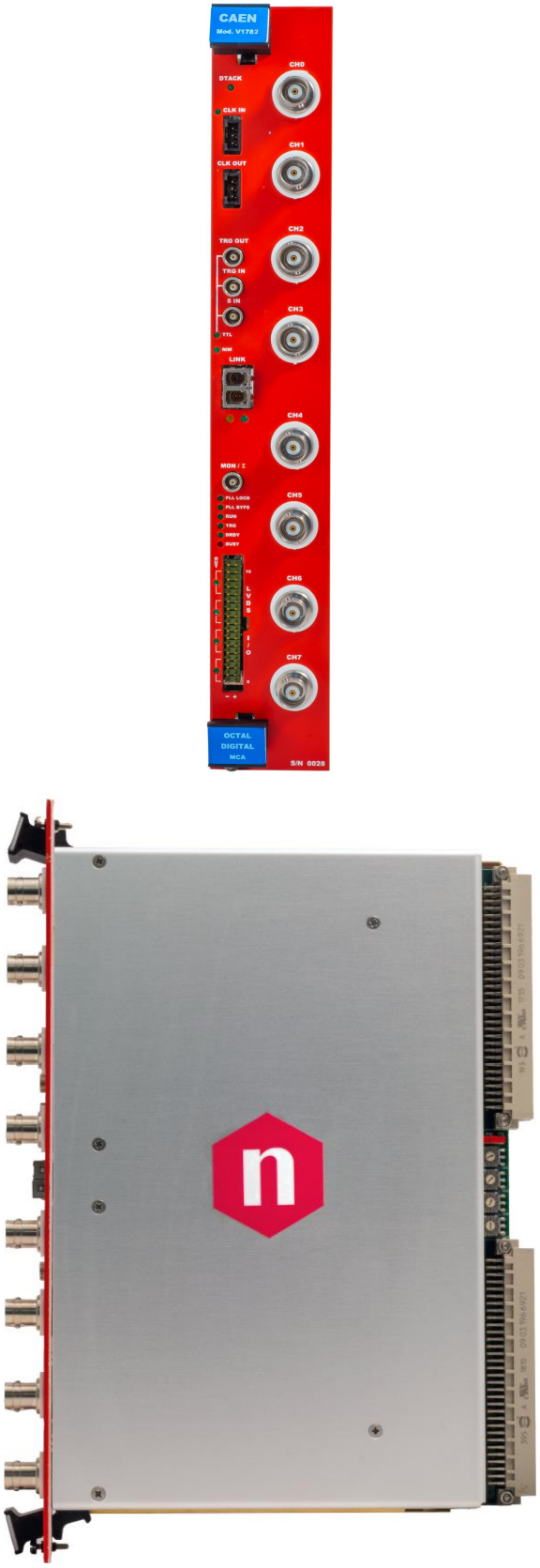


Fig. 3.1: Model view

CAUTION: to manage the product, consult the operating instructions provided.

A POTENTIAL RISK EXISTS IF THE OPERATING INSTRUCTIONS ARE NOT FOLLOWED!

CAUTION: this product needs proper cooling.

USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEATING THE BOARD MAY DEGRADE ITS PERFORMANCES!

CAUTION: this product needs proper handling.

V1782 DO NOT SUPPORT LIVE INSERTION (HOT SWAP)!

REMOVE OR INSERT THE BOARD WHEN THE VME CRATE IS POWERED OFF!

ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE!

CAEN provides the specific document "Precautions for Handling, Storage and Installation", available in the documentation tab of the product's web page, that the user is mandatory to read before to operate with CAEN equipment.

4 Power Requirements

The V1782 power consumptions per relevant supply voltage are shown in the table below.

SUPPLY VOLTAGE (Typ. ± 10%)		
+5V	+12V	-12V
5.6 A	0.320 A	0.180 A

Tab. 4.1: Power requirements table

Note: the values in **Tab. 4.1** refer to measures conducted on PCB rev. 4, at T = 21 °C, with floating I/O connectors, maximum FSR = 1 V_{pp}, DC coupling and Gain x1 for the input channels, other settings at their default value at power-on.

5 Panel Description

Fig. 5.1: Panel view

CH [i]

DESCRIPTION

Analog input connector (i = 0 to 7).

FUNCTION

Receives the analog signal from the detector.

ELECTRICAL SPECS

Input dynamics:

x1, x2, x4 x8 sw programmable coarse gain (x1 = 1 V_{pp}); x0.2 attenuation by on-board jumper (Chap. **6**).

Z_{in}: 1 kΩ.

MECHANICAL SPECS

Series: BNC connectors.

Type: R 141 557 000W.

Manufacturer: RADIALL.

CLK IN

DESCRIPTION

Input and output clock connectors.

FUNCTION

CLK-IN permits locking to an external clock reference.

CLK-OUT permits propagating the clock externally.

CLK-IN and CLK-OUT permit the Daisy chain of the clock signal in multi-board synchronization.

ELECTRICAL SPECS

Signal type:

differential (LVDS, ECL, PECL, VPECL, CML).

NOTE: single-ended-to-differential A318 cable adapter available (see **Tab. 1.1**).

Coupling: AC.

Z_{diff}: 100 Ω.

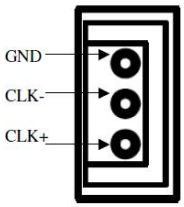
MECHANICAL SPECS

Series: MODU II connectors.

Type: 3-102203-4 (3-pin).

Manufacturer: AMP Inc.

PINOUT



CLK IN LED (GREEN): lights on if the external clock is enabled.

TRG OUT / TRG IN / S IN

DESCRIPTION

General purpose, software programmable, digital inputs/outputs.

FUNCTION

TRG-OUT

Reference registers 0x811C, 0x8110. Configurable as:

- Trigger output;
- Test logic level output;
- Motherboard probes output (Run/DelayedRun, ClockOut, ClockPhase, Busy/Unlock);
- Daughterboard probes output;
- S-IN signal propagation.

TRG-IN

Reference registers 0x811C, 0x8100. Configurable as:

- External trigger input;
- Acquisition Start;
- Acquisition Veto.

S-IN

Reference register 0x811C,

Configurable as:

- Reset of the time stamp counter;
- Synchronized Start/Stop acquisition.

ELECTRICAL SPECS

Signal level: NIM or TTL.

Z_{in} (TRG-IN/S-IN): 50 Ω.

TRG-OUT requires 50 Ω termination.

MECHANICAL SPECS

Series: 101 A 004 connectors.

Type: DLP 101 A 004-28.

Manufacturer: FISCHER.

Alternatively:

Type: EPL 00 250 NTN.

Manufacturer: LEMO.

TTL / NIM LEDs (GREEN): indicate the standard TTL or NIM set for TRG-OUT, TRG-IN, and S-IN (register 0x8110)**.**

OPTICAL LINK PORT

DESCRIPTION

Optical link communication port; transfer rate up to 80 MB/s.

FUNCTION

Data readout and flow control; Daisy chainable; compliant to Multimode 62.5/125 µm cable featuring LC connectors on both sides.

ELECTRICAL SPECS

N.A.

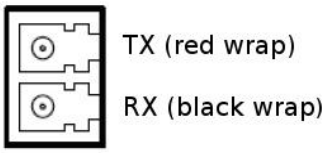
MECHANICAL SPECS

Series: SFF Transceivers.

Type: FTLF8519F-2KNL (LC connectors).

Manufacturer: FINISAR.

PINOUT



LINK LEDs (GREEN/YELOW): right GREEN indicates the network presence, left YELLOW signals the data transfer activity

MON / Σ

DESCRIPTION

Analog output connector from a 12-bit (100 MHz) internal DAC driven by the FPGA.

FUNCTION

Contact CAEN for information (Chap. **18**)

ELECTRICAL SPECS

Input dynamics: 1 V_{pp}.

Requires 50 Ω termination.

MECHANICAL SPECS

Series: 101 A 004 connectors.

Type: DLP 101 A 004-28.

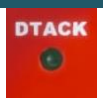
Manufacturer: FISCHER.

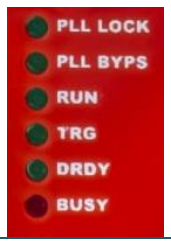
Alternatively:

Type: EPL 00 250 NTN.

Manufacturer: LEMO.

DIAGNOSTIC LEDs





DTACK (GREEN): indicates there is a VME read/write access to the board;

PLL LOCK (GREEN): indicates PLL is locked to the reference clock;

PLL BYPS (GREEN): *not used*;

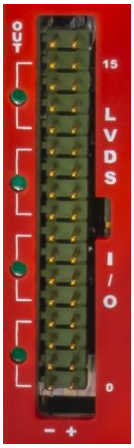
RUN (GREEN): indicates the acquisition is running (data taking);

TRG (GREEN): indicates the trigger is accepted;

DRDY (GREEN): indicates the event/data is present in the output buffer;

BUSY (RED): indicates all the memory aggregates are full for at least one channel.

SPARE LINK



DESCRIPTION

16-signal general purpose LVDS I/O connector, independently programmable by 4-signal groups as input or output and by function (see Chap. **9**)

FUNCTION

Default: a 16-bit pattern can be latched on the LVDS I/Os as the trigger arrives **[RD7]**.

Configurable as:

- LVDS I/O register (r/w logical level)
- Trigger in/out (individual self-triggers)
- Busy, Veto and Run in/out (sync.)
- Time Stamp Reset, Data Ready, Memory Full

MECHANICAL SPECS

Series: TE - AMPMODU Mod II Series.

Type: 5-826634-0 34-pin (lead spacing: 2.54 mm; row pitch: 2.54 mm).

Manufacturer: AMP Inc.

IDENTIFICATION

LABELS

Blue labels on top and bottom handles report the model description.

SERIAL NUMBER

4-digit serial number is positioned at bottom right of the panel.

6 Internal Components

If required to access the internal component, the metal plate covering the V1782 piggybacks must be removed by unskrewing the six countersunk Phillips screws.

VME Base Address, Clock Selection and Firmware Selection

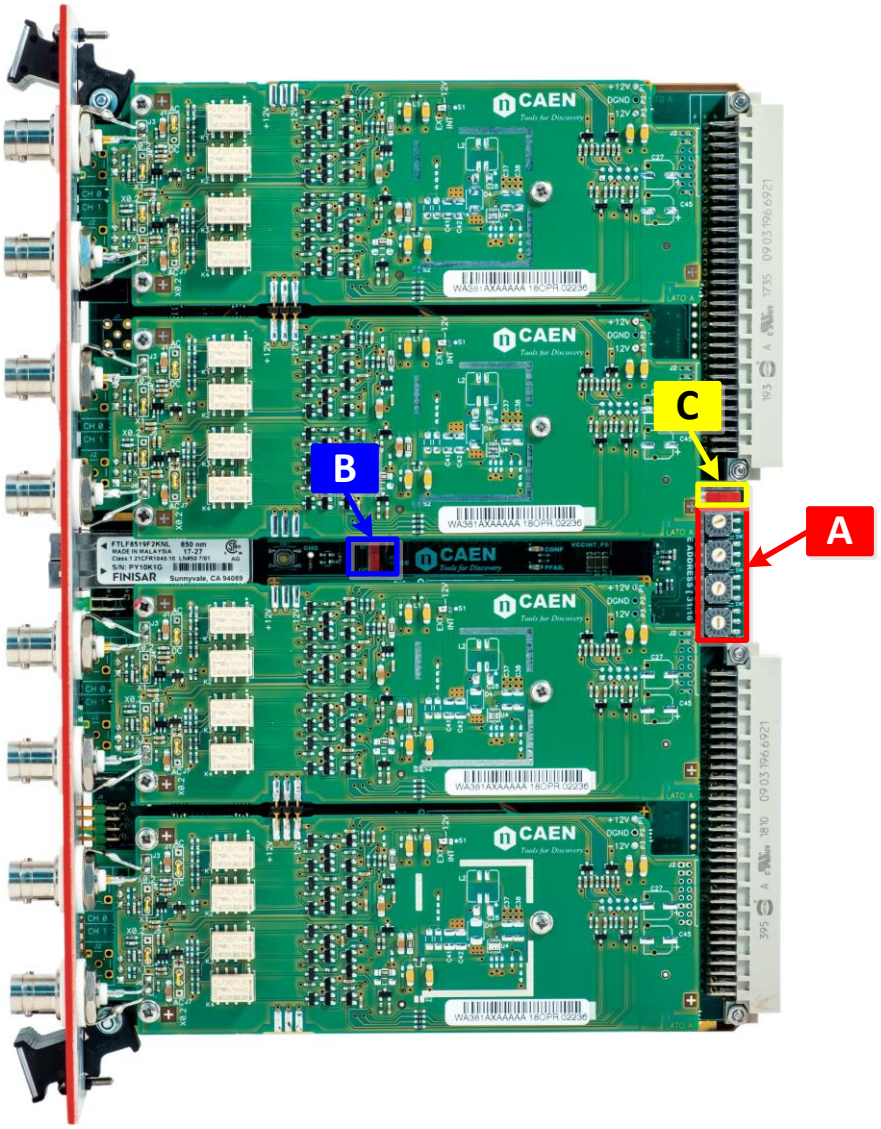


Fig. 6.1: Rotary and dip switches location

A	SW3,4,5,6: ”Base Address [31:16]”	Type: Rotary Switches	Function: Set the 16-bit MSB of the 32-bit VME Base Address of the module (LSB is 0000)
B	SW2: “CLOCK SOURCE” INT/EXT	Type: Dip Switch	Function: Selects the clock source (external or internal)
C	SW7: ”FW” BKP/STD	Type: Dip Switch	Function: Selects ”Standard” (STD) or ”Backup” (BKP) FLASH page as the first to be read at power-on to load the stored FW copy on the FPGAs (default position is STD). See Chap. **17**.

AC/DC Coupling and Coarse Gain

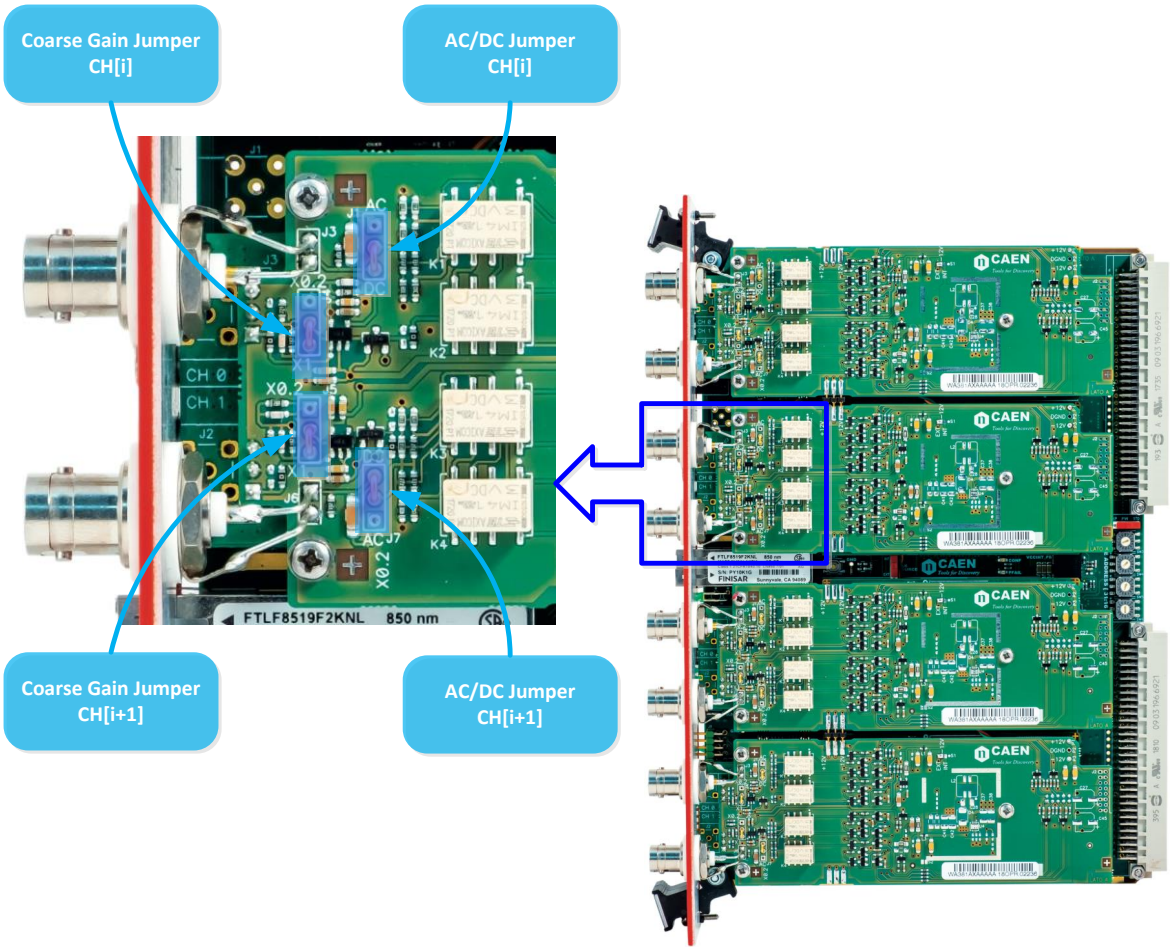


Fig. 6.2: Jumpers location

AC COUPLING	DC COUPLING	X1 SCALE	X0.2 SCALE
AC DC	AC DC	X0.2 X1	X0.2 X1
For fitting to signals from TRP	For fitting to signals from RSP	x1 / x2 / x4 / x8 coarse gain options by software (x1 = 1 V_{pp})	x1 / x2 / x4 / x8 coarse gain options by software

7 Acquisition Run/Stop

The acquisition can be started and stopped in different ways, according to bit[2:0] of register 0x8100:

- SW CONTROLLED (bit[1:0] = 00): Start and Stop take place by software command. Bit[2] = 0 means stopped, while bit[2] = 1 means running.
- S-IN CONTROLLED (bit[1:0] = 01): bit[2] = 1 arms the acquisition and the Start is issued as the S-IN signal is set high and the Stop occurs when it is set low. If bit[2] = 0 (disarmed), the acquisition is always off.
- FIRST TRIGGER CONTROLLED (bit[1:0] = 10): bit[2] = 1 arms the acquisition and the Start is issued on the first trigger pulse (rising edge) on the TRG-IN connector. This pulse is not used as a trigger; actual triggers start from the second pulse on TRG-IN. The Stop acquisition must be SW controlled (i.e. reset of bit[2]).
- LVDS I/Os CONTROLLED: this mode acts like the S-IN CONTROLLED (bit[1:0] = 01), but using the configurable features of the signals on the LVDS I/Os connector (see Chap. **9**).

8 Multi-board Synchronization

When multi-board systems are involved in an experiment, it is necessary to synchronize different boards.

In this way, the user can acquire from N boards with Y channel each, like if they were just one board with (N x Y) channels.

The main issue synchronizing a multi-board system is to propagate the sampling clock among the boards. This is made through input/output daisy chain connections among the digitizers. One board must be chosen to be the “master” board that propagates its own clock to the others. A programmable phase shift can adjust possible delays in the clock propagtion. This allows to have both the ADC sampling clock and the time reference in common for all boards. Having the same time reference means that the acquisition starts/stops at the same time, and that the time stamps of different boards are aligned to the same absolute time.

There are several ways to implement the trigger logic. The synchronization tool allows to propagate the trigger to all boards and acquire the events accordingly. Moreover, in case of busy state of one or more boards, the acquisition is inhibited for all boards.

Please, contact CAEN for detailed information about V1782 synchronization (see Chap. **18**).

9 Front Panel LVDS I/Os

The V1782 is provided with 16 general purpose programmable LVDS I/O signals (see Chap. **5**). These signals can be programmed in terms of direction (INPUT/OUTPUT) and function by groups of 4.

BIT[8] OF 0x811C REGISTER MUST BE 1 TO ENABLE THE LVDS I/Os CONFIGURATION MODES

The direction of the signals is then set by bit[5:2] of 0x811C register:

Bit[2] → LVDS I/O[3:0];

Bit[3] → LVDS I/O[7:4];

Bit[4] → LVDS I/O[11:8];

Bit[5] → LVDS I/O[15:12];

Setting at 0 enables the relevant signals in the group as INPUT, while 1 enables them as OUTPUT.

The default status of the LVDS I/O is bit[8] = 0 of 0x811C, and default signals are listed in **Tab. 9.1**.

Nr.	Direction	Function	Description
0	out	Ch 0 self-trigger	The over-threshold information from the relevant channel
1	out	Ch 1 self-trigger	
2	out	Ch 2 self-trigger	
3	out	Ch 3 self-trigger	
4	out	Ch 4 self-trigger	
5	out	Ch 5 self-trigger	
6	out	Ch 6 self-trigger	
7	out	Ch 7 self-trigger	
8	out	Memory Full	Memory full flag
9	out	Event Data Ready	Board event data ready flag
10	out	Channels Trigger	OR of the new-event-to-be-read signal
11	out	RUN Status	Board run flag
12	in	Trigger Time Tag Reset (active low)	Reset of the trigger time tag counter
13	in	Memory Clear (active low)	Clear command of all channel memories
14	-	reserved	N.A.
15	-	reserved	N.A.

Tab. 9.1: Front Panel LVDS I/Os default signals

When bit[8] = 1, each group of 4 signals of the LVDS I/O 16-pin connector can be configured in one of the 4 following modes (according to bit[15:0] of 0x81A0):

- Mode 0 (bit[n+3:n] = 0000): REGISTER
- Mode 1 (bit[n+3:n] = 0001): TRIGGER
- Mode 2 (bit[n+3:n] = 0010): nBUSY/nVETO
- Mode 3 (bit[n+3:n] = 0011): LEGACY

where n = 0, 4, 8, 12.

Note: whatever option is set, the LVDS I/Os are always latched with the trigger and the relevant status of the 16 signals is always written into the header PATTERN field **[RD7]**; the user can then choose to read it out or not.

GROUP	REGISTER	TRIGGER	nBUSY/nVETO	LEGACY
LVDS IN [15:12]	Reg[15:12]	TrigIn_Ch[7:4]	15: nRunIn 14: nTriggerIn 13: nVetoIn 12: nBusyIn	15: reserved 14: reserved 13: reserved 12: nClear_TTT
LVDS IN [11:8]	Reg[11:8]	TrigIn _Ch[3:0]	11: nRunIn 10: nTriggerIn 9: nVetoIn 8: nBusyIn	11: reserved 10: reserved 9: reserved 8: nClear_TTT
LVDS IN [7:4]	Reg[7:4]	TrigIn _Ch[7:4]	7: nRunIn 6: nTriggerIn 5: nVetoIn 4: nBusyIn	7: reserved 6: reserved 5: reserved 4: nClear_TTT
LVDS IN [3:0]	Reg[3:0]	TrigIn _Ch[3:0]	3: nRunIn 2: nTriggerIn 1: nVetoIn 0: nBusyIn	3: reserved 2: reserved 1: reserved 0: nClear_TTT

Tab. 9.2: Features description when LVDS group is configured as INPUT

GROUP	REGISTER	TRIGGER	nBUSY/nVETO	LEGACY
LVDS OUT [15:12]	Reg[15:12]	TrigOut_Ch[7:4]	15: nRun 14: nTrigger 13: nVeto 12: nBusy	15: Run 14: Trigger 13: DataReady 12: Busy
LVDS OUT [11:8]	Reg[11:8]	TrigOut_Ch[3:0]	11: nRun 10: nTrigger 9: nVeto 8: nBusy	11: Run 10: Trigger 9: DataReady 8: Busy
LVDS OUT [7:4]	Reg[7:4]	TrigOut_Ch[7:4]	7: nRun 6: nTrigger 5: nVeto 4: nBusy	7: Run 6: Trigger 5: DataReady 4: Busy
LVDS OUT [3:0]	Reg[3:0]	TrigOut_Ch[3:0]	3: nRun 2: nTrigger 1: nVeto 0: nBusy	3: Run 2: Trigger 1: DataReady 0: Busy

Tab. 9.3: Features description when LVDS group is configured as OUTPUT

Mode 0: REGISTER

Direction is INPUT: the logic level of the LVDS I/O signals can be read at register address 0x8118.

Direction is OUTPUT: the logic level of the LVDS I/O signals can be written at register address 0x8118.

Mode 1: TRIGGER

Direction is INPUT: the TrigIn_Ch[(n + 3) : n] signals (n = 0, 4) can be used as triggers according to the registers 0x810C and 0x8180.

Direction is OUTPUT: the TrgOut_Ch[(n + 3) : n] signals (n = 0, 4) consist of the channel self-triggers coming directly from the mezzanines.

Mode 2: nBUSY/nVETO

nBusy Signal

nBusyIn (INPUT) is an active low signal which, if enabled, is used to generate the nBusy signal (OUTPUT) as below.

The Busy signal (fed out on LVDS I/Os or TRG-OUT LEMO connector) is:

Almost_Full OR **(LVDS_BusyIn** AND **BusyIn_enable)**

Where

- Almost_Full indicates the filling of the Buffer Memory up to a programmable level (12-bit range) set at register address 0x816C;
- LVDS_BusyIn is available in nBUSY/nVETO configuration (see **Tab. 9.2**);
- BusyIn_enable is set by bit[8] of 0x8100.

nVETO Signal

Direction is INPUT: nVETOIn is an active low signal which, if enabled (register address 0x8100, bit[9] = 1), is used to veto the generation of the common trigger propagated to the channels for the event acquisition.

Direction is OUTPUT: the nVETO signal is the copy of nVETOIn.

nTrigger Signal

Direction is INPUT: nTriggerIn is an active low signal which, if enabled, is a real trigger able to cause the event acquisition. It can be propagated to TRG-OUT LEMO connector or to the individual triggers.

Direction is OUTPUT: nTrigger signal is the copy of the trigger signal propagated to the TRG-OUT LEMO connector or copy of the acquisiton common trigger. This is selected by bit[16] of 0x81A0.

nRun Signal

Direction is INPUT: nRunIn is an active low signal which can be used as Start for the digitizer (register address 0x8100, bit[1:0] = 11). It is possible to program the Start on the level or on the edge of the nRunIn signal (register address 0x8100, bit[11]).

Direction is OUTPUT: nRun signal is the inverse of the internal Run of the board.

Mode 3: LEGACY

nClear_TTT Signal

It is the only signal available as INPUT. It is the reset of the Trigger Time Tag counter.

Busy Signal

The Busy signal is active high, and it is exactly the inverse of the nBusy signal (see Sec. **Mode 2: nBUSY/nVETO**).

In case register address 0x816C is set to 0x0, and the BusyIn signal is disabled, the Busy is the FULL signal.

DataReady Signal

The DataReady is an active high signal indicating that the board has data available for readout (the same as the DataReady front panel LED does).

Trigger Signal

The active high Trigger signal is the copy of the acquisition trigger (common trigger) sent from the motherboard to the mezzanines (it is neither the signal provided out on the TRG-OUT LEMO connector nor the inverse of the signal sent to the LVDS connector).

Run Signal

The Run signal is active high and represents the inverse of the nRun signal (see Sec. **Mode 2: nBUSY/nVETO**).

10 Reset, Clear and Default Configuration

Global Reset

Global Reset is performed at the power-on of the module or via software by write access at register address 0xEF24. It allows to clear the data off the Output Buffer, the event counter and performs a FPGAs global reset which restores the FPGAs to the default configuration. It initializes all counters to their initial state and clears all detected error conditions.

Memory Reset

The Memory Reset clears the data off the Output Buffer.

The Memory Reset can be forwarded via a write access at register address 0xEF28. In the default LVDS I/O configuration, it is also possible to perform a memory clear by sending a pulse to the front panel dedicated Memory Clear input (see **Tab. 9.1**).

Timer Reset

The Timer Reset allows to initialize the timer which tags an event. The Timer Reset can be forwarded with a pulse sent either to the LVDS I/O dedicated input (see **Tab. 9.1** and Sec. **Mode 3: LEGACY**) or to the S-IN input (leading edge sensitive).

11 VMEbus Interface

The module is provided with a fully compliant VME64/VME64X interface, whose main features are:

- EUROCARD 9U Format
- J1/P1 and J2/P2 with either 160 pins (5 rows) or 96 (3 rows) connectors
- A24, A32 and CR-CSR address modes
- D32, BLT/MBLT, 2eVME, 2eSST data modes
- MCST write capability
- CBLT data transfers
- RORA interrupter
- Configuration ROM

Addressing Capabilities

- Base address: the module works in A24/A32 mode The Base Address of the module is selected through four rotary switches (see **Fig. 6.1**), then it is validated only with either a power-ON cycle or a System Reset (see Chap. **10**).

ADDRESS MODE	ADDRESS RANGE	NOTES
A24	[0x000000:0xFF0000]	SW2 and SW3 ignored

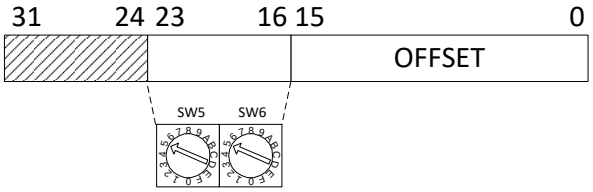


Fig. 11.1: A24 addressing

ADDRESS MODE	ADDRESS RANGE	NOTES
A32	[0x00000000:0xFFFF0000]	

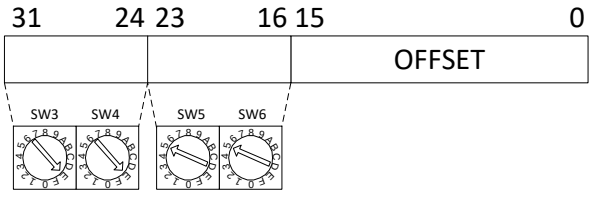


Fig. 11.2: A23 addressing

- CR/CSR address: the addressing is based on the slot number taken from the relevant backplane lines. The recognised Address Modifier for this cycle is 2F. *This feature is implemented only on versions with 160-pin connectors.*

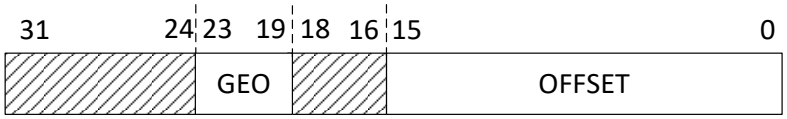


Fig. 11.3: CR/CSR addressing

Address Relocation

Bit[15:0] of 0xEF10 allow to set via software the board Base Address (valid values ≠ 0). Such register allows to overwrite the rotary switches settings; this setting must be enabled via bit[6] of 0xEF00.

The used addresses are shown in **Fig. 11.4**.

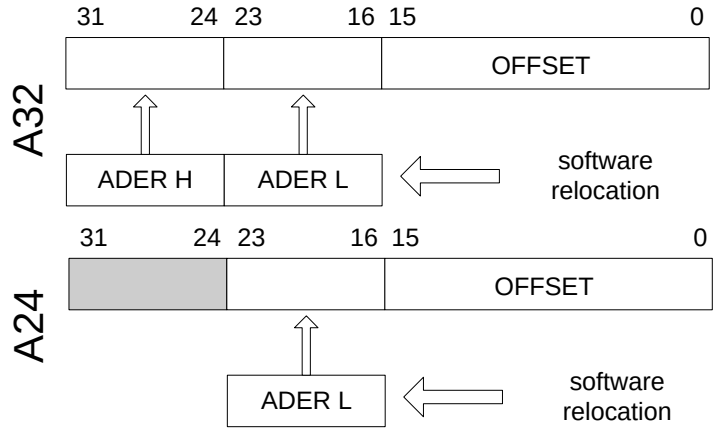


Fig. 11.4: Software relocation of the base address

12 Data Transfer Capabilities and Events Readout

The board features a Multi-Event digital memory per channel, which is divided into a programmable number of buffers (also called “aggregates”), where each buffer contains a programmable number of events. Once they are written in the memory, the events become available for readout via VMEbus or Optical Link. During the memory readout, the board can store other events (independently from the readout) on the available free buffers (aggregates).

Refer to the Appendix B **[RD7]** for a detailed description of the memory organization.

The board supports D32 single data readout, Block Transfer BLT32 and MBLT64, 2eVME and 2eSST cycles. Sustained readout rate is up to 60 MB/s with MBLT64, up to 100 MB/s with 2eVME and up to 160 MB/s with 2eSST.

Block Transfer D32/D64, 2eVME, and 2eSST

The Block Transfer readout mode allows to read N complete aggregates sequentially, where N is set at register address 0xEF1C, or by using the SetMaxNumAggregatesBLT function of the CAENDigitizer library **[RD3]**.

When developing programs, the readout process can be implemented on different basis:

- Using Interrupts: as soon as the programmed number of events is available for readout, the board sends an interrupt to the PC over the optical communication link (not supported by USB).
- Using Polling (interrupts disabled): by performing periodic read accesses to a specific register of the board it is possible to know the number of events present in the board and perform a BLT read of the specific size to read them out.
- Using Continuous Read (interrupts disabled): continuous data read of the maximum allowed size (e.g. total memory size) is performed by the software without polling the board. The actual size of the block read is determined by the board that terminates the BLT access at the end of the data, according to the configuration of register address 0xEF1C, or the library function SetMaxNumAggregatesBLT mentioned above. If the board is empty, the BLT access is immediately terminated and the “Read Block” function will return 0 bytes (it is the ReadData function in the CAENDigitizer Library).

While reading out the events, it is suggested to enable BERR signal during BLT32 cycles, in order to end the cycle avoiding filler readout. The last BLT32 cycle will not be completed, it will be ended by BERR after the #N event in memory istransferred.

Since some 64-bit CPU cut off the last 32-bit word of a transferred block, if the number of words composing such block is odd, it is necessary to add a dummy word (which has then to be removed via software) in order to avoid data loss. This can be achieved by setting the ALIGN64 bit (bit[5]) of 0xEF00). MBLT64 cycle is like the BLT32 cycle, except that the address and data lines are multiplexed to form 64-bit address and data buses. The 2eVME allows to achieve higher transfer rates thanks to the requirement of only two edges of the two control signals (DS and DTACK) to complete a data cycle.

Chained Block Transfer D32/D64

The V1782 allows to readout events from more daisy chained boards (Chained Block Transfer mode). The technique which handles the CBLT is based on the passing of a token between the boards; it is necessary to verify that the used VME crate supports such cycles.

Several contiguous boards, in order to be Daisy chained, must be configured as “first”, “intermediate” or “last” via register address 0xEF0C. A common Base Address is then defined via the same register; when a BLT cycle is executed at the address CBLT_Base + 0x0000 ÷ 0x0FFC, the “first” board starts to transfer its data, driving DTACK properly; once the transfer is completed, the token is passed to the second board via the IACKIN-IACKOUT lines of the crate, and so on until the “last” board, which completes the data transfer and asserts BERR (which has to be enabled): the Master then ends the cycle and the slave boards are rearmed for a new acquisition.

If the size of the BLT cycle is smaller than the events size, the board which has the token waits for another BLT cycle to begin (from the point where the previous cycle has ended).

Single D32 Transfer

This mode allows the user to readout a word per time, from the first word of the first available event, followed by all the words until the end of the event, then the second event is transferred. The readout data structure is described in the *MC²Analyzer User Manual* **[RD7]**. It is suggested, after the 1st word is transferred, to check the EVENT SIZE information (0x814C) and then do as many cycles as necessary (EVENT SIZE -1) in order to read completely the event.

13 Optical Link Access

The board houses a daisy chainable Optical Link (communication path which uses optical fiber cables as physical transmission line) able to transfer data at 80 MB/s; therefore, it is possible to connect up to eight V1782 to a single Optical Link Controller by using the A2818 PCI card, or up to thirty-two V1782 by the A3818 PCIe card.

Detailed information on CAEN PCI/PCIe Controllers can be find on CAEN website (www.caen.it) at the optical controller page.

The parameters for read/write accesses via Optical Link are the same used by VME cycles (Address Modifier, Base Address, data Width, etc); wrong parameter settings cause Bus Error.

Bit[3] of 0xEF00 enables the module to broadcast an interrupt request on the Optical Link; the enabled Optical Link Controllers propagate the interrupt on the PCI bus when a request from the Optical Link is sensed. Interrupts can also be managed at the CAENDigitizer library level **[RD3]**.

VME and Optical Link accesses take place on independent paths and are handled by board internal controller, with VME having higher priority; anyway, it is better to avoid accessing the board via VME and Optical Link simultaneously.

14 Drivers & Libraries

Drivers

To interface with V1782, CAEN provides the drivers for the supported physical communication channels, and compliant with Windows® and Linux®:

- CONET Optical Link drivers are managed by the A2818 PCI / A3818 PCIe CAEN Controllers. The driver installation packages are downloadable for free on CAEN website at the A2818 or A3818 page respectively (login required).

Note: Refer to the User Manual of the specific Controller for installation instructions.

- USB 2.0 drivers are managed by the V1718 USB-to-VME Bridge. The installation packages is downloadable for free on CAEN website at the V1718 page (login required).

Note: Refer to the User Manual of CAEN Bridge for installation instructions.

Libraries

CAEN provides a set of C libraries, which may include demo and example codes, required by its software tool, and available for users who want to develop their own software applications:

- **CAENComm** library manages the communication at low level (read and write access) **[RD2]**. The purpose of the CAENComm is to implement a common interface to the higher software layers, masking the details of the physical channel and its protocol, thus making the libraries and applications that rely on the CAENComm independent from the physical layer. Moreover, the CAENComm requires the CAENVMELib library (access to the VME bus) even in the cases where the VME is not used.
- **CAENDigitizer** is a library of functions designed specifically for the Digitizer family **[RD3]**, which supports the DPP firmware. The CAENDigitizer library is based on the CAENComm library.
- **CAENDPP** is a high-level library of C functions designed to completely control exclusively CAEN boards running the DPP-PHA firmware.

Note: CAENDPP library is stand-alone, no additional library or software but the drivers are required to be installed.

Find the library installation packages on CAEN web site (www.caen.it) at the relevant library product page.

Currently, the CAENComm (and so the CAENDigitizer) supports the following communication interfaces (see also **Fig. 14.1**):

PC → USB → V1718 → VME → V1782

PC → PCI (A2818) → CONET → V1782

PC → PCI (A2818) → CONET → V2718 → VME → V1782

PC → PCIe (A3818) → CONET → V1782

PC → PCIe (A3818) → CONET → V2718 → VME → V1782

CONET (Chainable Optical NETwork) indicates the CAEN proprietary protocol for communication interface using Optical Link.

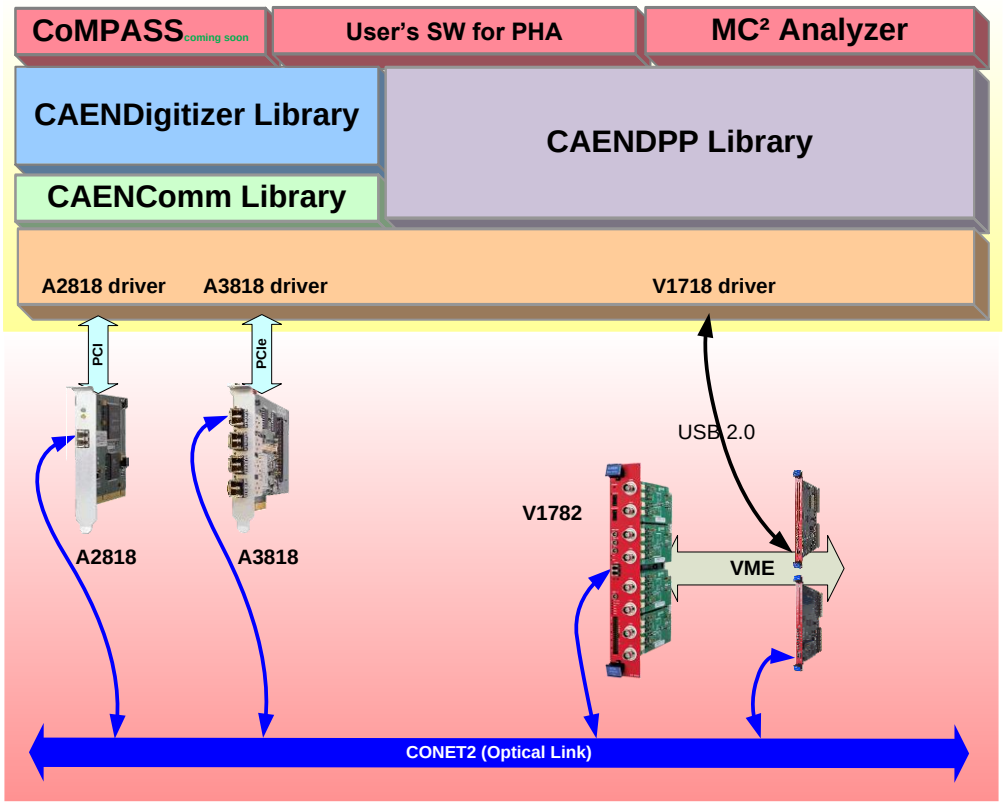


Fig. 14.1: Hardware and software layers scheme

15 Software

CAEN provides software tools and readout software to interface the V1782, which are available for free download on CAEN website (www.caen.it) from the V1782 page in the Download → Software area.

MC² Analyzer (MC²A) Readout Software

MC² Analyzer (MC²A) is a free software specifically designed for x780 Dual Digital MCA, x781 Dual/Quad/Octal Digital MCA or digitizers running the DPP-PHA (Digital Pulse Processing for the Pulse Height Analysis) firmware like 724 family.

The software completely controls and manages multiple boards acquiring data simultaneously, making therefore a multi-board system a "Multichannel - Multichannel Analyzer".

The user can set in the GUI all the relevant DPP-PHA parameters for each acquisition channel (trigger threshold, shaping parameters, etc.), handle the communication with the connected boards, run the data acquisition and plot both waveforms for on-line monitoring of the acquisition and histograms. The HV power supply channels can also be controlled, if they are supported by the board.

Moreover, MC² Analyzer performs basic mathematical analysis on both the ongoing histograms and collected spectra: ackground subtraction, peak fitting, energy calibration, ROI selection, dead time compensation, histogram re-bin and other features available.

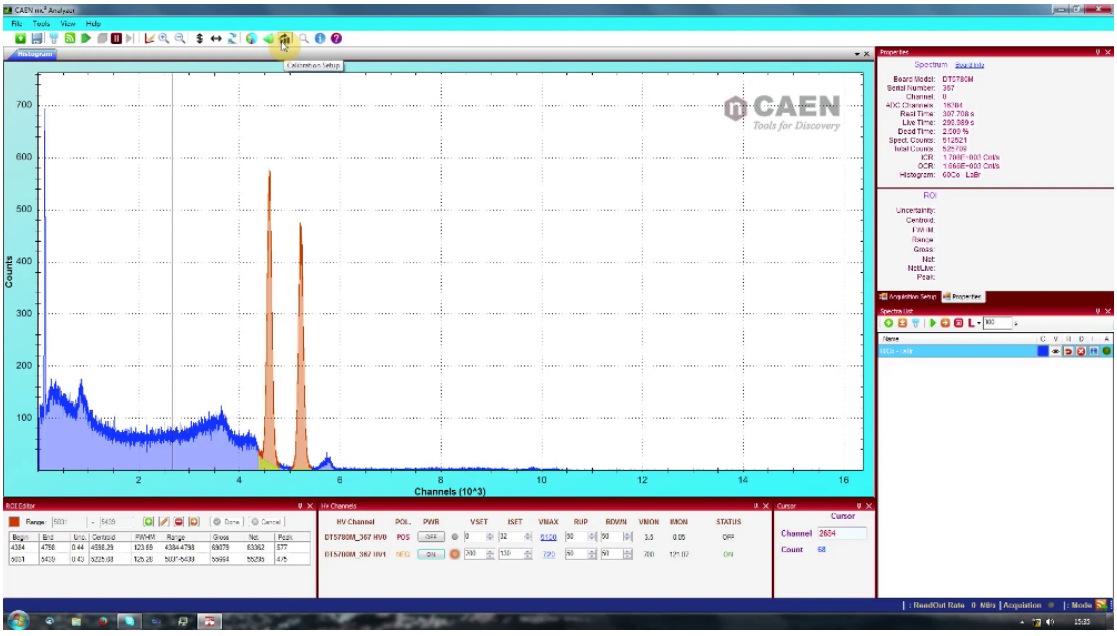


Fig. 15.1: MC² Analyzer (MC²A) readout software

MC² Analyzer runs on Microsoft Windows® platforms, 32 and 64-bit operating systems.

Refer to the *MC²Analyzer User Manual* for a complete software and firmware description, and to get start with MC²A [RD7].

Note: MC² Analyzer is stand-alone, the user needs to install only the driver for the communication link, while the software installs the DLLs of the required libraries locally in the destination directory.

CoMPASS

CAEN Multi-PArameter Spectroscopy Software (CoMPASS) is the free DAQ software from CAEN able to implement a Multiparametric Data Acquisition for Physics Applications: the detectors can be connected directly to the digitizers/MCAs inputs and the software acquires energy and timing spectra at the same time.

CoMPASS software has been designed as a user-friendly interface to manage the acquisition with all the CAEN DPP algorithms. It allows an easy setting of the acquisition parameters and to display up to six different plots and histograms at the same time.

CoMPASS can manage multiple boards and allows an easy synchronization of multi-board systems. Among the most important features, CoMPASS allows to implement event correlation between different channels (in hardware and/or software), apply energy and time selections, calculate and show the acquisition statistics (trigger rates, data throughput, percentage of discarded events due to the selections, etc.), perform a basic mathematical analysis of the recorded spectra (ROI selection, background subtraction, peak fitting, etc), save the output data files (raw data, lists, waveforms, spectra) and use the saved files to run offline with different processing parameters.

To the user familiar with the ROOT Analysis Framework, CoMPASS provides also the possibility of saving the output files (lists waveforms and spectra) in the ROOT TTree format for an easy post processing with user made analysis code.

CoMPASS supports the *Add-Back* mode with Clover detectors.

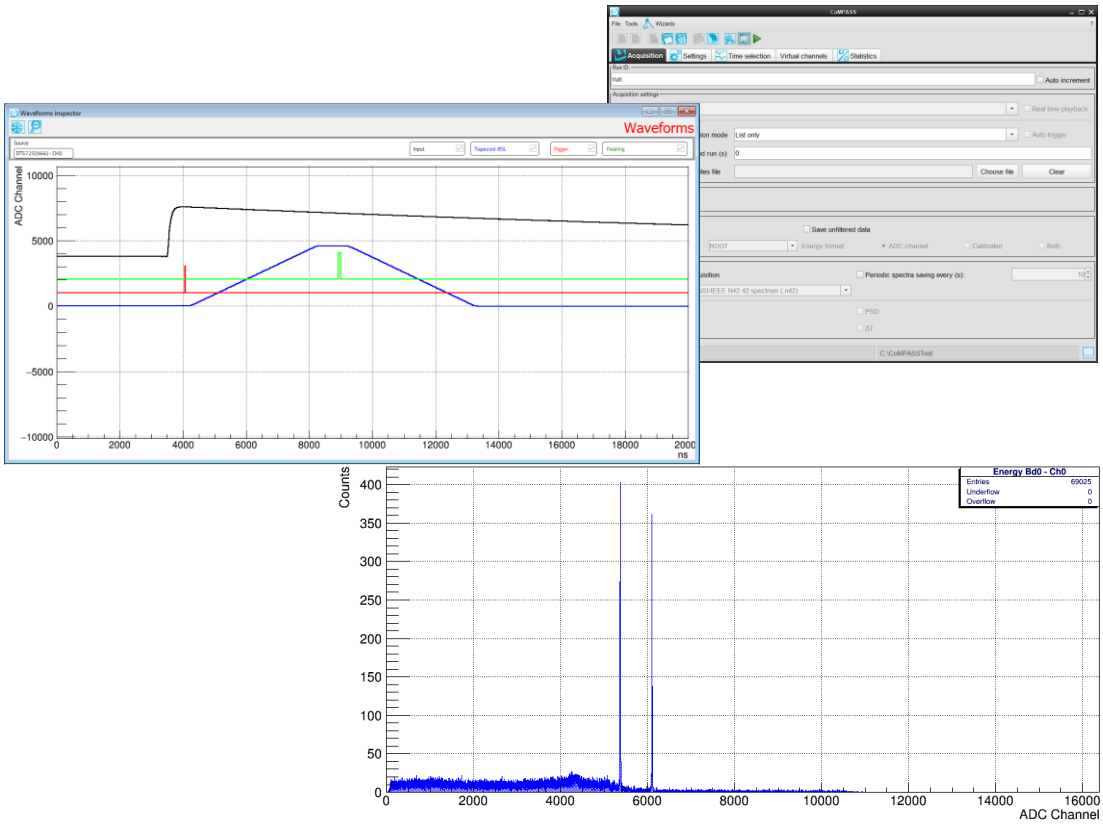


Fig. 15.2: CoMPASS readout software

CoMPASS runs on Windows® and Linux® platforms, 32 and 64-bit operation systems.

The software requires the third-party Oracle Java RE 8 or higher.

Refer to *CoMPASS User Manual* [RD8] and to *CoMPASS QuickStart Guide* [RD9] for installation instructions, software description and usage.

The support for V1782 has been implemented starting from CoMPASS release 1.2.0 on.

CAENUpgrader Software Tool

CAENUpgrader is a free software composed of command line tools together with a Java Graphical User Interface.

CAENUpgrader allows in few easy steps to:

- Upgrade the V1782 firmware
- Read the firmware release of V1782, and of the CAEN Controller or Bridge eventually used
- Upgrade the internal PLL (firmware file that can only be provided on demand by CAEN)
- Get the Board Info file, useful in case of support

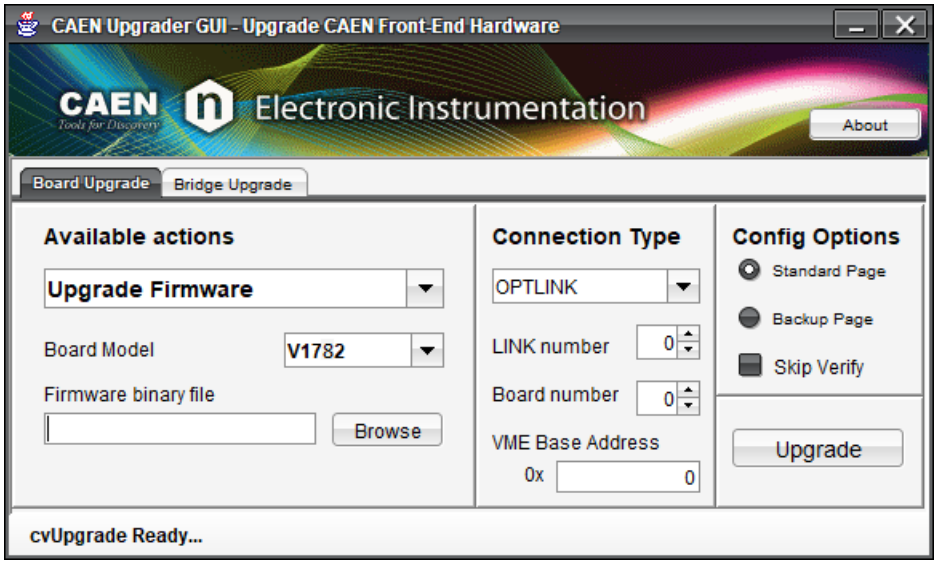


Fig. 15.3: CAENUpgrader Graphical User Interface

CAENUpgrader runs on Windows® and Linux® platforms, 32 and 64-bit operating systems.

The software requires the third-party Oracle Java RE 8 u40 or higher.

Refer to the *CAENUpgrader QuickStart Guide* [RD4] for installation instructions and software detailed description.

Note: the Windows® version of CAENUpgrader is stand-alone, the user needs to install only the driver for the communication link, while the software installs the DLLs of the required libraries locally in the destination directory., while the version for Linux needs the required libraries to be already installed apart by the user.

Note: the Linux® version of CAENUpgrader needs the required CAENVME and CAENCOMM libraries to be installed apart by the user

Note: V1782 is supported by CAENUpgrader rel. 1.6.4 or higher.

16 HW Installation

- The board fits into 6U VME crates.
- Use only crates with forced cooling air flow
- Turn the crate OFF before board insertion/removal
- Remove all cables connected to the front panel before board insertion/removal

CAUTION: this product needs proper cooling.

USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEATING THE BOARD MAY DEGRADE ITS PERFORMANCES!

CAUTION: this product needs proper handling.

V1782 DO NOT SUPPORT LIVE INSERTION (HOT SWAP)!

REMOVE OR INSERT THE BOARD WHEN THE VME CRATE IS POWERED OFF!

ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE!

Power-ON Sequence

To power on the board, perform the following steps:

1. Insert the V1782 into the crate;
2. power up the crate.

Power-ON Status

At Power-ON, the module is in the following status:

- the Output Buffer is cleared;
- registers are set to their default configuration values.

After Power-ON, only the **NIM** and **PLL LOCK** LEDs must stay ON (see **Fig. 16.1**)

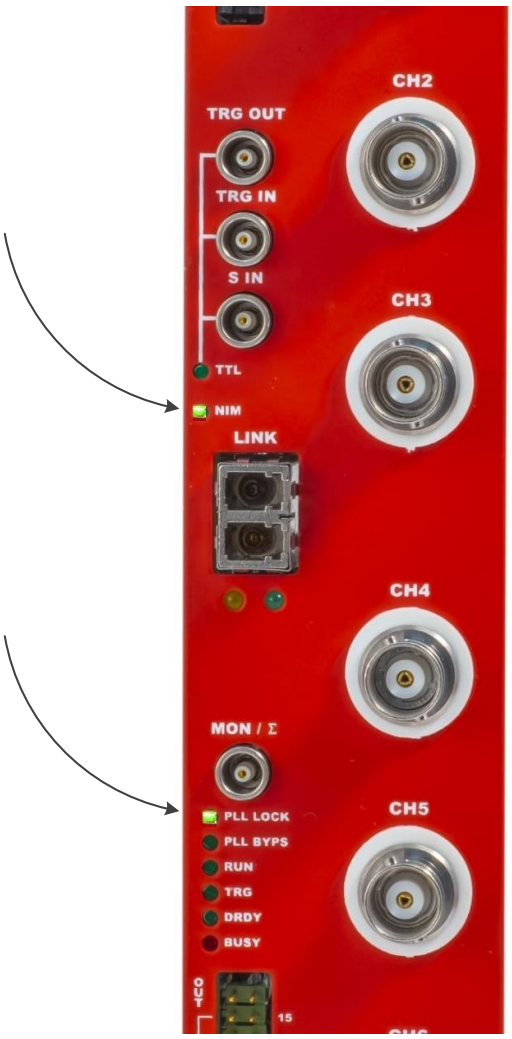


Fig. 16.1: Front panel LEDs status at power-ON

17 Firmware and Upgrades

The board hosts one FPGA on the mainboard (ROC FPGA) and two FPGAs per mezzanine (AMC FPGA), so that each AMC FPGA serves 2 channels. The AMC FPGA firmware is identical for all the mezzanines. A unique file is provided that will update all the FPGAs (ROC and AMC) at the same time.

ROC FPGA MAINBOARD FPGA (Readout Controller + VME interface):

FPGA Altera Cyclone EP1C20.

AMC FPGA CHANNEL FPGA (ADC readout/Memory Controller):

FPGA Altera Cyclone EP1C20

The firmware is stored onto on-board FLASH memory. Two copies of the firmware are stored in two different pages of the FLASH, referred to as Standard (STD) and Backup (BKP). At power-on, a microcontroller reads the FLASH memory and programs the module automatically loading the first working firmware copy, that is the STD one in normal operating.

The on-board dedicated SW7 dip switch, set on STD position by default, allows to select the first FLASH page to be read at power-on (see Chap. **6**).

The V1782 is delivered running a licensed version (i.e. not time-limited) of the DPP-PHA Firmware. This means that no license needs to be bought apart by the user when purchasing a V1782.

Firmware updates are available for download on CAEN web site (www.caen.it) at Download → Firmware in the V1782 web page **(login required)**.

Note: Upgrades of a DPP-PHA firmware file on the V1782 does not require further licensing.

It is possible to upgrade the board firmware via VMEbus or Optical Link by writing the FLASH with the CAENUpgrader software (see Chap. **15**)

IT IS STRONGLY SUGGESTED TO OPERATE THE DIGITIZER UPON THE STD COPY OF THE FIRMWARE. UPGRADES ARE SO RECOMMENDED ONLY ON THE STD PAGE OF THE FLASH. THE BKP COPY IS TO BE INTENDED ONLY FOR RECOVERY USAGE. IF BOTH PAGES RESULT CORRUPTED, THE USER WILL NO LONGER BE ABLE TO UPLOAD THE FIRMWARE VIA VMEbus OR OPTICAL LINK AGAIN AND THE BOARD NEEDS TO BE SENT TO CAEN FOR REPAIR!!

Firmware File Description

The DPP-PHA proggramming file has **CFA** extension (CAEN Firmware Archive), which is a sort of archive of DPP-PHA firmware files for a specific digitizer and/or MCA family.

The programming file name for the V1782 follows this general scheme:

x724_x781_x782_DPP-PHA_rev_X.Y_128.Z.CFA

where:

- x724_x781_x782 are all board supported by the CFA.
- DPP-PHA is the specific digital algorithm implemented into the firmware.
- X.Y is the major/minor revision number of the mainboard FPGA.
- 128.Z is the major/minor revision number of the channel FPGA; note that 128 is the major revision number fixed for the PHA algorithm of the supported boards.

Troubleshooting

In case of an upgrade failure (e.g. STD FLASH page is corrupted), the user can try to reboot the board: after a power cycle, the system programs the board automatically from the alternative FLASH page (e.g. BKP FLASH page), if this is not corrupted as well. The user can so perform a further upgrade attempt on the corrupted page to restore the firmware copy.

BECAUSE OF AN UPGRADE FAILURE, THE SW7 DIP SWITCH POSITION MAY NOT CORRESPOND TO THE FLASH PAGE FIRMWARE COPY LOADED ON THE BOARD FPGAs

If the procedures above described fails, it is recommended to send the board back to CAEN in repair (see Chap. **18**).

18 V1782 Use Case Example: Acquisition with Clover Detectors

This chapter shows the results of a measurement performed at IUAC (Delhi) on the INGA clover detectors with an ^{152}Eu source. The preamplifier outputs of one clover detector (4 crystals) are directly connected to the inputs 0-3 of the V1782. No shaping amplifier is used.
The V1782 is configured and read out by the digiTES[1] software, whose main settings for this test are listed in **Tab. 18.1** .

CoarseGain	x2 (0.5 Vpp dynamic range)
Coupling	DC
TrapRiseTime	8 µs
TrapFlatTop	1 µs
TrapPoleZero (decay Time)	52 µs
PeakingTime	0.6 µs
TrapNSBaseline	16386 samples

Tab. 18.1: digiTES settings

The digiTES reads the list of events from the V1782 (inputs 0-3) and makes the *Add-Back* in real time in the virtual input 8. Since the source is not located at the center of the detector, the ICR in the 4 crystals varies in the range from 500 cps to 1 Kcps; the rate in the *Add-Back* spectrum is 2.4 Kcps; the acquisition real time is about 240 s.
The energy spectra of the individual crystals and the *Add-Back* are shown in **Fig. 18.1**.

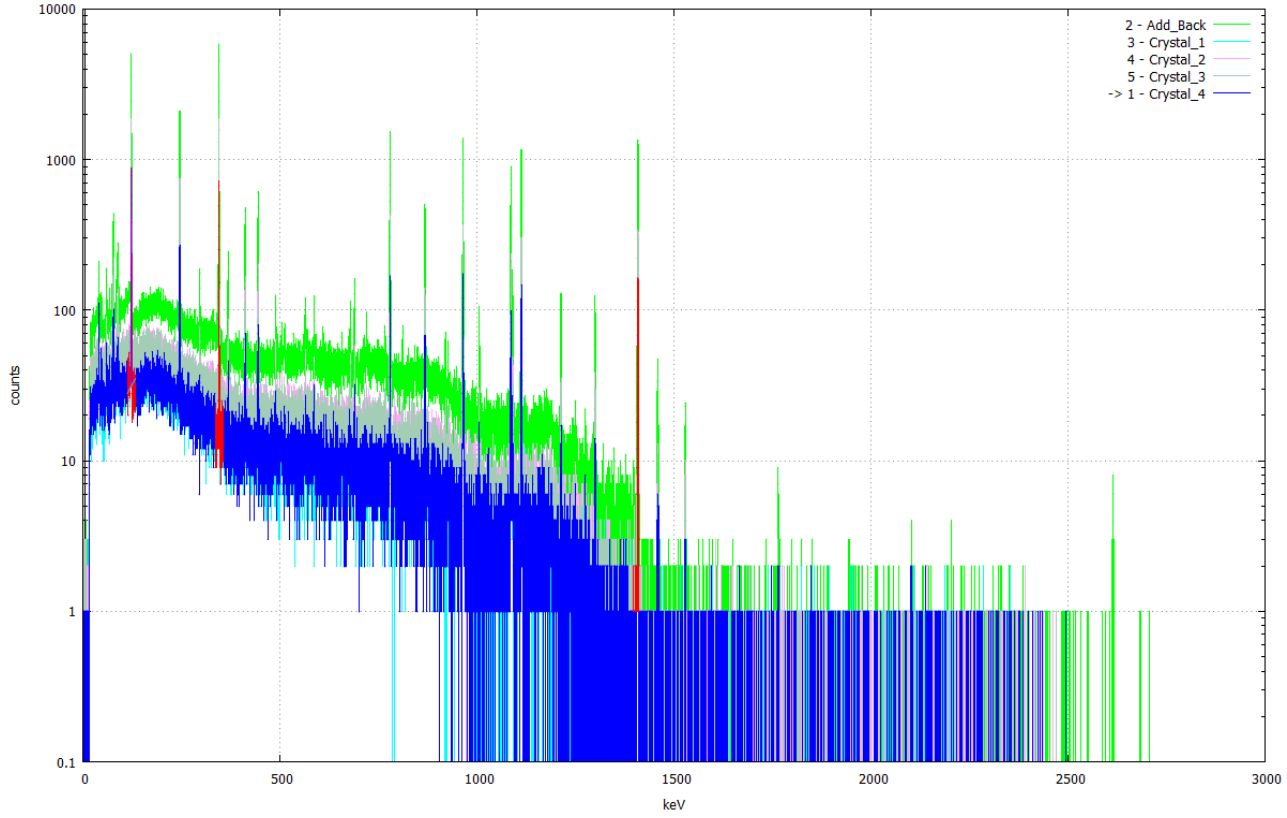


Fig. 18.1: Energy spectra of the individual crystals and *Add-Back*

[1] The digiTES software is a CAEN internal software, not officially available for the users, that has been selected for this test as the MC^{2}A software does not manage the *Add-Back* mode for Clover detectors. V1782 MCA and the *Add Back* mode will be supported by the coming soon CoMPASS software.

Fig. 18.2 shows the zoomed peaks @ 1408 keV.

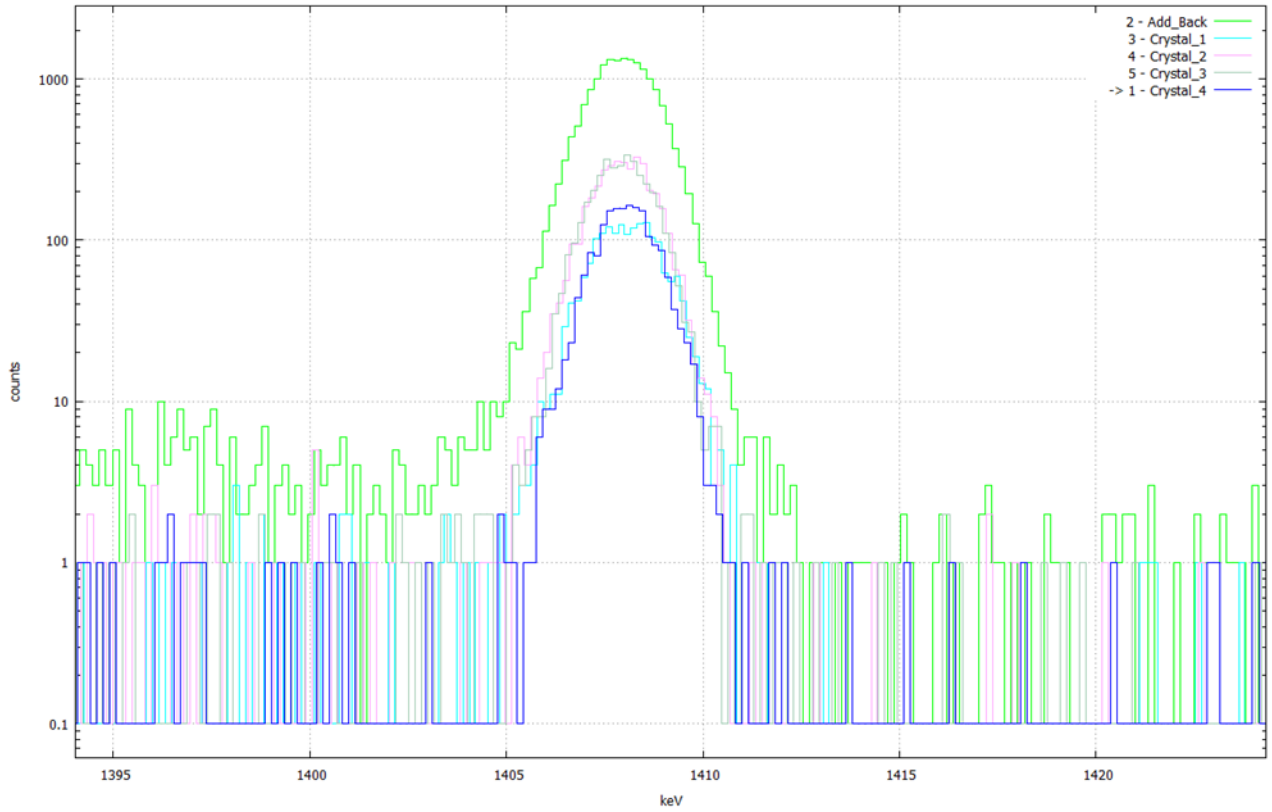


Fig. 18.2: Zoom on the peak @ 1408 keV

In the end, **Tab. 18.2** shows the results of three peak fits. The energy resolution of the *Add-Back* spectrum is about 2 keV FWHM @ 1408 keV (in line with the expected resolution of the detector) and the *Add-Back* ratio calculated with the fitted net areas is **1.55**.

		Peak Area		Centroid		FHWM	
	Peak	Gross (cnts)	Net (cnts)	channels	keV	channels	keV
Crystal 1 ICR = 516 cps	@ 121.78	9536	6242	770.43	121.78	8.68	1.37
	@ 344.28	8248	5713	2180.02	344.27	9.42	1.49
	@ 1408.0	1872	1872	8920.03	1408.09	13.59	2.14
Crystal 2 ICR = 950 cps	@ 121.78	18174	12147	744.14	121.80	5.93	0.97
	@ 344.28	17078	13819	2105.30	344.26	7.01	1.15
	@ 1408.0	3925	3925	8613.95	1407.98	11.47	1.87
Crystal 3 ICR = 930 cps	@ 121.78	17334	10647	734.22	121.79	6.18	1.02
	@ 344.28	18833	13497	2077.06	344.24	7.10	1.18
	@ 1408.0	3828	3828	8498.21	1407.94	11.12	1.84
Crystal 4 ICR = 508 cps	@ 121.78	9384	5434	740.68	121.80	5.90	0.97
	@ 344.28	7240	4842	2095.55	344.29	6.89	1.13
	@ 1408.0	1911	1911	8573.52	1408.06	10.69	1.76
Add Back ICR = 2.39 kcps	@ 121.78	50046	36366	734.75	121.77	6.41	1.06
	@ 344.28	56862	46450	2077.70	344.24	7.64	1.27
	@ 1408.0	18124	17869	8498.85	1407.96	12.12	2.01

Tab. 18.2: Fit results of three ^{152}Eu peaks at 121.78, 344.28 and 1408.0 keV

$$Add\ Back\ Ratio\ @1408\ keV = \frac{Net_{AB}}{\sum_{i=1}^{4} Net_i} = \frac{17869}{1872 + 3925 + 3828 + 1911} = 1.55$$

19 Technical Support

CAEN makes available the technical support of its specialists for requests concerning the software and hardware. Use the support form available at the following link:

https://www.caen.it/support-services/support-form/

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