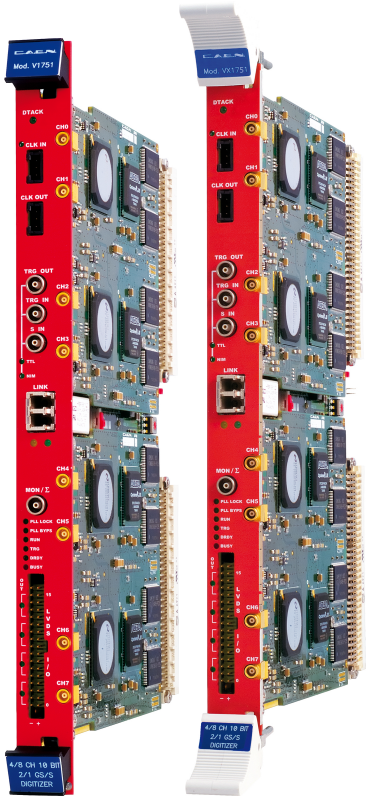
Rev.18- 20/12/2023

V1751 / VX1751

4/8 Channels 10 bit 2/1 GS/s Digitizer



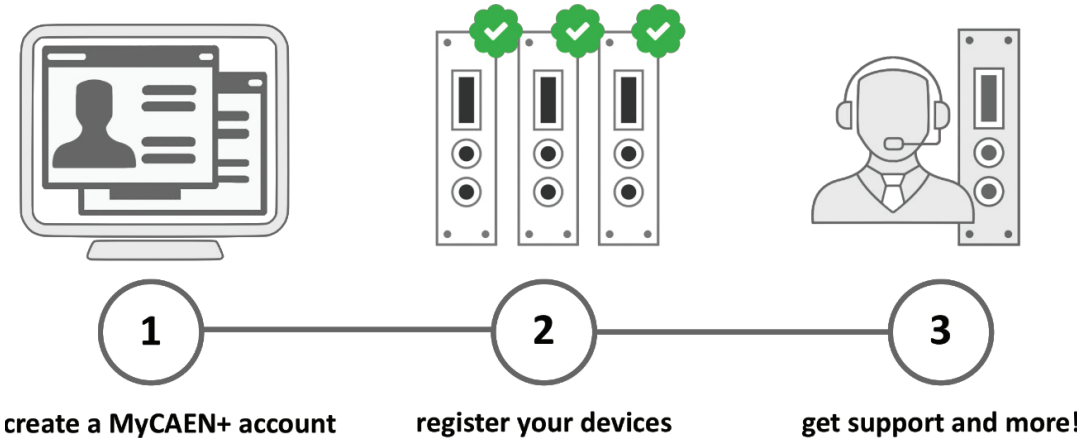
CAEN
Tools for Discovery

User Manual

Register your device

Register your device to your **MyCAEN+** account and get access to our customer services, such as notification for new firmware or software upgrade, tracking service procedures or open a ticket for assistance. **MyCAEN+** accounts have a dedicated support service for their registered products. A set of basic information can be shared with the operator, speeding up the troubleshooting process and improving the efficiency of the support interactions.

MyCAEN+ dashboard is designed to offer you a direct access to all our after sales services. Registration is totally free, to create an account go to https://www.caen.it/become-mycaenplus-user and fill the registration form with your data.



https://www.caen.it/become-mycaenplus-user/

Purpose of this Manual

This document contains the full hardware description of the V1751 and VX1751 CAEN digitizers and their principle of operating as **Waveform Recording Digitizer** (basing on the hereafter called **"waveform recording firmware"**).
The reference firmware revision is: **4.16_0.7**.
For any reference to registers in this user manual, please refer to document [RD1] on the digitizer web page.
For any reference to DPP firmware in this user manual, please refer to documents [RD2] and [RD3] present on the firmware web page.

Change Document Record

Date	Revision	Changes
-	00-15	Old manuals are available on request (see Chap. **14**)
Jun 12th, 2017	16	Revised layout and improved text
Dec 20th, 2023	18	Revised layout and improved text. Added up-to-date: controllers and adapters support, accessories. Updated **Safety Notices** and Chap. **3**, **11** , **12** and **13**. Updated Sec. **8.1**, **9.8.5**, **9.9**, **9.10**, **9.14**, **9.16**

Symbols, Abbreviated Terms and Notation

ADC	Analog-to-Digital Converter
AMC	ADC & Memory Controller
DAQ	Data Acquisition
DAC	Digital-to-Analog Converter
DC	Direct Current
LVDS	Low-Voltage Differential Signal
PLL	Phase-Locked Loop
ROC	ReadOut Controller
TTT	Trigger Time Tag
USB	Universal Serial Bus

Reference Documents

[RD1] UM6009 – 751 Registers Description
[RD2] UM5960 – CoMPASS User Manual
[RD3] UM2764 – DPP-ZLEplus User Manual
[RD4] UM2088 – DPP-PSD User Manual
[RD5] AN6308 – Downsampling measurements with CAEN Digitizer 720/724/740/751 families
[RD6] GD2512 – CAENUpgrader QuickStart Guide
[RD7] Precautions for Handling, Storage and Installation
[RD8] AD9510. Available at `http://www.analog.com/UploadedFiles/Data_Sheets/AD9510.pdf`
[RD9] UM1935 – CAENDigitizer User & Reference Manual

[RD10] UM2091 – CAEN WaveDump User Manual
[RD11] GD2817 – How to make coincidences with CAEN digitizers
[RD12] AN2086 – Synchronization of a multi-board acquisition systems with CAEN digitizers
[RD13] AN2472 – CONET1 to CONET2 migration
[RD14] UM4413 – A2818 Technical Information Manual
[RD15] UM3121 – A3818 Technical Information Manual
[RD16] DS7799 A4818 Adapter Data Sheet
[RD17] UM7685 - V3718 & VX3718 User & Reference Manual
[RD18] UM8305 - V4718 & VX4718 User & Reference Manual
[RD19] UM1934 – CAENComm User & Reference Manual
[RD20] GD2512 – CAENUpgrader QuickStart Guide
[RD21] x751 Family DPP-PSD Firmware Compatibility

All CAEN documents can be downloaded at:
`www.caen.it/support-services/documentation-area`

Manufacturer Contacts

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Limitation of Responsibility

If the warnings contained in this manual are not followed, CAEN will not be responsible for damage caused by improper use of the device. The manufacturer declines all responsibility for damage resulting from failure to comply with the instructions for use of the product. The equipment must be used as described in the user manual, with particular regard to the intended use, using only accessories as specified by the manufacturer. No modification or repair can be performed.

Disclaimer

The information contained herein has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies. CAEN SpA reserves the right to modify its products specifications without giving any notice; for up to date information please visit www.caen.it.

Made in Italy

We remark that all our boards have been designed and assembled in Italy. In a challenging environment where a competitive edge is often obtained at the cost of lower wages and declining working conditions, we proudly acknowledge that all those who participated in the production and distribution process of our devices were reasonably paid and worked in a safe environment (while this is true for the boards marked ”MADE IN ITALY”, we cannot guarantee for third-party manufactures).

Index

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Safety Notices

N.B. Read carefully the "Precautions for Handling, Storage and Installation document provided with the product before starting any operation.

The following HAZARD SYMBOLS may be reported on the unit:

	Caution, refer to product manual
	Caution, risk of electrical shock
	Protective conductor terminal
	Earth (Ground) Terminal
	Alternating Current
	Three-Phase Alternating Current

The following symbol may be reported in the present manual:

	General warning statement

The symbol could be accompanied by the following terms:

- **DANGER**: indicates a hazardous situation which, if not avoided, will result in serious injury or death.
- **WARNING**: indicates a hazardous situation which, if not avoided, could result in death or serious injury.
- **CAUTION**: indicates a situation or condition which, if not avoided, could cause physical injury or damage the product and / or the surrounding environment.

CAUTION: To avoid potential hazards

USE THE PRODUCT ONLY AS SPECIFIED.
ONLY QUALIFIED PERSONNEL SHOULD PERFORM SERVICE PROCEDURES

CAUTION: Avoid Electric Overload

TO AVOID ELECTRIC SHOCK OR FIRE HAZARD, DO NOT POWER A LOAD OUTSIDE OF ITS SPECIFIED RANGE

CAUTION: Avoid Electric Shock

TO AVOID INJURY OR LOSS OF LIFE, DO NOT CONNECT OR DISCONNECT CABLES WHILE THEY ARE CONNECTED TO A VOLTAGE SOURCE

CAUTION: Do Not Operate without Covers

TO AVOID ELECTRIC SHOCK OR FIRE HAZARD, DO NOT OPERATE THIS PRODUCT WITH COVERS OR PANELS REMOVED

CAUTION: Do Not Operate in Wet/Damp Conditions

TO AVOID ELECTRIC SHOCK, DO NOT OPERATE THIS PRODUCT IN WET OR DAMP CONDITIONS

CAUTION: Do Not Operate in an Explosive Atmosphere

TO AVOID INJURY OR FIRE HAZARD, DO NOT OPERATE THIS PRODUCT IN AN EXPLOSIVE ATMOSPHERE

THIS DEVICE SHOULD BE INSTALLED AND USED BY SKILLED TECHNICIAN ONLY OR UNDER HIS SUPERVISION

DO NOT OPERATE WITH SUSPECTED FAILURES.
IF YOU SUSPECT THIS PRODUCT TO BE DAMAGED, PLEASE CONTACT THE TECHNICAL SUPPORT

See Chap. **14** for the Technical Support contacts.

CAUTION: This product needs proper cooling.

USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEATING MAY DEGRADE THE MODULE PERFORMANCES

V1751 DIGITIZERS CANNOT BE OPERATED WITH CAEN CRATES VME8001, VME8002, VME8004, AND VME8004A. OVERHEAT MAY DAMAGE THE MODULE

CAUTION: This product needs proper handling.

THE VME DIGITIZER DOES NOT SUPPORT LIVE INSERTION (HOT-SWAP)
REMOVE OR INSERT THE BOARD WHEN THE CRATE IS POWERED OFF

ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE

1 Introduction

The V1751 is a 1-unit wide VME 6U module housing a 8 Channel 10 bit 1 GS/s Flash ADC Waveform Digitizer with 1 V_{pp} input dynamic range on single ended MCX coaxial connectors (see **Tab. 1.1**). Versions with 200 mV_{pp} single ended customization is also available (see **Tab. 1.1**). The DC offset is adjustable via a 16-bit DAC on each channel in the $\pm$0.5 V (@1 V_{pp}), $\pm$100 mV (@200 mV_{pp}) range. The digitizer can work in Dual Edge Sampling (DES mode) at 2 GS/s. In this mode only half of the channels are enabled for acquisition.

Considering the sampling frequency and bit number, these 751 digitizer family is well suited for fast signals as the ones coming from fast organic, inorganic and liquid scintillators coupled with PMTs or Silicon Photomultiplier, Diamond detectors and others.

A common acquisition trigger signal (common to all the channels) can be fed externally via the front panel TRG-IN input connector or via software. Alternatively, each channel is able to generate a self-trigger when the input signal goes under/over a programmable threshold. The trigger from one board can be propagated out of the board through the front panel TRG-OUT connector.

During the acquisition, data stream is continuously written in a circular memory buffer. When the trigger occurs, the digitizer writes additional samples for the post trigger and freezes the buffer that can be read by one of the provided readout links.

Each channel has a SRAM digital memory (see **Tab. 1.1** for the available memory size options) divided into buffers of programmable size (1 $\div$ 1024). The size of the memory doubles when working in DES mode. The readout (from VMEbus or Optical link) of a frozen buffer is independent from the write operations in the active circular buffer (ADC data storage).

V1751 features front panel CLK-IN connector as well as an internal PLL for clock synthesis from internal/external references. Multi-board synchronization is supported, so all V1751 can be synchronized to a common clock source ensuring Trigger Time Stamps alignment. Once synchronized, all data will be aligned and coherent across multiple V1751 boards. CLK-IN / CLK-OUT connectors allow for a Daisy-chained clock distribution.

16 general purpose LVDS I/Os FPGA-controlled can be programmed for Busy, Data Ready, Memory Full, or Individual Trig-Out management. An Input Pattern (external signal) can be provided on the LVDS I/Os to be latched to each trigger as an event marker (see Sec. **9.11**).

An analog output (MON/Σ) from internal 12-bit 125-MHz DAC, controlled by the FPGA, allows the user to reproduce four types of outgoing information: Trigger Majority, Test Pulses, Memory Occupancy, Voltage Level (see Sec. **9.12**).

V1751 is equipped with a VME64 interface (VM64X in case of VX1751) where the data readout can be performed in Single Data Transfer (D32), 32/64-bit Block Transfer (BLT, MBLT, 2eVME. 2eSST) and 32/64-bit Chained Block Transfer (CBLT).

The module houses Optical Link interface (CAEN proprietary CONET protocol) supporting transfer rate up to 80 MB/s and offers daisy chain capability. Therefore, it is possible to connect up to 8 ADC modules to a single A4818 Adapter (or to a single A2818 Optical Link Controller, Obsolete), or up to 32 using a 4-link A3818 version (see Tab. **1.1**). VME and Optical Link accesses take place on independent paths and are handled by the on-board controller, therefore when accessed through Optical Link the board can be operated outside the VME Crate.

In addition to the waveform recording firmware, CAEN provides for this digitizer two types of Digital Pulse Processing firmware (DPP):

- Pulse Shape Discrimination (DPP-PSD) **[RD4]**, which combines the functionalities of a digital QDC (charge integration) and discriminator of different shapes for particle identification.
- Zero Length Encoding (DPP-ZLE*plus*) **[RD3]**, for the Zero suppression and data reduction.

These special firmware make the digitizer an enhanced system for Physics Applications.

Board Model	Description
V1751	4/8 Ch. 10 bit 2/1 GS/s Digitizer: 3.6/1.8MS/ch, EP3C16, SE
V1751C	4/8 Ch. 10 bit 2/1 GS/s Digitizer: 28.8/14.4MS/ch, EP3C16, SE
VX1751	4/8 Ch. 10 bit 2/1 GS/s Digitizer: 3.6/1.8MS/ch, EP3C16, SE
VX1751C	4/8 Ch. 10 bit 2/1 GS/s Digitizer: 28.8/14.4MS/ch, EP3C16, SE
WPERS0175102	x751 Customization - 200mVpp Input Range, SE
DPP Firmware	**Description**
DDP-PSD 8ch	DDP-PSD Digital Pulse Processing for Pulse Shape Discrimination (8ch x751)
DDP-ZLEplus 8ch	Digital Pulse Processing Zero Length Encoding for (8ch x 751)
Related Products	**Description**
A3818A	A3818A – PCIe 1 Optical Link
A3818B	A3818B – PCIe 2 Optical Link
A3818C	A3818C – PCIe 4 Optical Link
A4818	A4818 - USB3 to Conet2 Adapter
V3718	V3718 - VME-USB Bridge
VX3718	VX3718 - VME-USB Bridge
V4718	V4718 - VME64-USB 3.0, Ethernet and Optical Link Bridge
VX4718	VX4718 - VME64-USB 3.0, Ethernet and Optical Link Bridge
A2818 (Obsolete)	A2818 – PCI Optical Link (Rhos compliant)
Accessories	**Description**
DT4700	Clock Generator and FAN-OUT
A316	Cable assembly 2.54mm 2-pin header female - 5 cm
A317	Cable assembly for Clock distribution 3-pin AMPMODU IV female terminations - 18 cm
A317L	Cable assembly for Clock distribution 3-pin AMPMODU IV female terminations - 25 cm
A318	Adapter for Clock signal FISCHER S101A004 male to 3-pin AMPMODU IV female - 10 cm
A319B	Clock Cable for Digitizer Series 1.0 to 2.0 interconnection (L=20cm)
A654	Cable assembly LEMO 00 male to MCX male – 1 m
A654 KIT4	4 Cable assembly LEMO 00 male to MCX male - 1 m
A654 KIT8	8 Cable assembly LEMO 00 male to MCX male - 1 m
A659	Cable assembly BNC male to MCX male – 1 m
A659 KIT4	4 MCX TO BNC Cable Adapter
A659 KIT8	8 MCX TO BNC Cable Adapter
A952	Cable assembly 2.54mm 34 pin female to 2.54mm 34 pin female - 50 cm
A953	Cable assembly 2.54mm 34 pin female to two 2.54mm 34 pin female - 50 cm
A954	Cable assembly 2.54mm 34 pin female to two 2.54mm 16 pin female - 50 cm
AI2730	Optical Fibre 30 m simplex
AI2720	Optical Fibre 20 m simplex
AI2705	Optical Fibre 5 m simplex
AI2703	Optical Fibre 30 cm simplex
AY2730	Optical Fibre 30 m duplex
AY2720	Optical Fibre 20 m duplex
AY2705	Optical Fibre 5 m duplex (Rohs compliant)

Tab. 1.1: Table of models and related items.

2 Block Diagram

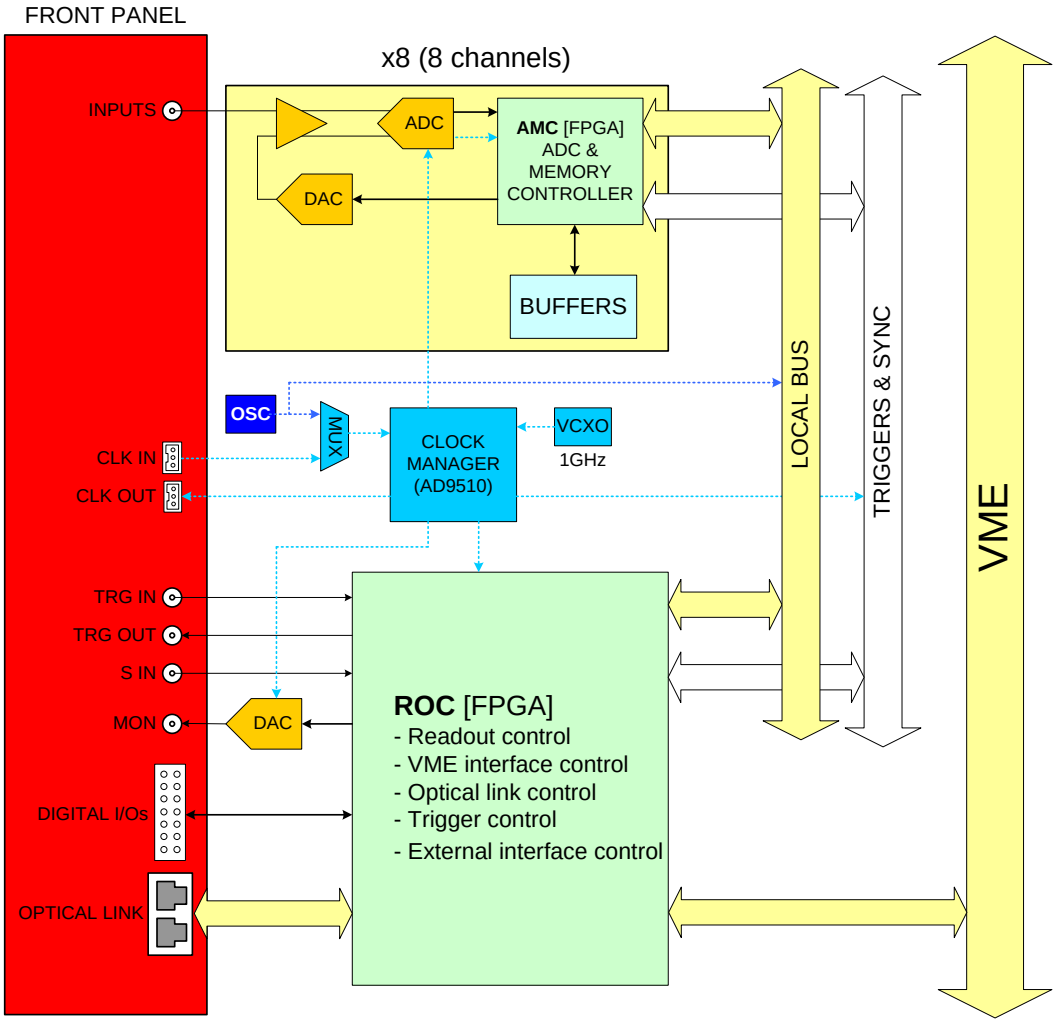


Fig. 2.1: Block Diagram.

3 Technical Specifications

ANALOG INPUTS	**Number of Channels** • 8 channels/4 channels in DES mode[1](EVEN channels must be disconnected) • Single ended **Full Scale Range (FSR)** 1 V_{pp} or customizable to 200 mV_{pp}	**Absolute Max Analog Input Voltage** @1V_{pp}: 3 V_{pp} (with V_{rail} max +3 V or –3 V for any DAC offset value) @200 mV_{pp}: 2 V_{pp} (with V_{rail} max +2 V or –2 V for any DAC offset value) **Impedance** Z_{in} = 50 Ω	**DC Offset** Programmable DAC for DC offset adjustment on each channel in the full range **Connector** MCX **Bandwidth** 500 MHz
DIGITAL CONVERSION	**Resolution** 10 bits	**Sampling Rate** 1 GS/s (2 GS/s DES mode) simultaneously on each channel 250 MS/s minimum by hardware downsampling [2]	
SYSTEM PERFORMANCES	ENOB: 9.04 (56 kS Buffer) SINAD: 56.19 dB THD: 70.2 dB SFDR: 79.7 dB SIGMA: 0.58 LSB rms (56 kS buffer, open input)		
FPGA	Altera Cyclone EP3C16 (one FPGA serves 2 channels)		
TRIGGER	**Trigger Source** • *Self-trigger*: channel over/under-threshold for common (waveform recording firmware) or individual (DPP firmware only) trigger generation • *External-trigger*: common trigger by TRG IN connector or individual by LVDS connector (DPP firmware only) • *Software-trigger*: common trigger by software command **Trigger Propagation** TRG-OUT programmable digital output	**Trigger Time Stamp** *Waveform recording FW/DPP-ZLEplus*: • 31-bit counter • 16 ns resolution • 17 s range • 48 bit fw extension; *DPP-PSD*: • 32-bit counter • 1 ns resolution (1 ps fine time stamp resolution with dCFD) • 4 s range • 48 bit fw extension • 64 bit sw extension	
ACQUISITION MEMORY	1.835 MS/ch (3.6 MS/ch in DES mode) or 14.4 MS/ch (28.8 MS/ch in DES mode) (see **Tab. 1.1**) Multi Event Buffer divisible into 1 ÷ 1024 Independent read and write access Programmable event size and pre/post trigger		
ADC CLOCK GENERATION	Clock source: internal/external On-board programmable PLL provides generation of the main board clocks from an internal (50 MHz local Oscillator) or external (front panel CLK-IN connector) reference		

DIGITAL I/O	**CLK-IN (AMP Modu II)** AC coupled differential input clock LVDS, ECL, PECL, LVPECL, CML, accuracy<100ppm, Z_{diff} = 100 Ω **CLK-OUT (AMP Modu IV)** DC coupled differential LVDS clock output locked to ADC sampling clock, Z_{diff} = 100 Ω	**TRG-IN (LEMO)** External trigger digital input Signal Width > 8 ns NIM/TTL, Z_{in} = 50 Ω **TRG-OUT (LEMO)** Trigger digital output NIM/TTL, R_t = 50 Ω **S-IN (LEMO)** SYNC/START front panel digital input Signal Width > 8 ns NIM/TTL, Z_{in} = 50 Ω	**LVDS I/O** 16 general purpose LVDS I/O controlled by the FPGA: Busy, Data Ready, Memory full, Individual Trig-Out and other functions can be programmed An Input Pattern from the LVDS I/O can be associated to each trigger as an event marker
SYNCHRONIZATION	**Clock Propagation** • *Daisy chain*: through CLK-IN/CLK-OUT connectors • *One-to-many*: clock distribution from an external clock source on CLK-IN connector Clock Cable delay compensation	**Acquisition Synchronization** Sync, Start/Stop through digital I/O (S-IN or TRG-IN input / TRG-OUT output) **Trigger Time Stamps Alignment** By S-IN input connector	
COMMUNICATION INTERFACES	**Optical Link** CAEN CONET proprietary protocol Up to 80 MB/s transfer rate Daisy-chain capability	**VME** VME 64X compliant Data transfer mode: BLT32, MBLT64 (70 MB/s using CAEN Bridge), CBLT32/64, 2eVME, 2eSST (up to 200 MB/s)	
ANALOG MONITOR	12-bit / 125 MHz DAC FPGA controlled; four operating modes: • Test pulses: 1 V_{pp} ramp generator • Majority signal: proportional to the nr. Of channels under/over threshold (steps of 125 mV) • Memory Occupancy signal: proportional to the Multi Event Buffer Occupancy (1 buffer 1mV) • Voltage level: programmable output voltage level		
FIRMWARE	**Waveform Recording Firmware** Free firmware for waveform recording	**DPP Firmware** DPP-PSD for the Pulse Shape Discrimination DPP-ZLE*plus* for the Zero Length Encoding	**Upgrades** Firmware can be upgraded via VMEbus/Optical Link
SOFTWARE	**Readout SW** CAEN software for users and developers: WaveDump, CAENScope, CoMPASS (Windows®, Linux®)	**Libraries and Tools** General purpose C libraries with readout demos (Windows®, Linux® and LabVIEW™ support) and configuration tools	
MECHANICAL	**Form Factor** 1-unit wide VME64/VME64X	**Weight** 535 g	**Dimension** 6U × 160 mm
ENVIRONMENTAL	**Environment:** Indoor use **Operating Temperature:** 0°C to +40°C **Storage Temperature:** –10°C to +60°C **Operating Humidity:** 10% to 90% RH non condensing **Storage Humidity:** 5% to 90% RH non condensing **Altitude:** < 2000m **Pollution Degree:** 2 **Overvoltage Category:** II **EMC Environment:** Commercial and light industrial **IP Degree:** IPX0 Enclosure, not for wet location		
REGULATORY COMPLIANCE	**EMC** CE 2014/30/EU Electromagnetic compatibility Directive	**Safety** CE 2014/35/EU Low Voltage Directive	

POWER REQUIREMENTS	6.5 A @ +5V 200 mA @ +12V 300 mA @ -12V

Tab. 3.1: Specification table.

[1] DES mode is available only in case of waveform recording firmware installed on the board.
[2] The minimum value may depend on the digitizer model, on the firmware or on the hardware downsampling mode (refer to **[RD5]**).

4 Packaging and Compliancy

The V1751/VX1751 digitizer modules are available in 1-unit wide VME64/VME64X boards, EMC compliant.

The devices are inspected by CAEN before the shipment, and they are guaranteed to leave the factory free of mechanical or electrical defects.

The content of the delivered package standardly consists of the part list shown in the table below (**Tab. 4.1**).

	Part	Description	Qt
	V1751/VX1751	8 Channel 10 bit 2/1 GS/s Digitizer	x1
	Documentation	UM3350 - V1751/VX1751 User Manual	-

Tab. 4.1: Delivered kit content.

CAUTION: to manage the product, consult the operating instructions provided.

When receiving the unit, the user is strictly recommended to:

- Inspect containers for damage during shipment. Report any damage to the freight carrier for possible insurance claims.
- Check that all the components received match those listed on the enclosed packing list as in **Tab. 4.1** . (CAEN cannot accept responsibility for missing items unless any discrepancy is promptly notified.)
- Open shipping containers; be careful not to damage contents.
- Inspect contents and report any damage. The inspection should confirm that there is no exterior damage to the unit such as broken knobs or connectors and that the front panel is not scratched or cracked. Keep all packing material until the inspection has been completed.
- If damage is detected, file a claim with carrier immediately and notify CAEN service (see Chap. **14**).
- If equipment must be returned, carefully repack equipment in the original shipping container with original packing materials, if possible. Please contact CAEN service.
- If equipment is not installed when unpacked, place equipment in original shipping container and store in a safe place until ready to install.

DO NOT SUBJECT THE ITEM TO UNDUE SHOCK OF VIBRATIONS

DO NOT BUMP, DROP OR SLIDE SHIPPING CONTAINERS

DO NOT LEAVE ITEMS OR SHIPPING CONTAINERS UNSUPERVISED IN AREAS WHERE UNTRAINED PERSONNEL MAY MISHANDLE THE ITEMS

USE ONLY ACCESSORIES WICH MEET THE MANUFACTURER SPECIFICATIONS

For a correct and safe use of the module, refer to Chap. **6** and **7**.

5 PID (Product Identifier)

PID is the CAEN product identifier, an incremental number greater than 10000 that is unique for each product[1]. The PID is on a label affixed to the product (**Fig. 5.1**) and it is even stored in an on-board non-volatile memory readable at bit [7:0] of registers 0xF080 or 0xF084 **[RD1]**. The PID information is also available through CAENUpgrader Software, with the Get Information function of the GUI (for more details refer to **[RD6]**).

Note: The serial number is still valid to identify older boards, where the PID label is not present.

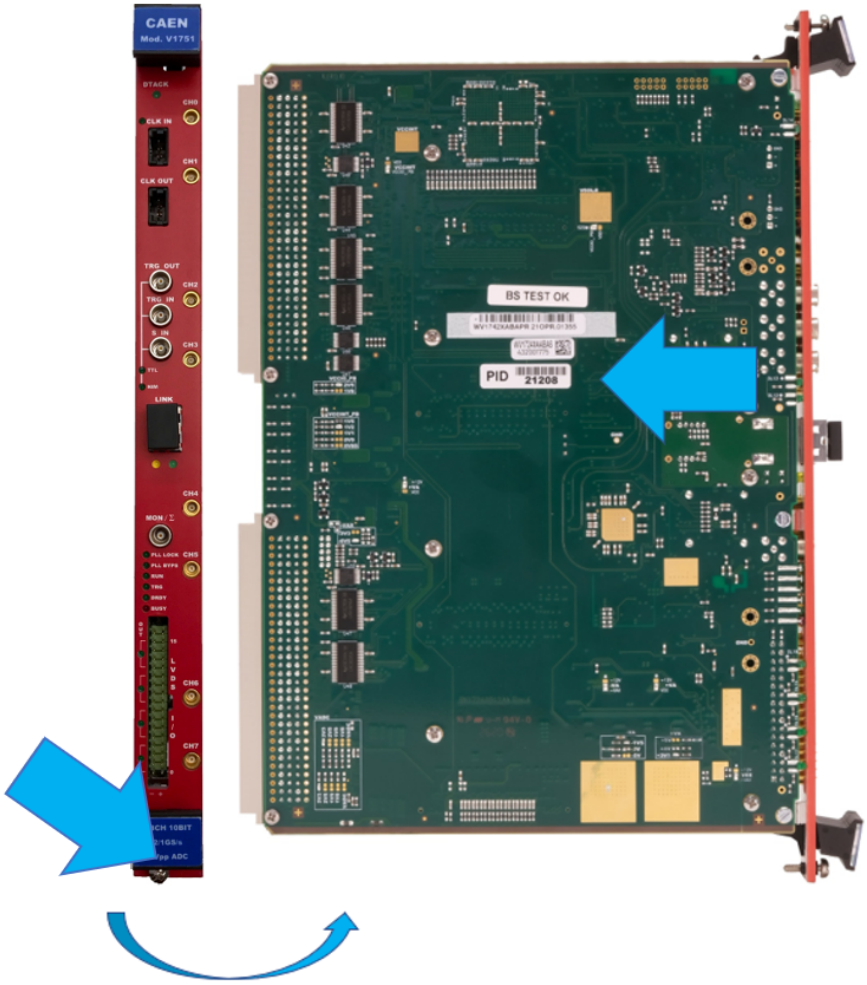


Fig. 5.1: PID location on V1751 (the number in the picture is purely indicative).

[1]The PID substitutes the serial number previously identifying the boards.

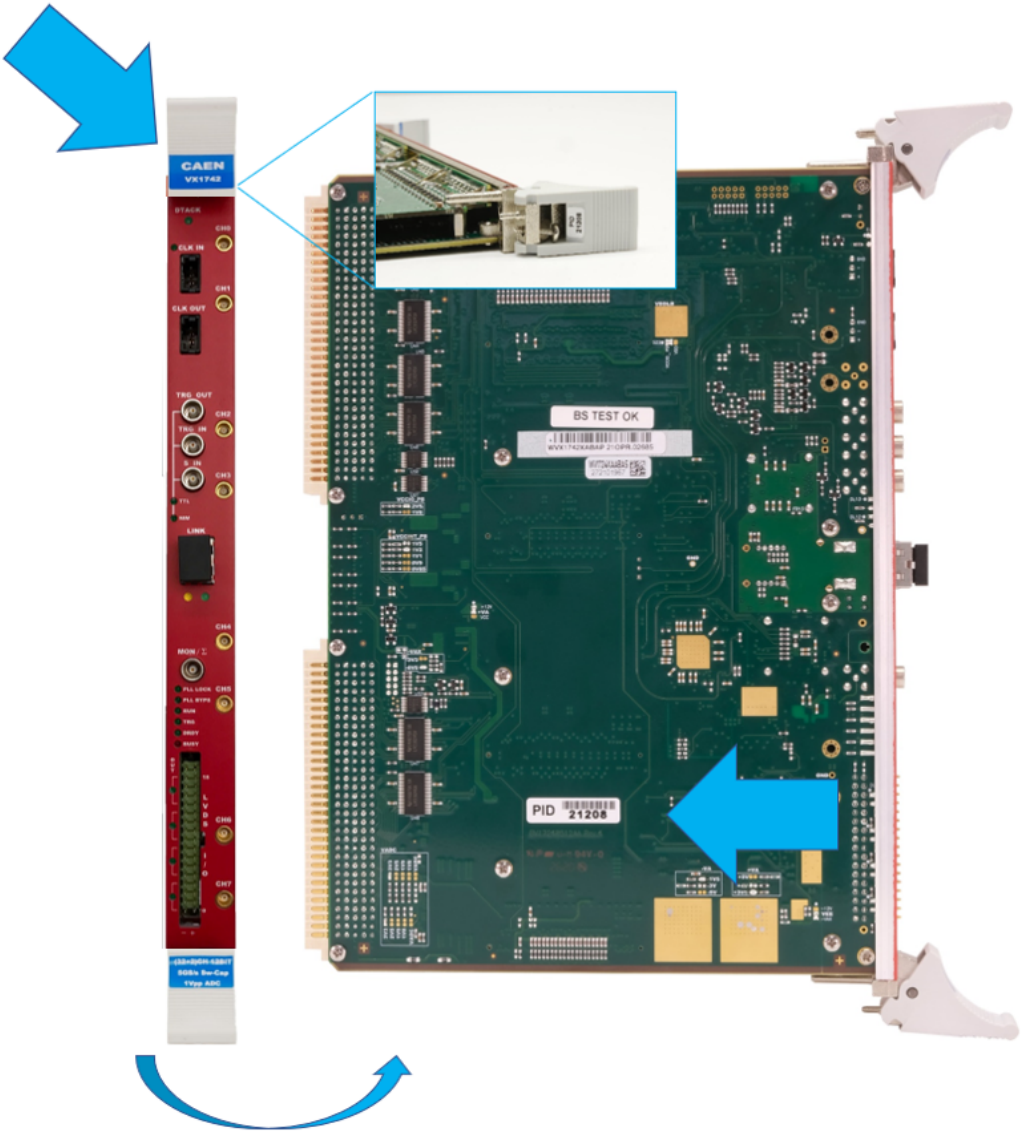


Fig. 5.2: PID location on VX1751 (the number in the picture is purely indicative).

6 Power Requirements

The table below resumes the V1751/VX1751 power consumptions per relevant power supply voltage.

MODULE	SUPPLY VOLTAGE		
	+5 V	+12 V	-12 V
V1751/VX1751	6.5 A	200 mA	300 mA

Tab. 6.1: Power requirements table.

7 Cooling Management

The V1751/VX1751 Digitizers can operate in the temperature range 0° ÷ +40°C **[RD7]**.

The VME models must be operated in ventilated crates as recommended in the **Safety Notices**.

EXTERNAL FANS MUST BE USED WHEN THE BOARD IS INSTALLED IN A SETUP WITH POOR AIR FLOW

The User must take care to provide a proper cooling to the board with external fan if the board is used in an enclosure or if the board is installed in a setup with poor air flow.
Excessive temperature will, in first instance, reduce the performance and the quality of the measurements and can also damage the board.

If the board is stored in cold environment, please check for water condensation before power on.

The board has not been tested for radiation hardness. High energy particles can be source of errors and can damage the FPGA. If used in strong proton or neutron beams, arrange proper shielding, or remote the sensors with a custom cable.

7.1 ADC chips temperature readout

The V1751 features an internal ADC temperature monitoring system, useful in order to estimate the steady thermal state of the ADCs and to perform the calibration procedure (see Sec. **9.8.1**). Since each ADC manages two channels (0-1, 2-3, 4-5, 6-7) identical temperature values will be found for couples of channels; such values can be readout using register 0x1nA8.

7.2 ADC chips over temperature protection

Each ADC will be automatically powered off whenever the core temperature reaches 90°C. The relevant channels will not therefore participate any more to data event, and bit[7] and bit[8] of register 0x1n88 will set to 1 (channel power down and over-temperature flags respectively).

When the ADC core temperature decreases under 65°C, the bit[8] will return to 0, and the relevant channels can be restored to normal operation following these steps:

- Wait until bit 8 of 0x1n88 register returns to 0
- Set bit[0] = 0 of 0x1n9C; bit[7] of 0x1n88 will return to 0.
- Perform a calibration procedure on the restored channels (see Sec. **9.8.1**)

7.3 Cleaning Air Vents

CAEN recommends to occasionally clean the air vents on all vented sides of the board or crate, if present. Lint, dust, and other foreign matter can block the vents and limit the airflow. Be sure to power off the

board and disconnect it from the power by physically detach the power chord before cleaning the air vents and follow the general cleaning safety precautions.

IT IS UNDER THE RESPONSIBILITY OF THE CUSTOMER A NON-COMPLIANT USE OF THE PRODUCT

8 Panels Description

Fig. 8.1: Front panel view of V1751.

8.1 Front Panel

ANALOG INPUT

FUNCTION
Input connectors from CH0 to CH7 receive the input analog signals.

ELECTRICAL SPECS
Input dynamics: 1 V_{pp}
Input impedance (Z_{in}): 50 Ω.
Absolute max analog input voltage:
@1 V_{pp}: 3 V_{pp} (with V_{rail} max +3 V or -3 V)
@200 mV_{pp}: 2 V_{pp} (with V_{rail} max +2 V or -2 V) for any DAC offset value.

Note: 200 mV_{pp} input range (50 Ω impedance) is available by ordering option (see **Tab. 1.1**).

MECHANICAL SPECS
Series: MCX connectors.
Type: CS 85MCX-50-0-16.
Manufacturer: SUHNER
Suggested plug: MCX-50-2-16 type.
Suggested cable: RG174 type.

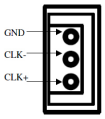
CLOCK IN/CLOCK OUT

FUNCTION
Input and output connectors for the external clock.

ELECTRICAL SPECS
Sign. type: differential (LVDS, ECL, PECL, LVPECL, CML). CAEN provides single ended-to-differential A318 cable adapter (see **Tab. 1.1**) for CLK-IN.
Coupling: AC (CLK-IN); DC (CLK-OUT).
Z_{diff}: 100 Ω.

MECHANICAL SPECS
Series: AMPMODU connectors.
Type: 3-102203-4 (3-pin).
Manufacturer: AMP Inc.

PINOUT



CLK IN LED (GREEN): indicates the external clock is enabled.

TRG-IN / TRG-OUT / S-IN

FUNCTION

- TRG-OUT: digital output connector to propagate:
  - the internal trigger sources;
  - signals (probes) from the mezzanines;
  - S-IN signal
  - signals (probes) from the motherboard, like Run, ClkOut, ClockPhase, PLL_Unlock or Busy signal

according to 0x8110 and 0x811C registers, or

- TRG-IN: digital input connector for the external trigger or veto signal.
- S-IN: SYNC/START/STOP digital input connector configurable as reset of the time stamp (see Sec. **9.14**) or to start/stop the acquisition (see Sec. **9.8.2**).

ELECTRICAL SPECS
Signal level: NIM or TTL.
TRG-IN/S-IN input Signal Width > 8 ns
TRG-IN/S-IN Input impedance (Z_{in}): 50 Ω
TRG-OUT requires 50 Ω termination.

MECHANICAL SPECS
Series: 101 A 004 connectors.
Type: DLP 101 A 004-28.
Manufacturer: FISCHER.
Alternatively:
Type: EPL 00 250 NTN.
Manufacturer: LEMO.

TTL (GREEN), NIM (GREEN): indicate the standard TTL or NIM set for TRG-OUT, TRG-IN, and S-IN.

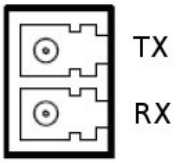
OPTICAL LINK PORT

FUNCTION
Optical LINK connector for data readout and flow control. Daisy chainable. Compliant with Multimode 62.5/125 µm cable featuring LC connectors on both sides.

ELECTRICAL SPECS
Transfer rate: up to 80 MB/s.

MECHANICAL SPECS
Series: SFF Transceivers.
Type: FTLF8519F-2KNL (LC connectors).
Manufacturer: FINISAR.

PINOUT



LINK LEDs (GREEN/YELOW): right LED (GREEN) indicates the network presence, while left LED (YELLOW) signals the data transfer activity.

ANALOG MONITOR

FUNCTION
Analog Monitor output connector with 4 programmable modes (see Sec. **9.12**):

- Trigger Majority
- Test Pulses
- Memory Occupancy
- Voltage Level

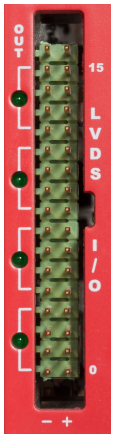
ELECTRICAL SPECS
12-bit (125 MHz) DAC output.
1 V_{pp} on R_t = 50 Ω

MECHANICAL SPECS
Series: 101 A 004 connectors.
Type: DLP 101 A 004-28.
Manufacturer: FISCHER.
Alternatively:
Type: EPL 00 250 NTN.
Manufacturer: LEMO.

DIAGNOSTICS LEDs

DTACK (GREEN): indicates there is a VME read/write access to the board;
PLL LOCK (GREEN): indicates the PLL is locked to the reference clock;
PLL BYPS (GREEN): not used;
RUN (GREEN): indicates the acquisition is running (data taking). See Sec. **9.8.2**;
TRG (GREEN): indicates the trigger is accepted;
DRDY (GREEN): indicates the event/data is present in the Output Buffer;
BUSY (RED): indicates all the buffers are full for at least one channel.

LVDS I/Os CONNECTOR



FUNCTION

16-pin connector with programmable general purpose LVDS I/O signals organized in 4 independent signal groups: 0÷3; 4÷7; 8÷11; 12÷15.
In/Out direction is software controlled.
Different selectable modes (see Sec. **9.11**):

- Register
- Trigger
- nBusy/nVeto
- Legacy

ELECTRICAL SPECS

Level: differential LVDS
Z_{diff}: 100 Ω

MECHANICAL SPECS

Series : TE - AMPMODU Mod II Series
Type: 5-826634-0 34 pin (lead spacing: 2.54 mm; row pitch: 2.54 mm)
Manufacturer: AMP Inc.

LVDS I/O LEDs (GREEN): Each LED close to a 4-pin group lights on if the pins are set as outputs.

IDENTIFICATION LABELS

On top and bottom of insertion/extraction handle:

- Manufacturer
- Board model
- Brief functional description

On the bottom (V1751) or on the HANDLE (VX1751):

- Product Identifier (PID)

Note: With Serial Number (S/N) identification, a 4-digit number is reported on a little silver label on the bottom of the VME board's front panel.

8.2 Internal Components

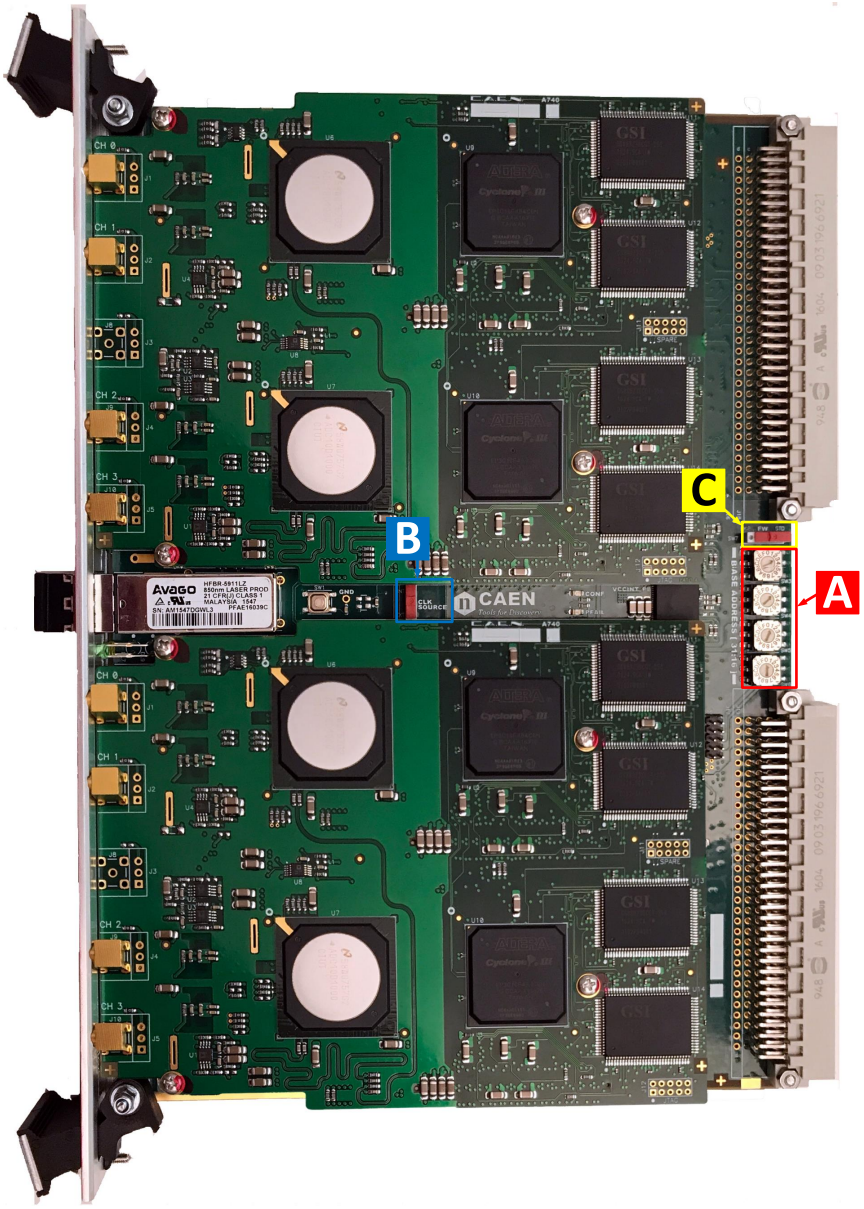


Fig. 8.2: Rotary and dip switches location.

A	**SW3,4,5,6**: **"Base Address [31:16]"**	**Type**: Rotary Switches	**Function**: Set the VME Base Address of the module
B	**SW2**: **"CLOCK SOURCE" INT/EXT**	**Type**: Dip Switch	**Function**: Selects the clock source (External or Internal)
C	**SW7**: **"FW" BKP/STD**	**Type**: Dip Switch	**Function**: Selects "Standard" (STD) or "Backup" (BKP) FLASH page as first to be read at power-on to load the FW on the FPGAs (default position is STD); see Sec. **13.1**

9 Functional Description

9.1 Analog Input Stage

Input dynamic is 1 V_{pp}; 200 mV_{pp} version is available upon request (see **Tab. 1.1**). In order to preserve the full dynamic range with unipolar input signal, positive or negative, it is possible to add a DC offset by means of a 16 bit DAC, which is up to $\pm$ 0.5 V @ 1 V_{pp} and $\pm$ 0.1 V @ 200 mV_{pp}. The input bandwidth ranges from DC to 500 MHz (with 2^{nd} order linear phase anti-aliasing low pass filter).

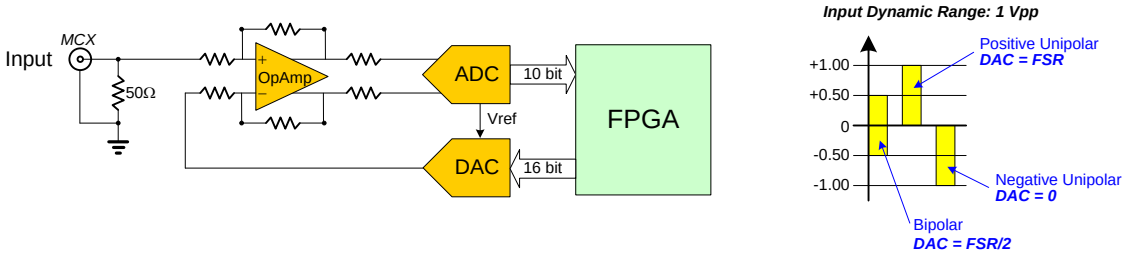


Fig. 9.1: Analog input diagram.

9.1.1 DC Offset Individual Setting

Setting the DC offset for channel n requires a write access at register addresses 0x1n98. Writing at 0x8098, the DC offset will apply to all channels at once. Refer to **[RD1]** for more details.

9.2 Clock Distribution

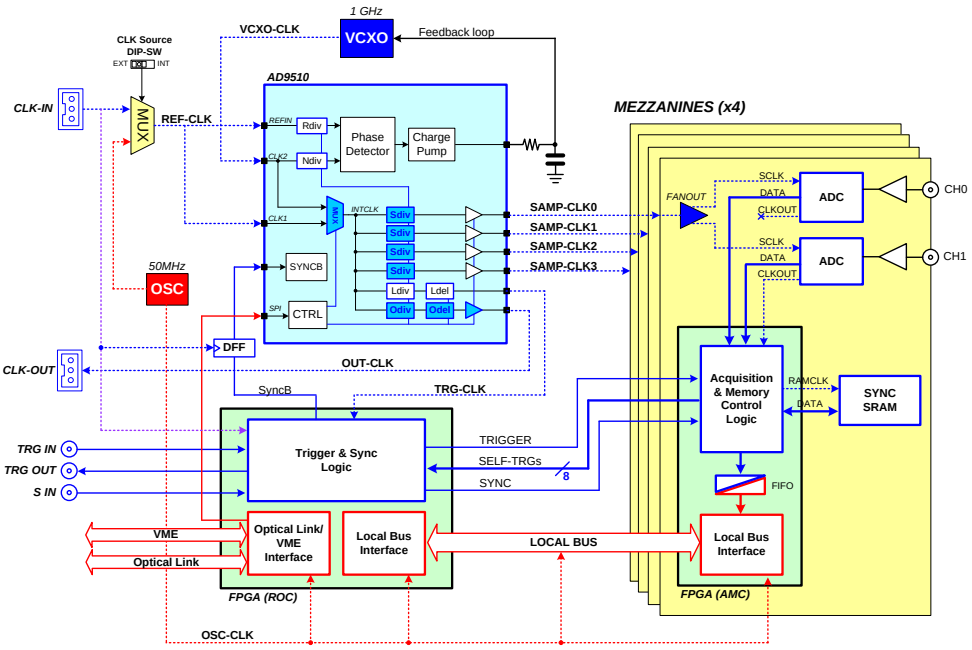


Fig. 9.2: Clock distribution diagram.

The clock distribution of the module takes place on two domains: OSC-CLK and REF-CLK.

OSC-CLK is a fixed 50-MHz clock coming from a local oscillator which handles VMEbus, Optical Link and Local Bus, that takes care of the communication between motherboard and mezzanines (see red traces in **Fig. 9.2**).

REF-CLK handles ADC sampling, trigger logic, and acquisition logic (samples storage into RAM, buffer freezing on trigger) through a clock chain. REF-CLK can be either an external (via the front panel CLK-IN connector) or an internal (via the 50-MHz local oscillator) source. In the latter mode, OSC-CLK and REF-CLK will be synchronous (the operation mode remains the same).

REF-CLK clock source selection can be done by an on-board dedicated dip switch (see **Fig. 8.2**) between the following modes:

- INT mode (default) means REF-CLK is the 50 MHz of the local oscillator (REF-CLK = OSC-CLK);
- EXT mode means REF-CLK source is the external frequency fed on CLK-IN connector.

The external clock signal must be differential (LVDS, ECL, PECL, LVPECL, CML) with a jitter lower than 100 ppm (see Chap. **3**). CAEN provides the A318 cable to adapt single ended signals coming from an external clock unit into the differential CLK-IN connector (see **Tab. 1.1**).

The V1751 is equipped with a phase-locked-loop (PLL) and clock distribution device, AD9510. It receives the REF-CLK and generates the sampling clock for ADCs and the mezzanine FPGA (SAMP-CLK0 up to SAMP-CLK3), as well as the trigger logic synchronization clock (TRG-CLK) and the output clock (CLK-OUT).

AD9510 configuration can be changed and stored into non-volatile memory. Changing the AD9510 configuration is primarily intended to be used for external PLL reference clock frequency change (see Sec. **9.3**). The V1751 locks to an external 50 MHz reference clock with default AD9510 configuration.

Refer to the AD9510 datasheet **[RD8]** for more details.

9.3 PLL Mode

The Phase Detector within the AD9510 device allows to couple REF-CLK with an external VCXO, which provides the nominal ADCs frequency (1 GS/s).

As introduced in Sec. **9.2**, the source of the REF-CLK signal (see **Fig. 9.2**) can be external on CLK-IN front panel connector or internal from the 50 MHz local oscillator. Programming the REF-CLK source internal or external can be performed by acting on the on-board dip switch SW2 (see Sec. **8.2**).

The following options are allowed:

1. 50 MHz internal clock source - this is the standard operation mode: the AD9510 dividers do not require to be reprogrammed (the digitizer works in the AD9510 default configuration). The clock source selection dip switch SW2 is in default INT mode. REF-CLK = OSC-CLK.
2. 50 MHz external clock source - in this case, the clock source is taken from an external device; the AD9510 dividers do not need to be reprogrammed as the external frequency is the same as the default one. The clock source selection dip switch must be set in EXT mode. CLK-IN = REF-CLK = OSC-CLK.
3. External clock source different from 50 MHz - the clock source is externally provided as in point 2, but the AD9510 dividers must now be reprogrammed to lock the the VCXO to the new REF-CLK in order to provide out the nominal sampling frequency at 1 GS/s. The clock source selection dip switch must be set in EXT mode. CLK-IN = REF-CLK $\neq$ OSC-CLK.

If the digitizer is locked, the PLL-LOCK front panel LED must be on.

Note: the user can configure the clock parameters, generate the PLL programming file and load it on the board by using the CAENUpgrader software tool (see Chap. **11**).

9.4 Reducing the Sampling Frequency

In case the board is required to work at a sampling frequency (SAMP-CLK) lower than the nominal, it can be achieved by reprogramming the AD9510 dividers. REF-CLK can be configured as in Sec. **9.3**. Not all the frequencies are admitted and a lower frequency limit must be considered, due to the internal electronics. Please contact CAEN (see Sec. **14**) to check the feasibility.

Note: The mimimum sampling frequency by hardware downsampling is 250 MS/s **[RD5]**.

9.5 Trigger Clock

The TRG-CLK logic works at 125 MHz, equal to 1/8 of the sampling frequency: TRG-CLK = 1/8· SAMPL-CLK. Eight samples of trigger “uncertainty” occurs over the acquisition window (16 samples uncertainty in DES mode).

9.6 Output Clock

The AD9510 output can be available on the front panel CLK-OUT connector (see **Fig. 9.2**). This option is particularly useful in case of multi-board synchronization to propagate the clock reference source in Daisy Chain. This option can be enabled by the user while configuring the PLL programming file in the CAENUpgrader software.

9.7 DES Mode

The board can be programmed to operate in Dual Edge Sampling (DES) mode, at 2 GS/s.

DES Mode is configurable by setting bit[12] = 1 of register 0x8000 (see **[RD1]**).

Note: Only even channels are managed when operating the digitizer in DES mode.

Note: DES mode is not available in case of DPP-PSD firmware usage.

9.8 Acquisition Modes

9.8.1 Channel Calibration

The module performs a self-calibration of the ADCs at its power-on. Anyway, in order to achieve the best performance, the calibration procedure is recommended to be executed by the user, on command, after the ADCs have stabilized their operating temperature. The calibration will not need to be repeated at each run unless the operating temperature changes significantly, or clock settings are modified (e.g. switching from internal to external clock).

The diagram below synthesises the flow for a proper calibration:

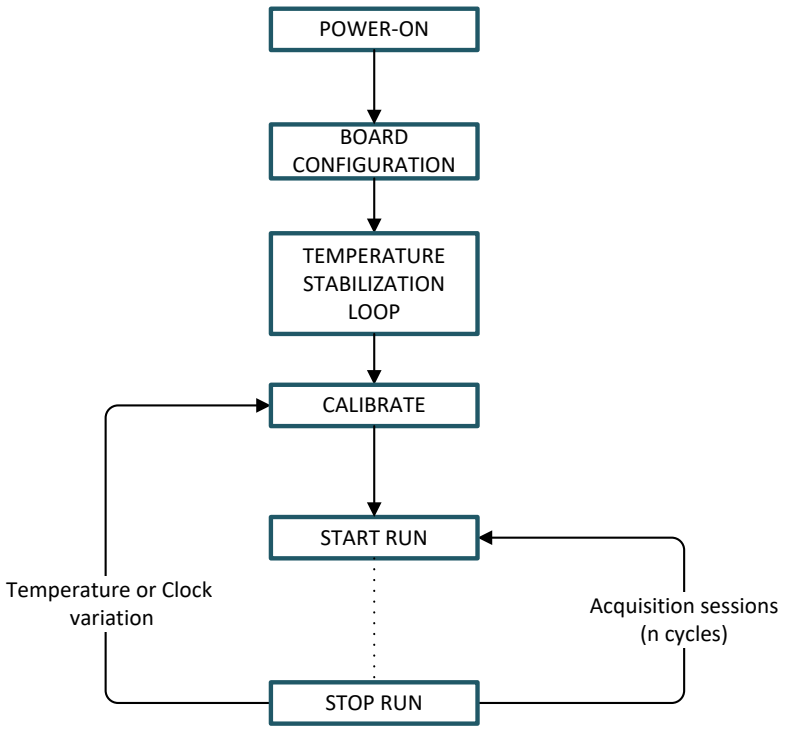


Fig. 9.3: Diagram of the ADCcalibration flow.

- At low level, the ADCs temperature can be read at the register address 0x1nA8 **[RD1]**, while the calibration must be performed through register address 0x809C. The following steps are required:
  - set bit[1] = 0 of register 0x809C;
  - set bit[1] = 1 of register 0x809C. The self calibration process will start simultaneously on each channel of the board and bit[6] of register 0x1n88 will be set to 0;
  - poll bit[6] of register 0x1n88 until it returns to 1 (few milliseconds);
  - set again bit[1] = 0 of register 0x809C.

  Steps in case of DES mode are:
  - make sure that EVEN channels are disconnected;
  - disable EVEN channels;
  - enable DES mode by setting bit[12] = 1 of register 0x8000;
  - set bit[1] = 0 of register 0x809C;
  - set bit[1] = 1 of register 0x809C. The self calibration process will start simultaneously on each channel of the board and bit[6] of register 0x1n88 will be set to 0;
  - poll bit[6] of register 0x1n88 until it returns to 1 (few milliseconds);
  - set again bit[1] = 0 of register 0x809C.

Note: Whenever switching from Normal mode to DES mode and vice-versa, the ADC calibration must be repeated.

Note: It is normally not required to calibrate after a board reset but, if a Reset command is intentionally issued to the digitizer (write access at register address 0xEF24) to be directly followed by a calibration procedure, it is recommended to wait for the board to reach stable conditions (indicatively 100 ms) before starting the calibration.

Note: At power-on, a Sync command is also issued by the firmware to the ADCs to synchronize all of them to the board's clock. In the standard operating, this command is not required to be repeated by the user. If a Sync command is intentionally issued (write access at register address 0x813C), the user must consider that a new calibration procedure is needed for a correct board operating.

- At the library level, developers can exploit the CAENDigitizer library (see Sec. **10.2**) dedicated routines which are *ReadTemperature()* function for temperature readings and the *Calibrate()* function which executes the channel calibration steps above described.

Note: Starting from CAENDigitizer release 2.6.1, the *Reset()* function has been modified so that it no longer includes the channel calibration routine implemented in the code. This calibration must be performed on command by the dedicated *Calibrate()* function. Please, see the Library user manual for reference ([RD9]).

- At software level, CAEN manages the command channel calibration in different readout software (please, refer the relevant software User Manual **[RD10]** and **[RD2]** for details).

  ◇ ***WaveDump***

  1. Lauch WaveDump. This software performs an automatic ADC calibration and displays a message when it is completed (see **Fig. 9.4**). This allows the user to start using the program sure that the digitizer has been calibrated at least once.

     NOTE THAT: If SKIP_STARTUP_CALIBRATION parameter is set to YES in WaveDump configuration file, the automatic start-up calibration is not performed and no message is displayed

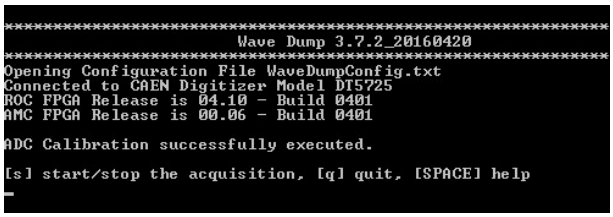


Fig. 9.4: Automatic calibration at WaveDump first run.

2. At any time, the user can check the channel temperatures (with the acquisition not running) by issuing multiple “m” commands from the keyboard.
3. In case of significant variations, issuing a “c” command provokes a manual channel calibration to be executed (see **Fig. 9.5**).

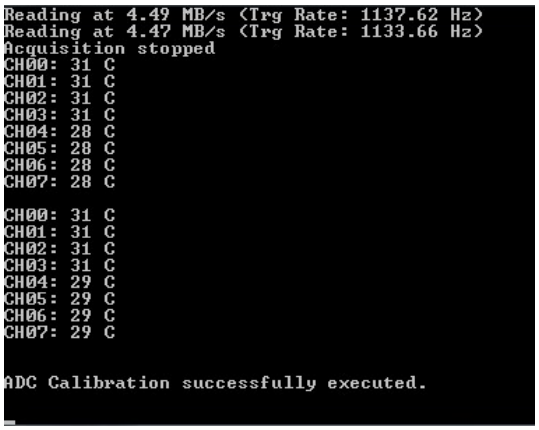


Fig. 9.5: Temperature monitoring with manual calibration in WaveDump software.

4. A new acquisition can start.

Please, refer to WaveDump User Manual for complete software description **[RD10]**.

♢ ***CoMPASS***

1. Launch CoMPASS Software
2. Connect to the digitizer
3. Before to start the acquisition, go to the “Input” tab and enable ”Calib.ADC” checkcell.
4. Start the acquisition: the calibration of the channel ADCs is performed at every start acquisition.

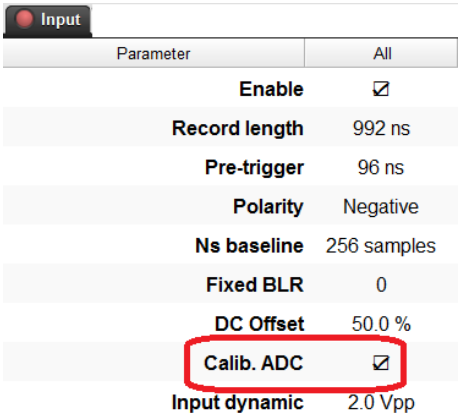


Fig. 9.6: Channel calibration in CoMPASS Software.

9.8.2 Acquisition Run/Stop

The acquisition can be started and stopped in different ways, according to bits[2:0] of register 0x8100 **[RD1]**:

- SW CONTROLLED (bits[1:0] = 00): Start and Stop take place by software command. Bit[2] = 0 means stopped, while bit[2] = 1 means running.
- S-IN CONTROLLED (bits[1:0] = 01): acquisition is armed by setting bit[2] = 1, the two options are selectable throuh bit[11] of the same register:
  - START/STOP ON LEVEL - If bit[11] = 0, then acquisition starts when the S-IN signal is high and stops when it is low; if bit[2] = 0 (disarmed), the acquisition is always off.
  - START ON EDGE - If bit[11] = 1, then acquisition starts on the rising edge of the S-IN signal and must be stopped by software command (bit[2] = 0).

Note: the START ON EDGE option is implemented from ROC FPGA fw revision 4.22 on.

- FIRST TRIGGER CONTROLLED (bits[1:0] = 10): bit[2] = 1 arms the acquisition and the Start is issued on the first trigger pulse (rising edge) on the TRG-IN connector. This pulse is not used as a trigger; actual triggers start from the second pulse on TRG-IN. The Stop acquisition must be SW controlled (i.e. reset of bit[2]).
- LVDS I/Os CONTROLLED: this mode acts like the S-IN CONTROLLED (bits[1:0] = 01), but using the configurable features of the signals on the LVDS I/Os connector (see Sec. **9.11**).

9.8.3 Acquisition Triggering: Samples and Events

When the acquisition is running, a trigger signal allows to:

- store a 31-bit counter value of the Trigger Time Tag (TTT).
  The counter (representing a time reference), like the Trigger Logic Unit (see **Fig. 9.2**), operates at a frequency of 125 MHz (i.e. 8 ns, that is to say 8 ADC clock cycles). Due to the way acquired data is written into the board internal memory (i.e. in 4-sample bunches), the TTT counter is read every 2 trigger logic clock cycles, which means the trigger time stamp resolution results in 16 ns (i.e. 62.5 MHz). Basing on that, the LSB of the TTT is always “0”;
- increment the EVENT COUNTER;
- fill the active buffer with the pre/post-trigger samples, whose number is programmable via register address 0x8114 **[RD1]**; the acquisition window width (also referred to as record length) is determined

via register addresses 0x800C and 0x8020; then, the buffer is frozen for readout purposes, while the acquisition continues on another buffer.

An event is therefore composed by the trigger time tag, pre- and post-trigger samples and the event counter.

Overlap between “acquisition windows” may occur (a new trigger occurs while the board is still storing the samples related to the previous trigger); this overlap can be either rejected or accepted (programmable via software by writing at register address 0x8000 **[RD1]**).

If the board is programmed to accept the overlapping triggers, as soon as the ”overlapping” trigger arrives, the current active buffer is filled up, then the samples storage continues on the subsequent one. In this case, not all events will have the same size (see Fig. **9.7**).

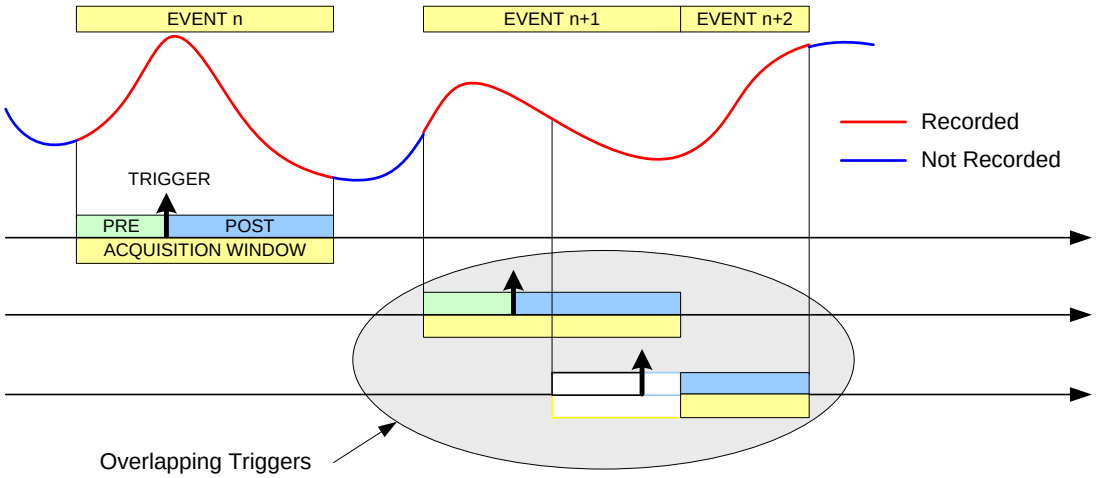


Fig. 9.7: Trigger Overlap.

A trigger can be refused for the following causes:

- Acquisition is not active.
- Memory is FULL and therefore there are no available buffers.
- The required number of samples for building the event pre-trigger is not reached yet; this happens typically as the trigger occurs too early either with respect to the RUN Acquisition command (see Sec. **9.8.2**) or with respect to a buffer emptying after a Memory FULL status (see Sec. **9.8.6**).
- The trigger overlaps the previous one and the board is not enabled for accepting overlapped triggers.

As a trigger is refused, the current buffer is not frozen and the acquisition continues writing on it. The EVENT COUNTER can be programmed in order to be either incremented or not. If this function is enabled, the EVENT COUNTER value identifies the trigger number sent (but the event number sequence is lost); if the function is not enabled, the EVENT COUNTER value coincides with the sequence of buffers saved and readout.

9.8.4 Multi-Event Memory Organization

Each channel of the V1751 features a SRAM memory to store the acquired events. The memory size in the standard event storage mode is 1.75 MS or 13.73 MS[1], where M = 1024 · 1024, according to the board version (see Tab **. 1.1**). The channel memory can be divided in a programmable number of buffers, N_b (N_b from 1 up to 1024), by the register address 0x800C **[RD1]**, as described in **Tab. 9.1**.

Note: in case of DES mode, values must be multiplied by 2.

Register Value BUFFER_CODE	Number of Buffers (N_b)	Size of one Buffer	
		SRAM 2.33 MB/ch (1.75 MS)	SRAM 18.3 MB/ch (13.73 MS)
0x00	1	2.333 MB/ch (1.75 MS)	18.3 MB/ch (13.73 MS)
0x01	2	1.167 MB/ch (896 kS)	9.1 MB/ch (6.8 MS)
0x02	4	597.2 kB/ch (448 kS)	4.6 MB (3.4 MS)
0x03	8	298.6 kB/ch (224 kS)	2.3 MB/ch (1.7 MS)
0x04	16	149.3 kB/ch (112 kS)	1.1 MB/ch (878.7 kS)
0x05	32	74.6 kB/ch (56 kS)	586.2 kB/ch (439.3 kS)
0x06	64	37.3 kB/ch (28 kS)	293.1 kB/ch (219.7 kS)
0x07	128	18.7 kB/ch (14 kS)	146.6 kB/ch (109.8 kS)
0x08	256	9.3 kB/ch (7 kS)	73.3 kB/ch (54.9 kS)
0x09	512	4.7 kB/ch (3.5 kS)	36.6 kB/ch (27.4 kS)
0x0A	1024	2.3 kB/ch (1.75 kS)	18.3 kB/ch (13.7 kS)

Tab. 9.1: Buffer organization of 751 family series. For each value of buffer size it is reported the memory size and the number of samples of one buffer, where k = 1024 and M = 1024 · 1024.

Having 1.75 MS memory size as reference, this means that each buffer contains $^{1.75M}/_{N_b}$ samples (e.g. N_b = 1024 means 1.75k samples in each buffer).

9.8.4.1 Custom size events

In case an event size less than the buffer size is needed, the user can set the N_LOC value at register address 0x8020 **[RD1]**, where N_LOC is the number of memory locations. The size of the event is so forced to be according to the formula:

$$1 \cdot N\_LOC = 7 \cdot N_{Sample} \text{ (normal mode)}$$

$$1 \cdot N\_LOC = 14 \cdot N_{Sample} \text{ (DES mode)}$$

When N_LOC = 0 the custom size is disabled.

Note: The value of N_LOC must be set in order that the relevant number of samples does not exceed the buffer size and it must not be modified while the acquisition is running. Even using the custom size setting, the number of buffers and the buffer size are not affected by N_LOC, but they are still determined by N_b.

The concepts of buffer organization and custom size directly affect the width of the acquisition window (i.e. number of the digitized waveform samples per event). The Record Length parameter defined in CAEN software (such as WaveDump and CAENScope introduced in Chap. **11**) and the *Set/GetRecordLength()* functions of the CAENDigitizer library rely on these concepts **[RD9]**.

[1] Memory size is 1.8 MS and 14.4 MS in case of M = 1000 · 1000.

9.8.5 Event structure

The event can be readout via VMEbus or Optical Link; data format is 32-bit long word (see **Fig. 9.10**).

An event is structured as:

- **Header** (four 32-bit words)
- **Data** (variable size and format)

9.8.5.1 Header

The Header consists of four words including the following information:

- **EVENT SIZE** (bits[27:0] of 1st header word) is the total size of the event, i.e. the number of 32-bit long words to be read.
- **BOARD ID** (bits[31:27] of 2nd header word) is the GEO address, meaningful for VME64X modules.
- **BOARD FAIL FLAG** (bit[26] of 2nd header word) implemented from ROC FPGA firmware revision 4.5 on (reserved otherwise), it is set to "1" in consequence of a hardware problem (e.g. PLL unlocking). The user can collect more information about the cause by reading at register address 0x8178 and contact CAEN Support Service if necessary (see Chap. **14**).
- **PATTERN/TRG OPTIONS** (bits[23:8] of 2nd header word) can be configured:
  - as 16-bit PATTERN latched on the LVDS I/Os as the trigger arrives
  - to provide trigger information

  setting bits[22:21] at register address 0x811C (see **Tab 9.2**).

Note: The PATTERN/TRG OPTIONS configuration is available starting from revision **4.6** of the ROC FPGA firmware.

REGISTER 0x811C Bits[22:21]	FUNCTIONAL DESCRIPTION	PATTERN /TRG OPTIONS INFORMATION (bit[23:8] of 2nd header word)
00 (default)	PATTERN	Pattern of the 16 LVDS signals
01	Event Trigger Source	Indicates the trigger source causing the event acquisition: Bits[23:19] = 00000 Bit[18] = Software Trigger Bit[17] = External Trigger Bit[16] = Trigger from LVDS connector Bits[15:8] = Channel self-trigger (refer to Sec. **9.9.3**)
10	Extended Trigger Time Tag (ETTT)	A 48-bit Trigger Time Tag (ETTT) information is configured, where Bits[23:8] contributes as the 16 most significant bits together to the 32-bit TTT field (4th header word) **Note**: in the ETTT option, the overflow bit is not provided
11	Not used	If configured, it acts like "00" setting

Tab. 9.2: Pattern/Trg Options configuration table.

- **CHANNEL MASK** (bits[7:0] of 2nd header word) is the mask of the channels participating in the event (e.g. CH5 and CH7 participating → Channel Mask = 0xA). This information must be used by the software to acknowledge from which channel the samples are coming (the first event contains the samples from the channel with the lowest number).

Note: in DES mode even channels are automatically disabled.

- **EVENT COUNTER** (bits[23:0] of 3rd header word) is the trigger counter; it can count either accepted triggers only, or all triggers (bit[3] of register address 0x8100).
- **TRIGGER TIME TAG** (bits[31:0] of 4th header word) is the 31-bit Trigger Time Tag (TTT) information, which is the trigger time reference (see Sec. **9.8.3**). The word is composed of the value of the 31-bit counter of the Trigger Time Tag (bit[30:0]) plus the overflow bit (bit[31]) indicating that the timestamp counter has overflowed at least once (**Fig. 9.8**). If the ETTT option is enabled, then this field becomes the 32 less significant bits of the 48-bit Extended Trigger Time Tag information in addition to the 16 bits (MSB) of the TRG OPTIONS field (2nd event word). Note that, in the ETTT case, the overflow bit is no more provided (**Fig. 9.9**). The trigger time tag is reset either at the start of acquisition, or via front panel signal on S-IN or LVDS I/O connectors, and increments with 250 MHz frequency (i.e. every 8 ADC clock cycles). The TTT value is read at half the frequency (i.e. 125 MHz) so that the specifications are 16 ns resolution and 17 s range (8 ns $\times$ ($2^{31}-1$)), which can be extended to 625 h (8 ns $\times$ ($2^{48}-1$)) if ETTT is enabled.

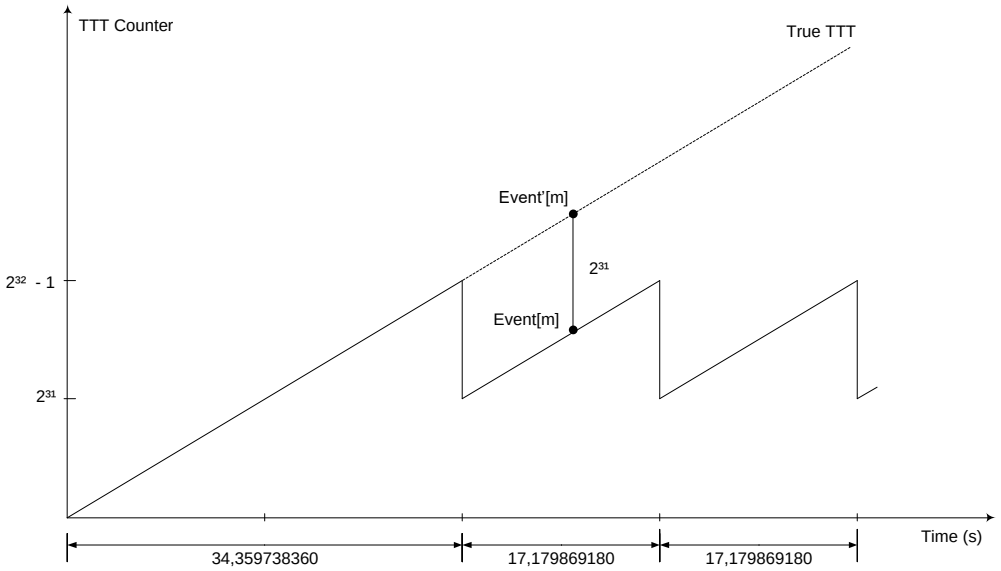


Fig. 9.8: TTT description.

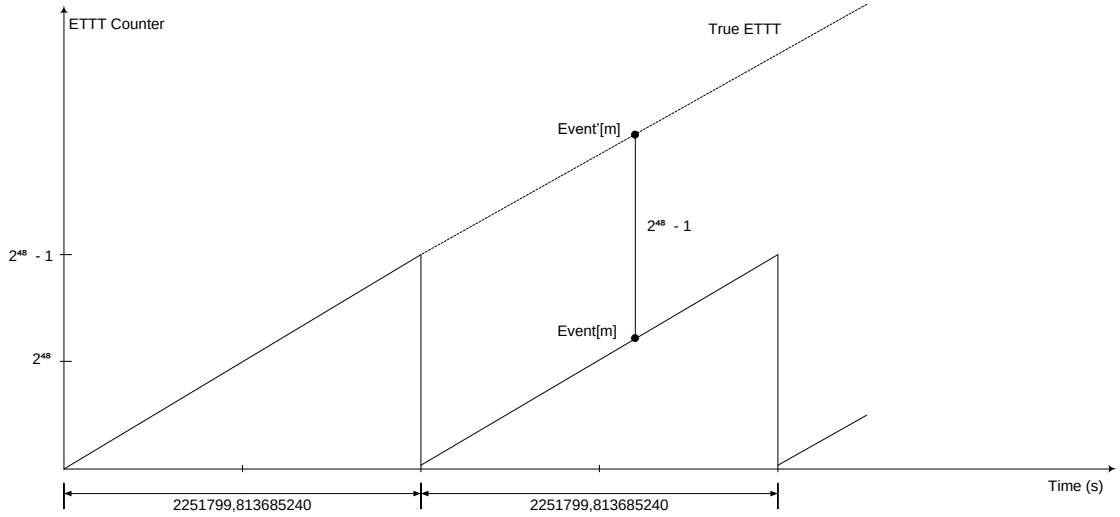


Fig. 9.9: ETTT description.

9.8.5.2 Data

Data are the stored samples. Data from masked channels are not read. When operating in DES mode the EVEN channels are automatically disabled. Bits[31:30] of the data words identifies how many samples are stored in the corresponding word. The example in Sec. **9.8.5.3** shows the case of two samples in the last word.

9.8.5.3 Event Format Examples

The event format is shown in the following figure (case of 8 channels enabled):

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

1	0	1	0	EVENT SIZE																												HEADER
BOARD ID						BF	RES	0	PATTERN/TRG OPTIONS																CHANNEL MASK							
RESERVED									EVENT COUNTER																							
TRIGGER TIME TAG																																
1	1	SAMPLE [2] - CH[0]										SAMPLE [1] - CH[0]										SAMPLE [0] - CH[0]										DATA CH0
1	1	SAMPLE [5] - CH[0]										SAMPLE [4] - CH[0]										SAMPLE [3] - CH[0]										
.....																																
1	0											SAMPLE [N-1] - CH[0]										SAMPLE [N-2] - CH[0]										
1	1	SAMPLE [2] - CH[1]										SAMPLE [1] - CH[1]										SAMPLE [0] - CH[1]										DATA CH1
1	1	SAMPLE [5] - CH[1]										SAMPLE [4] - CH[1]										SAMPLE [3] - CH[1]										
.....																																
1	0											SAMPLE [N-1] - CH[1]										SAMPLE [N-2] - CH[1]										
.....																																.....
1	1	SAMPLE [2] - CH[7]										SAMPLE [1] - CH[7]										SAMPLE [0] - CH[7]										DATA CH7
1	1	SAMPLE [5] - CH[7]										SAMPLE [4] - CH[7]										SAMPLE [3] - CH[7]										
.....																																
1	0											SAMPLE [N-1] - CH[7]										SAMPLE [N-2] - CH[7]										

Fig. 9.10: Event Format in Normal Mode.

Note: The firmware saves the waveforms in the memory of the digitizer with a granularity of n (i.e. in groups of n samples). This way of writing the waveforms in memory allows for a potential ΔT between the instant when the trigger physically arrives and when it is sensed by the digitizer. The resulting effect is a jitter in the acquisition window between one event and the next. This jitter can be observed by graphing the waveforms of the enabled channels using an acquisition software. The channels may jitter together between one event and the next, but not among themselves.

9.8.6 Acquisition Synchronization

Each channel of the digitizer is provided with a SRAM memory that can be organized in a programmable number N_b of circular buffers (N_b = [1 : 1024], see **Tab. 9.1**). When the trigger occurs, the FPGA writes further a programmable number of samples for the post-trigger and freezes the buffer, so that the stored data can be read via VME or Optical Link. The acquisition can continue in a new buffer.

When all buffers are filled, the board is considered FULL: no trigger is accepted and the acquisition stops (i.e. the samples coming from the ADC are not written into the memory, so they are lost). As soon as one buffer is read out and freed, the board exits the FULL condition and acquisition restarts.

IMPORTANT: When the acquisition restarts, no trigger is accepted until at least the entire buffer is written. This means that the dead time is extended for a certain time (depending on the size of the acquisition window) after the board exits the FULL condition.

A way to eliminate this extra dead time is by setting bit[5] = 1 at register address 0x8100 **[RD1]**. The board is so programmed to enter the FULL condition when $N_b - 1$ buffers are filled: no trigger is then accepted, but samples writing continues in the last available buffer. As soon as one buffer is read out and becomes free, the boards exits the FULL condition and can immediately accept a new trigger. This way, the FULL reflects the BUSY condition of the board (i.e. inability to accept triggers).

Note: when bit[5] = 1, the minimum number of circular buffers to be programmed is N_b = 2.

In some cases, the BUSY propagation from the digitizer to other parts of the system has some latency and it can happen that one or more triggers occur while the digitizer is already FULL and unable to accept those triggers. This condition causes event loss and it is particularly unsuitable when there are multiple digitizers running synchronously, because the triggers accepted by one board and not by other boards cause event misalignment.

In these cases, it is possible to program the BUSY signal to be asserted when the digitizer is close to FULL condition, but it has still some free buffers (Almost FULL condition). In this mode, the digitizer remains able to accept some more triggers even after the BUSY assertion and the system can tolerate a delay in the inhibit of the trigger generation. When the Almost FULL condition is enabled by setting the Almost FULL level to “X” (register address 0x816C **[RD1]**), the BUSY signal is asserted as soon as X buffers are filled, although the board still goes FULL (and rejects triggers) when the number of filled buffers is N_b or $N_b - 1$, depending on bit[5] at register address 0x8100 as described above.

It is possible to provide the BUSY signal on the digitizer front panel TRG-OUT output (bit[20], bits[19:18] and bits[17:16] at register address 0x811C are involved **[RD1]**). In case of multi-board setup, the BUSY signal can be propagated among boards through the front panel LVDS I/O connector (see Sec. **9.11**).

9.9 Trigger Management

When operating the waveform recording firmware, all board channels share the same trigger (board common trigger), so they acquire an event simultaneously and in the same way (determined number of samples according to buffer organization and custom size settings, as well as position with respect to the trigger defined by the post-trigger).

Note: For the trigger management in the DPP firmware operating, please refer to the DPP documentation **[RD2] [RD3]**.

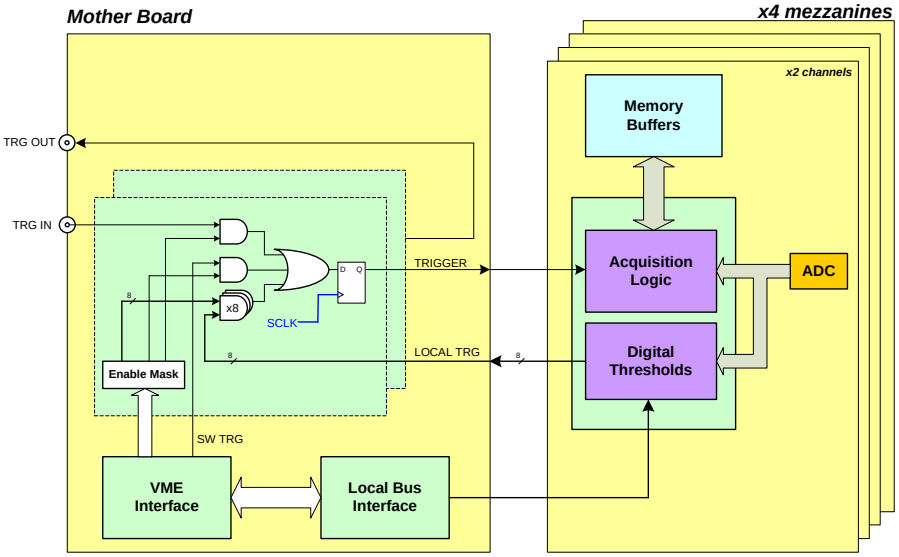


Fig. 9.11: Block diagram of Trigger management.

The digitizer supports different sources for the generation of the board common trigger (configurable at register address 0x810C):

- **Software Trigger**
- **External Trigger**
- **Self-trigger**
- **Coincidences**
- **TRG-IN as Gate**
- **LVDS I/O Trigger**

9.9.1 Software Trigger

Software triggers are internally produced via software command (write access at register address 0x8108) through VMEbus or Optical Link.

9.9.2 External Trigger

A TTL or NIM external signal can be provided to the front panel TRG-IN connector (configurable at register address 0x811C). When setting up a system of multiple digitizers (see Sec. **9.10**), there could be a random

jitter of 1 TRG-CLK hit (see Sec. **9.5**) if the external signal is provided asynchronously with the internal clock of the boards (e.g. from external trigger FAN-IN on TRG-IN). One board could then sense the trigger at clock_hit[N], while another board at clock_hit[N+1] and the same jitter is then present between the pulse acquired by one board and that acquired by the other board.

9.9.3 Self-Trigger

Each channel can generate a self-trigger signal (SELF-TRG) when the digitized input pulse exceeds a configurable threshold set through the register address 0x1n80 **[RD1]**.

The individual self-triggers from all channels are propagated to the central trigger logic on the motherboard (see **Fig. 9.11**) where they participate in logic OR to produce the board common trigger, which is finally distributed back to all channels on the mezzanines causing the event acquisition (see Sec. **9.9.7**).

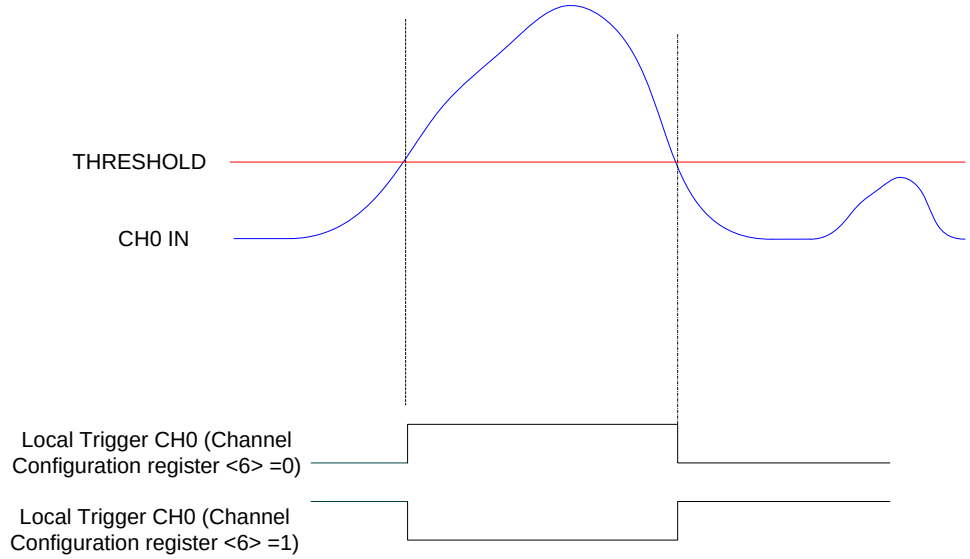


Fig. 9.12: Self-trigger generation.

Bits[7:0] of register 0x810C allows the user to program which channel participates to the global trigger generation.

9.9.4 LVDS I/O Trigger

LVDS I/O specific pins on the front panel dedicated connector can be programmed as trigger inputs and enabled to participate in the common trigger generation with other trigger sources. Refer to Sec. **9.11** for details.

9.9.5 Trigger Coincidence Level

Operating the waveform recording firmware, the acquisition trigger is common to the whole board. This common trigger allows the coincidence acquisition mode to be performed through the Majority operation.

Enabling the coincidences is possible by writing at register address 0x810C :

- Bits[7:0] enable a specific channel self-trigger to participate in the coincidence;
- Bits[23:20] set the coincidence window (T_{TVAW}) linearly in steps of the Trigger clock (8 ns);
- Bits[26:24] set the Majority (i.e. Coincidence) level;

The coincidence takes place when:

Number of enabled channels > Majority level

Supposing that bits[7:0] = FF (i.e. all channels are enabled) and bits[26:24] = 01 (i.e. Majority level = 1), a common trigger is issued whenever at least two of the enabled self-triggers are in coincidence within the programmed T_{TVAW}.

The Majority level must be smaller than the number of channels enabled via bits[7:0] mask. By default, bits[26:24] = 00 (i.e. Majority level = 0), which means the coincidence acquisition mode is disabled and the T_{TVAW} is meaningless. In this case, the common trigger is simple OR of the enabled channel self-triggers.

Note: in order not to overload the plots but preserve the clearness of concept, only CH0 and CH1 are supposed to be fed with input pulses in the following figures.

Fig. 9.13 shows the trigger management in case the coincidences are disabled.

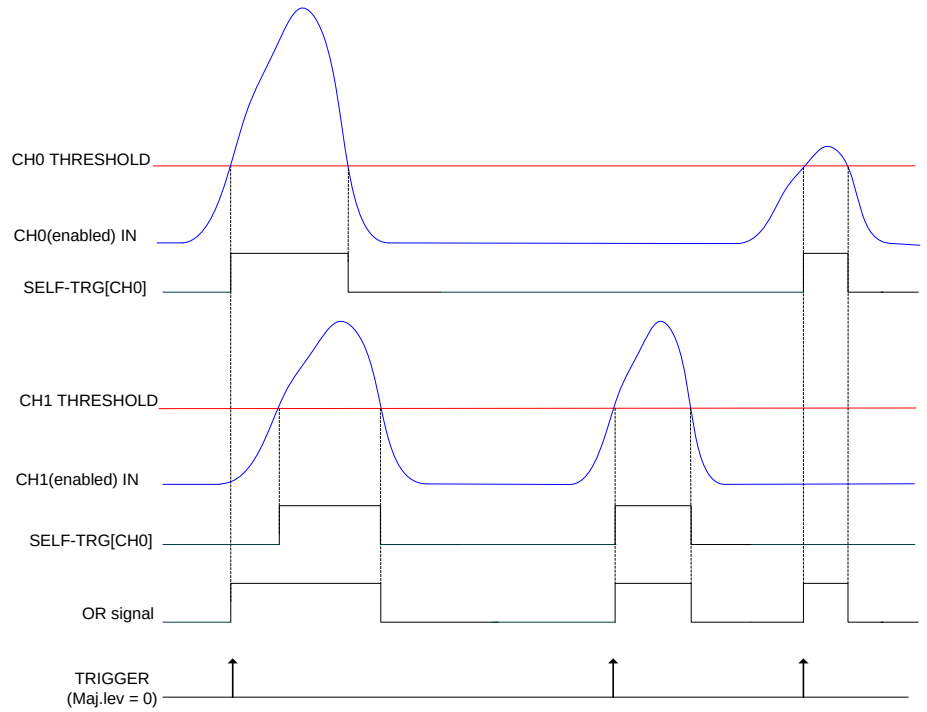


Fig. 9.13: Self-trigger relationship with Majority level = 0.

Fig. 9.14 shows the trigger management in case the coincidences are enabled with Majority level = 1 and T_{TVAW} is a value different from 0.

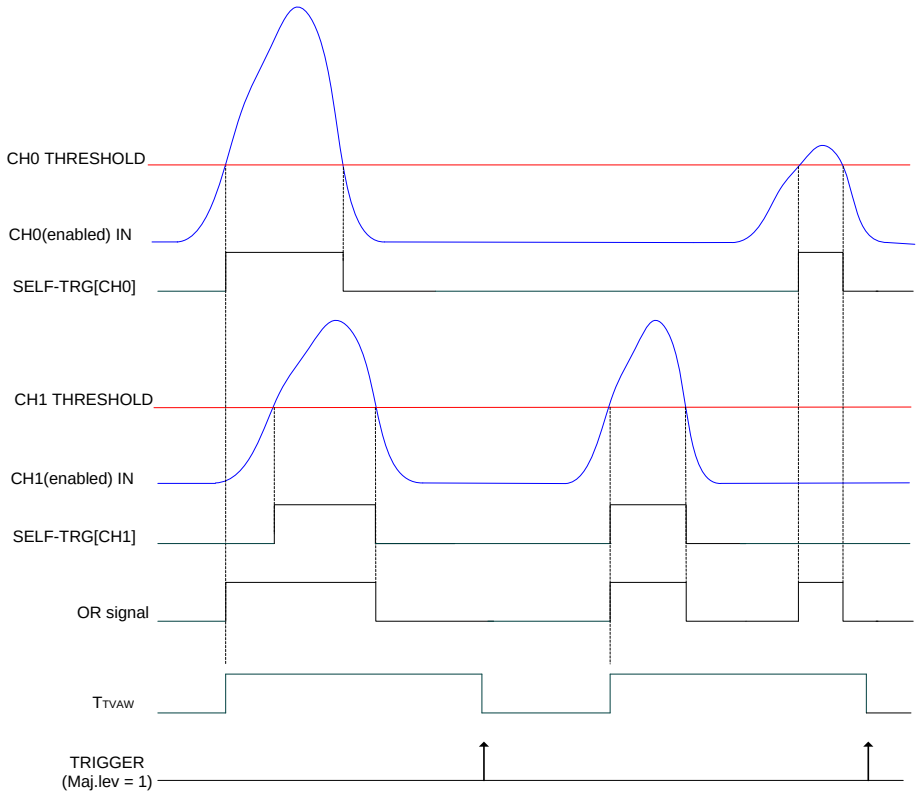


Fig. 9.14: Self-trigger relationship with Majority level = 1 and $T_{TVAW} \neq 0$.

Note: with respect to the position where the common trigger is generated, the portion of input signal stored depends on the programmed length of the acquisition window and on the post trigger setting.

Fig. 9.15 shows the trigger management in case the coincidences are enabled with Majority level = 1 and T_{TVAW} = 0 (i.e. 1 clock cycle).

Note: CAEN provides a guide to coincidences including a practical example of making coincidences with the waveform recording firmware **[RD11]**.

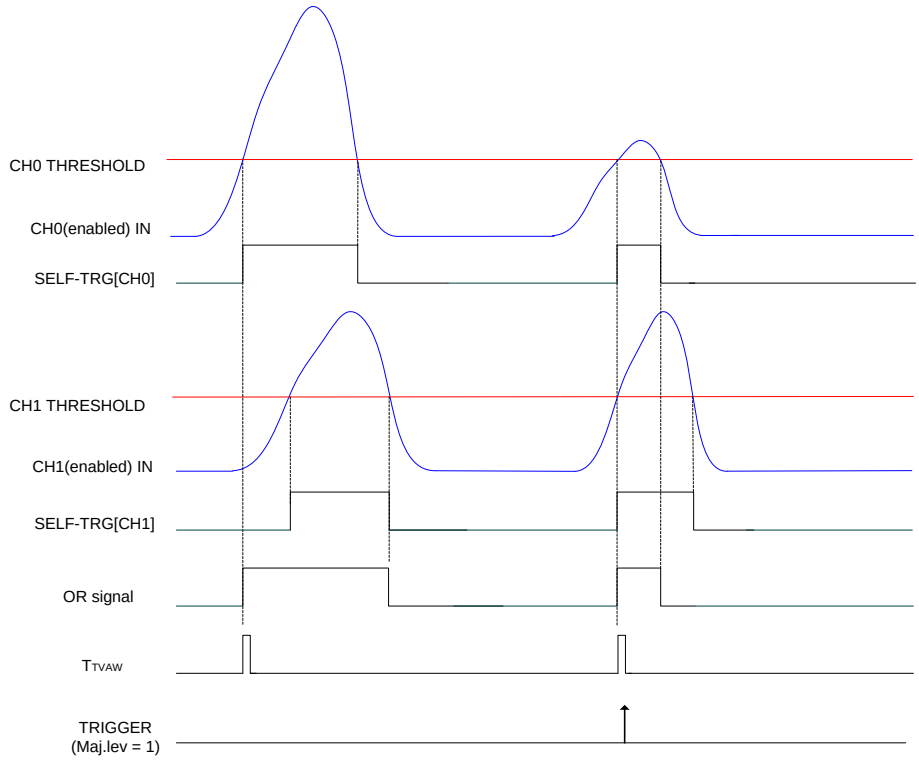


Fig. 9.15: Self-trigger relationship with Majority level = 1 and T_{TVAW} = 0.

9.9.6 TRG-IN as Gate

It is possible to configure TRG-IN as a gate for trigger anti-veto function. The common acquisition trigger is then issued upon the AND between the external signal on TRG-IN and the other trigger sources but the software trigger (i.e. the software trigger cannot participate in the Trigger as Gate mode).

This mode is enabled by setting bit[27] = 1 of register 0x810C and bit[10] = 1 of register 0x811C . The trigger sources participating in AND with TRG-IN are configurable through register 0x810C as well.

9.9.7 Trigger distribution

As described in Sec. **9.9**, the OR of all the enabled trigger sources, synchronized with the internal clock, becomes the common trigger of the board that is fed in parallel to all channels, consequently causing the capture of an event. By default, only the Software Trigger and the External Trigger participate in the common acquisition trigger (refer to the red path on top of **Fig. 9.16**).

A Trigger Out signal is also generated on the relevant front panel TRG-OUT connector (NIM or TTL), and allows to extend the trigger signal to other boards. Thanks to its configurability, TRG-OUT can propagate out:

- the OR of all the enabled trigger sources (only the Software Trigger is provided by default, as in the red path of **Fig. 9.16**);
- the OR, AND or MAJORITY exclusively of the channel self-triggers.

The registers involved in the TRG-OUT programming are:

- Register address 0x8110;
- Register address 0x811C.

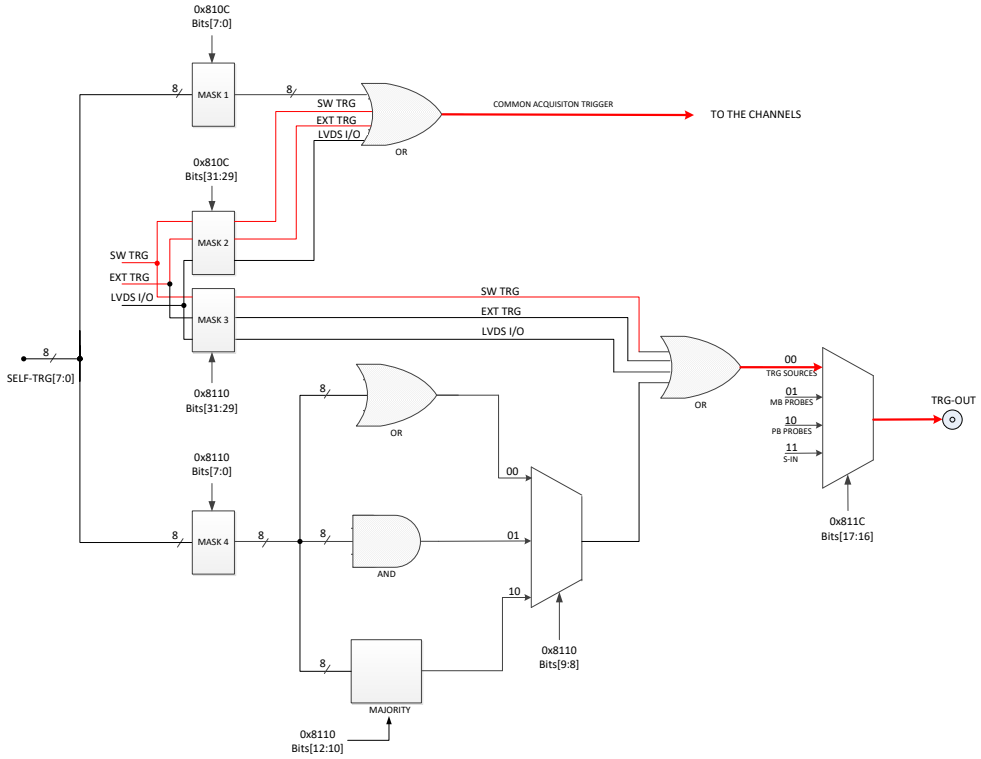


Fig. 9.16: Trigger configuration of TRG-OUT front panel connector.

9.9.7.1 Example

It could be required to start the acquisition on all the channels of a multi-board system as soon as one of the board channels (board “n”) crosses its threshold. Trigger Out signal is then fed to an external Fan Out logic unit (e.g. CAEN V2495 board); the obtained signal has then to be provided to the external trigger input TRG-IN of all the boards in the system (including the board which generated the Trigger Out signal). In this case, the programming steps to perform are thereafter described.

1. Register 0x8110 on board “n”:
   - Enable the desired self-trigger as Trigger Out signal on board “n” (by bits[7:0] mask).
   - Disable Software Trigger, External Trigger and LVDS I/O Trigger as Trigger Out signal on board “n” (bits[31:29] = 000).
   - Set Trigger Out signal as the OR of the enabled self-trigger on board “n” (bits[9:8] = 00).
2. Register 0x811C on board “n”:
   - Configure the digitizer to propagates on TRG-OUT the internal trigger sources according to the 0x8110 settings (i.e. the enabled self-trigger, in the specific case) on board “n” (bits[17:16] = 00).
3. Register 0x810C on all the boards in the system (including board “n”):
   - Enable External Trigger to participate in the board common acquisition trigger, disable Software Trigger , LVDS I/O Trigger and the channel self-triggers (bits[31:29] = 010; bits[7:0] = 00000000)

9.10 Multi-board Synchronization

When multi-board systems are involved in an experiment, it is necessary to synchronize different boards. In this way, the user can acquire from N boards with Y channel each, like if they were just one board with (N$\times$Y) channels.

While all the channels of the same board are simultaneously sampled at the same clock frequency by design, the main issue in the synchronization of a multi-board system is to have both the same ADC sampling clock and the same time reference for all boards. Having the same time reference means that the acquisition starts/stops at the same time, and that the time stamps of different boards is aligned to the same absolute time.

There are two alternative ways for the clock propagation:

- Daisy chain of the clock between boards through CLK-OUT / CLK-IN connector and the A317 clock distribution cable; one board is the “clock master” that propagates its own clock to the slave ones; a programmable phase shift can adjust possible delays in the clock propagation.
- One-to-many mode, based on an external clock unit like CAEN DT4700, which generates the needed reference clock and can provide it in fan-out on the CLK-IN connector of up to ten digitizers.

Other issues are the synchronization of the start of the run to let all the boards have the same zero for time stamps, the trigger synchronization to propagate and combine the triggers from all the boards to have the same common acquisition trigger, and the event data synchronization to keep event data aligned across boards (busy/veto management). For a detailed guide to multi-board synchronization, refer to **[RD12]**, or contact CAEN for clarifications (see Chap. **14**).

9.11 Front Panel LVDS I/Os

The V1751 is provided with 16 general purpose programmable LVDS I/O signals (see Chap. **8**). From the ROC FPGA firmware revision 3.8 on, a more flexible configuration management has been introduced, which allows these signals to be programmed in terms of direction (INPUT/OUTPUT) and functionality by groups of 4.

THE USER MUST SET BIT[8] = 1 AT 0x811C IN ORDER TO ENABLE THE NEW LVDS I/Os CONFIGURATION MODES

NOTE ABOUT LVDS I/Os CONFIGURATIONS IMPLEMENTED IN ROC FW RELEASES <3.8

THE WAVEFORM RECORDING FIRMWARE MAKES ALSO AVAILABLE THE OLD CONFIGURATIONS (bit[8] = 0). USERS WHOSE SOFTWARE BASES ON THE OLD LVDS I/Os CONFIGURATION MANAGEMENT CAN REFER TO THE USER MANUAL OF THE RELEVANT DIGITIZER OR CAN CONTACT CAEN FOR INFORMATION (see Chap. **14**).
SINCE THIS COULD BE NO LONGER GUARANTEED IN THE FUTURE, THE USER IS HEARTLY RECOMMENDED TO TAKE THE NEW CONFIGURATION MANAGEMENT AS REFERENCE!

The direction of the signals are set by the bits[5:2] at register address 0x811C:

Bit[2] → LVDS I/O[3:0]

Bit[3] → LVDS I/O[7:4]

Bit[4] → LVDS I/O[11:8]

Bit[5] → LVDS I/O[15:12]

Where setting the bit to 0 enables the relevant signals in the group as INPUT, while 1 enables them as OUTPUT.

By default, the new modes are disabled (i.e. bit[8] = 0) and the status of the LVDS I/O signals is congruent with the old Programmed I/O mode (see **Tab. 9.3**).

Nr.	Direction	Function	Description
0	out	Ch 0 self-trigger	The over-threshold information from the relevant channel
1	out	Ch 1 self-trigger	
2	out	Ch 2 self-trigger	
3	out	Ch 3 self-trigger	
4	out	Ch 4 self-trigger	
5	out	Ch 5 self-trigger	
6	out	Ch 6 self-trigger	
7	out	Ch 7 self-trigger	
8	out	Memory Full	Memory full flag
9	out	Event Data Ready	Board event data ready flag
10	out	Channels Trigger	OR of the new event to be read signal
11	out	RUN Status	Board run flag
12	in	Trigger Time Tag Reset (active low)	Reset of the trigger time tag counter
13	in	Memory Clear (active low)	Clear command of all channel memories
14	-	reserved	N.A.
15	-	reserved	N.A.

Tab. 9.3: Front Panel LVDS I/Os default settings.

When enabled (i.e. bit[8] = 1), the new management allows each group of 4 signals of the LVDS I/O 16-pin connector to be configured in one of the 4 following modes (according to bits[15:0] at register address 0x81A0):

- Mode 0 (bits[n+3:n] = 0000): REGISTER
- Mode 1 (bits[n+3:n] = 0001): TRIGGER
- Mode 2 (bits[n+3:n] = 0010): nBUSY/nVETO
- Mode 3 (bits[n+3:n] = 0011): LEGACY

where n = 0, 4, 8, 12.

Note: Whatever option is set, the LVDS I/Os are always latched with the trigger and the relevant status of the 16 signals is always written into the header Pattern field (see Sec. **9.8.5**); the user can then choose to read it out or not.

	REGISTER	TRIGGER	nBUSY/nVETO	LEGACY
LVDS IN [15:12]	Reg[15:12]	*Not available*	15: nRunIn 14: nTriggerIn 13: nVetoIn 12: nBusyIn	15: reserved 14: reserved 13: reserved 12: nClear_TTT
LVDS IN [11:8]	Reg[11:8]	*Not available*	11: nRunIn 10: nTriggerIn 9: nVetoIn 8: nBusyIn	11: reserved 10: reserved 9: reserved 8: nClear_TTT
LVDS IN [7:4]	Reg[7:4]	*Not available*	7: nRunIn 6: nTriggerIn 5: nVetoIn 4: nBusyIn	7: reserved 6: reserved 5: reserved 4: nClear_TTT
LVDS IN [3:0]	Reg[3:0]	*Not available*	3: nRunIn 2: nTriggerIn 1: nVetoIn 0: nBusyIn	3: reserved 2: reserved 1: reserved 0: nClear_TTT

Tab. 9.4: Features description when LVDS group is configured as INPUT (waveform recording firmware).

	REGISTER	TRIGGER	nBUSY/nVETO	LEGACY
LVDS IN [15:12]	Reg[15:12]	TrigIn_Couple[7:4]	15: nRunIn 14: reserved 13: reserved 12: reserved	15: reserved 14: reserved 13: reserved 12: reserved
LVDS IN [11:8]	Reg[11:8]	TrigIn_Couple[3:0]	11: nRunIn 10: reserved 9: reserved 8: reserved	11: reserved 10: reserved 9: reserved 8: reserved
LVDS IN [7:4]	Reg[7:4]	TrigIn_Couple[7:4]	7: nRunIn 6: reserved 5: reserved 4: reserved	7: reserved 6: reserved 5: reserved 4: reserved
LVDS IN [3:0]	Reg[3:0]	TrigIn_Couple[3:0]	3: nRunIn 2: reserved 1: reserved 0: reserved	3: reserved 2: reserved 1: reserved 0: reserved

Tab. 9.5: Features description when LVDS group is configured as INPUT (DPP firmware).

	REGISTER	TRIGGER	nBUSY/nVETO	LEGACY
LVDS OUT [15:12]	Reg[15:12]	TrigOut_Ch[7:4]	15: nRun 14: nTrigger 13: nVeto 12: nBusy	15: Run 14: Trigger 13: DataReady 12: Busy
LVDS OUT [11:8]	Reg[11:8]	TrigOut_Ch[3:0]	11: nRun 10: nTrigger 9: nVeto 8: nBusy	11: Run 10: Trigger 9: DataReady 8: Busy
LVDS OUT [7:4]	Reg[7:4]	TrigOut_Ch[7:4]	7: nRun 6: nTrigger 5: nVeto 4: nBusy	7: Run 6: Trigger 5: DataReady 4: Busy
LVDS OUT [3:0]	Reg[3:0]	TrigOut_Ch[3:0]	3: nRun 2: nTrigger 3: nVeto 0: nBusy	3: Run 2: Trigger 1: DataReady 0: Busy

Tab. 9.6: Features description when LVDS group is configured as OUTPUT (waveform recording firmware).

	REGISTER	TRIGGER	nBUSY/nVETO	LEGACY
LVDS OUT [15:12]	Reg[15:12]	TrigOut_Ch[7:4]	15: nRun 14: reserved 13: reserved 12: reserved	15: Run 14: reserved 13: reserved 12: reserved
LVDS OUT [11:8]	Reg[11:8]	TrigOut_Ch[3:0]	11: nRun 10: reserved 9: reserved 8: reserved	11: Run 10: reserved 9: reserved 8: reserved
LVDS OUT [7:4]	Reg[7:4]	TrigOut_Ch[7:4]	7: nRun 6: reserved 5: reserved 4: reserved	7: Run 6: reserved 5: reserved 4: reserved
LVDS OUT [3:0]	Reg[3:0]	TrigOut_Ch[3:0]	3: nRun 2: reserved 3: reserved 0: reserved	3: Run 2: reserved 1: reserved 0: reserved

Tab. 9.7: Features description when LVDS group is configured as OUTPUT (DPP firmware).

9.11.1 Mode 0: REGISTER

Direction is INPUT: the logic level of the LVDS I/O signals can be read at register address 0x8118.

Direction is OUTPUT: the logic level of the LVDS I/O signals can be written at register address 0x8118.

9.11.2 Mode 1: TRIGGER

Direction is INPUT: Not available.

Direction is OUTPUT: the TrgOut_Ch[(n + 3) : n] signals (n = 0, 4) consist of the channel self-triggers coming directly from the mezzanines.

9.11.3 Mode 2: nBUSY/nVETO

Note: In case a DPP firmware is loaded on the FLASH page, only the nRun signal (among those described below) is available in the nBusy/nVETO mode (see **Tab. 9.5** and **Tab. 9.7**).

nBusy Signal

nBusyIn (INPUT) is an active low signal which, if enabled, is used to generate the nBusy signal (OUTPUT) as below.

The Busy signal (fed out on LVDS I/Os or TRG-OUT LEMO connector) is:

Almost_Full OR **(LVDS_BusyIn** AND **BusyIn_enable)**

where

- **Almost_Full** indicates the filling of the Buffer Memory up to a programmable level (12-bit range) set at register address 0x816C;
- **LVDS_BusyIn** is available in nBUSY/nVETO configuration (see **Tab. 9.6**);
- **BusyIn_enable** is set at register address 0x8100, bit[8].

nVETO Signal

Direction is INPUT: nVETOIn is an active low signal which, if enabled (register address 0x8100, bit[9] = 1), is used to veto the generation of the common trigger propagated to the channels for the event acquisition.

Direction is OUTPUT: the nVETO signal is the copy of nVETOIn.

nTrigger Signal

Direction is INPUT: nTriggerIn is an active low signal which, if enabled, is a real trigger able to cause the event acquisition. It can be propagated to TRG-OUT LEMO connector or to the individual triggers.

Direction is OUTPUT: nTrigger signal is the copy of the trigger signal propagated to the TRG-OUT LEMO connector or copy of the acquisition common trigger. This is selected by bit[16] of the 0x81A0 register.

nRun Signal

Direction is INPUT: nRunIn is an active low signal which can be used as Start for the digitizer (register address 0x8100, bits[1:0] = 11). It is possible to program the Start on the level or on the edge of the nRunIn signal (register address 0x8100, bit[11]).

Direction is OUTPUT: nRun signal is the inverse of the internal Run of the board.

9.11.4 Mode 3: LEGACY

Legacy Mode has been introduced in order the LVDS connector (properly programmed) to be able to feature the same I/O signals available in the ROC FPGA firmware revisions lower than 3.8.

nClear_TTT Signal

It is the only signal available as INPUT. It is the Trigger Time Tag (TTT) reset, like in the old configuration.

Busy Signal

The Busy signal is active high and it is exactly the inverse of the nBusy signal (see Sec. **9.11.3**).

In case register address 0x816C is set to 0x0 and the BusyIn signal is disabled, the Busy is the FULL signal present in the old configuration.

DataReady Signal

The DataReady is an active high signal indicating that the board has data available for readout (the same as the DataReady front panel LED does).

Trigger Signal

The active high Trigger signal is the copy of the acquisition trigger (common trigger) sent from the motherboard to the mezzanines (it is neither the signal provided out on the TRG-OUT LEMO connector nor the inverse of the signal sent to the LVDS connector).

Run Signal

The Run signal is active high and represents the inverse of the nRun signal (see Sec. **9.11.3**).

Note: The Memory Clear is not implemented in the LEGACY LVDS configuration mode.

9.12 Analog Monitor

The board houses a 12bit (125 MHz) DAC with 0 ÷ 1 V dynamics on a 50 Ω load (see **Fig. 2.1**), whose input is controlled by the ROC FPGA and the signal output (driving 50 Ω) is available on the MON/Σ output connector. MON output of more boards can be summed by an external Linear Fan In.

The DAC control logic implements four operating modes according to the value of bits[2:0] at register address 0x8144:

- Trigger Majority Mode (0x8144 = 0x0)
- Test Mode (0x8144 = 0x1)
- Buffer Occupancy Mode (0x8144 = 0x3)
- Voltage Level Mode (0x8144 = 0x4)

9.12.1 Trigger Majority Mode

It is possible to generate a Majority signal with the DAC: a voltage signal whose amplitude is proportional to the number of channels under/over threshold (1 step = 125 mV); this allows, via an external discriminator, to produce a common trigger signal, as the number of triggering channels has exceeded a particular threshold.

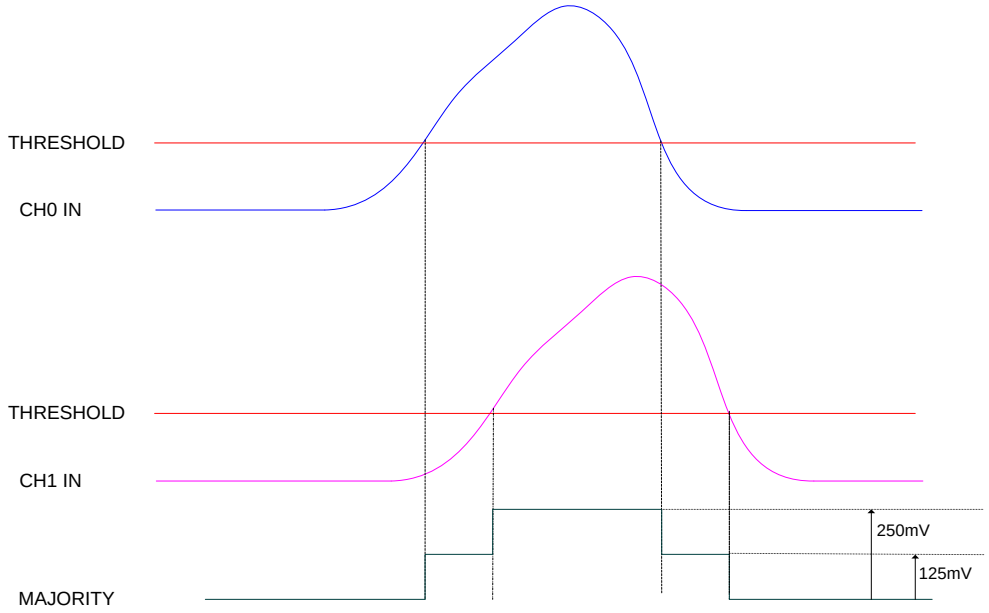


Fig. 9.17: Majority logic (2 channels over-threshold; bit[6]=0 register address 0x8000).

In the example depicted in **Fig. 9.17**, the MON output provides a signal whose amplitude is proportional to the number of channels over the trigger threshold.

9.12.2 Test Mode

In this mode the MON output provides a sawtooth signal with 1 V amplitude and 30.52 kHz frequency.

9.12.3 Buffer Occupancy Mode

In this mode, MON output connector provides a voltage value increasing, proportionally with the number of buffers filled with events, in fixed steps of 0.976 mV given by:

$$\frac{V_{max}}{N_{bmax}}$$

where $V_{max} \approx 1$ V and $N_{bmax} = 1024$ is the Maximum_Number_of_Buffers (i.e. the value of the register address 0x800C, as introduced in Sec. **9.8.4**).

Example: if 0x800C = 0x4 (i.e. 16 buffers), the maximum Buffer Occupancy output voltage level is given by 0.976 mV $\times$ 16.

This mode allows to test the readout efficiency: in fact, if the average event readout throughput is as fast as trigger rate, then MON out value remains constant; otherwise if MON out value grows in time, this means that readout rate is slower than trigger rate.

Starting from revision **4.9** of the ROC FPGA (motherboard) firmware, it is possible to apply a digital gain to the fixed step, particularly when the memory is organized in a small number of buffers. The gain can be set as powers of two ranging between $2^0 = 1$ (no gain, which is the default setting) and 2^A, where the exponent is the value to write at register address 0x81B4.

9.12.4 Voltage Level Mode

In this mode, MON out provides a voltage value programmable via the 12-bit 'N' parameter written in the 0x8138 register, with: $V_{mon} = 1/4096 \times N$ (Volt).

9.13 Test Pattern Generator

The FPGA AMC can emulate the ADC and write into memory a sawtooth signal for test purposes. It can be enabled via register 0x8000. **Fig. 9.18** shows the test ramps for even and odd channels respectively.

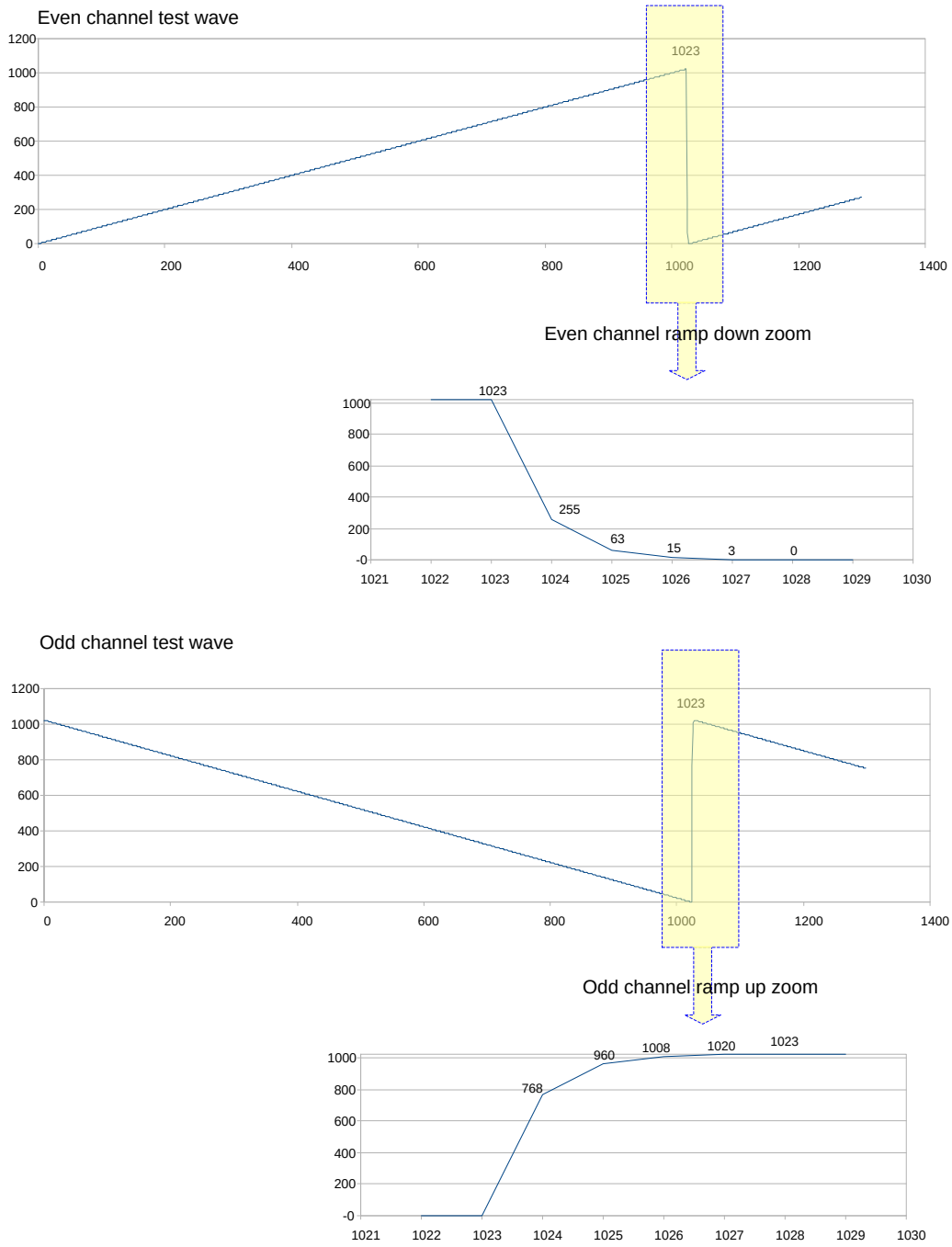


Fig. 9.18: FPGA Test Waveform.

9.14 Reset, Clear and Default Configuration

9.14.1 Global Reset

Global Reset is performed at power-on of the module or via software by write access at register address 0xEF24 . It allows to clear the data off the Output Buffer, the event counter and performs a FPGAs global reset, which restores the FPGAs to the default configuration. It initializes all counters to their initial state and clears all detected error conditions.

9.14.2 Memory Reset

The Memory Reset clears the data off the Output Buffer.

The Memory Reset can be forwarded via a write access at register address 0xEF28. In the old LVDS I/O configuration (ROC FPGA revision before **3.8**), it is also possible to perform a memory clear by sending a pulse to the front panel dedicated Memory Clear input (see **Tab. 9.3**).

9.14.3 Timer Reset

The Timer Reset allows to initialize the timer which tags an event. Time counters are reset after a SW Clear command (register address 0xEF28); the reset (leading edge sensitive) can also be forwarded with a pulse sent either to the front panel Trigger Time Tag Reset input of LVDS I/Os (see **Tab. 9.3** and Sec. **9.11.4**) or to the S-IN input.In case the S-IN connector needs to be used to reset the trigger time stamps, no configurations or access to registers are necessary. The user only has to transmit a NIM or TTL signal to the input, depending on the software selected logic level for the S-IN connector. The time stamps reset occurs at every leading edge of the logic signal sent to the S-IN connector.

9.15 VMEBus Interface

The module is provided with a fully compliant VME64/VME64X interface, whose main features are:

- EUROCARD 9U Format
- J1/P1 and J2/P2 with either 160 pins (5 rows) or 96 (3 rows) connectors
- A24, A32 and CR-CSR address modes
- D32, BLT/MBLT, 2eVME, 2eSST data modes
- MCST write capability
- CBLT data transfers
- RORA interrupter
- Configuration ROM

9.15.1 Addressing Capabilities

- Base address: the module works in A24/A32 mode The Base Address of the module is selected through four rotary switches (see **Fig. 8.2**), then it is validated only with either a power-ON cycle or a System Reset (see Sec. **9.14**).

ADDRESS MODE	ADDRESS RANGE	NOTES
A24	[0x000000:0xFF0000]	SW2 and SW3 ignored

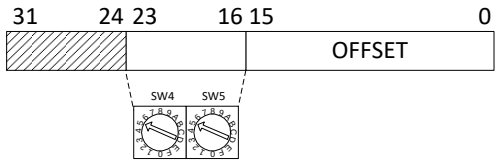


Fig. 9.19: A24 addressing.

ADDRESS MODE	ADDRESS RANGE	NOTES
A32	[0x00000000:0xFFFF0000]	

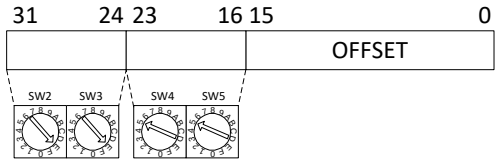


Fig. 9.20: A32 addressing.

- CR/CSR address: the addressing is based on the slot number taken from the relevant backplane lines. The recognised Address Modifier for this cycle is 2F. *This feature is implemented only on versions with 160-pin connectors.*

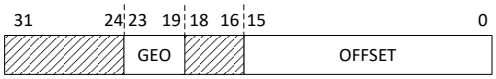


Fig. 9.21: CR/CSR addressing.

9.15.2 Address Relocation

The bit[15:0] of register address 0xEF10 allow to set via software the board Base Address (valid values ≠ 0). Such register allows to overwrite the rotary switches settings; its setting is enabled via bit[6] of the register address 0xEF00. The used addresses are:

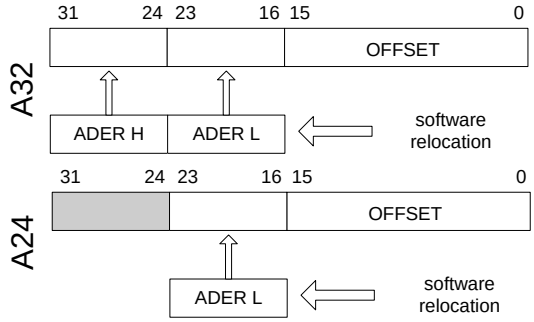


Fig. 9.22: Software relocation of base address.

9.16 Data Transfer Capabilities and Events Readout

The board features a Multi-Event digital memory per channel, configurable by the user to be divided into 1 up to 1024 buffers, as detailed in Sec. **9.8.4**. Once they are written in the memory, the events become available for readout via VMEbus or Optical Link. During the memory readout, the board can store other events (independently from the readout) on the available free buffers.

The events are read out sequentially and completely, starting from the Header of the first available event, followed by the samples of the enabled channels (from 0 to 7) as reported in **Fig. 9.10**. Once an event is completed, the relevant memory buffer becomes free and ready to be written again (old data are lost). After the last word in an event, the first word (Header) of the subsequent event is readout. It is not possible to read out an event partially.

The size of an event (EVENT SIZE) is configurable and depends on register addresses 0x8020 and 0x800C , as well as on the number of enabled channels. The board supports D32 single data readout, Block Transfer BLT32 and MBLT64, 2eVME and 2eSST cycles. Sustained readout rate is up to 60 MB/s with MBLT64, up to 100 MB/s with 2eVME and up to 160 MB/s with 2eSST.

9.16.1 Block Transfer D32/D64, 2eVME, and 2eSST

The Block Transfer readout mode allows to read N complete events sequentially, where N is set at register address 0xEF1C , or by using the *SetMaxNumEventsBLT* function of the CAENDigitizer library **[RD9]**.

When developing programs, the readout process can be implemented on different basis :

- Using **Interrupts**: as soon as the programmed number of events is available for readout, the board sends an interrupt to the PC over the optical communication link **(not supported by USB)**.
- Using **Polling** (interrupts disabled): by performing periodic read accesses to a specific register of the board it is possible to know the number of events present in the board and perform a BLT read of the specific size to read them out.
- Using **Continuous Read** (interrupts disabled): continuous data read of the maximum allowed size (e.g. total memory size) is performed by the software without polling the board. The actual size of the block read is determined by the board that terminates the BLT access at the end of the data, according to the configuration of register address 0xEF1C, or the library function *SetMaxNumEventsBLT* mentioned above. If the board is empty, the BLT access is immediately terminated and the “Read Block” function will return 0 bytes (it is the *ReadData* function in the CAENDigitizer Library).

The event is configurable as indicated in the introduction of the paragraph, namely:

[Event Size] = [8*(Buffer Size)] + [16 bytes]

Then, it is necessary to perform as many cycles as required in order to readout the programmed number of events.

It is suggested to enable BERR signal during BLT32 cycles, in order to end the cycle avoiding filler readout. The last BLT32 cycle will not be completed, it will be ended by BERR after the #N event in memory is transferred (see example in the figure below).

Since some 64-bit CPU cut off the last 32- bit word of a transferred block, if the number of words composing such block is odd, it is necessary to add a dummy word (which has then to be removed via software) in order to avoid data loss. This can be achieved by setting the ALIGN64 bit (bit[5]) at register address 0xEF00.

MBLT64 cycle is similar to the BLT32 cycle, except that the address and data lines are multiplexed to form 64 bit address and data buses.

The 2eVME allows to achieve higher transfer rates thanks to the requirement of only two edges of the two control signals (DS and DTACK) to complete a data cycle

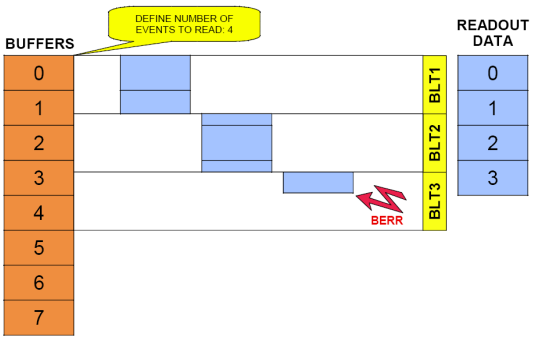


Fig. 9.23: Example of BLT readout.

9.16.2 Chained Block Transfer D32/D64

The V1751 allows to readout events from more daisy chained boards (Chained Block Transfer mode).

The technique which handles the CBLT is based on the passing of a token between the boards; it is necessary to verify that the used VME crate supports such cycles.

Several contiguous boards, in order to be Daisy chained, must be configured as “first”, “intermediate” or “last” via register address 0xEF0C. A common Base Address is then defined via the same register; when a BLT cycle is executed at the address CBLT_Base + 0x0000 ÷ 0x0FFC, the “first” board starts to transfer its data, driving DTACK properly; once the transfer is completed, the token is passed to the second board via the IACKIN-IACKOUT lines of the crate, and so on until the “last” board, which completes the data transfer and asserts BERR (which has to be enabled): the Master then ends the cycle and the slave boards are rearmed for a new acquisition.

If the size of the BLT cycle is smaller than the events size, the board which has the token waits for another BLT cycle to begin (from the point where the previous cycle has ended).

9.16.3 Single D32 Transfer

This mode allows the user to readout a word per time, from the header (actually 4 words) of the first available event, followed by all the words until the end of the event, then the second event is transferred. The exact sequence of the transferred words is shown in Sec. **9.8.5**.

It is suggested, after the 1^{st} word is transferred, to check the EVENT SIZE information and then do as many cycles as necessary (actually EVENT SIZE -1) in order to read completely the event.

9.17 Optical Link Access

The board houses a daisy chainable Optical Link (communication path which uses optical fiber cables as physical transmission line) able to transfer data at 80 MB/s supported by CAEN A2818 PCI, A3818 PCIe controllers, and A4818 USB3 adapter (see **Tab. 1.1**).

A single link can connect up to 8 digitizers in Daisy chain, so a maximum of 8 boards can be Daisy chained by the single-link A2818 card or the A4818 adapter, and a maximum of 32 boards by the 4-link A3818 card (A3818C).

All the information on CAEN PCI/PCIe controllers and PCIe adapter can be found on CAEN website at the A2818, A3818, and A4818 pages.

The parameters for read/write accesses via Optical Link are the same used by VME cycles (Address Modifier, Base Address, data Width, etc). Wrong parameter settings cause Bus Error.

Bit[3] at register address 0xEF00 enables the module to broadcast an interrupt request on the Optical Link (not supported on A4818); the enabled Optical Link Controllers propagate the interrupt on the PCI bus when a request from the Optical Link is sensed. Interrupts can also be managed at the CAENDigitizer library level **[RD9]**.

VME and Optical Link accesses take place on independent paths and are handled by board internal controller, with VME having higher priority; anyway it is better to avoid accessing the board via VME and Optical Link simultaneously.

Note: CONET2 is CAEN proprietary serial protocol developed to allow the optical link communication between the host PC, equipped with a A2818 or a A3818 Controller, or a A4818 Adapter, and a CAEN CONET slave. CONET2 is 50% more efficient in the data rate transfer than the previous CONET1 version. The two protocol versions are not compliant to each other and before to migrate from CONET1 to CONET2 it is recommended to read the instructions provided by CAEN in the dedicated Application Note **[RD13]**.

Note: The CONET protocol implemented in the A4818 adapter from USB-3.0 to Optical Link does not support the interrupts.

10 Drivers & Libraries

10.1 Drivers

In order to interface with the board, CAEN provides the drivers for the supported physical communication channels and compliant with Windows® and Linux® OS:

- **CONET Optical Link**, managed by the A2818 PCI card (Obsolete), the A3818 PCIe card or the A4818 Adapter. The driver installation package is available on CAEN website in the "Software/Firmware" tab at the A2818, A3818 and A4818 pages, respectively (**login required**).

Note: For the installation of the Optical Link driver, refer to the controller User Manuals **[RD14]**, **[RD15]** and adapter Data Sheet **[RD16]**.

- **USB 2.0 Link**, managed by CAEN (USB-to-VME) Bridges V3718. The driver installation package are downloadable for free on CAEN website at the V3718 page (**login required**).
- **USB 3.0 Link**, managed by the V4718 USB-to-VME Bridge and by the A4818 (USB3-to-CONET) Adapter. The driver installation packages are downloadable for free on CAEN website at the V4718 and A4818 page respectively (**login required**). The driver for the V4718 has to be installed for Linux users only, while the driver for the A4818 is reserved to Windows users only

Note: To install the USB Link driver, follow the instructions inside the ReadMe file included in the packet or refer to the V3718, V4718 User Manuals **[RD17][RD18]** or A4818 adapter Data Sheet **[RD16]** .

10.2 Libraries

CAEN libraries are a set of middleware software required by CAEN software tools for a correct functioning. These libraries, including also demo and example programs, represent a powerful base for users who want to develop customized applications for the digitizer control (communication, configuration, readout, etc.):

- **CAENDigitizer [RD9]** is a library of C functions specifically designed for the Digitizer families and supports both waveform recording and DPP firmware. The CAENDigitizer library is based on the CAENComm which, in turn, is based on CAENVMELib. For this reason, **the CAENVMELib and CAENComm libraries must be already installed on the host PC before installing the CAENDigitizer**.
- **CAENComm** library **[RD19]** manages the communication at low level (read and write access). The purpose of this library is to implement a common interface to the higher software layers, masking the details of the physical channel and its protocol, thus making the libraries and applications that rely on the CAENComm independent from the physical layer. **The CAENComm requires the CAENVMELib library (access to the VME bus), even in the cases where the VME is not used**.

Installation packages are available for free download on CAEN web site (*www.caen.it*) at each library page (**login required**).

CAENComm (and other libraries here described) supports the following communication channels (**Fig. 10.1**):

PC → USB3 → A4818 → CONET → V1751(VX1751) Digitizer

PC → USB → V3718/VX3718 → VMEbus → V1751(VX1751) Digitizer

PC → USB3 → V4718/VX4718 → VMEbus → V1751(VX1751) Digitizer

PC → USB3 → A4818 → CONET → V3718/VX3718 → VMEbus → V1751(VX1751) Digitizer

PC → USB3 → A4818 → CONET → V4718/VX4718 → VMEbus → V1751(VX1751) Digitizer

PC → PCI/PCIe → A2818/A3818 → CONET → V1751(VX1751) Digitizer

PC → PCI/PCIe → A2818/A3818 → CONET → V3718/VX3718 → VMEbus → V1751(VX1751) Digitizer

PC → PCI/PCIe → A2818/A3818 → CONET → V4718/VX4718 → VMEbus → V1751(VX1751) Digitizer

PC → ETHERNET → V4718/VX4718 → VMEbus → V1751(VX1751) Digitizer

WHEN TO INSTALL CAEN LIBRARIES:

WINDOWS® and LINUX® compliant customized software. The user must install the required libraries apart.

LINUX® compliant non-stand alone CAEN software. The user must install the required libraries apart to run the software.

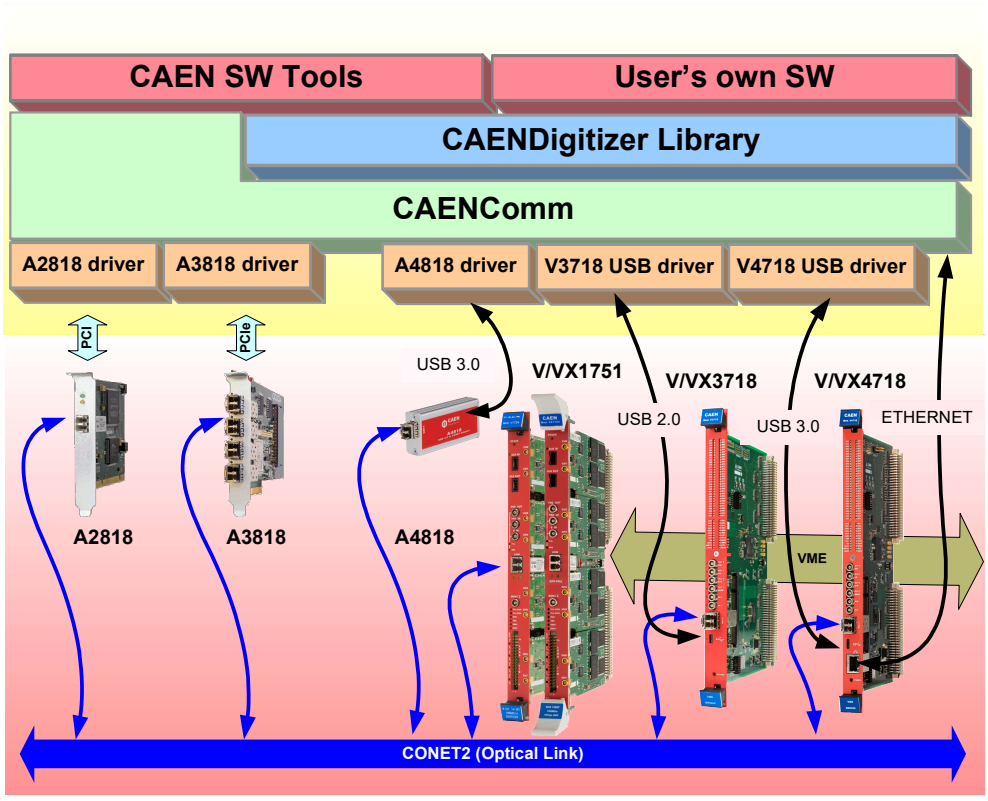


Fig. 10.1: Drivers and software layers.

11 Software Tools

CAEN provides software tools to interface the 751 digitizer family, which are available for free download on CAEN web site (*www.caen.it*) in the software and firmware product pages (**login required).**

11.1 CAENUpgrader

CAENUpgrader is free software composed of command line tools together with a Java Graphical User Interface.
CAENUpgrader, for the V1751 , allows in few easy steps to:

- Upgrade the FPGA firmware of the board
- Read the FPGA firmware release of the board and the Controller (when included in the communication chain)
- Load a programming file to configure the internal PLL
- Get the Board Info file

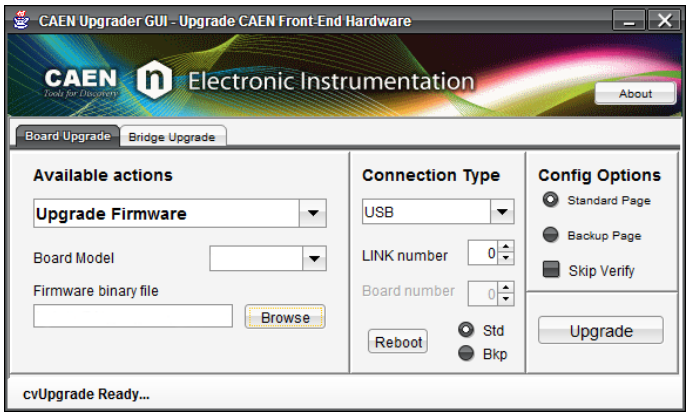


Fig. 11.1: CAENUpgrader Graphical User Interface.

CAENUpgrader runs on Windows® and Linux® platforms, 32 and 64-bit operating systems. User must also install the required third-party Oracle Java RE 8 u40 or higher.

The software relies on the CAENComm library (see Chap. **10**).

Note: CAENUpgrader for Windows® is stand-alone, the user needs to install only the driver for the communication link, while the software locally installs the DLLs of the required libraries.
The Linux® version of the software needs the required CAENVME and CAENComm libraries to be installed apart by the user.

Refer to the CAENUpgrader documentation for installation instructions and for a detailed description **[RD6]**.

11.2 CAENComm Demo

CAENComm Demo is simple software developed in C/C++ source code and provided both with Java™ and LabVIEW™ GUI interface. The demo mainly allows for a full board configuration at low level by direct read/write access to the registers and may be used as a debug instrument.

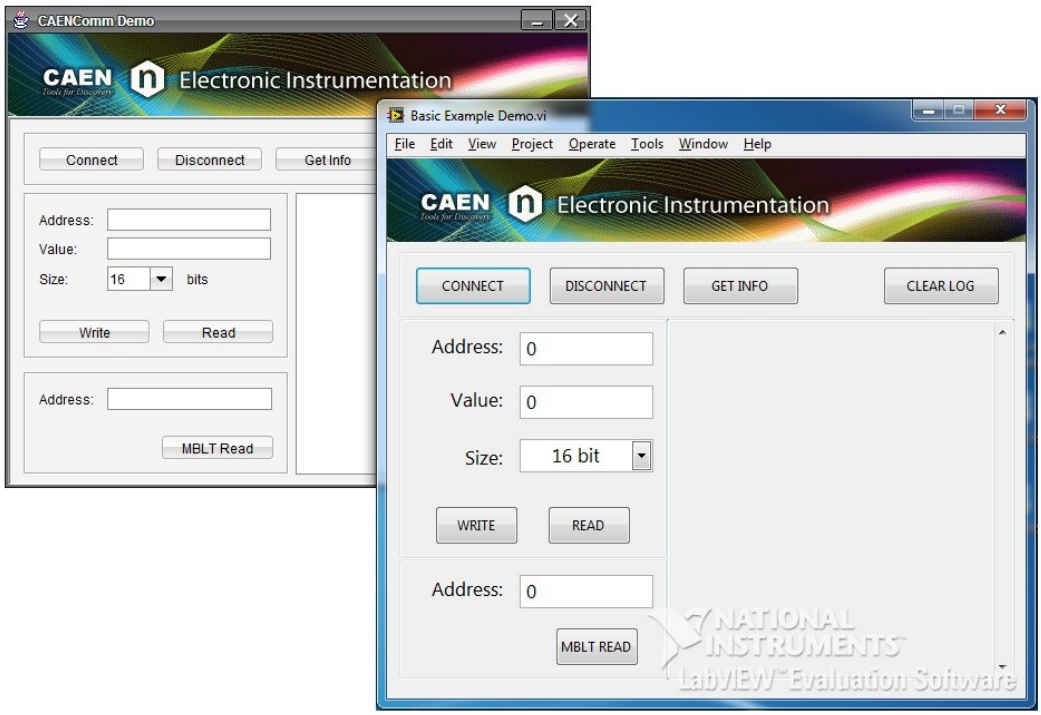


Fig. 11.2: CAENComm Demo Java and LabVIEW graphical interface.

The Demo is included in the CAENComm library Windows® installation package only.

Refer to the CAENComm documentation for installation instructions and for a detailed description **[RD19]**.

11.3 CAEN WaveDump

WaveDump is a basic console application, with no graphics, supporting only CAEN digitizers running the waveform recording firmware. It allows the user to program a single board (according to a text configuration file containing a list of parameters and instructions), to start/stop the acquisition, read the data, display the readout and trigger rate, apply some post-processing (e.g. FFT and amplitude histogram), save data to a file and also plot the waveforms using Gnuplot third-party graphing utility (*www.gnuplot.info*).

WaveDump is a very helpful example of C code demonstrating the use of libraries and methods for an efficient readout and data analysis. Thanks to the included source files and the VS project, starting with this demo is strongly recommended to all those users willing to write the software on their own.

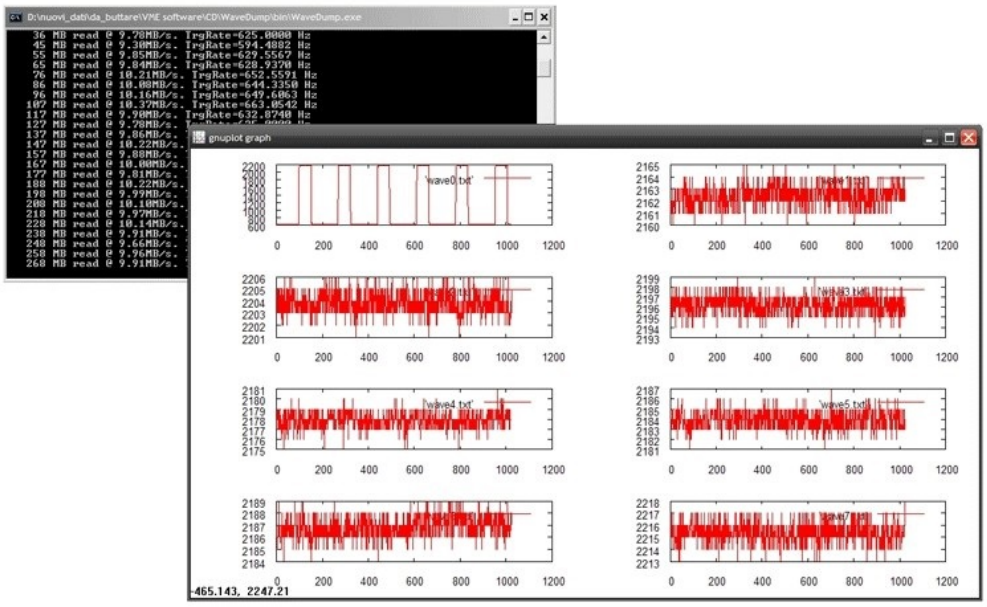


Fig. 11.3: CAEN WaveDump.

CAEN WaveDump runs on Windows® and Linux® platforms; Linux users are required to install the third-party Gnuplot.

The software relies on the CAENDigitizer and CAENComm libraries (see Chap. **10**).

Note: WaveDump for Windows® is stand-alone, the user needs to install only the driver for the communication link, while the software locally installs the DLLs of the required libraries.
The Linux® version of the software needs the required CAENVMELib and CAENComm libraries to be installed apart by the user.

Refer to the WaveDump documentation for installation instructions and for a detailed description **[RD10]**.

CAEN WaveDump does not work with digitizers running DPP firmware.

11.4 CoMPASS

CoMPASS (CAEN Multi-PArameter Spectroscopy Software) is the new software from CAEN able to implement a Multi-parametric DAQ for Physics Applications, where the detectors can be connected directly to the digitizers inputs and the software acquires energy, timing, and PSD spectra.

CoMPASS software has been designed as a user-friendly interface to manage the acquisition with all the CAEN DPP algorithm. CoMPASS can manage multiple boards, even in synchronized mode, and the event correlation between different channels (hardware and/or software), apply energy and PSD cuts, calculate and show the statistics (trigger rates, data throughput, etc...), save the output data files (raw data, lists, waveforms, spectra) and use the saved files to run off-line with different processing parameters.

CoMPASS Software supports CAEN first generation digitizers x720, x724, x725, x730, x740D, x751 digitizer families running the DPP-PSD, DPP-PHA and DPP-QDC firmware, the x780, x781 and x782 MCA family, the DT5790 Pulse Processor and the second generation digitizer x2740, x2745 and x2730 running the DPP-PSD and DPP-PHA firmware.

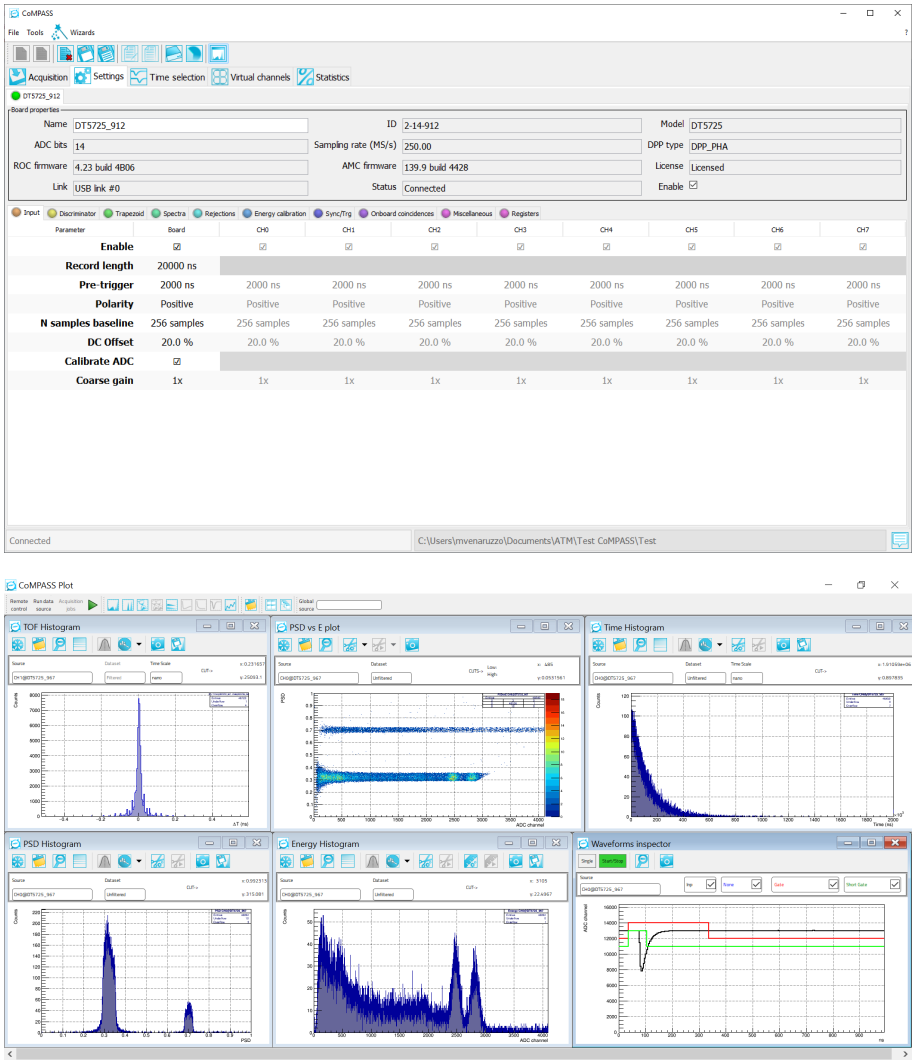


Fig. 11.4: CoMPASS software tool.

Refer to CoMPASS documentation for installation instructions and a detailed description **[RD2]**.

CoMPASS does not work with waveform recording firmware.

11.5 DPP-ZLE*plus* Control Software

DPP-ZLEplus Control Software is a demo application introducing the user to understand the principle of operation of the Digital Pulse Processing for the Zero Length Encoding (DPP-ZLE*plus*).

The user can make an entire acquisition through this software, as well use the source code to develop his/her customized readout program. Indeed, the package includes the C source files and the Visual Studio project.

The DPP-ZLE*plus* Control Software is a C-based application that programs the Digitizer according to a set of parameters in the configuration text file, starts/stops the acquisition and manages the data readout. The waveforms elaborated by the DPP-ZLE*plus* algorithm are plotted using gnuplot, an external plotting tool, or saved to output text files.

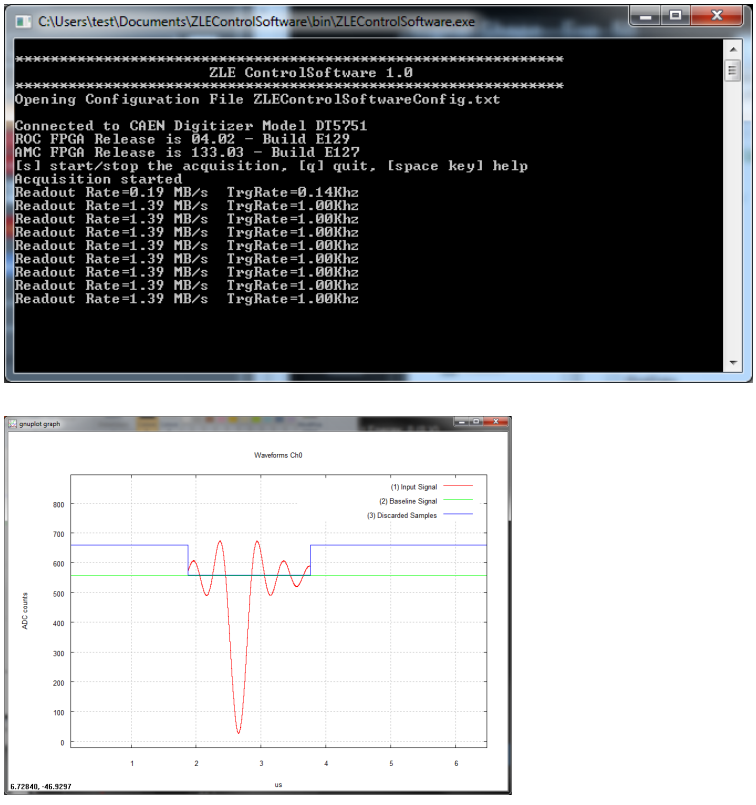


Fig. 11.5: Screen-shots of DPP-ZLEplus Control Software.

Refer to the software documentation **[RD3]** for installation instructions and a detailed.

DPP-ZLE*plus* Control Software does not work with waveform recording firmware.

12 HW Installation

- The V1751 fits into 6U VME crates
- VX1751 versions require VME64X compliant crates
- Use only crates with forced cooling air flow
- **The V1751 cannot be operated with CAEN crates VME8001, VME8002, VME8004 and VME8004A**
- Turn the crate OFF before board insertion/removal
- Remove all cables connected to the front panel before board insertion/removal

To power on the board, perform the following steps:

1. Insert the V1751 into the crate;
2. power up the crate.

USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEATING MAY DEGRADE THE MODULE PERFORMANCES

V1751 DIGITIZERS CANNOT BE OPERATED WITH CAEN CRATES VME8001, VME8002, VME8004, AND VME8004A. OVERHEAT MAY DAMAGE THE MODULE

ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE

V1751 THIS DIGITIZER DOES NOT SUPPORT LIVE INSERTION (HOT SWAP). REMOVE OR INSERT THE BOARD WHEN THE CRATE IS POWERED OFF

ONLY QUALIFIED PERSONNEL SHOULD PERFORM INSTALLATION OPERATIONS

DO NOT INSTALL THE EQUIPMENT IN A SETUP WHERE IT IS DIFFICULT TO ACCESS THE BACK PANEL FOR DISCONNECTING THE DEVICE

IT IS RECOMMENDED THAT THE SWITCH OR CIRCUIT-BREAKER IS NEAR THE EQUIPMENT

THE SAFETY OF ANY SYSTEM THAT INCORPORATES THE DEVICE IS UNDER THE RESPONSIBILITY OF THE ASSEMBLER OF THE SYSTEM

12.1 Power-on Status

At power-on, the module is in the following status:

- the Output Buffer is cleared;
- registers are set to their default configuration

After the power-on, only the NIM and PLL LOCK LEDs must stay ON (see **Fig. 12.1**).

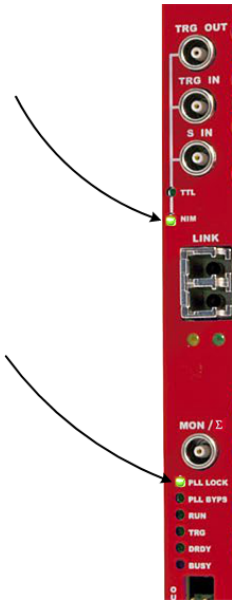


Fig. 12.1: Front panel LEDs status at power-on.

13 Firmware and Upgrades

The board hosts one FPGA on the mainboard and two FPGAs per mezzanine (i.e. one FPGA per channel). The channel FPGAs firmware is identical. A unique file is provided that will update all the FPGAs at the same time.

ROC FPGA MAINBOARD FPGA (Readout Controller + VME interface):

FPGA Altera Cyclone EP3C16

AMC FPGA MEZZANINE FPGA (ADC readout/Memory Controller):

FPGA Altera Cyclone EP3C16

The firmware is stored onto the on-board FLASH memory. Two copies of the firmware are stored in two different pages of the FLASH, referred to as Standard (STD) and Backup (BKP). In case of waveform recording firmware, the board is delivered equipped with the same firmware version on both pages.
At power-on, a micro-controller reads the FLASH memory and programs the module automatically loading the first working firmware copy, that is the STD one in normal operating.

The on-board dedicated SW7 dip switch, set on STD position by default, allows to select the first FLASH page to be read at power-on (see Sec. **8.2**).

It is possible to upgrade the board firmware via VMEbus or Optical Link by writing the FLASH with the CAENUpgrader software (see Chap. **11**).

IT IS STRONGLY SUGGESTED TO OPERATE THE DIGITIZER UPON THE STD COPY OF THE FIRMWARE. UPGRADES ARE SO RECOMMENDED ONLY ON THE STD PAGE OF THE FLASH. THE BKP COPY IS TO BE INTENDED ONLY FOR RECOVERY USAGE. IF BOTH PAGES RESULT CORRUPTED, THE USER WILL NO LONGER BE ABLE TO UPLOAD THE FIRMWARE VIA VMEbus OR OPTICAL LINK AGAIN AND THE BOARD NEEDS TO BE SENT TO CAEN FOR REPAIR!

13.1 Firmware Upgrade

Firmware updates are available for download on CAEN website (*www.caen.it*) at the digitizer page (**login required**).

Different firmware are available for the 751 family:

- The waveform recording firmware;
- The special DPP firmware for Physics Applications:
  - DPP-PSD firmware to use the digitizer as a digital replacement Dual Gate QDC, Discriminator and Gate Generator.
  - DPP-ZLE*plus* firmware to transfer the waveform in a compact format performing an advanced Zero Suppression algorithm.

The waveform recording is free firmware and updates are free downloadable.

Note: The DPP firmware is a paid firmware: the trial version can be free downloaded and is fully functional for a 30-minute per power cycle operation. The user must then purchase a license and store the provided unlock code onto the digitizer to run the firmware and its updates without time limitation. The licence is managed by the CAENUpgrader tool **[RD20]**.

Note: The 751 family has been produced with FLASH memory of two different sizes. As a consequence, a DPP firmware compatible with each flash memory size is available. To understand the firmware compatibility, refer to **[RD21]**.

13.1.1 Firmware File Description

The programming file is a .CFA (CAEN Firmware Archive) file. It is an archiving file format that aggregates all the programming files of the same firmware kind which are compatible with the same digitizer family.

The name of the CFA file follows a general convention:

- *<DIGITIZER>*_rev_X.Y_W.Z.CFA for the waveform recording firmware
- *<DIGITIZER>_<DPP_ALGORITHM>*_rev_X.Y_W.Z.CFA for the DPP firmware

where:

- *<DIGITIZER>* are all the boards that can be updated by the .CFA file. The x751 family includes DT5751, N6751, V1751, VX1751;
- *<DPP_ALGORITHM>* is the kind of DPP firmware (options are DPP-PSD, DPP-ZLEplus);
- X.Y is the major/minor revision number of the ROC FPGA;
- W.Z is the major/minor revision number of the AMC FPGA.

To discriminate between the waveform recording firmware and the DPP ones by the firmware version, the reference is the major revision number of the AMC FPGA (W):

- W < 128 means a waveform recording firmware;
- W $\geq$ 128 means a DPP firmware, and it is a fixed number specific for each algorithm and digitizer family. For the 751 series: W=132 means DPP-PSD firmware, W=133 means DPP-ZLEplus firmware.

13.2 Troubleshooting

In case of upgrade failure (e.g. STD FLASH page is corrupted), the user can try to reboot the board: after a power cycle, the system programs the board automatically from the alternative FLASH page (e.g. BKP FLASH page), if this is not corrupted as well. The user can so perform a further upgrade attempt on the STD page to restore the firmware copy.

BECAUSE OF AN UPGRADE FAILURE, THE SW7 DIP SWITCH POSITION MAY NOT CORRESPOND TO THE FLASH PAGE FIRMWARE COPY LOADED ON THE BOARD FPGAs.

Note: old versions of the digitizer motherboard have a slightly different FLASH management. Use CAENUpgrader 1.6.0 or later to get the BoardInfoFile (using the ”Get Information” function) and check that the FLASH_TYPE=0. Alternatively, use a software utility like CAENComm Demo to read at register address 0xF050 and check that bit[7]=0. In this case, at power-on, the micro-controller loads exactly the firmware copy from the FLASH page selected through the SW7 dip switch (e.g. STD by default) .

When a failure occurs during the upgrade of the STD page of the FLASH, which compromises the communication with the V1751 , the user can perform the following recovering procedure as first attempt:

- force the board to reboot loading the copy of the firmware stored on the BKP page of the FLASH. For this purpose, power off the crate, switch the dedicated SW1 switch to BKP position and power on the crate .
- use CAENUpgrader to read the firmware revision (in this case the one of the BKP copy). If this succeeds, it is so possible to communicate again with the board;
- use CAENUpgrader to load the proper firmware file on the STD page, then power off the crate, switch SW7 back to STD position and power on the crate.

If neither of the procedures here described succeeds, it is recommended to send the board back to CAEN in repair (see Chap. **14**).

14 Technical Support

To contact CAEN specialists for requests on the software, hardware, and board return and repair, it is necessary a MyCAEN+ account on www.caen.it:

https://www.caen.it/support-services/getting-started-with-mycaen-portal/

All the instructions for use the Support platform are in the document:

A paper copy of the document is delivered with CAEN boards.
The document is downloadable for free in PDF digital format at:

https://www.caen.it/wp-content/uploads/2022/11/Safety_information_Product_support_W.pdf

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