Rev. 1 - January 3rd, 2024

V1741

64 Channels Peak Sensing ADC

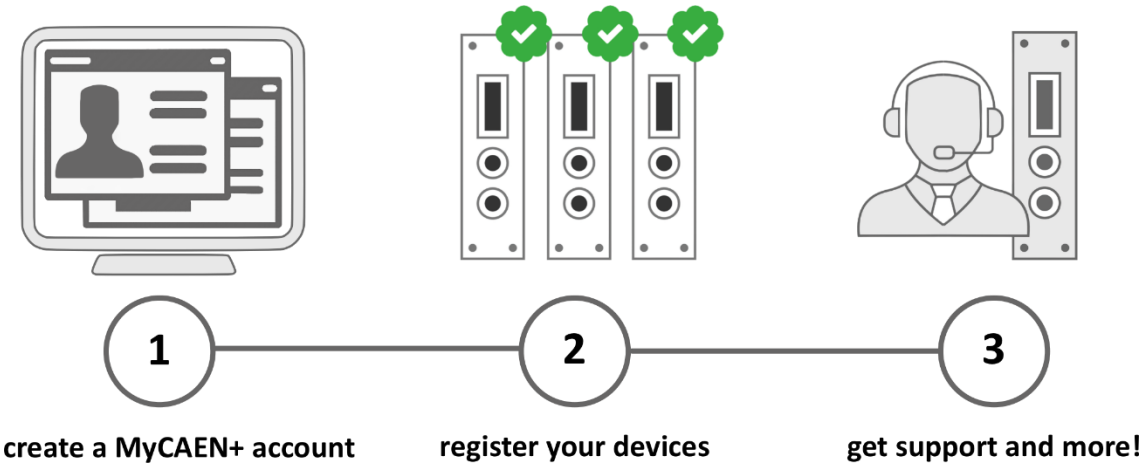
CAEN
Tools for Discovery

User Manual
UM7494

Register your device

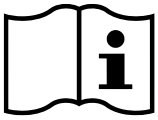
Register your device to your **MyCAEN+** account and get access to our customer services, such as notification for new firmware or software upgrade, tracking service procedures or open a ticket for assistance. **MyCAEN+** accounts have a dedicated support service for their registered products. A set of basic information can be shared with the operator, speeding up the troubleshooting process and improving the efficiency of the support interactions.

MyCAEN+ dashboard is designed to offer you a direct access to all our after sales services. Registration is totally free, to create an account go to https://www.caen.it/become-mycaenplus-user and fill the registration form with your data.



https://www.caen.it/become-mycaenplus-user/

Purpose of this User Manual



This document contains the full hardware description of the V1741 Digital Peak Sensing ADC and its principle of operations. The firmware version of reference is 4.18_01.00.

For any reference to registers in this user manual, please refer to [RD1].

Change Document Record

Date	Revision	Changes
June 9th, 2020	00	Initial release
January 3rd, 2024	01	General document review. Fixed minor typos in Chap. **1**. Updated the "Analog Input" connector specifications in Chap. **3**. Added Chap. **5**, Chap. **14**, Chap. **15**, Chap. **16**.

Symbols, Abbreviated Terms, and Notations

GUI	Graphical User Interface
ADC	Analog-to-Digital Converter
AMC	ADC & Memory Controller
DAQ	Data Acquisition
DAC	Digital-to-Analog Converter
DC	Direct Current
FSR	Full Scale Range
LVDS	Low-Voltage Differential Signal
DSP	Digital Signal Processing
DPP	Digital Pulse Processing
OS	Operating System
PLL	Phase-Locked Loop
ROC	ReadOut Controller
SW	Software
USB	Universal Serial Bus
TTT	Trigger Time Tag

Reference Document

[RD1] UM7155 – 741 Registers Description
[RD2] GD2512 – CAENUpgrader QuickStart Guide
[RD3] UM1934 – CAENComm User & Reference Manual
[RD4] UM1935 – CAENVMELib User & Reference Manual
[RD5] AN2472 – CONET1 to CONET2 migration
[RD6] V785 Technical Information Manual
[RD7] G. F. Knoll. *Radiation detection and measurement*. Ed. by J. Wiley and sons. IV ed.
[RD8] UM3148 – N1068 User Manual
[RD9] UM7327 – N1168 User Manual
[RD10] AN7537 – Energy spectra with N1168 and comparisons
[RD11] AN7498 - Performances of the analog system N1068 Shaping Amplifier and N6741 Peak Sensing ADC
[RD12] UM5312 – DT5810 Fast Digital Detector Emulator User Manual
[RD13] UM4413 - A2818 Technical Information Manual
[RD14] UM3121 - A3818 Technical Information Manual
[RD15] DS7799 - A4818 USB-3.0 to Optical Link Adapter Datasheet
[RD16] UM7685 - V3718/VX3718 VME to USB-2.0/Optical Link Bridge User Manual
[RD17] UM8305 - V4718/VX4718 VME to USB-3.0/Ethernet/Optical Link Bridge User Manual

https://www.caen.it/support-services/documentation-area/

Manufacturer Contacts

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Limitation of Responsibility

If the warnings contained in this manual are not followed, CAEN will not be responsible for damage caused by improper use of the device. The manufacturer declines all responsibility for damage resulting from failure to comply with the instructions for use of the product. The equipment must be used as described in the user manual, with particular regard to the intended use, using only accessories as specified by the manufacturer. No modification or repair can be performed.

Disclaimer

The information contained herein has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies. CAEN spa reserves the right to modify its products specifications without giving any notice; for up to date information please visit www.caen.it.

Made in Italy

We remark that all our boards have been designed and assembled in Italy. In a challenging environment where a competitive edge is often obtained at the cost of lower wages and declining working conditions, we proudly acknowledge that all those who participated in the production and distribution process of our devices were reasonably paid and worked in a safe environment (this is true for the boards marked "MADE IN ITALY", while we cannot guarantee for third-party manufactures).

Table of Contents

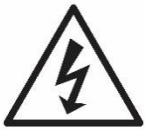
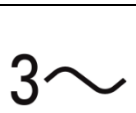
List of Figures

List of Tables

Safety Notices

N.B. Read carefully the "SAFETY, STORAGE AND SETUP INFORMATION, PRODUCT SUPPORT SERVICE AND REPAIR" document provided with the product before starting any operation.

The following HAZARD SYMBOLS may be reported on the unit:

	Caution, refer to product manual
	Caution, risk of electrical shock
	Protective conductor terminal
	Earth (Ground) Terminal
	Alternating Current
	Three-Phase Alternating Current

The following symbol may be reported in the present manual:

	General warning statement

The symbol could be followed by the following terms:

- **DANGER**: indicates a hazardous situation which, if not avoided, will result in serious injury or death.
- **WARNING**: indicates a hazardous situation which, if not avoided, could result in death or serious injury.
- **CAUTION**: indicates a situation or condition that, if not avoided, could cause physical injury or damage the product and / or its environment.

CAUTION: To avoid potential hazards

USE THE PRODUCT ONLY AS SPECIFIED.
ONLY QUALIFIED PERSONNEL SHOULD PERFORM SERVICE PROCEDURES

CAUTION: Avoid Electric Overload

TO AVOID ELECTRIC SHOCK OR FIRE HAZARD, DO NOT POWER A LOAD OUTSIDE OF ITS SPECIFIED RANGE

CAUTION: Avoid Electric Shock

TO AVOID INJURY OR LOSS OF LIFE, DO NOT CONNECT OR DISCONNECT CABLES WHILE THEY ARE CONNECTED TO A VOLTAGE SOURCE

CAUTION: Do Not Operate without Covers

TO AVOID ELECTRIC SHOCK OR FIRE HAZARD, DO NOT OPERATE THIS PRODUCT WITH COVERS OR PANELS REMOVED

CAUTION: Do Not Operate in Wet/Damp Conditions

TO AVOID ELECTRIC SHOCK, DO NOT OPERATE THIS PRODUCT IN WET OR DAMP CONDITIONS

CAUTION: Do Not Operate in an Explosive Atmosphere

TO AVOID INJURY OR FIRE HAZARD, DO NOT OPERATE THIS PRODUCT IN AN EXPLOSIVE ATMOSPHERE

THIS DEVICE SHOULD BE INSTALLED AND USED BY SKILLED TECHNICIAN ONLY OR UNDER HIS SUPERVISION

DO NOT OPERATE WITH SUSPECTED FAILURES.
IF YOU SUSPECT THIS PRODUCT TO BE DAMAGED, PLEASE CONTACT THE TECHNICAL SUPPORT

See Chap. **17** for the Technical Support contacts.

CAUTION: This product needs proper cooling.

USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEATING MAY DEGRADE THE MODULE PERFORMANCES!

DO NOT USE THE VX2730 DIGITIZER WITH VME8001, VME8002, VME8004, AND VME8004A CRATES AS OVERHEAT MAY DAMAGE THE MODULE!

CAUTION: This product needs proper handling.

THE VME DIGITIZER DOES NOT SUPPORT LIVE INSERTION (HOT-SWAP)! REMOVE OR INSERT THE BOARD WHEN THE CRATE IS POWERED OFF!

ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE!

1 Introduction

The V1741 is a Digital Peak Sensing ADC belonging to a new generation of detector readout systems based on a mixed analog-digital acquisition chain, combining a high channel density (up to 64 channels) and a low dead time (less than 50 ns). Results of some measurements with the Peak Sensing ADC are reported in the application notes **[RD10]** and **[RD11]** where the board has been used in combination with the CAEN Shaping Amplifiers N1068 **[RD8]** and N1168 **[RD9]**.

The peak measurement approach of the V1741 is to use a moderate ADC sampling frequency at the input stage to sample the input signal and process it through proper algorithms implemented in the FPGA. In older analog peak-sensing devices, like the CAEN V785 **[RD6]**, the signal height was measured through a peak stretcher, a gating circuit and a slow A/D converter: this approach presented several drawbacks, most notably a higher dead time.

When a typical slow signal, e.g. from a Charge-Sensitive Preamplifier followed by a Shaping Amplifier, is fed into the board, the FPGA identifies the peak of the pulse within a gate by means of digital filters. The height data is stored with the time stamp of 16 ns resolution (8 ns steps) in a multi-event buffer and it is available for the readout through VMEbus or by optical link interface (daisy-chainable). Data throughput can be reduced by the Amplitude Zero Suppression algorithm, which rejects events whose amplitude is less than a programmable threshold.

The Digital Signal Processing (DSP) algorithm implemented in the FPGA, calculates the pulse height with a low Differential Non-Linearity (DNL) thanks to the sliding scale correction technique. This technique adds an analog voltage value to the pulse amplitude before conversion and then subtracts its digital equivalent after the conversion, spreading equal-height pulses over different channels in order to reduce the effect of the channels' different widths **[RD7]**. Through this technique, the DNL is less than 1%. The energy spectrum (up to 16k channels) is then built at the software level. The software can also retrieve the time stamp and pulse height information for each event and save that information in a list file.

In addition, the FPGA-algorithm allows the user to achieve an extremely low conversion time of the pulse peak, so that a new conversion can take place less than 50 ns after the previous gate closes. This is the measured dead time of the system (see Sect. **8.2.3**).

The board hosts three input LEMO connectors (NIM/TTL polarity selectable by software) in the front panel for the Gate signal and for the event discard during the acquisition in case of pile-up (called “GATE” and “REJ” respectively). The user can decide to use the same gate width of the external gate, or to set a programmable value through the software. Gate propagation can be done through the LEMO GPO connector.

The V1741 board is provided with drivers for the supported communication interfaces, C-based control and acquisition libraries, and an open-source acquisition software for user customization. Firmware upgrade can be performed via optical link or VMEbus by the user using the CAEN Upgrader tool **[RD2]**.

Board Models	Description
V1741	V1741 – 64 channel Peak Sensing ADC
Related Products	**Description**
A2818	A2818 – PCI Optical Link (Rhos compliant)
A3818A	A3818A – PCIe 1 Optical Link
A3818B	A3818B – PCIe 2 Optical l Link
A3818C	A3818C – PCIe 4 Optical Link
V1718	V1718 - VME-USB 2.0 Bridge
V1718LC	V1718LC - VME-USB 2.0 Bridge (Rohs Compliant)
V2718	V2718 - VME-PCI Bridge
V2718LC	V2718LC - VME-PCI Bridge (Rohs compliant)
V2718LC KIT	V2718KITLC - VME-PCI Bridge (V2718) + PCI Optical Link (A2818) + Optical Fibre 5m duplex (AY2705) (Rohs)
V2718 KIT	V2718KIT - VME-PCI Bridge (V2718) + PCI Optical Link (A2818) + Optical Fibre 5m duplex (AY2705)
V2718 KIT-B	V2718KITB - VME-PCI Bridge (V2718) + PCIe Optical Link (A3818A) + Optical Fibre 5m duplex (AY2705)
Accessories	**Description**
A746B	64 Channels Adapter for Lemo connector
A371	32 Channels Adapter for Flat Cable connector
A385	16 Channels Cable Adapter (Flat to Lemo)
A317	Clock Distribution Cable
A318	SE to Differential Clock Adapter
AI2730	Optical Fibre 30 m simplex
AI2720	Optical Fibre 20 m simplex
AI2705	Optical Fibre 5 m simplex
AI2703	Optical Fibre 30 cm simplex
AY2730	Optical Fibre 30 m duplex
AY2720	Optical Fibre 20 m duplex
AY2705	Optical Fibre 5 m duplex

Table 1.1: Table of models and related items

2 Block Diagram

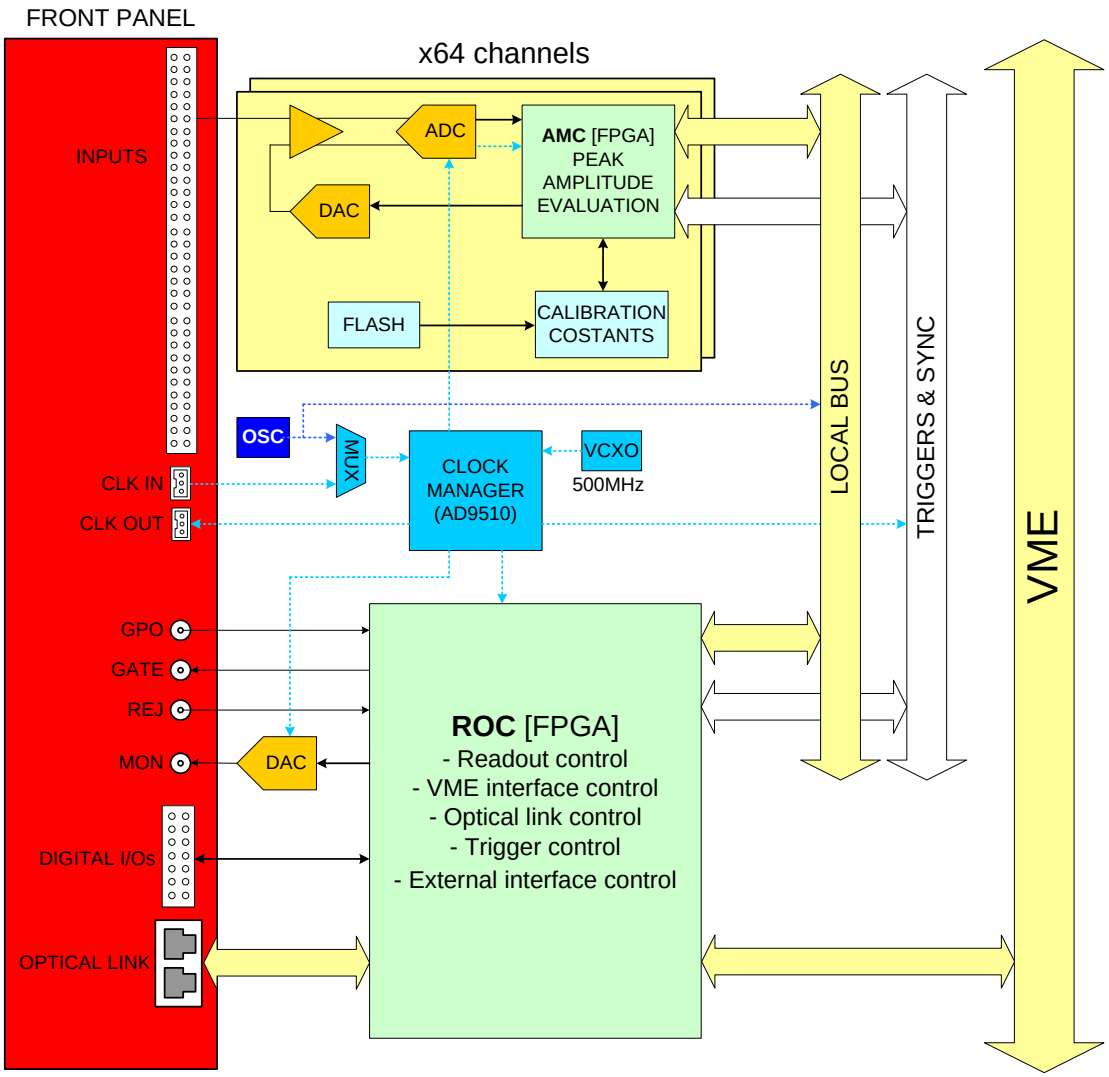


Figure 2.1: Block Diagram

3 Technical Specifications

GENERAL	**Form Factor** 1-unit wide, 6U VME64		**Weight** 535 g
ANALOG INPUT	**Channels** 64 channels Single-ended **Impedance** Z_{in} = 2.5 kΩ	**Connector** 68-pin ERNI SMC with 1.27mm pitch **Full Scale Range (FSR)** 4 V_{pp} (3.75 V_{pp} with sliding scale enabled) or 8 V_{pp} (7.5 V_{pp} with sliding scale enabled) SW selectable	**Offset** The Sliding Scale automatically manages the DAC for DC offset adjustment on each channel.
DIGITAL CONVERSION	**Resolution** 12 bits[1]	**Sampling Rate** 62.5 MS/s simultaneously on each channel	
CONVERSION GAIN	1k, 2k, 4k, 8k, 16k		
DEAD TIME	50 ns		
MINIMUM RISE TIME	2 ns		
INTEGRAL NON-LINEARITY (INL)	< 0.05% in the range of (1:99) % of FSR		
DIFFERENTIAL NON-LINEARITY (DNL)	≤ 1%		
ZERO SUPPRESSION	Zero Suppression threshold common to 8-channel groups and programmable in steps of ADC counts over the entire FSR		
GATE	GATE mode with linear gate width or programmable by software. The GATE signal is fed into the GATE LEMO connector **Gate Propagation** Gate_IN/Gate_OUT propagation through GATE/GPO Lemo connectors		
MEMORY	Multi-event Buffer of 1024 events		
DIGITAL I/O	**CLK-IN (AMP Modu II)** AC coupled differential input clock LVDS, ECL, PECL, LVPECL, CML (single ended NIM/TTL available by A318 adapter) Jitter<100ppm requested **GATE (LEMO)** Front panel digital input of NIM/TTL logic: when high, the event is acquired; Z_{in} = 50 Ω	**CLK-OUT (AMP Modu II)** DC coupled differential LVDS clock output locked at ADC sampling clock **GPO (LEMO)** Digital output that automatically propagates the GATE input NIM/TTL; R_t = 50 Ω	**REJ (LEMO)** Front panel digital input of NIM/TTL logic: when high, the event is rejected Z_{in} = 50 Ω
TIME STAMP	48-bit counter, 8 ns step, 16 ns resolution, 625 h range		
LVDS I/O	16 general purpose LVDS I/O controlled by the FPGA: Run, Busy, Veto, Trigger and other functions can be programmed An Input Pattern from the LVDS I/O can be associated to each trigger as an event marker		
ADC & MEM. CONTROLLER	Altera Cyclone EP1C16 (one FPGA serves 16 channels)		
COMMUNICATION INTERFACE	**Optical Link** CAEN CONET proprietary protocol Up to 80 MB/s transfer rate Daisy chainable: it is possible to connect up to 8 or 32 ADC modules to a single Optical Link Controller (respectively A2818 or A3818)	**VME** VME 64X compliant Data transfer mode: BLT32, MBLT64 (70 MB/s using CAEN Bridge), CBLT32/64, 2eVME, 2eSST (up to 200 MB/s)	
DPP FW SUPPORTED	Peak Sensing firmware		
FIRMWARE UPGRADE	Firmware can be upgraded via VMEbus/Optical Link		
SOFTWARE	General purpose C libraries, configuration tools, readout software (Windows and Linux support)		
POWER CONSUMPTIONS	5.4 A @ +5V; 270 mA @ +12V, -12V not used		

Table 3.1: Technical specifications table

[1] This value leads to 14-bit dynamics.

4 Packaging and compliancy

V1741 module is 1-unit wide 6U VME64 board.

The unit is inspected by CAEN before the shipment, and it is guaranteed to leave the factory free of mechanical or electrical defects.

The content of the delivered package standardly consists of the part list shown in the table below (**Table 4.1**). All the official documentation, firmware updates, software tools, and accessories are available on *www.caen.it* at the product web page.

	Part	Description	Qt
	V1741	Digital Peak Sensing ADC	x1
	Documentation	UM7494 – V1741 User Manual	x1

Table 4.1: Delivered kit content

CAUTION: to manage the product, consult the operating instructions provided.

When receiving the unit, the user is strictly recommended to:

- Inspect containers for damage during shipment. Report any damage to the freight carrier for possible insurance claims.
- Check that all the components received match those listed on the enclosed packing list as in **Table 4.1** (CAEN cannot accept responsibility for missing items unless any discrepancy is promptly notified.)
- Open shipping containers; be careful not to damage contents.
- Inspect contents and report any damage. The inspection should confirm that there is no exterior damage to the unit such as broken knobs or connectors and that the front panel and display face are not scratched or cracked. Keep all packing material until the inspection has been completed.
- If damage is detected, file a claim with carrier immediately and notify CAEN service (see Chap. **17**).
- If equipment must be returned, carefully repack equipment in the original shipping container with original packing materials, if possible. Please contact CAEN service.
- If equipment is not installed when unpacked, place equipment in original shipping container and store in a safe place until ready to install.

DO NOT SUBJECT THE ITEM TO UNDUE SHOCK OF VIBRATIONS

DO NOT BUMP, DROP OR SLIDE SHIPPING CONTAINERS

DO NOT LEAVE ITEMS OR SHIPPING CONTAINERS UNSUPERVISED IN AREAS WHERE UNTRAINED PERSONNEL MAY MISHANDLE THE ITEMS

USE ONLY ACCESSORIES WHICH MEET THE MANUFACTURER'S SPECIFICATIONS

Official documentation, firmware updates, software tools, and accessories are available on the CAEN website *www.caen.it* at the Digitizer web page. MyCAEN+ account needed for download (see Chap. **17**).

5 PID (Product Identifier)

PID is the CAEN product identifier, an incremental number greater than 10000 that is unique for each product[2]. PID is on a label affixed to the product (**Figure 5.1**) and readable by software using the Get Information function of CAEN Upgrader tool (see Chap. **11**).

Note: The serial number is still valid to identify older boards, where the PID label is not present.

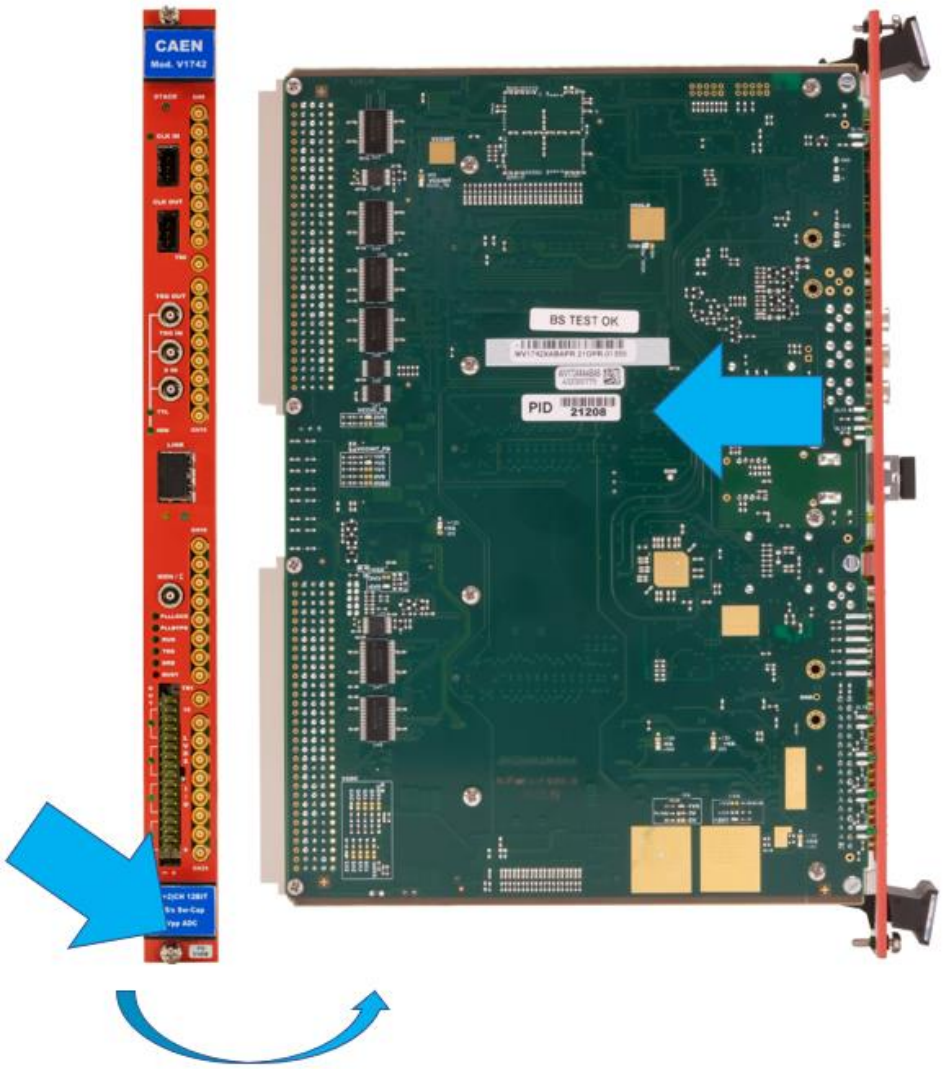


Figure 5.1: PID location on the VME device (the number in the picture and the device model are purely indicative)

[2] The PID substitutes the serial number previously identifying the boards.

6 Power Requirements

The table below resumes the V1741 power consumptions per relevant power supply rail.

MODULE	SUPPLY VOLTAGE		
	+6V	+12V	-12V
V1741	5.4 A	270 mA	not used

Table 6.1: Power requirements table

7 Panels Description

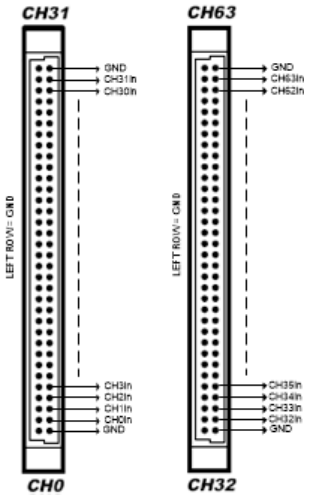
7.1 Front Panel

ANALOG INPUT

FUNCTION
Two input connectors from CH0 to CH31 and from CH32 to CH63 receive the input analog signals.

ELECTRICAL SPECS
Input dynamics: 4Vpp or 8Vpp[3]
Input impedance (Z_{in}): 2.5 kΩ
Absolute max analog input voltage: 8 Vpp (with Vrail max +4 V or –4 V) for any DAC offset value.

PINOUT



Note: ensure that alignment is correct during insertion/extraction operations of the accessories; incorrect alignment may lead to connector damage. See also Sect. **10.2** for more details.

MECHANICAL SPECS
Series: ERNI SMC 68P connectors.
Type: ERNI SMC-15476.
Manufacturer: ERNI Electronics.

ACCESSORIES
Analog signals can be fed into each channel using LEMO cables plugged into either the A746B adapter, or the adapters system made of A371 and A385 (see figure below)

A746B

A371

A385

[3] When the sliding scale is enabled, the full-scale range of the ADC is reduced by 1/16 (~3.75 V @4V and ~7.5 V @8V).

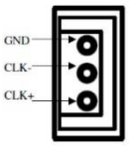
CLK IN / CLK OUT

FUNCTION
Input and output connectors for the external clock.

ELECTRICAL SPECS
Sign. type: differential (LVDS, ECL, PECL, LVPECL, CML).
CAEN provides single-ended to differential A318 cable adapter for CLK-IN.
Coupling: AC (CLK-IN); DC (CLK-OUT).
Z_{diff}: 100 Ω.

MECHANICAL SPECS
Series: AMPMODU connectors.
Type: 3-102203-4 (3-pin).
Manufacturer: AMP Inc.

PINOUT



CLK IN LED (GREEN): indicates that the external clock is enabled.

GPO / GATE / REJ

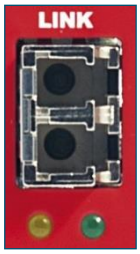
FUNCTION
- GPO: digital output connector to propagate the Gate signal with its correct length, either linear with the gate input, or programmed via software.
- GATE: digital input connector for the external gate signal.
- REJ: digital input connector configurable as gate rejector.

ELECTRICAL SPECS
Signal level: NIM or TTL.
GATE/REJ Input impedance (Zin): 50 Ω
GPO requires 50 Ω termination.

MECHANICAL SPECS
Series: 101 A 004 connectors.
Type: DLP 101 A 004-28.
Manufacturer: FISCHER.
Alternatively:
Type: EPL 00 250 NTN.
Manufacturer: LEMO.

TTL (GREEN), NIM (GREEN): indicate the standard TTL or NIM is set for GPO, GATE, REJ.

OPTICAL LINK PORT



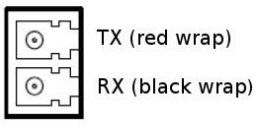
FUNCTION
Optical LINK connector for data readout and flow control. Daisy chainable. Compliant to Multimode 62.5/125µm cable featuring LC connectors on both sides.

ELECTRICAL SPECS

Transfer rate: up to 80 MB/s.

MECHANICAL SPECS
Series: SFF Transceivers.
Type: FTLF8519F-2KNL (LC connectors).
Manufacturer: FINISAR.

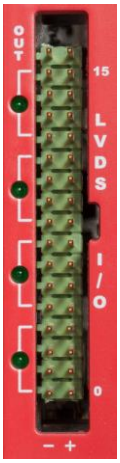
PINOUT

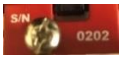


LINK LEDs (GREEN/YELOW): right LED (GREEN) indicates the network presence, while left LED (YELLOW) signals the data transfer activity.

MON / Σ	
	NOT USED

DIAGNOSTICS LEDs	
	**DTACK (GREEN):** indicates whether there is a VME read/write access to the board.
	**PLL LOCK (GREEN):** indicates the PLL is locked to the reference clock. **PLL BYPS (GREEN):** not used. **RUN (GREEN):** indicates the acquisition is running (data taking). **TRG (GREEN):** indicates the gate is accepted. **DRDY (GREEN):** indicates the event/data is present in the Output Buffer. **BUSY (RED):** indicates all the buffers are full for at least one channel.

LVDS I/Os CONNECTOR		
	**FUNCTION** 16-pin connector with programmable general purpose LVDS I/O signals organized in 4 independent signal groups: 0÷3; 4÷7; 8÷11; 12÷15. In/Out direction is software controlled. Different selectable modes (see Sect **8.9**): – Register – Trigger – nBusy/nVeto – Legacy **ELECTRICAL SPECS** Level: differential LVDS Zdiff: 100 Ω	**MECHANICAL SPECS** Series: TE - AMPMODU Mod II Series Type: 5-826634-0 34 pins (lead spacing: 2.54 mm; row pitch: 2.54 mm) Manufacturer: AMP Inc.

LABELS	
	Top handle: – Board model Bottom handle: – Brief functional description of the module
	Bottom: – S/N: 4-digit Serial Number (old boards) – PID: 10-digit Product Identifier (recent boards)

7.2 Internal Components

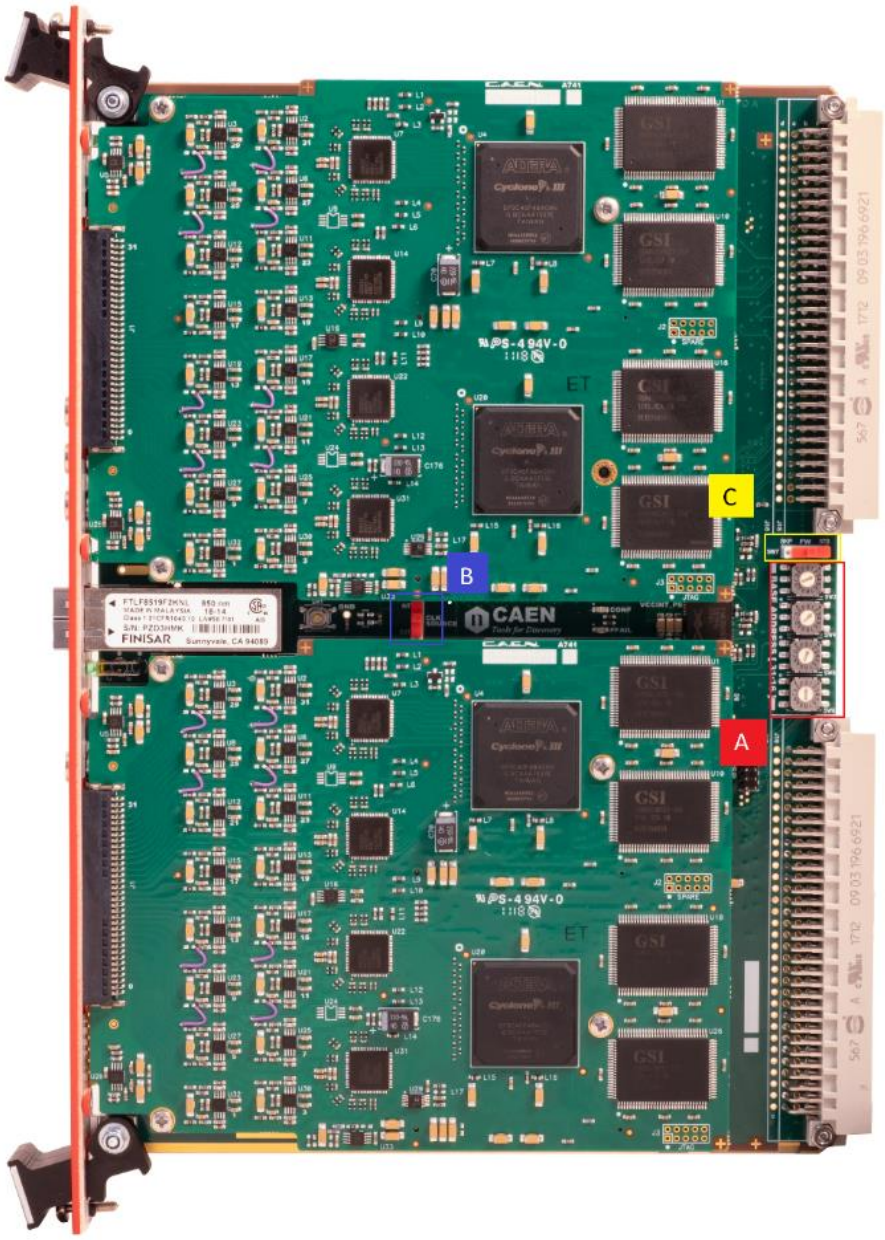


Figure 7.1: Rotary and dip switches location

A	SW3,4,5,6: "Base Address [31:16]"	Type: Rotary Switches	Function: Set the VME Base Address of the module
B	SW2: "CLOCK SOURCE" INT/EXT	Type: Dip Switch	Function: Selects the clock source (External or Internal)
C	SW7: "FW" BKP/STD	Type: Dip Switch	Function: Selects "Standard" (STD) or "Backup" (BKP) FLASH page as first to be read at power-on to load the FW on the FPGAs (default position is STD); see Chap. **13**

8 Functional Description

In the following Chapter, operation principles and functional descriptions of the module are described in detail. The block diagram of the module can be found in **Figure 8.1**.

8.1 Analog Input Stage

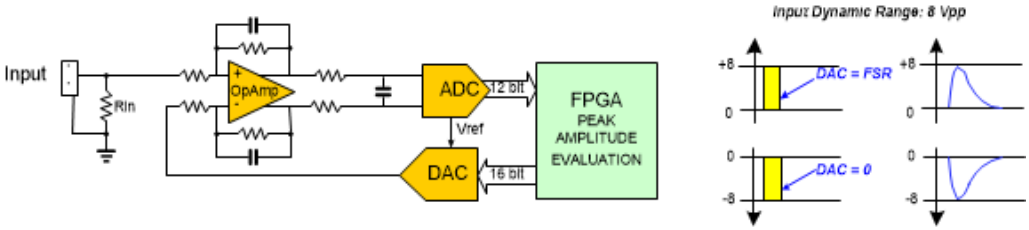


Figure 8.1: Analog Input Diagram

8.1.1 Board Calibration

During the production phase, the board is calibrated through a procedure that calculates the ADC value corresponding to each spanned DAC value on 1/16 of the full DAC scale (roughly corresponding to 1/16 of the full ADC scale) as the mean of a few thousand events. The calibration is required for the Sliding Scale technique, which is able to reduce the effect of the ADC's Differential Non-Linearity (DNL) on the measurement: during the acquisition a DAC offset, slowly varying (about 0.001%/msec of the full analog range) within the aforementioned DAC calibration interval, is continuously added to the analog input in order to convert a given pulse height over different ADC channels. After the A/D conversion, the FPGA subtracts to the measured peak height the ADC value measured during the calibration process at the DAC value used for the pulse acquisition, so that the actual pulse height value is subsequently processed. When the sliding scale is enabled, the full-scale range of the ADC is therefore reduced by about 1/16 of the full scale (~3.75 V @4V and ~7.5 V @8V).

8.1.2 Principles of Operation

The conversion is always initiated by an external signal feeding the GATE input (NIM or TTL) on the board front panel; the gate is common to all the 32 channels, whose conversion is therefore simultaneous. The algorithm in the FPGA recognizes the rising edge of the input pulse and evaluates the signal moving average for all the whole gate duration.

Two gate options are available for the peak search:

- **gate mode** (level sensitive): the gate lasts for the duration of the GATE input signal (see **Figure 8.2**)
- **edge mode** (edge sensitive): the gate starts with the leading edge of the GATE signal and lasts for a user programmable time, that can be set through register 0x8020 **[RD1]** (see **Figure 8.3**).

The V1741 is busy for the duration of the gate. In both cases, when the gate is over, each channel saves the converted value (up to 14 bits) into the local memory buffer and gets armed for a new gate. The readout logic creates an event data packet with a common header (including a 48-bit time stamp with 8 ns steps and 16 ns resolution and a trigger counter, among other information) followed by the converted peak values of the enabled channels.

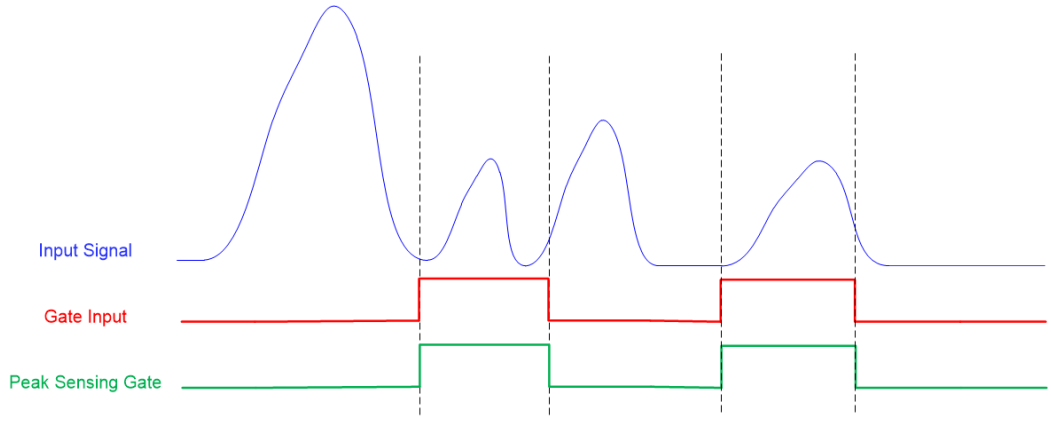


Figure 8.2: Gate mode acquisition: the gate width is equal to the input gate width

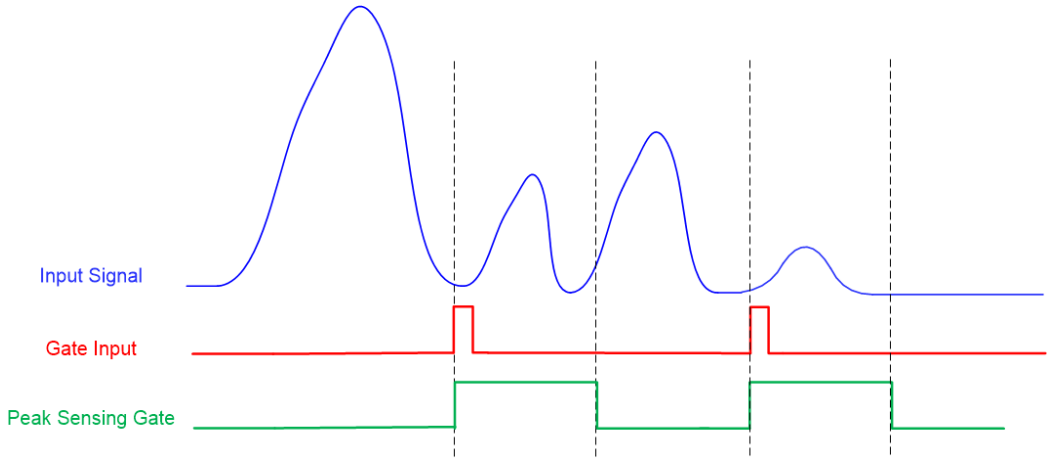


Figure 8.3: Edge mode acquisition: the gate width is defined via 0x8020 register **[RD1]**

The REJ input on the front panel (NIM or TLL) is used to "discard" unwanted events, for example, it can be the logic output of a shaper that has identified a piled-up event. If the REJ signal is activated at any time during the gate, the event data packet will be made of a header and a flag identifying the rejected event (see Sect. **8.8**).

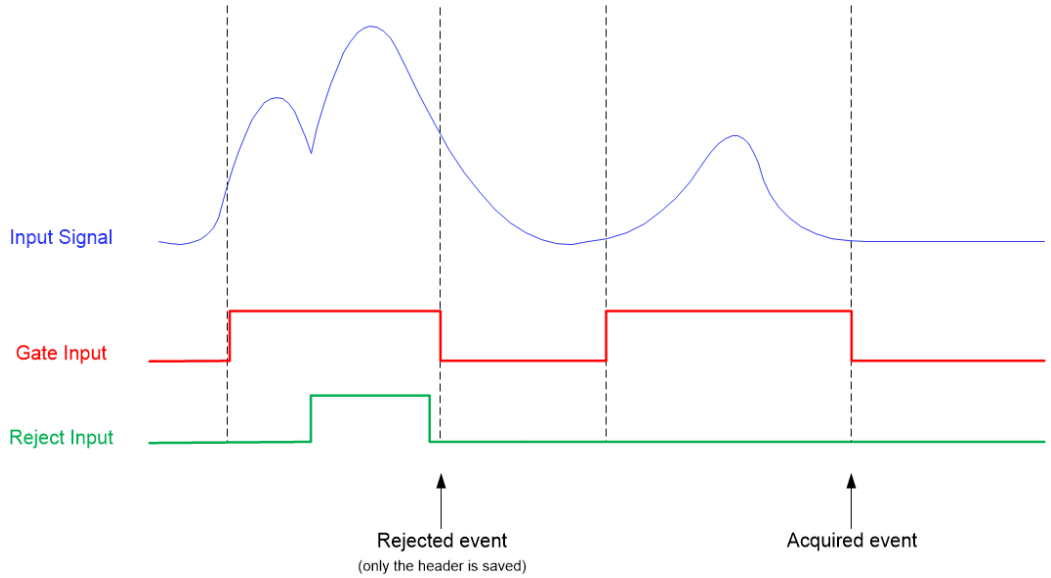


Figure 8.4: Signal processing in case of Reject gate

It is also possible to enable the channel Amplitude Suppression: amplitude values below a programmable threshold will be discarded and will not be present in the data packet. The threshold value is common to groups of 8 channels.

During the entire peak sensing gate width (both in gate and edge mode), other gates are inhibited. The board will anyway count all the gates/edges arriving, also those rejected by the REJ input. After the end of the gate width, there is a very short extra dead time (less than 50 ns) before the board is armed to accept a new gate. The total dead time (gate width + extra dead time) is counted by an internal *Dead Time Counter*, whose value can be read from a specific register **[RD1]**. A *Real Time Counter*, that represents the time since the start of the acquisition, is also available.

8.2 Technical Features

8.2.1 Integral Non-linearity

The *Integral Non-Linearity (INL)* represents the deviation of the entire transfer function from the ideal function. It is a commonly used measure of performance in analog-to-digital converters.

The system INL evaluation has been performed as shown in Figure 8.5. The signals coming from a Charge Sensitive Preamplifier are emulated by the Digital Detector Emulator (DDE, CAEN DT5800). The emulated signal has a rising edge of 100 ns and an exponential decay with a time constant of 50 µs. The pulse frequency is constant at 1 kHz and the pulse height changes according to the Poissonian distribution.

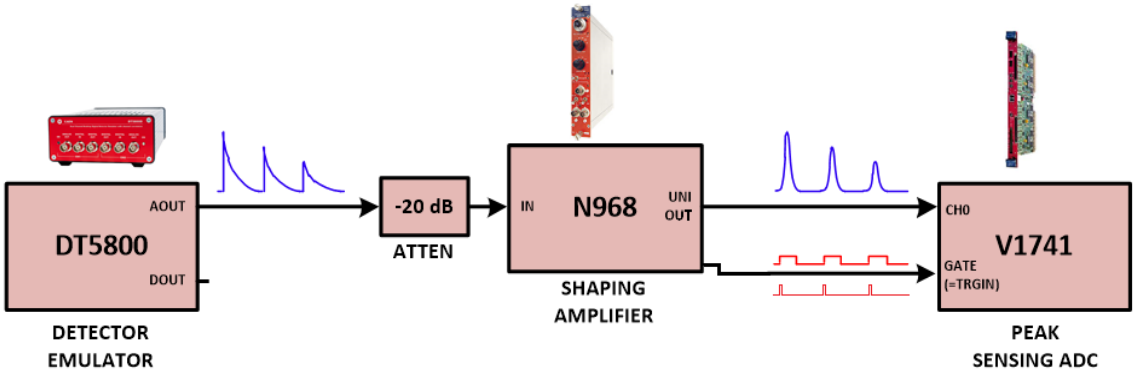


Figure 8.5: Setup to estimate the *Integral Non-Linearity* of the system

The output of the DDE (attenuated by 20 dB) feeds the CAEN Shaping Amplifier (Mod. N968). The coarse gain of the amplifier is 20 (minimum value), while the fine gain is tuned to have the last peak of the spectrum at 3750 channels of the peak sensing ADC. The shaping time ranged from 0.5 to 10 µs. The output of the shaping amplifier feeds the channel input of the V1741, which is triggered by the digital output of the DDE.

The measurements have been performed at the shaping time values allowed by the N968 (namely: 0.5, 1, 2, 3, 6 and 10 µs) and at 4K and 16K conversion gains, that is number of channels in the energy spectrum. In **Figure 8.6**, the INL values at 1,3 and 10 µs shaping times are displayed. The INL of the N6741 digital chain has been measured to be less than 0.07% over 99% of the Full-Scale Range (FSR).

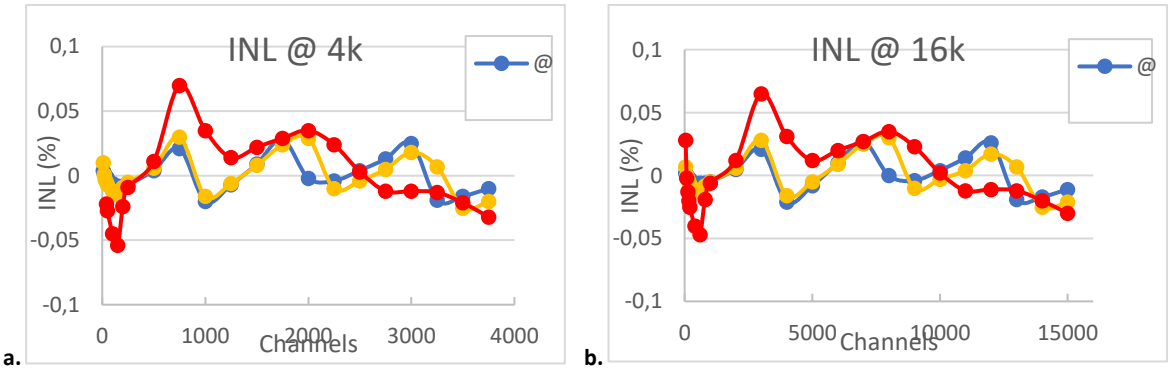


Figure 8.6: Typical integral non-linearity for the system composed of the V1741 Peak Sensing ADC and the CAEN N968 Shaping Amplifier at different values of shaping time (1, 3 and 10 µs) and spectrum channels (4K and 16K)

The intrinsic resolution of the acquisition chain as a function of the shaping time is shown in **Figure 8.7** for amplitudes corresponding to half and full dynamic scale (4V and 8V respectively). The resolution has been measured at different values of spectrum channels (4k, 8k, and 16k).

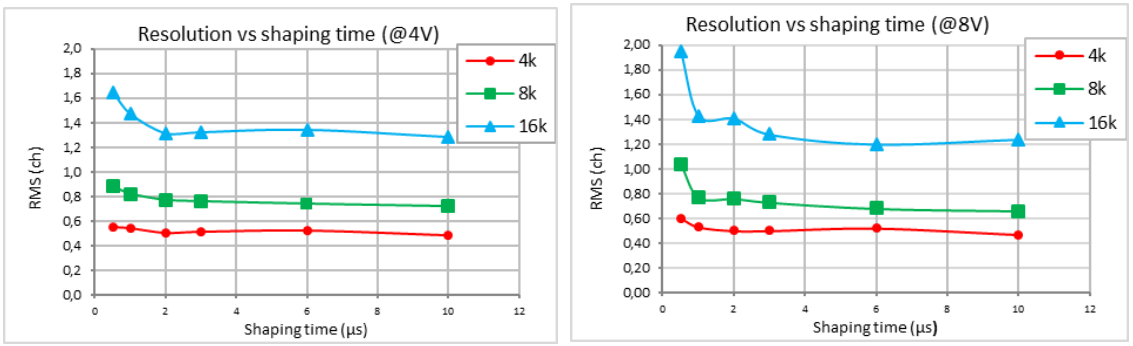


Figure 8.7: System resolution composed of the V1741 Peak Sensing ADC and the CAEN N968 Shaping Amplifier as a function of the shaping time for the two input dynamic range (4V and 8V)

8.2.2 Differential Non-linearity

The *Differential Non-Linearity* (*DNL*) of the signal height measurement, is an important parameter for measuring the error in the analog-to-digital conversion. It has been measured using an analog pulse generator whose reference amplitude was externally provided through a ramp generator. In order not to be limited by statistics, the number of events collected for each amplitude bin was >> 10^4, the latter being the statistics required for the measurement to have a statistical precision of 1%.

The result is shown in the plot below: the DNL is better than 1%, the main uncertainty of the measurement coming from the non-flat distribution of the generated amplitudes.

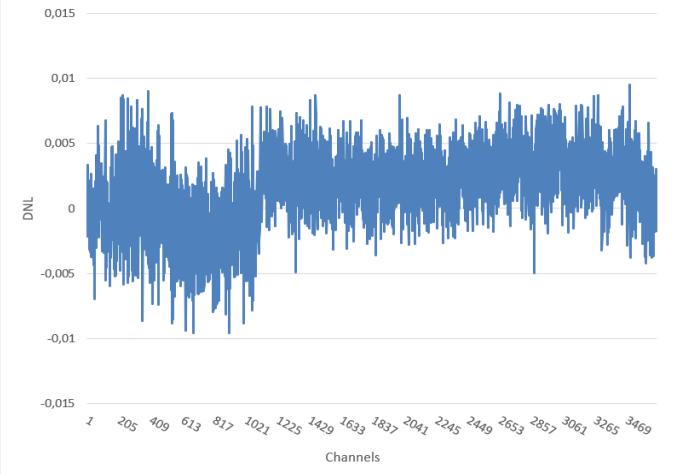


Figure 8.8: Differential Non-Linearity of the system

Note: the DNL documented in this section does not refer to the ADC chip used to digitize the analog signals, but to the whole procedure leading to the measurement of the signal amplitude.

8.2.3 Throughput and Dead Time

The maximum rate for a specific connection link and number of channels is defined as the rate at which the board goes full, i.e. when no more gate received by the board can be processed and are therefore discarded.

The result could vary according to the specifications of the PC and the memory occupancy. In the test, these factors were not significant for the measurement. Results are shown in **Figure 8.9**, where the measurements were taken both with the N6741 and V1741, in particular: VME USB for V1741 and the V1718 bridge, Direct USB for N6741, Direct fiber for V1741 with direct optical link connection (results are the same in the case of N6741 with direct optical link connection), VME fiber for V1741 with the V2718 bridge.

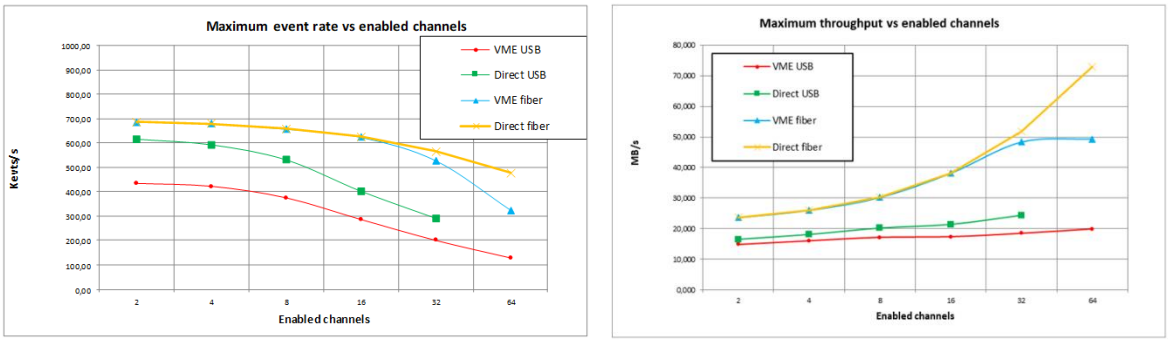


Figure 8.9: x741 rate and throughput as a function of the number of enabled channels and of different connection types: VME USB, Direct USB, VME fiber and Direct fiber. Refer to the text for more details

The V1741 dead time has been estimated by sending two gate pulses at a fixed frequency (the two signals were summed together before feeding the GATE connector). The time difference between the two was decreased until the readout data rate became half the input rate: when this happens the time distance between two consecutive triggers is lower than the sum between the acquisition window and the dead time, and therefore the peak sensing can process any other gate. The distance between the end of the acquisition window of a collected gate and the start of the subsequent gate at the largest possible trigger rate without trigger losses represents the dead time of the device: this was measured to be about 48 ns, corresponding to three clock cycles (the FPGA internal processing proceeds at 62.5 MHz clock) and is independent of the selected width of the acquisition window. **Figure 8.10** shows the GPO output, where the two consecutive gates (NIM levels) are represented and the distance between the two is about 40-48 ns (top and bottom respectively).

Figure 8.10: V1741 Dead-time measurement

8.2.4 Rise Time

The response of a traditional Peak Sensing board was strongly dependent of the input rise time value: for a correct peak detection the rise time should be at least of some tens of ns, while signals with too short rise time were not detected at all. In the case of Peak Sensing ADC, the input is sampled by the ADC with a sampling rate of 16 ns. In addition, at the peak detection, a mean value is taken of the peak samples, thus allowing the user to feed even shorter rise time. A test of the minimum accepted rise time has been made to measure the smallest rise time allowed to measure the peak.

The pulse emulator DT5810 **[RD12]** generated signals with fixed amplitude and decay time of 20 µs. The rise time was varied in the range of 2 ns – 1 µs. The minimum value of 2 ns was still accepted by the Peak Sensing ADC, and the peak resolution was compatible with all the other RMS values.

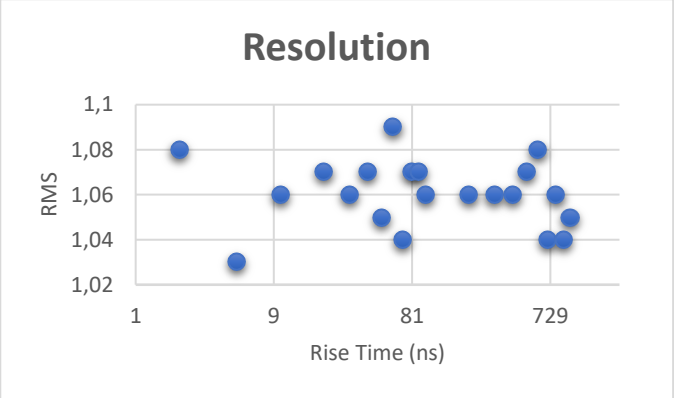


Figure 8.11: Peak resolution (RMS) vs rise time of the input pulse. Minimum value is 2 ns

8.3 Clock Distribution

The clock distribution of the module takes place on two domains: OSC-CLK and REF-CLK.

OSC-CLK is a fixed 50-MHz clock coming from a local oscillator which handles VMEbus, Optical Link and Local Bus, that takes care of the communication between motherboard and mezzanines (see red traces in **Figure 8.12**).

REF-CLK handles ADC sampling, trigger logic, acquisition logic (samples storage into RAM, buffer freezing on trigger) through a clock chain. REF-CLK can be either an external (via the front panel CLK-IN connector) or an internal (via the 50-MHz local oscillator) source. In the latter mode, OSC-CLK and REF-CLK will be synchronous (the operation mode remains the same).

REF-CLK clock source selection can be done by an on-board dedicated dip switch (see **Figure 7.1**) between the following modes:

- INT mode (default) means REF-CLK is the 50 MHz of the local oscillator (REF-CLK = OSC-CLK);
- EXT mode means REF-CLK source is the external frequency fed on CLK-IN connector.

The external clock signal must be differential (LVDS, ECL, PECL, LVPECL, CML) with a jitter lower than 100 ppm (see Chap. **3**). CAEN provides the A318 cable to adapt single ended signals coming from an external clock unit into the differential CLK-IN connector (see Chap. **7**).

The V1741 is equipped with a phase-locked-loop (PLL) and clock distribution device, AD9510. It receives the REF-CLK and generates the sampling clock for ADCs and the mezzanine FPGA (SAMP-CLK0 up to SAMPCLK3), as well as the trigger logic synchronization clock (TRG-CLK) and the output clock (CLK-OUT).

AD9510 configuration can be changed and stored into non-volatile memory. Changing the AD9510 configuration is primarily intended to be used for external PLL reference clock frequency change (see Sect. **8.4**). The V1741 locks to an external 50 MHz reference clock with default AD9510 configuration.

Refer to the AD9510 datasheet for more details:

http://www.analog.com/UploadedFiles/Data_Sheets/AD9510.pdf

(in case the active link above does not work, copy and paste it on the internet browser)

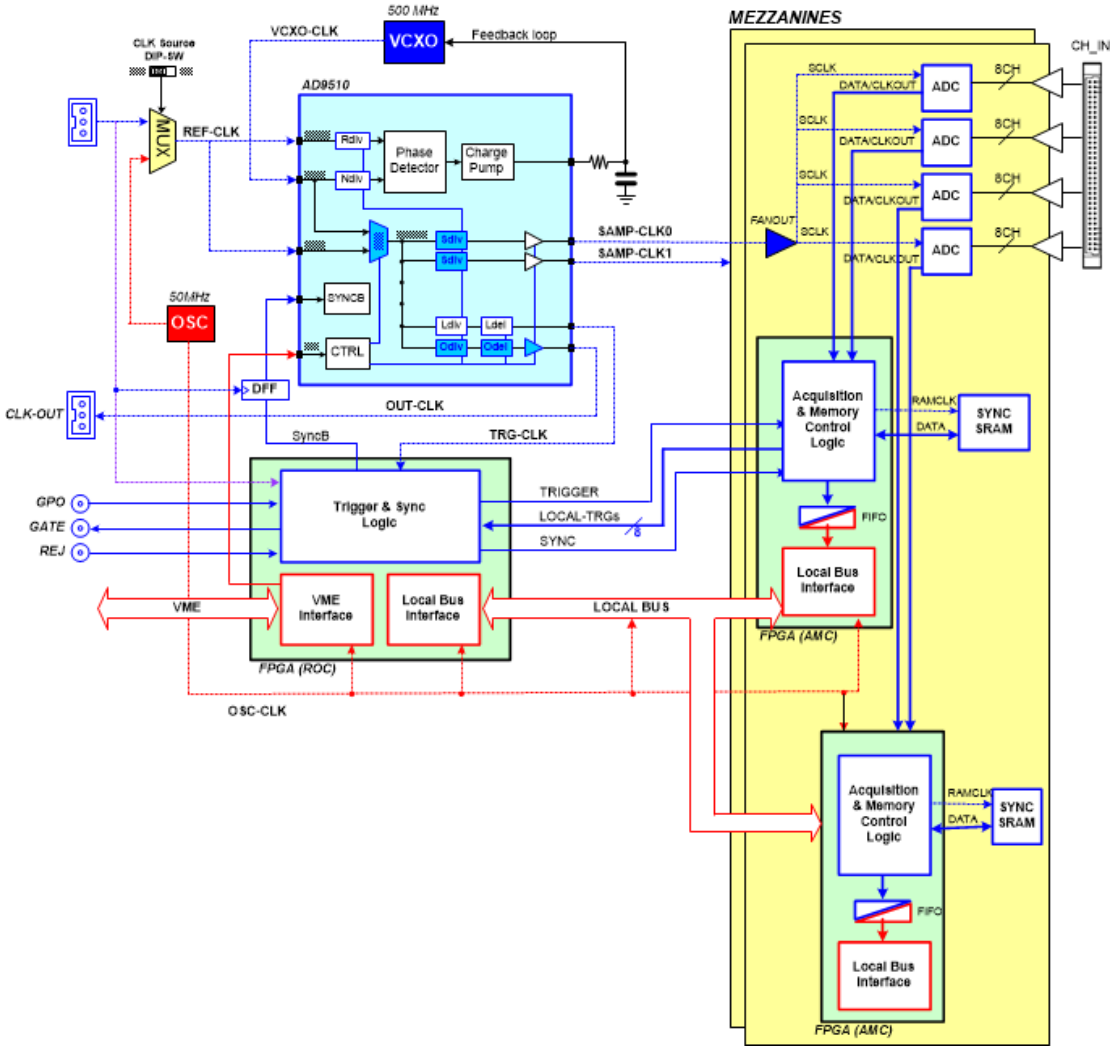


Figure 8.12: Clock Distribution Diagram

8.4 PLL Mode

The Phase Detector inside the AD9510 device allows to couple REF-CLK with an external VCXO, which provides the nominal ADC frequency (62.5 MS/s).

As introduced in Sect. **8.3**, the source of the REF-CLK signal (see **Figure 8.12**) can be external on CLK-IN front panel connector or internal from the 50 MHz local oscillator. Programming the REF-CLK source internal or external can be performed by acting on the on-board dip switch SW2 (see Sect. **7.2**).

The following options are allowed:

1. 50 MHz internal clock source – this is the standard operation mode: the AD9510 dividers do not require to be reprogrammed (the board works in the AD9510 default configuration). The clock source selection dip switch SW2 is in default INT mode. REF-CLK = OSC-CLK.

2. 50 MHz external clock source – in this case, the clock source is taken from an external device; the AD9510 dividers do not need to be reprogrammed as the external frequency is the same as default one. The clock source selection dip switch must be set in EXT mode. CLK-IN = REF-CLK = OSC-CLK.

3. External clock source different from 50 MHz – the clock source is externally provided as in point 2, but the AD9510 dividers must now be reprogrammed to lock the VCXO to the new REF-CLK in order to provide out the nominal sampling frequency at 62.5 MS/s. The clock source selection dip switch must be set in EXT mode. CLK-IN = REF-CLK ≠ OSC-CLK.

If the board is locked, the PLL-LOCK front panel LED must be on.

Note: the user can update the PLL on the board by using the CAEN Upgrader software tool **[RD2]**.

8.5 Trigger Clock

The Trigger logic works at 125 MHz, equal to 2SAMP-CLK, while triggers are sensed, generated, and distributed by the motherboard at 62.5 MHz. The actual trigger clock has so the same frequency as the sampling clock (TRG-CLK = SAMPL-CLK).

8.6 Output Clock

The AD9510 output can be available on the front panel CLK-OUT connector (see **Figure 8.12**). This option is particularly useful in case of multi-board synchronization to propagate the clock reference source in Daisy Chain.

Please, contact CAEN for more information (see Chap. **17**).

8.7 Multi-Event Memory Organization

The internal memory of the V1741 can contain up to 1024 events. When the memory goes full, no further gate/trigger is accepted. The dead time counter also accounts for the dead time due to the memory full conditions. Read access to the memory for readout is always possible and it is completely independent of the data conversion and acquisition.

The data structure of the event is described in the following section, and it can be retrieved in the binary output format (RAW data dump, refer to next section and Sect. **10.4.3**).

8.8 Event Structure

The event can be read out via VMEbus or Optical Link. The data saving is enabled through the start acquisition, and it stops at the stop acquisition command. Data can be saved into three different ways: Raw, List and Histo.

8.8.1 List Format

The LIST mode allows to save the energy and time information related to all the enabled channels. The output file (*run0_b0_seg0.txt*) is a text file in column format. The first column represents the Trigger (namely the event number), the second one the Time Stamp and the other columns represent the pulse height (Energy in channels) of the event for each input channel.

When a channel is not enabled, the reported value is N/A. In case of enabled zero suppression, if the event does not exceed the zero-suppression threshold, the reported value is ZS.

8.8.2 Histo Format

The HISTO mode allows to save the spectrum of each channel (for channel 0, the output file is "*run0_b0_ch0.txt*", for channel 1 the output file is "*run0_b0_ch1.txt*", etc). Each channel has its own histo file and the file format is two column spectrum (.txt). The order of the columns is: channel number and counts.

The HISTO mode allows to save the spectrum of each channel (for channel 0, the output file is "*run0_b0_ch0.txt*", for channel 1 the output file is "*run0_b0_ch1.txt*", etc). Each channel has its own histo file and the file format is two column spectrum (.txt). The order of the columns is: channel number and counts.

8.8.3 Raw Data Format

The user can select if saving or not the raw data of the subsequent run. Raw data are saved in binary format and corresponds to the board dump.

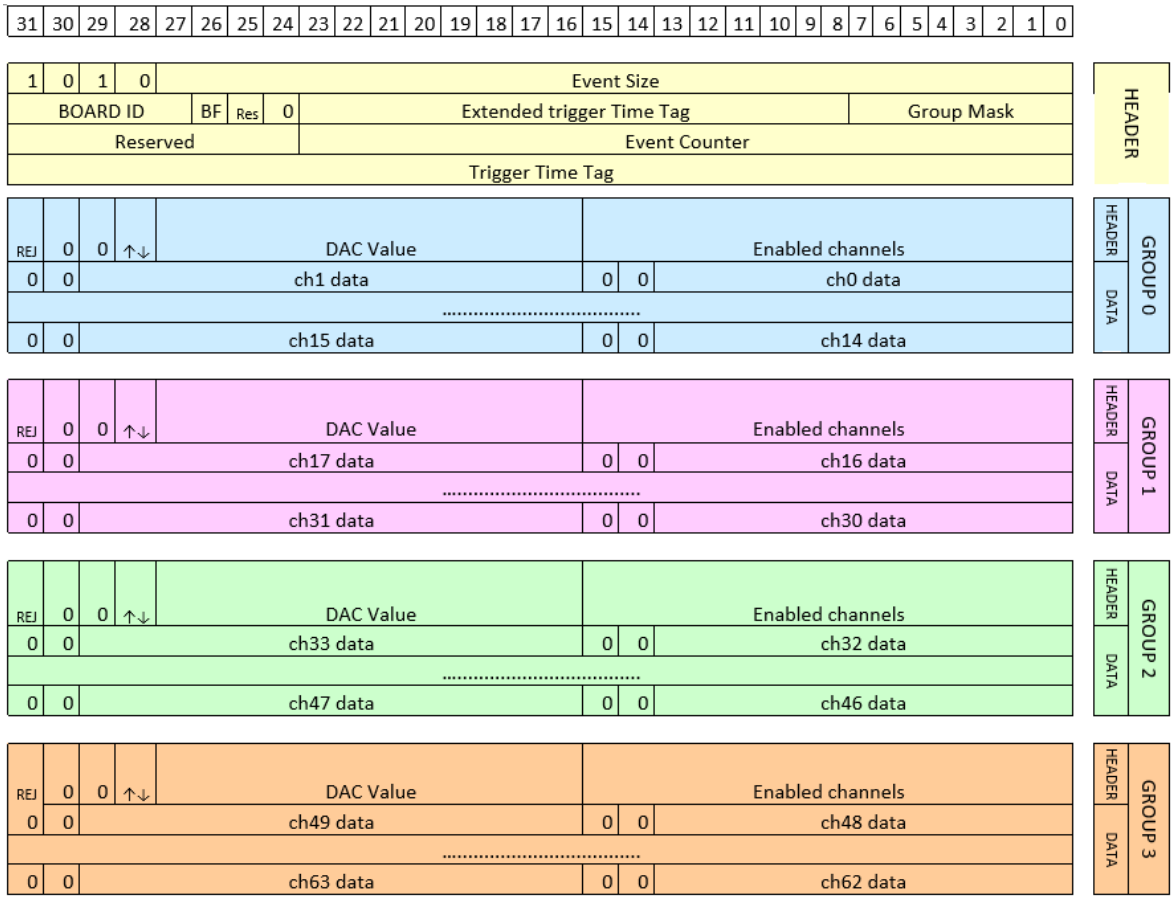


Figure 8.13: Event Format Example

An event is structured in:

HEADER: The Header (see **Figure 8.13**) consists of four words including the following information:

EVENT SIZE (bits[27:0] of 1st header word) is the total size of the event, i.e. the number of 32-bit long words to be read.

BOARD ID (bits[31:27] of 2nd header word) is the GEO address, meaningful for VME64X modules only.

BOARD FAIL FLAG (bit[26] of 2nd header word) is set to "1" as a consequence of a hardware problem (e.g. PLL unlocking). The user can collect more information about the cause by reading at register address 0x8178 and contacting CAEN Support Service if necessary (see Chap. **17**).

EXTENDED TRIGGER TIME TAG (bits[23:8] of 2nd header word) are the 16-bit most significant bit of the trigger timestamp.

GROUP MASK (bits[7:0] of 2nd header word) is the mask of the groups participating in the event (for example, GR1 and GR3 participating → Group Mask = 0xA). Each group is made of 16 channels. This information must be used by the software to associate the correct amplitude to each channel (the first amplitude is related to the lowest active channel).

EVENT COUNTER (bits[23:0] of 3rd header word) is the trigger counter; it can count either accepted triggers only, or all triggers (bit[3] of register address 0x8100).

TRIGGER TIME TAG (bits[31:0] of 4th header word) are the 32 less significant bits of the 48-bit Extended Trigger Time Tag information in addition to the 16 bits (MSB) of the 2nd event word. The trigger time tag is reset either at the start of acquisition, or via the LVDS I/O connectors. It increments with 125 MHz frequency (i.e. every 1/2 ADC clock cycle). The TTT value is read at half this frequency (i.e. 62.5 MHz) so that the specifications are 16 ns resolution and 625 h range (8 ns x (2^{48} – 1))

DATA: Data can be of variable format. An example of data format is reported in **Figure 8.13**. The data section is composed of four groups of 16 channels, when enabled. For each group, the header is a single 32-bit word, regardless the number of enabled channels.

The information reported in the **group header** is:

REJ (bit[31]): when 1, the event has been rejected by the logic signal coming from the REJ LEMO front panel connector.

(↑↓) (bit[28]) represents the DAC direction. In the figure, it is symbolized by upward and backward arrows.

DAC value (bits[27:16]) is the value of the DAC used by the sliding scale algorithm, when enabled.

ENABLED CHANNELS (bit[15:0]) is the mask of the enabled channels, for example, if ch0 and ch10 are enabled, then this field will be equal to: 0x401.

The header is followed by the 32-bit data words for each group, where each word corresponds to two channels. Therefore, the number of data words is half of the number of enabled channels. If this number is odd, the number of words is rounded off to the biggest number of words.

For example, if channel 0 is the only enabled channel, the data format will consist of:

- board header (4 words)
- group 0 header (1 word)
- channel 0 data (1 word)
- header of the remaining groups (3 words)

Note: The 16th bit of each channel in DATA can be 1 if at list one point is overrange during the moving average.

Note: Data transfer starts from Channel 0 of Group 0; once all the data from one Group is transferred, data transfer from the subsequent Group begins.

8.9 Front Panel LVDS I/Os

The V1741 is provided with 16 general purpose programmable LVDS I/O signals (see Chap. **7**) with a flexible configuration management that allows these signals to be programmed in terms of direction (INPUT/OUTPUT) and function by groups of 4.

The following configuration modes are enabled by setting bit[8] = 1 @ 0x811C **[RD1]**.

The direction of the signals are set by the bits[5:2] at register address 0x811C:

Bit[2] → LVDS I/O[3:0]
Bit[3] → LVDS I/O[7:4]
Bit[4] → LVDS I/O[11:8]
Bit[5] → LVDS I/O[15:12]

Where setting the bit to 0 enables the relevant signals in the group as INPUT, while 1 enables them as OUTPUT.

If this mode is disabled (i.e. bit[8] = 0), the status of the LVDS I/O signals is as follows **Table 8.1**.

Nr.	Direction	Function	Description
0	out	GR 0 trigger request	Over-threshold information
1	-	Reserved	
2	out	GR 1 trigger request	
3	-	Reserved	
4	out	GR 2 trigger request	
5	-	Reserved	
6	out	GR 3trigger request	
7	-	Reserved	
8	out	Memory Full	Memory full flag
9	out	Event Data Ready	Board event data ready flag
10	-	Reserved	N.A.
11	out	RUN Status	Board run flag
12	-	Reserved	N.A.
13	-	Reserved	N.A.
14	-	Reserved	N.A.
15	-	Reserved	N.A.

Table 8.1: Front Panel LVDS I/Os default settings

When enabled (i.e. bit[8] = 1), the new management allows each group of 4 signals of the LVDS I/O 16-pin connector to be configured in one of the 4 following modes (according to bits[15:0] at register address 0x81A0):

- Mode 0 (bits[n+3:n] = 0000): REGISTER
- Mode 1 (bits[n+3:n] = 0001): TRIGGER
- Mode 2 (bits[n+3:n] = 0010): nBUSY/nVETO
- Mode 3 (bits[n+3:n] = 0011): LEGACY

where n = 0, 4, 8, 12.

Note: Data transfer starts from Channel 0 of Group 0; once all the data from one Group are transferred, data transfer from the subsequent Group begins.

Whatever option is set, the LVDS I/Os are always latched with the trigger, the user can then choose to read it out or not.

	REGISTER	TRIGGER	nBUSY/nVETO	LEGACY
LVDS IN [15:12]	Reg[15:12]	*Not available*	15: Reserved 14: Reserved 13: nVetoIn 12: nBusyIn	*Not available*
LVDS IN [11:8]	Reg[11:8]	*Not available*	11: Reserved 10: Reserved 9: nVetoIn 8: nBusyIn	*Not available*
LVDS IN [7:4]	Reg[7:4]	*Not available*	7: Reserved 6: Reserved 5: nVetoIn 4: nBusyIn	*Not available*
LVDS IN [3:0]	Reg[3:0]	*Not available*	3: Reserved 2: Reserved 1: nVetoIn 0: nBusyIn	*Not available*

Table 8.2: Features description when LVDS group is configured as INPUT

	REGISTER	TRIGGER	nBUSY/nVETO	LEGACY
LVDS OUT [15:12]	Reg[15:12]	15: Reserved 14: Gate 13: Reserved 12: Gate	15: nRun 14: nGate 13: nVeto 12: nBusy	15: Run 14: Gate 13: DataReady 12: Busy
LVDS OUT [11:8]	Reg[11:8]	11: Reserved 10: Gate 9: Reserved 8: Gate	11: nRun 10: nGate 9: nVeto 8: nBusy	11: Run 10: Gate 9: DataReady 8: Busy
LVDS OUT [7:4]	Reg[7:4]	7: Reserved 6: Gate 5: Reserved 4: Gate	7: nRun 6: nGate 5: nVeto 4: nBusy	7: Run 6: Gate 5: DataReady 4: Busy
LVDS OUT [3:0]	Reg[3:0]	3: Reserved 2: Gate 1: Reserved 0: Gate	3: nRun 2: nGate 1: nVeto 0: nBusy	3: Run 2: Gate 1: DataReady 0: Busy

Table 8.3: Features description when LVDS group is configured as OUTPUT

8.9.1 MODE 0: REGISTER

Direction is INPUT: the logic level of the LVDS I/O signals can be read at register address 0x8118.

Direction is OUTPUT: the logic level of the LVDS I/O signals can be written at register address 0x8118.

8.9.2 MODE 1: TRIGGER

Direction is INPUT: Not available.

Direction is OUTPUT: even pins provides a copy of the internal gate Gate.

8.9.3 MODE 2: nBusy/nVeto

- The **nBusy** as INPUT (nBusyIn) is an active low signal which, if enabled, is used to generate the nBusy signal OUTPUT as below.

The Busy signal (fed out on LVDS I/Os or TRG-OUT LEMO connector) is:

Almost_Full OR (**LVDS_BusyIn** AND **BusyIn_enable**)

Where

- **Almost_Full** indicates the filling of the Buffer Memory up to a programmable level (12-bit range) set at register address 0x816C;
- **LVDS_BusyIn** is available in nBUSY/nVETO configuration (see **Table 8.2**);
- **BusyIn_enable** is set at register address 0x8100, bit[8].

- The **nVETO** as INPUT (nVetoIn) is an active low signal which, if enabled (register address 0x8100, bit[9] = 1), is used to veto the generation of the common trigger propagated to the channels for the event acquisition. The nVETO as OUTPUT is the copy of nVETOIn signal.
- The **nGate** as INPUT is not available. As OUTPUT, the nGate signal is the copy of the trigger signal propagated to the GPO LEMO connector or copy of the acquisition common gate. This is selected by bit[16] of the 0x81A0 register.
- The **nRun** as INPUT is not available. As OUTPUT, the nRun signal is the inverse of the internal Run of the board.

8.9.4 MODE 3: LEGACY

Legacy Mode corresponds to the case when bit[8]=0 @ 0x8100.

Only output signals are available:

- **Busy signal** is active high and it is exactly the inverse of the nBusy signal (see Sect. **8.9.3**). In case register address 0x816C is set to 0 and the BusyIn signal is disabled, the Busy is the FULL signal present in the old configuration.
- **DataReady signal** is an active high signal indicating that the board has data available for readout (the same as the DataReady front panel LED does).
- **Gate signal** is active high Gate signal and it is the copy of the acquisition Gate.
- **Run signal** is active high and represents the inverse of the nRun signal (see Sect. **8.9.3**).

8.10 Reset, Clear, and Default Configiuration

8.10.1 Global Reset

Global Reset is performed at power-on of the module or via software by write access at register address 0xEF24. It allows the board to clear the data off the Output Buffer, the event counter and performs a FPGAs global reset, which restores the FPGAs to the default configuration. It initializes all counters to their initial state and clears all detected error conditions.

8.10.2 Memory Reset

The Memory Reset clears the data off the Output Buffer.

The Memory Reset can be forwarded via a write access at register address 0xEF28 (whatever 32-bit value can be written).

8.10.3 Time Reset

The Timer Reset allows to initialize the trigger timer and it can be done at the start acquisition.

8.11 VMEBus Interface

The module is provided with a fully compliant VME64 interface, whose main features are:

- EUROCARD 9U Format
- J1/P1 and J2/P2 with either 160 pins (5 rows) or 96 (3 rows) connectors
- A24, A32 and CR-CSR address modes
- D32, BLT/MBLT, 2eVME, 2eSST data modes
- MCST write capability
- CBLT data transfers
- RORA interrupter
- Configuration ROM

8.11.1 Addressing Capabilities

- Base address: the module works in A24/A32 mode The Base Address of the module is selected through four rotary switches (see **Figure 7.1**), then it is validated only with either a Power-ON cycle or a System Reset (see Sect. **8.10**).

ADDRESS MODE	ADDRESS RANGE	NOTES
A24	[0x000000:0xFF0000]	SW2 and SW3 ignored

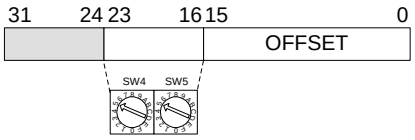


Table 8.4: A24 addressing

ADDRESS MODE	ADDRESS RANGE	NOTES
A32	[0x00000000:0xFFFF0000]	-

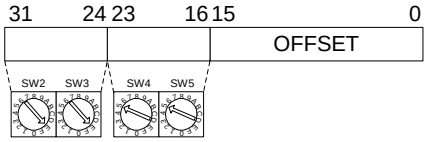


Table 8.5: A32 addressing

- CR/CSR address: the addressing is based on the slot number taken from the relevant backplane lines. The recognised Address Modifier for this cycle is 2F. *This feature is implemented only on versions with 160-pin connectors*.

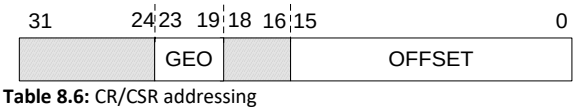


Table 8.6: CR/CSR addressing

8.11.2 Address Relocation

The bit[15:0] of register address 0xEF10 allow to set via software the board Base Address (valid values ≠ 0). Such register allows to overwrite the rotary switches settings; its setting is enabled via bit[6] of the register address 0xEF00. The used addresses are:

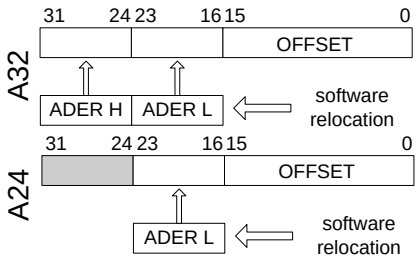


Table 8.7: Software relocation of base address

8.12 Data Transfer Capabilities and Events Readout

The board features a Multi-Event digital memory; once the event is written in the memory, it becomes available for readout via VMEbus or Optical Link. During the memory readout, the board can store other events (independently from the readout) on the available free buffers.

The events are read out sequentially and completely, starting from the Header of the first available event, followed by the data from the enabled groups (from 0 to 3). Once an event is completed, the relevant memory buffer becomes free and ready to be written again (old data is lost). After the last word in an event, the first word (Header) of the subsequent event is readout. It is not possible to read out an event partially.

The size of an event (EVENT SIZE) is configurable and depends on register addresses 0x8020 and 0x800C, as well as on the number of enabled channels. The board supports D32 single data readout, Block Transfer BLT32 and MBLT64, 2eVME and 2eSST cycles. Sustained readout rate is up to 70 MB/s with MBLT64, up to 200 MB/s with 2eSST.

8.13 Optical Link Access

The board houses a Daisy chainable Optical Link (communication path which uses optical fiber cables as physical transmission line) able to transfer data at 80 MB/s. Therefore, it is possible to connect up to eight V1741 to a single Optical Link Controller by using the A2818 PCI card or up to thirty-two V1741 with the A3818 PCIe card.

Detailed information can be found at the relevant controller web page on CAEN website.

The parameters for read/write accesses via Optical Link are the same used by VME cycles (Address Modifier, Base Address, data Width, etc); wrong parameter settings cause Bus Error.

VME and Optical Link accesses take place on independent paths and are handled by board internal controller, with VME having higher priority; anyway, it is better to avoid accessing the board via VME and Optical Link simultaneously.

9 Drivers & Libraries

9.1 Drivers

To interface with the board, CAEN provides Windows® and Linux® drivers for the different types of the supported physical communication links:

- **CONET Optical Link**, managed by the A2818 (PCI) and A3818 (PCIe) cards. The driver installation packages are downloadable for free on CAEN website at the A2818 or A3818 page respectively (**login required**).

Note: For the installation of the Optical Link driver, refer to the User Manual of the specific card **[RD13][RD14]**.

- **USB-2.0 Link**, managed by the CAEN (USB-to-VME) Bridges V3718 or V1718 (obsolete). The driver installation packages are downloadable for free on CAEN website at the V3718 and V1718 page respectively (**login required**).
- **USB-3.0 Link**, managed by the V4718 (USB3-to-VME) Bridge and by the A4818 (USB3-to-CONET) Adapter. The driver installation packages are downloadable for free on CAEN website at the V4718 and A4818 page respectively (login required).

Note: To install the USB Link driver, follow the instructions inside the ReadMe file included in the packet, or refer to the V3718 V4718 User Manuals **[RD15][RD16]**, or A4818 Data Sheet **[RD15]**.

9.2 Libraries

CAEN libraries are a set of middleware software required by CAEN software tools for a correct functioning. These libraries, including also demo and example programs, represent a powerful base for users who want to develop customized applications for the digitizer control (communication, configuration, readout, etc.):

- **CAENComm** library manages the communication at low level (read and write access). The purpose of the CAENComm is to implement a common interface to the higher software layers, masking the details of the physical channel and its protocol, thus making the libraries and applications that rely on the CAENComm independent from the physical layer. Moreover, the CAENComm requires the CAENVMELib library (access to the VME bus) even in the cases where the VME is not used. This is the reason **why CAENVMELib must be already installed on your PC before installing the CAENComm.**
  The CAENComm installation package, the relevant documentation Errore. L'origine riferimento non è stata trovata. and the link to the required CAENVMELib, are available on CAEN website in the ”Download” tab at the CAENComm Library page.

- **CAENPeakSensingLib** is a set of functions specifically designed for the x741 Digital Peak Sensing ADC boards. The CAENPeakSensingLib library is based on the CAENComm which is in turn based on CAENVMELib. For this reason, **the CAENVMELib and CAENComm libraries must be already installed on the host PC before installing the CAENPeakSensingLib**.
  The CAENPeakSensingLib installation package is available on CAEN website in the “Download” tab at the Peak Sensing page.

CAENComm (and other libraries here described) supports the following communication channels (see **Figure 9.1**)

PC → USB3 → A4818 → CONET → V1741

PC → USB → V3718/VX3718 → VMEbus → V1741

PC → USB3 → V4718/VX4718 → VMEbus → V1741

PC → USB → V1718/VX1718 (Obsolete) → VMEbus → V1741

PC → USB3 → A4818 → CONET → V3718/VX3718 → VMEbus → V1741

PC → USB3 → A4818 → CONET → V4718/VX4718 → VMEbus → V1741

PC → PCI/PCIe → A2818/A3818 → CONET → V1741

PC → PCI/PCIe → A2818/A3818 → CONET → V3718/VX3718 → VMEbus → V1741

PC → PCI/PCIe → A2818/A3818 → CONET → V4718/VX4718 → VMEbus → V1741

PC → PCI/PCIe → A2818/A3818 → CONET → V2718/VX2718 (Obsolete) → VMEbus → V1741

PC → ETHERNET → V4718/VX4718 → VMEbus → V1741

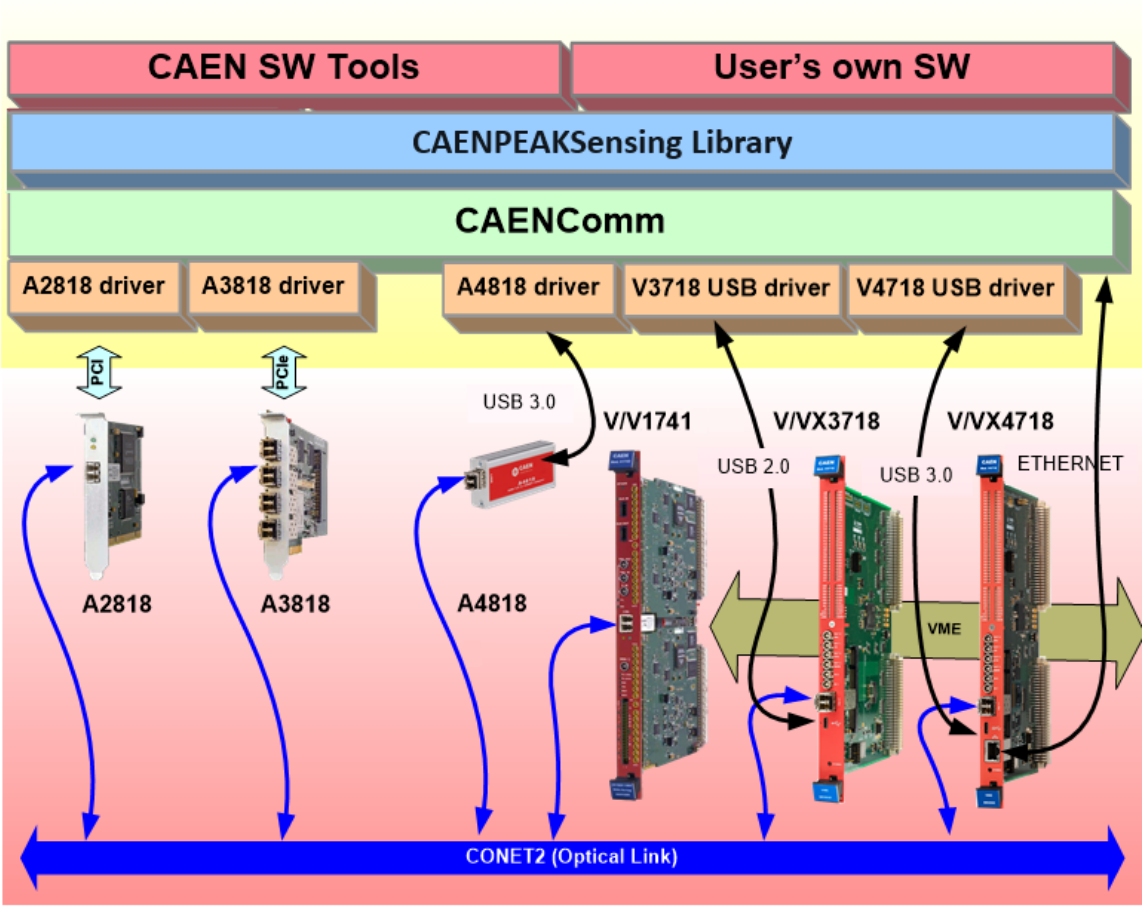


Figure 9.1: Drivers and software layers

10 Software

This Section will guide you through the installation of the Peak Sensing Data Acquisition Software and will highlight the main features of the V1741 board.

10.1 Software Installation

Peak Sensing Data Acquisition Software is a command line application which shows the x741 operation using the APIs displayed by **CAENPeakSensingLib**.

The installation steps of the **Peak Sensing Data Acquisition Software** are:

- Go to CAEN V1741 web page:

  www.caen.it/download/?filter=V1741

- Download the **CAENPeakSensingLib** and the **Peak Sensing Demo Software** package related to your OS.
- Unzip the downloaded packages.
- Install first the CAENPeakSensingLib and all the CAEN libraries needed. The installation order is:
  - CAENVME Lib
  - CAENComm Lib
  - CAENPeakSensingLib
- Install the **Peak Sensing Demo Software** according to the corresponding OS:
  - **For Windows users:** launch the CAEN Upgrader Setup executable file, then follow the installer instructions.

    To open the software, go under the path: `C:\Users\<USERNAME>\PeakSensing_DAQ`

    Launch the executable. The *configuration file* can be modified in the folder itself.
  - **For Linux users:** follow the installation instructions within the README file inside the package.

    The *library* can be installed with the command:

    ```
    sudo sh install
    ```
    (32bit OS)

    ```
    sudo sh install_64
    ```
    (64bit OS)

    The *software* package can be installed with the commands:

    ```
    ./configure
    make
    sudo make install
    ```

To launch the software, write `PeakSensing_DAQ` in a command shell. The *configuration file* is located by default under the folder `/etc/PeakSensing_DAQ/PeakSensing_Config.txt`. The user can also modify a local copy of the file and write the command `PeakSensing_DAQ Config_file.txt` to execute that specific file.

10.2 Acquisition Setup

The section is intended to deal with the main features of CAEN x741 – Digital Peak Sensing ADC step by step. A typical spectroscopy acquisition chain, by using x741 module, is shown in **Figure 10.1**.

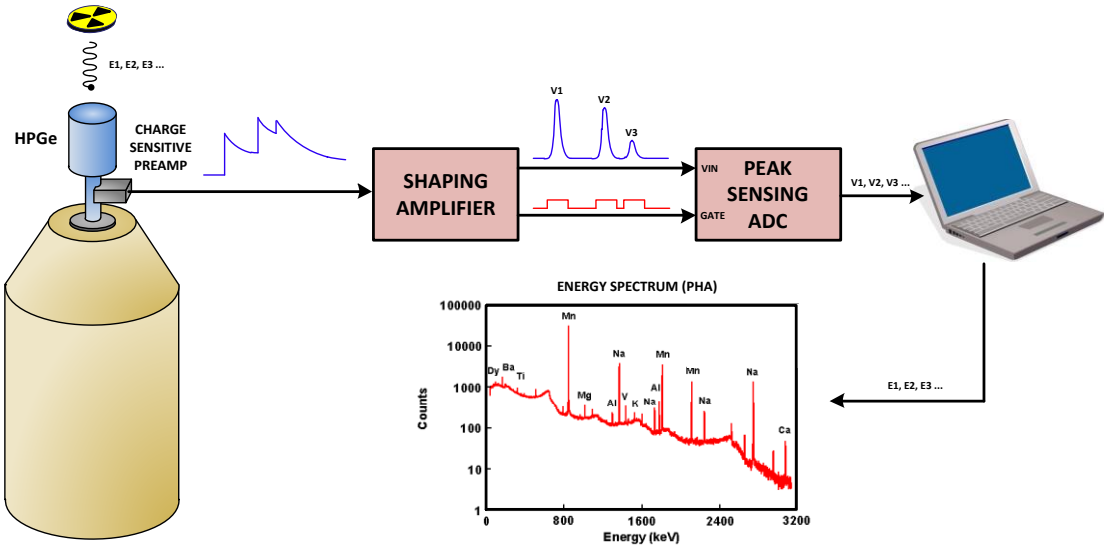


Figure 10.1: Typical spectroscopy acquisition chain with x741 module

To run the system, the signals and gate must be plugged in the Channel Inputs and GATE connector, respectively. The acquisition gate used for the peak detection can be generated using this signal in two different ways:

- **gate mode**: the gate lasts for the duration of the GATE signal (NIM or TTL);
- **edge mode**: the gate starts with the leading edge of the GATE signal and lasts for a user programmable time.

The board is busy for the whole duration of the gate and it does not accept any further trigger until the gate is over, although it counts all the triggers, including the rejected ones.

Figure 10.2 shows the typical signals related to a system with x741. The blue signal is the preamplified signal, the cyan one is the gaussian signal from shaping amplifier (in this example CAEN Mod. N1068 **[RD8]**) fed in input to the peak sensing, the magenta one is the GATE start and finally the green signal is the user programmed gate, approximately 10 µs long.

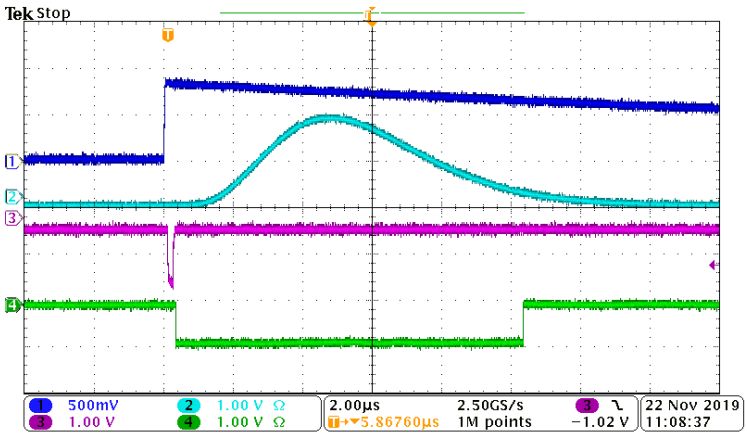


Figure 10.2: Oscilloscope screenshot of the typical x741 trigger mode working conditions. From top to bottom, the signal from preamplifier (blue), the output of the shaping amplifier (cyan), the GATE start (signal fed into the GATE connector, magenta), and user programmed gate, approximately 10 µs long (green)

The connection between the V1741 and the shaping amplifier can be established in two ways:

- Using the A746B adapter (**Figure 10.3**);
- Using the A371 32-ch adapter in combination with two A385 16-ch LEMO adapter (**Figure 10.4** and **Figure 10.5**).

The A746B is a 2U VME unit with 64-ch LEMO connectors. The board can be plugged into the two ERNI SMC-114805 connectors of the V1741 to convert the 64-ch inputs into LEMO connector inputs. The board must be placed on a side of the V1741 in the VME crate.

Figure 10.3: Connection of the V1741 to the A746B 64-ch LEMO adapter

In the second case, two A371 adapters must be screwed into the ERNI ports of the V1741. **Figure 10.4** shows the correct mounting side of the A371 adapters, while **Figure 10.5** shows how to connect the A371 with two A385 adapters.

The upper row in the A371 corresponds to channel 0. The first pin series corresponds to ch0 to 15, where the last pin is not used, the second row correspond to ch16 to ch31, with again the last pin not used.

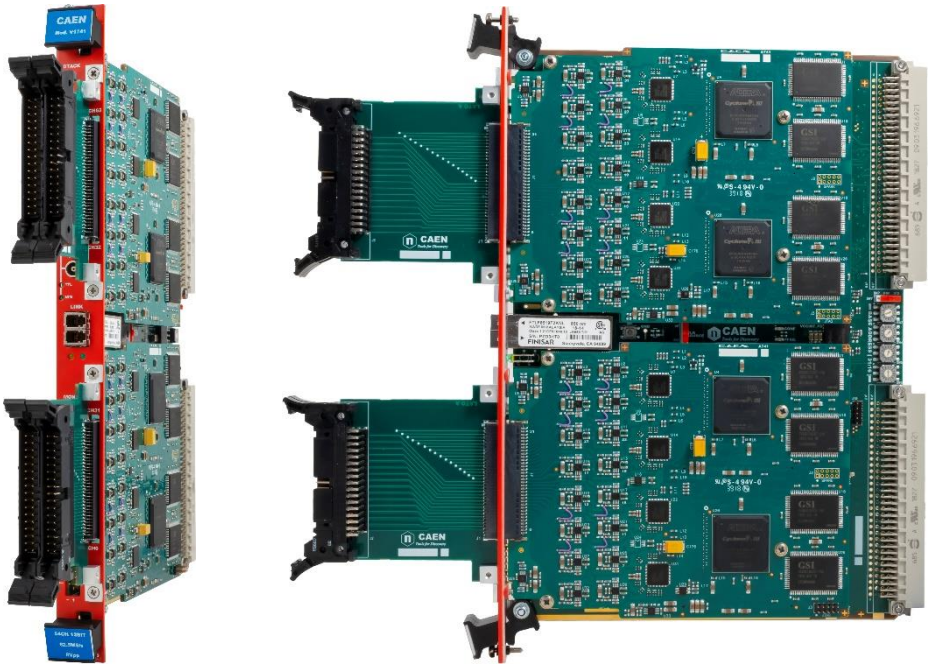


Figure 10.4: A371 32-ch ERNI adapter plugged into the ERNI connectors of V1741, side and front view on the right and left pictures respectively

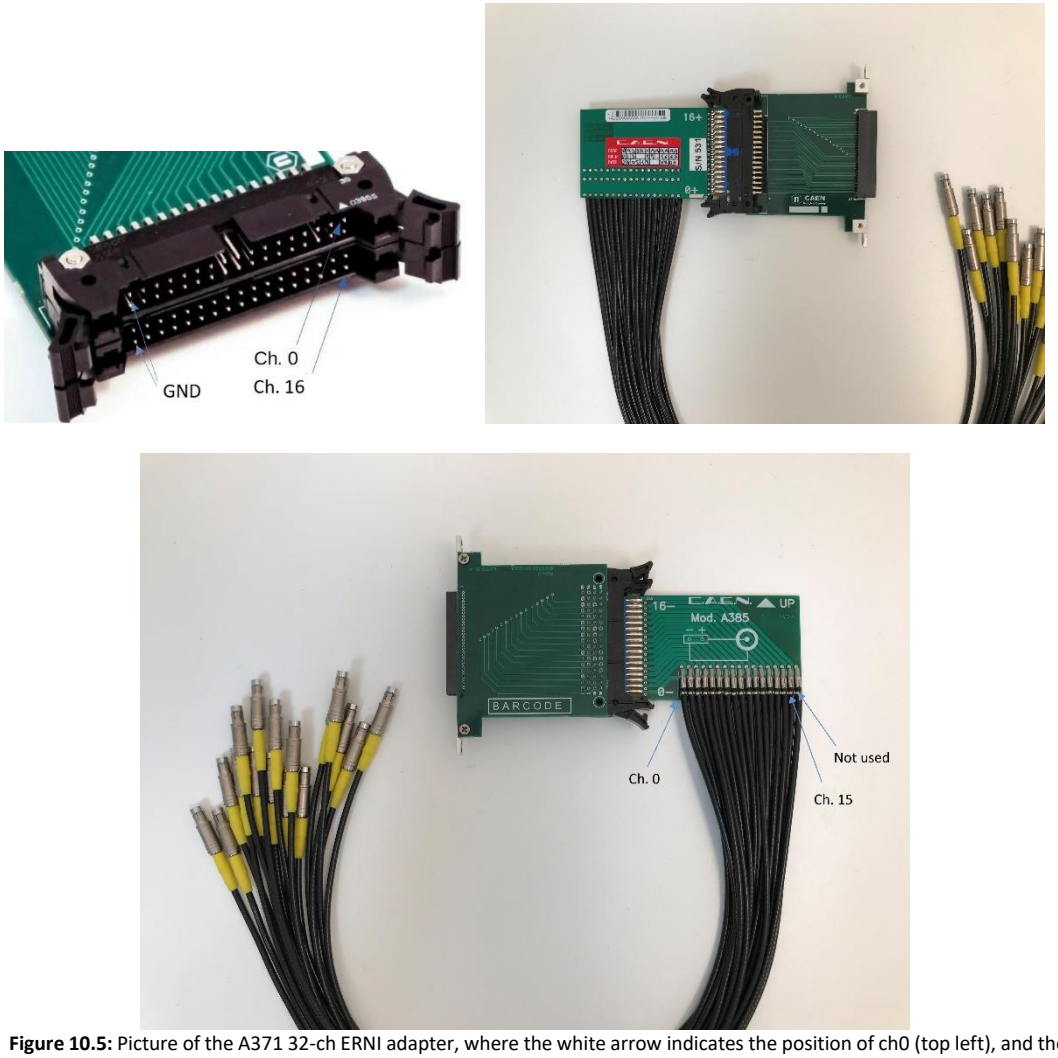


Figure 10.5: Picture of the A371 32-ch ERNI adapter, where the white arrow indicates the position of ch0 (top left), and the connection of A371 and A385 with the correspondence of the cables to channels

10.3 Getting Started

The paragraphs below highlight the main functions provided by CAEN Peak Sensing Data Acquisition Software after you have performed two basic actions:

- turn on the system and connect it to the PC;
- launch the CAEN Peak Sensing Data Acquisition Software.

All the boards have been calibrated previously and, after launch, the software allows to upload the calibration (see **Figure 10.6**).

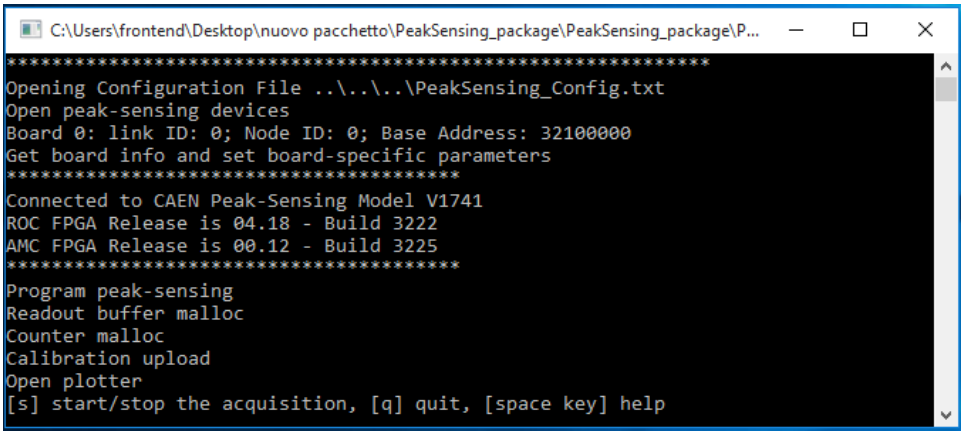


Figure 10.6: Command window opening

The command window allows to run the main actions like Start/Stop the acquisition via “s” button and other operations listed by “space key”, as shown in the following picture (**Figure 10.7**).

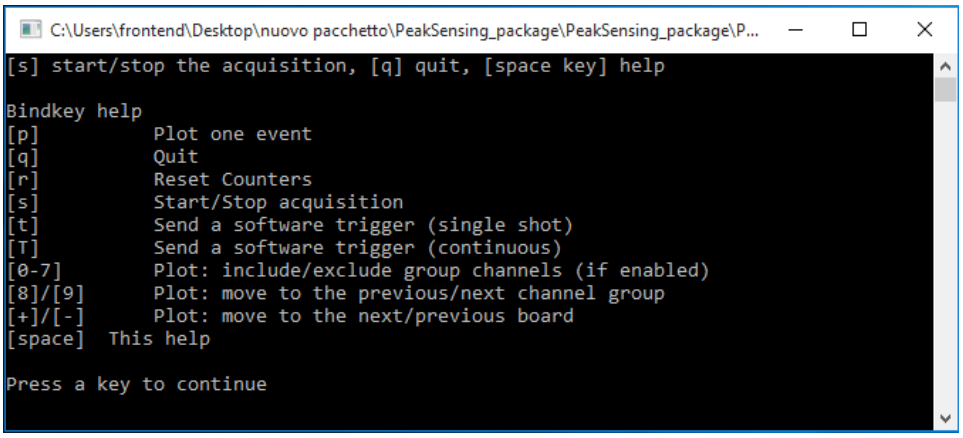


Figure 10.7: List of the main software commands

During the acquisition, the command window reports the information related to the board activity. More in details:

- Board: board number;
- Real time: full acquisition time;
- Live Time: time available for data taking;
- Dead Time: time unavailable for data taking as % of full acquisition time;
- Throughput: amount of transmitted data;
- Detected trigger rate: rate of valid triggers/gates at the GATE input connector;
- Processed trigger rate: rate of the processed triggers/gates;
- Pile-up Rate: rate of the pile-up event occurred;
- Channel index: name of the input channel being displayed;
- Saturated (SAT): percentage of excluded events due to the saturation effect;
- Suppressed: percentage of suppressed events due to the rejection gate;

- OCR: output counting rate, namely number of processed events;
- OCR (incl. SAT): output counting rate that includes the saturated events;
- Trigger index: event number;

Event timestamp: time of the recorded event.

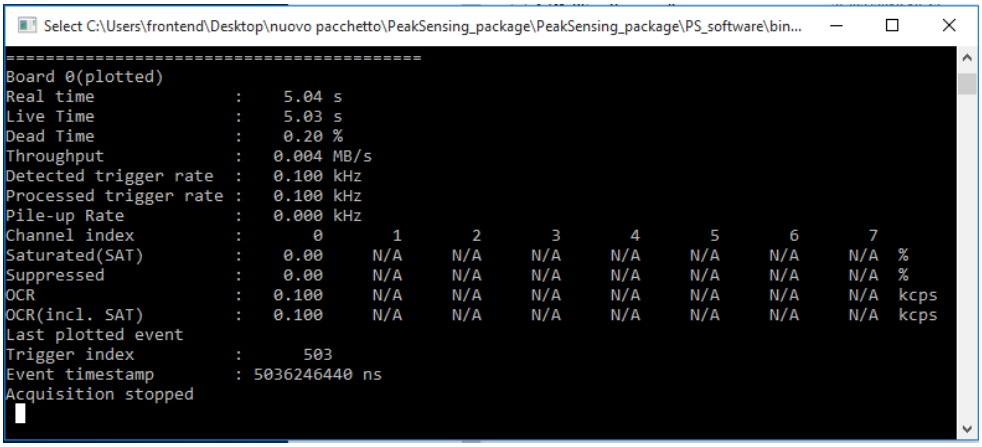


Figure 10.8: Acquisition report

While **PeakSensing.exe** is running, a gnuplot window containing the live acquisition spectrum is also active. **Figure 10.9** shows an example of a **^{137}Cs** energy spectrum, in both linear and logarithmic scale, obtained with the x741 peak sensing on channel 0. The source signal was provided by a $LaBr_3$ scintillator, while the readout was made of the CAEN N1068 shaping amplifier and the x741 in the 4096 channels configuration, settable in the peak sensing configuration file as it will be explained in the next section. Examples of applications with Peak Sensing ADC are also reported in **[RD10]** and **[RD11]**.

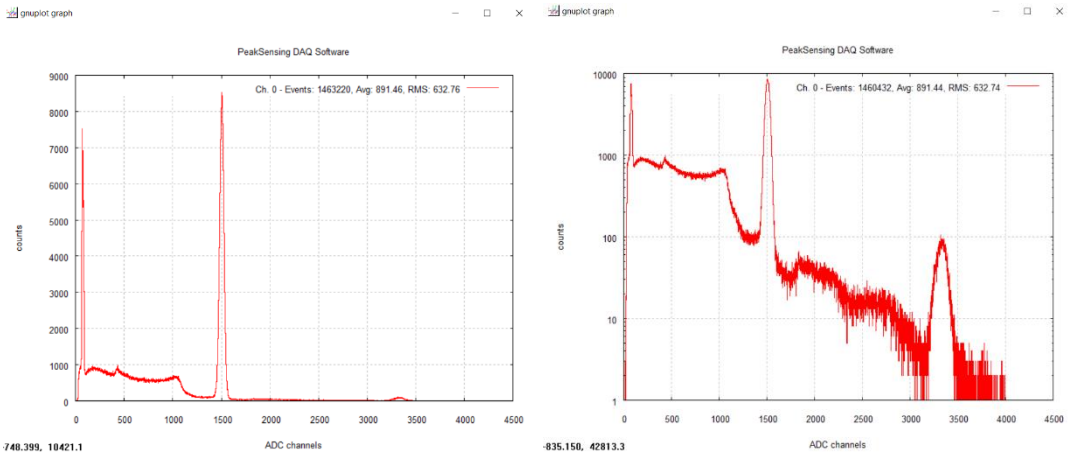


Figure 10.9: ^{137}Cs energy spectrum acquired on channel 0 of the Peak Sensing ADC in linear and logarithmic scale (left and right respectively)

10.4 Configuration File

The CAEN Peak Sensing Acquisition Software configures the board according to the parameters provided by the configuration files and executes readout cycles from the board itself. The acquisition settings and connection type can be modified before launching the program.

The setting modes can be related to a single board or can be the same for several boards, and moreover they can be spread to some or all the channel groups. The software manages the 64 channels of the module via 4 groups. Each group is composed of 16 channels set in the same way, except for the Zero-suppression threshold, which is common among 8-channels groups. There is a hierarchy in the modes concerning a specific setting: if a setting can be GROUP-dependent, it can also be BOARD-dependent or COMMON, but not all option that are COMMON can also be BOARD- or GROUP-dependent.

The configuration file format is text type, structured in separate lines commands. For each line, initial spacing characters (spaces, tabs, etc.) are ignored.

If the first character line is #, the line is considered commented, and all content is ignored. The valid lines (not commented) are structured as follows, where:

parameter_id [parameter_value]

- *parameter_id*: a keyword that specifies the parameter name
- *parameter_value*: the value of the parameter

parameter_id and *parameter_value* must be separated at least by a space character.

Note: parameters values must be modified before starting an acquisition cycle. Any modification to the parameters during an acquisition will become valid only after closing and relaunching the **PeakSensing_DAQ.exe** file.

10.4.1 Connection Type

Select your connection type among the possible choices, USB or OPTICAL LINK:

```
OPEN [LINK TYPE] [LINK NUM] [CONET NODE] [BA]

Where LINK TYPE:

# USB [LINKNUM] 0   ->  Desktop/NIM board connected through USB

# USB [LINKNUM] [BA]  ->  VME board connected through USB-V1718 (BA = BaseAddress of the VME board, 32 bit hex)

# PCI [LINKNUM] [CONET NODE] 0 ->  Desktop/NIM/VME board connected through CONET (optical link)

# PCI [LINKNUM] [CONET NODE] [BA] -> VME board connected through V2718 (BA = BaseAddress of the VME board, 32 bit hex)
```

In the following example, the V1741 board is connected to the computer through the CAEN USB V1718 bridge. The USB connection has and the VME Base address of the board (rotary switches setting) must be set:

OPEN USB 0 0x32100000

Note: The base address (if required) must be expressed as a 32-bit number ("0xXXXXXXXX").

10.4.2 Display Area

The acquired spectra are displayed via GnuPlot graphical interface. The GnuPlot executable is automatically loaded by the software, anyway the user can define the path of its own version.

```
# GNUPLOT_PATH ".\gnuplot_exec\win\"
```

The refresh of the statistics and plot can be modified via STAT_REFRESH and PERIODIC_PLOT. For example, the following setting corresponds to a refresh period of 1msec:

```
STAT_REFRESH 1000

PERIODIC_PLOT YES
```

10.4.3 Data Saving Options

The data output can be saved according to the three options listed in Sect. **8.8**: “Raw” (binary format) “List” (a list of time stamp and pulse height for each enabled channel in .txt format), and “Histo” (the histogram of pulse height in .txt format). Options are YES/NO to enable/disable the corresponding output file.

```
OUTFILE_RAW YES
OUTFILE_LIST YES
OUTFILE_HISTO YES
```

Files are saved in the same directory of the executable file, or in the user-defined folder by writing the path in the following line command:

```
OUTFILE_PATH PeakSensing_output\
OUTFILE_NAME run0
```

Note: The default output directory created by the software is: *"UserDir"**Peaksensinsg_DAQ**PeakSensing_output*\ (Windows), and *"UserDir"/PeakSensing_output/* (Linux)

The default file name is run0. According to the user “file_name”, the file name will then be written as:

"file_name"_raw_b#_seg#.bin for the raw

"file name"_list_b#_seg#.txt for the list

"file_name"_histo_b#_c#.txt for the histo

Where *b*, *c*, and *seg* identify the board, channel, and output segment respectively (segmented according to OUTFILE_MAXSIZE, the maximum size of each segment, in MB).

```
OUTFILE_MAXSIZE 300
```

10.4.4 Input Signal

The available input range options are 4V and 8V. Polarity and range of the input signals can be set via the following command line:

```
POLARITY (POSITIVE/NEGATIVE)
INPUT RANGE (8V/4V)
```

For example, a positive signal and 8V range correspond to the following settings:

POLARITY POSITIVE

INPUT_RANGE 8V

The channels acquisition can be configured in several way via the command line:

```
ENABLE_INPUT(VALUE)
```

Where VALUE is the mask of enabled channels expressed as a hex number where each bit corresponds to a channel index and 1 is set for each enabled channel. VALUE ranges from 0x1 to 0xFFFFFFFFFFFFFFFF for VME.

For example, if only channel 0 is enabled, VALUE = 0x1, if the first 8 channels are enabled (ch0 to ch7), VALUE = 0xFF. To enable all the 64 channels, write VALUE = 0xFFFFFFFFFFFFFFFF

ENABLE_INPUT 0x1 → Channel 0 is enabled for the acquisition

ENABLE_INPUT 0xFFFFFFFF → The first 32 channels are enabled for the acquisition

10.4.5 Gate

The Gate is the same for all channels and can be set in a range from 16 nanoseconds to 16 milliseconds. The Gate parameter value is expressed in microseconds.

GATE_WIDTH (0/16 msec)

- *GATE_WIDTH = 0* → the board accepts an acquisition gate signal from the GATE connector
- *GATE_WIDTH > 0* → the board opens an acquisition gate of width GATE_WIDTH when a Gate edge is detected on GATE connector

For example:

GATE_WIDTH 16 → corresponds to a Gate width equal to 16 microseconds.

Note: The programmable time for the gate width must be less than 16 ms .

The signal type of the front panel I/O LEMO connectors can be set as NIM or TTL, via the command line:

FPIO_LEVEL(NIM/TTL)

FPIO_LEVEL TTL → corresponds to TTL signal selection.

10.4.6 Sliding Scale

The sliding scale parameter allows to enable/disable the corresponding algorithm (see Sect. **8.2.2**). If it is enabled, the ADC scale is limited to 4096-256 counts and the calibration value (loaded in the SRAM) is subtracted to the sample value. If it is not enabled, the calibration subtraction is not performed.

SLIDING SCALE(YES/NO)

SLSCALE_ENABLE YES → enables the sliding scale algorithm.

Note: It is recommended to leave the sliding scale **ENABLED**.

10.4.7 Data Plot

The number of channels of the spectrum is selectable by the command line:

SPECTRUM_CHANNEL (1k, 2k, 4k, 8k, 16k)

For example:

SPECTRUM_CHANNEL 4k → generates spectra with 4k channels.

Note: When the input range is 4V, the SPECTRUM_CHANNEL value equal to 16k is not allowed.

The channels plotting can be enabled via the command line:

ENABLE_GRAPH(CHANNEL_MASK)

Where CHANNEL_MASK corresponds to the mask of enabled channels of each group to be plotted. CHANNEL_MASK ranges from 0x1 to 0xFF (from channel 0 to all channels enabled). During the acquisition, the plotted channels for the plotted group can be enabled/disabled by pressing the 0-7 keys:

ENABLE_GRAPH 0x1 → Channel 0 is enabled for plotting

A similar command is available for the groups, where each group is made of 8 consecutive channels.

GROUP_GRAPH (GROUP_INDEX)

Where GROUP_INDEX ranges from 0 to 7. During the acquisition, the group index can be incremented/decremented by pressing the 8(-) and 9(+) keys.

GROUP_GRAPH 0 → The first group is enabled for plotting

10.4.8 Zero Suppression

The zero suppression allows the user to reduce the amount of data transferred from the board by transferring only those events with pulse height higher than the zero-suppression threshold. When it is enabled, the user can select a threshold value for each group of eight channels. The same value is then applied to all channels of the same group.

ZS_ENABLE(YES/NO)

ZS_THRESHOLD (0-Spectrum N channels)

For example, if the zero suppression is enabled, with thresholds given by the ZS_THRESHOLD group parameter, the configuration file could be:

ZS_ENABLE YES

[GROUP 0]
ZS_THRESHOLD 50
[GROUP 1]
ZS_THRESHOLD 40
[GROUP 2]
ZS_THRESHOLD 50

11 Software Tools

CAEN provides additional tools to interface the 741 Peak Sensing family, which are available for free download at the "Software" section on CAEN website.

11.1 CAEN Upgrader

CAEN Upgrader is a free software composed of command line tools together with a Java Graphical User Interface.

CAEN Upgrader, for the V1741, allows in few easy steps to:

- Upload different FPGA firmware versions on the board
- Read the firmware release of the board and the bridge (when included in the communication chain)
- Upgrade the internal PLL
- Get the Board Info file, useful in case of support

CAEN Upgrader can operate with Windows and Linux, 32 and 64-bit OSs.

The software relies on the CAENComm and CAENVMELib libraries (see Chap**. 9**) and requires third-party Java™ SE 8 update 40 (or later) to be installed.

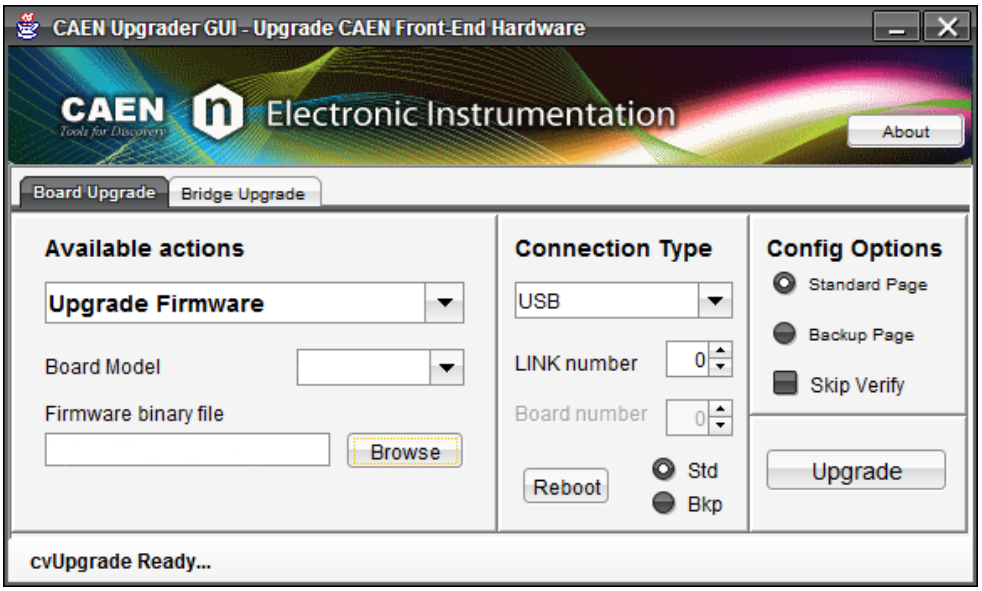


Figure 11.1: CAEN Upgrader Graphical User Interface

CAEN Upgrader installation package can be downloaded on CAEN web site in the "Configuration Tools" section (**login required**).

CAEN provides a guide to the software features and usage **[RD2]**, free downloadable at the same section above.

Note: CAEN Upgrader is available for Windows® platforms (32 and 64-bit) as stand-alone version (all the required CAEN libraries are installed locally with the program). Only the drivers for the specific communication link must be installed apart by the user. The CAEN Upgrader version for Linux® platform is not stand-alone, so it needs the required libraries to be installed apart by the user.

11.2 CAENComm Demo

CAENComm Demo is a simple program developed in C/C++ source code and provided both with Java™ and LabVIEW™ GUI interface. The demo mainly allows for a full board configuration at low level by direct read/write access to the registers and may be used as a debug instrument.

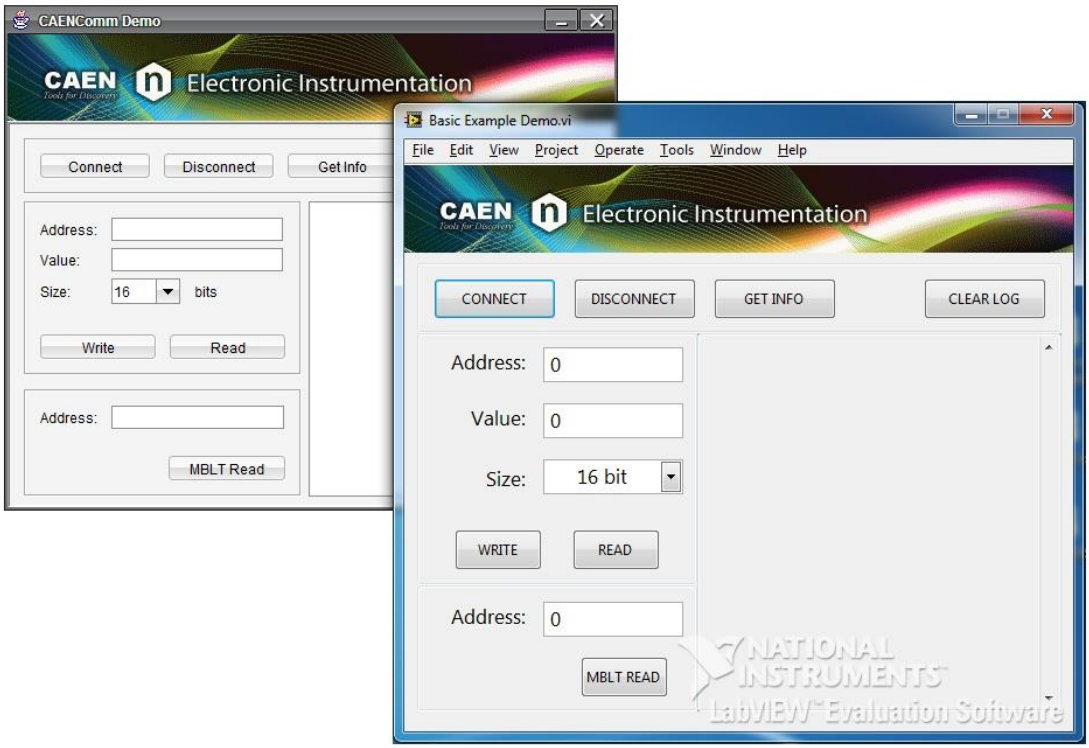


Figure 11.2: CAENComm Demo Java and LabVIEW graphical interface

The Demo is included in the CAENComm library installation Windows package, which can be downloaded on CAEN web site in the ”Software Libraries” section (**login required**).

CAEN provides the Demo description in the CAENComm library User Manual **[RD3]**, free downloadable at the section above.

Note: CAENComm Demo is available for Windows® platforms (32 and 64-bit) and requires CAENComm and CAENVMELib as additional software to be installed by the user (see Chap. **9**).

12 HW Installation

- The V1741 fits into 6U VME crates
- Turn the crate OFF before board insertion/removal
- Remove all cables connected to the front panel before board insertion/removal

CAUTION: this product needs proper cooling:

USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEATING THE BOARD MAY DEGRADE ITS PERFORMANCES!

V1741 CANNOT BE OPERATED WITH CAEN CRATES VME8001/8002/8004!

CAUTION: this product needs proper handling.

V1741 DO NOT SUPPORT LIVE INSERTION (HOT SWAP)! REMOVE OR INSERT THE BOARD WHEN THE VME CRATE IS POWERED OFF!

ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE!

12.1 Power-on Sequence

To power on the board, perform the following steps:

1. Insert the V1741 into the crate;
2. Power up the crate.

12.2 Power-on Status

At power-on the module is in the following status:

- The Output Buffer is cleared;
- Registers are set to their default configuration.

After powering on, only the NIM and PLL LOCK LEDs must stay ON (see **Figure 12.1**).

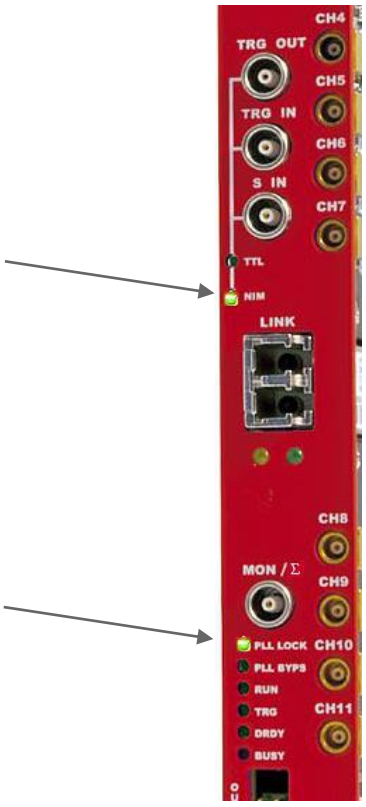


Figure 12.1: Front panel LEDs status at power-on

13 Firmware and Upgrades

The board hosts one FPGA on the mainboard and two FPGAs per mezzanine (i.e. one FPGA per 16 channels). The channel FPGAs firmware is identical. A unique file is provided that will update all the FPGAs at the same time.

ROC FPGA MAINBOARD FPGA (Readout Controller + VME interface):

FPGA Altera Cyclone EP1C20.

AMC FPGA MEZZANINE FPGA (ADC readout/Memory Controller):

FPGA Altera Cyclone EP3C40

The firmware is stored onto the on-board FLASH memory. Two copies of the firmware are stored in two different pages of the FLASH, referred to as Standard (STD) and Backup (BKP). At power-on, a micro-controller reads the FLASH memory and programs the module automatically loading the first working firmware copy, that is the STD one in normal operating.

The on-board dedicated SW7 dip switch, set on STD position by default, allows to select the first FLASH page to be read at power-on (see Sect**. 7.2**).

It is possible to upgrade the board firmware via VMEbus or Optical Link by writing the FLASH with the CAEN Upgrader software (see Chap. **10**).

IT IS STRONGLY SUGGESTED TO OPERATE THE BOARD UPON THE STD COPY OF THE FIRMWARE. UPGRADES ARE SO RECOMMENDED ONLY ON THE STD PAGE OF THE FLASH. THE BKP COPY IS TO BE INTENDED ONLY FOR RECOVERY USAGE. IF BOTH PAGES RESULT CORRUPTED, THE USER WILL NO LONGER BE ABLE TO UPLOAD THE FIRMWARE VIA VMEbus OR OPTICAL LINK AGAIN AND THE BOARD NEEDS TO BE SENT TO CAEN IN REPAIR!

13.1 Firmware Updates

The V1741 is delivered running the Peak Sensing firmware.

The firmware updates are available for free download at the V1741 Downloads page on CAEN website (**login required**).

13.2 Firmware File Description

The programming file has the CFA extension (CAEN Firmware Archive). It is an archiving file format that aggregates all the programming files of the same firmware kind which are compatible with the same board family.

The CFA naming convention follows this general scheme:

- x<FAMILY>_rev_X.Y_W.Z.CFA

where x<FAMILY> are all the supported boards (the x741 includes DT5741, N6741 and V1741), X.Y is the major/minor revision number of the mainboard FPGA, and W.Z is the major/minor revision number of the channel FPGA.

13.3 Troubleshooting

In case of upgrade failure (e.g. STD FLASH page is corrupted), the user can try to reboot the board: after a power cycle, the system programs the board automatically from the alternative FLASH page (e.g. BKP FLASH page), if this is not corrupted as well. The user can so perform a further upgrade attempt on the corrupted page to restore the firmware copy.

BECAUSE OF AN UPGRADE FAILURE, THE SW7 DIP SWITCH POSITION MAY NOT CORRESPOND TO THE FLASH PAGE FIRMWARE COPY LOADED ON THE BOARD FPGAs.

When a failure occurs during the upgrade of the STD page of the FLASH, which compromises the communication with the V1741, the user can perform the following recovering procedure as first attempt:

- force the board to reboot loading the copy of the firmware stored on the BKP page of the FLASH. To do that, power off the crate, switch the dedicated SW1 switch to BKP position and power on the crate;
- use CAEN Upgrader to read the firmware revision (in this case the one of the BKP copy). If this succeeds, it is so possible to communicate again with the board;
- use CAEN Upgrader to load the proper firmware file on the STD page, then power off the crate, switch SW1 back to STD position and power on the crate.

If neither of the procedures here described succeeds, it is recommended to send the board back to CAEN in repair (see Chap. **17**).

14 Instructions for Cleaning

The equipment may be cleaned with isopropyl alcohol or deionized water and air dried. Clean the exterior of the product only.
Do not apply cleaner directly to the items or allow liquids to enter or spill on the product.

14.1 Cleaning the Touchscreen

To clean the touchscreen (if present), wipe the screen with a towelette designed for cleaning monitors or with a clean cloth moistened with water.
Do not use sprays or aerosols directly on the screen; the liquid may seep into the housing and damage a component. Never use solvents or flammable liquids on the screen.

14.2 Cleaning the Air Vents

It is recommended to occasionally clean the air vents (if present) on all vented sides of the board. Lint, dust, and other foreign matter can block the vents and limit the airflow. Be sure to unplug the board before cleaning the air vents and follow the general cleaning safety precautions.

14.3 General Cleaning Safety Precautions

CAEN recommends cleaning the device using the following precautions:

1) Never use solvents or flammable solutions to clean the board.
2) Never immerse any parts in water or cleaning solutions; apply any liquids to a clean cloth and then use the cloth on the component.
3) Always unplug the board when cleaning with liquids or damp cloths.
4) Always unplug the board before cleaning the air vents.
5) Wear safety glasses equipped with side shields when cleaning the board.

15 Device Decommissioning

After its intended service, it is recommended to perform the following actions:

- Detach all the signal/input/output cable.
- Wrap the device in its protective packaging.
- Insert the device in its packaging (if present).

THE DEVICE SHALL BE STORED ONLY AT THE ENVIRONMENT CONDITIONS SPECIFIED IN THE MANUAL, OTHERWISE PERFORMANCES AND SAFETY WILL NOT BE GUARANTEED

16 Disposal

The disposal of the equipment must be managed in accordance with Directive 2012/19 / EU on waste electrical and electronic equipment (WEEE).

The crossed bin symbol indicates that the device shall not be disposed with regular residual waste.

17 Technical Support

To contact CAEN specialists for requests on the software, hardware, and board return and repair, it is necessary a MyCAEN+ account on www.caen.it:

https://www.caen.it/support-services/getting-started-with-mycaen-portal/

All the instructions for use the Support platform are in the document:

A paper copy of the document is delivered with CAEN boards.

The document is downloadable for free in PDF digital format at:

https://www.caen.it/safety-information-product-support

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