Rev. 06 - 06/12/2016

FW1495SC

V1495 FPGA Scaler User Manual

CAEN
Tools for Discovery

User Manual
UM5792

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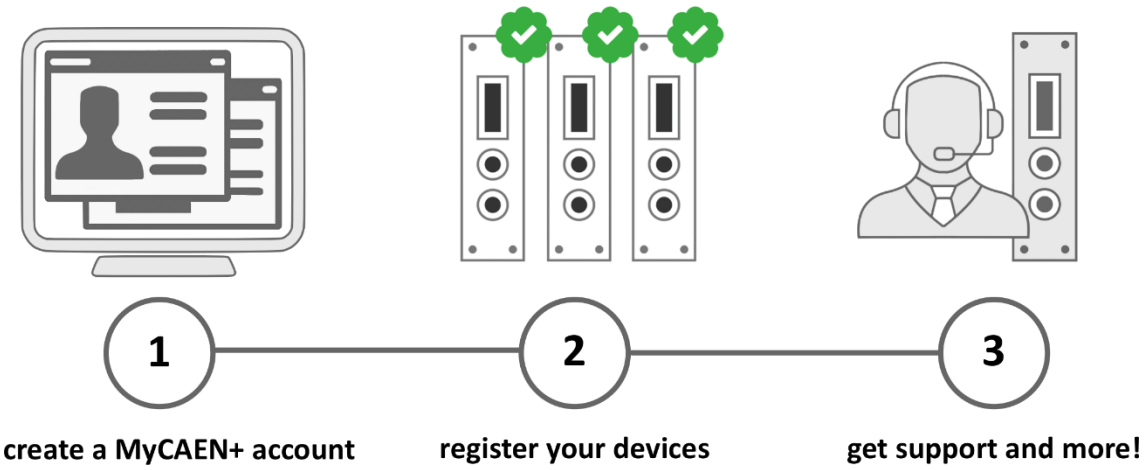

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Technical Information Manual

Revision n. 6

December 6th, 2016

MOD. FW1495SC

V1495 FPGA SCALER FIRMWARE

NPO:
00117/09:FWSCL.MUTx/06

Purpose of this Manual

This document contains the description of the FW1495SC Scaler Firmware and Software for V1495 board. Please, refer to the board user manual for full details about the hardware (**[RD1]**).

Change Document Record

Date	Revision	Changes
n.a.	00-04	Internal use
June 14th, 2012	05	Updated § **2**. Added CAENUpgrader software tool references.
December 6th, 2016	06	Updated § **4**, § **4.1**, § **4.2**, § **4.3**.

Reference Documents

[RD1] UM5175 – V1495 User Manual

[RD2] GD2512 – CAENUpgrader QuickStart Guide

All documents can be downloaded at: http://www.caen.it/csite/LibrarySearch.jsp

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1 Functional Description

FW1495SC is a FPGA firmware for CAEN V1495 model that allows to use the Mod. V1495 as a Multievent latching scaler housing up to 128 independent counting channels. Each channel has 32 bit counting depth and accepts LVDS/ECL/PECL differential inputs; the maximum input frequency is 250 MHz. The standard version of the board houses 64 input channels on two P50E-068-P1-SR1-TG connectors; in order to implement 96 or 128 channels it is necessary to plug the Mod. A395A expansion boards into the D and/or E slot. A Multievent latching Scaler with NIM/TTL input signals is achievable using the Mod. A395D expansion boards (8 NIM/TTL input channels on each A395D).

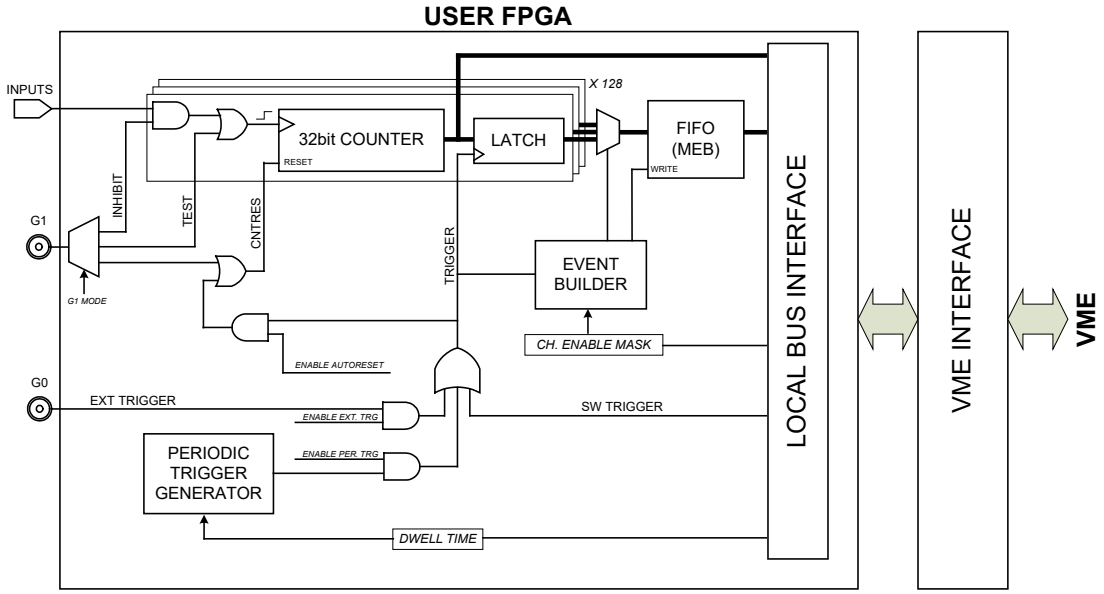


Fig. 1.1: Block Diagram

Each channel counts on the input signals leading edge; as a trigger arrives, all counters are latched simultaneously.

This operation takes place independently from the counting that can continue unaffected; thanks to synchronization technique the readout value is always significant, even if the counter changes its value when is readout.

After the trigger has arrived and the latch are loaded, the FPGA reads the latches and writes the enabled channels values into the FIFO memory (Multi Event Buffer) with a Header and an optional Trigger Time Tag, thus making an Event, that can be readout via VME.

Once the event is written, the Scaler can accept another trigger even if the previous event is not readout yet, as long as the FIFO memory has enough space left for other data.

The trigger signal can be either fed to the G0 connector (NIM or TTL) or internally generated by the FPGA, with a certain trigger period (DWELL TIME), from 1µs to 4000 s with 1 µs step.

The trigger can also be sent via VME, by a write access to a certain register.

The counters value can be also read via VME on the fly, independently from the counting, the trigger and the relevant event recording.

The G1 connector can be used in three ways:

- counting inhibit
- test signal in order to allow all channels counting in parallel
- counters reset

The counters reset can be also asserted every time the trigger is sent (auto-reset option); in this way, the read values represent the counting value between two triggers instead of the absolute counting value from the beginning. The counters can also be reset via VME command (see § 3.1).

2 Getting started

To upgrade the V1495 with FW1495SC via VME, it is necessary to use the CAENUpgrader software tool available at www.caen.it (both software and documentation for installation and use are downloadable from the CAENUpgrader home page), then follow these steps:

- Go to www.caen.it
- Browse the **FW1495SC** home page on CAEN web site.
- Click on the Download thumbnail.
- Download the **V1495 multievent latching scaler firmware** package.
- Unzip the downloaded package.
- Launch the CAENUpgrader GUI.
- Select the "Upgrade Firmware" function, check the USER FPGA option, set the proper communication parameters and upgrade the USER FPGA device with the **v1495scaler_rev_xxx.x.rbf** file contained in the downloaded package.

The www.caen.it website provides the free downloadable **FW1495SC Trial version:**

- The User can download the Trial Version for evaluation.
- The trial version is fully functional but with a DAQ time frame limitation: every 30 min the user must restart (power off/power on) the board.
- After evaluation, to remove the time limitation, the user must purchase a License and register it.
- The licensing and unlocking procedure is described in the CAENUpgrader Quick Start Guide (**[RD2]**) and requires a first step to be completed via www.caen.it web site, then the CAENUpgrader tool must be used to unlock the firmware on the board.

IMPORTANT

For V1495 with PCB revision < 2, FW1495SC firmware works only with time frame limitation (the firmware licensing is not supported).

For V1495 with PCB revision >= 2, FW1495SC firmware licensing is possible only on V1495 boards running VME FPGA firmware rel. 1.0 and higher.

The PCB revision can be read by the following modes:

- from the Configuration ROM (see **[RD1]**);
- from the silkscreen on the mainboard bottom side (BV14950516AA Rev. 0 is an example of PCB revision number 0).

- In case the V1495 board is ordered together with the FW1495SC, the user will be delivered with the board already equipped with a licensed scaler firmware.

3 Registers and VME interface

All the module's registers can be accessed via D32 VME mode, with either A32 or A24 address in any mode (USER/SUPERVISOR, DATA/PROGRAM, CR/CSR, etc…). The data space (MEB) readout can be done either via D32 single cycle or via Block Transfer (32bit BLT). The following table reports the FPGA USER address offsets, to be added to the module's base address; the FPGA VME address offsets are the same as reported in the V1495 User's Manual.

Register	*Address*	*Type*	*Description*
MEB	0x0000 (*)	R	Multi Event Buffer
ACQ_CTRL	0x1000	R/W	Control Register
ACQ_CTRL_SET	0x1004	R/W	Control Register BitSet
ACQ_CTRL_CLR	0x1008	R/W	Control Register BitClear
FWREV	0x100C	R	Firmware Revision
STATUS	0x1010	R	Status Register
COMMANDS	0x1014	W	Commands Register
CHEN_A	0x1020	R/W	Channel Enable Mask for the group A
CHEN_B	0x1024	R/W	Channel Enable Mask for the group B
CHEN_D	0x1028	R/W	Channel Enable Mask for the group D
CHEN_E	0x102C	R/W	Channel Enable Mask for the group E
DWELL_TIME	0x1030	R/W	Dwell Time (period of the internal trigger)
COUNTERS_A	0x1100 – 0x117C	R	Direct read access to the counters of the group A
COUNTERS_B	0x1180 – 0x11FC	R	Direct read access to the counters of the group B
COUNTERS_D	0x1200 – 0x127C	R	Direct read access to the counters of the group D
COUNTERS_E	0x1280 – 0x12FC	R	Direct read access to the counters of the group E

(*) any address between 0x0000 and 0xFFFC is mapped onto the MEB.

Tab. 3.1: Register Map

3.1 Register Description

ACQ_CTRL

address 0x1000, 0x1004, 0x1008, R/W

There are three ways to access this register; by writing to address

0x1000: the value is directly written to the register

0x1004: bits written to 1 are set; bits written to 0 remain unchanged

0x1008: bits written to 1 are reset; bits written to 0 remain unchanged

bit	name	description
[0]	EN_EXTTRG	0 => External Trigger Disabled, 1 => External Trigger Enabled
[1]	EN_INTTRG	0 => Internal Trigger Disabled, 1 => Internal Trigger Enabled
[2]	G_PORT_TYPE	1 => G and A395D (if present) ports are TTL, 0 => G and A395D (if present) ports are NIM
[3]	AUTO_RESET	0 => AutoReset Disabled, 1 => the counters are reset with the trigger
[5:4]	G1_MODE	[00] => G1 is used as INHIBIT [01] => G1 is used to reset the counters [10] => G1 is used as TEST SIGNAL [11] => RESERVED
[6]	EN_TIMETAG	0 => Time Tag not reported in the event data, 1 => Time Tag reported in the event data

FWREV

address 0x100C, R only

This read-only register reports the FPGA USER firmware revision with the following format (32bit):

YMDDMMmm (each letter corresponds to one nibble)

Y = year (9 stands for 2009)

M = month (1 =JAN, C = DEC)

DD = day (decimal: '12' stands for, not for 18)

MM = major number = 0x80 (128 decimal, code corresponding to Scaler)

mm = minor number (example: if mm = 2, version is 128.2)

STATUS

address 0x1010, R only

bit	name	description
[0]	MEB FULL	when 1, the MEB is full and no more trigger can be accepted until the MEB is read and there is enough space to write an event

COMMANDS

address 0x1014, W only

A write access to this register allows the FPGA to execute one or more command; bit must be set to one to perform the corresponding function.

bit	name	description
[0]	SWTRG	Generates a software trigger (not maskable)
[1]	SWCNTRES	Reset to 0 all counters
[2]	SWCLR	Clear MEB
[4]	BDRESET	Board reset

CHEN_X

address 0x1020, 0x1024, 0x1028, 0x102C R/W

This register allows to enable the channels of A (*0x1020)*, B (*0x1024)*, D (*0x1028)* and E (*0x102C)* connectors; each register's 32bit correspond to the relevant channel on the connector (1 = ch enabled).

DWELL_TIME

address 0x1030, R/W

This register allows to set the internal trigger period: T_{TRG} = N * 1µs

With N = register value (32 bit); to use the internal trigger, it is also necessary to enable by setting bit 1 of the Control Register.

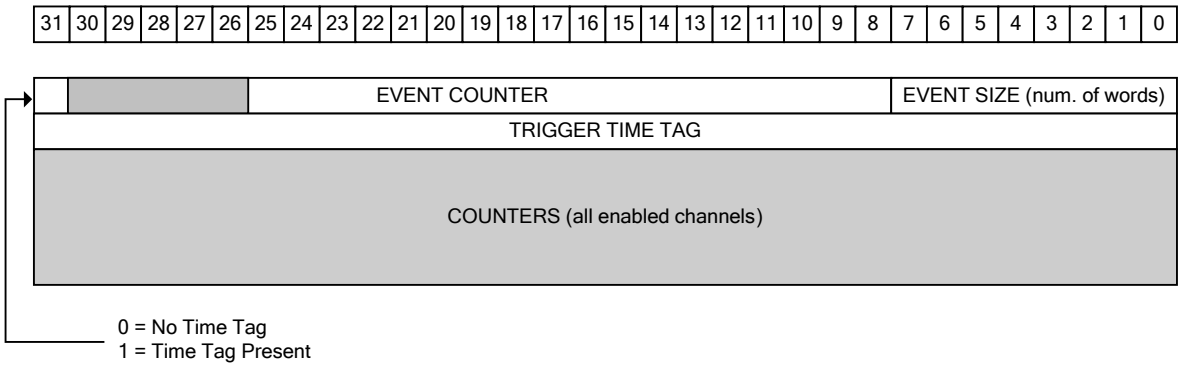
COUNTERS_X

address from 0x1100 to 0x12FC, R only

A read access to one of these addresses allows to read "on the fly" the value of the corresponding counter. The address of channel N is given by 0x1100 + N * 4.

3.2 Event Data Format

One event's data are organized as shown by the following figure:



The Trigger Time Tag is optional (bit 6 of control register); if enabled, it represents the arrival time of the trigger (µs) from the latest board reset. Counters value are in sequential order.

Bit 31 allows to either have (1) or have not (0), the Trigger Time Tag written.

4 V2495scaler_daq Demo

The **V2495scaler_daq software**, which is a demo application developed to manage data acquisition with FW2495SC, can also be used with the V1495 board when equipped with FW1495SC.

The source code is included as a guide for applications developed by the Users.

System requirements:

- CAENComm library rel. 1.02 or later (locally installed by the program itself)
- Microsoft Windows 7/8/8.1/10
- GNUplot 4.2 (www.gnuplot.org)

4.1 V2495scaler_daq Installation

To install the V2495scaler_daq demo application:

- Go to www.caen.it and browse the **FW1495SC** home page
- Make sure that the procedure described in § **2** is completed
- Click on the *Download* thumbnail
- Download the package **V2495Scaler_daq** installation package
- Decompress, run the installer file and complete the installation wizard
- By default, the destination path is: *C:\Program Files (x86)\CAEN\VME*

4.2 V1495 Connection

The V2495scaler_daq demo program requires a CAEN VME Bridge (V1718/V2718).

To run the program, optionally:

- Double-click on the *V2495scaler_daq.exe* file in the bin subfolder (see § **4.3**)
- From the DOS shell, type *"V2495scaler_daq.exe V2495scaler_Config.txt"*

OFFLINE MODE

When connected to a V1495 with FW1495SC firmware, the V2495scaler_daq demo doesn't support the Offline Mode.

4.3 Demo Getting Started

Go to the destination folder and open the **bin** subfolder:

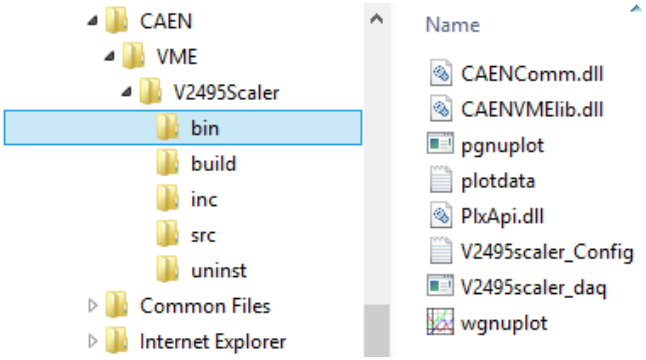


Fig. 4.1: V2495scaler_daq destination folder

Set the **V2495scaler_Config** text file according to your purpose.

V2495scaler_Config FILE

The description is intended to clarify which demo software settings can be used with a V1495 board running FW1495SC firmware.

Base Address

```
# ------------------------------------------------------------------------
# Base Address of the V2495 (hex 32 bit)
# ------------------------------------------------------------------------
BaseAddress      32100000
```

First, the VME Base Address (BA) must be set to connect the V1495 board. It is a hexadecimal 8-digit value (32 bits), where the upper 4 digits are given by the status of the 4 on-board rotary switches (see the V1495 User Manual **[RD1]**). The lower 4 digits (BA offset) are 0000.

Channel Enable Mask

```
# ------------------------------------------------------------------------
ChEnableA        ffffffff
ChEnableB        ffffffff
ChEnableD        00000000
ChEnableE        00000000
ChEnableF        00000000
```

IMPORTANT

The F connector is meaningless in case of V1495 board, and the relevant mask must be set to 0.

ChEnableX hexadecimal value represents the 32-bit mask to enable the presence of the channels counters of the X connector (X = A, B, D, E) inside the data packet. The bit position in the mask corresponds to the channel number (e.g. 0x0000A000 means channel 15 and channel 13 are enabled).

If the mezzanine type plugged in the V1495 connector features less than 32 channels (e.g. the 8-channel A395D), the unsupported channels will be masked.

Counter Autoreset

```
# ------------------------------------------------------------------------
# Counter autoreset (0=disabled, 1=enabled)
# ------------------------------------------------------------------------
AutoReset        0
```

This flag allows to enable the autoreset option. The counter will be reset at each trigger arrival, so that each counter reading represents the counting between two consecutive triggers.

Trigger Mode

```
# ------------------------------------------------------------------------------
# Trigger Source
# 0 = SW only
# 1 = External + SW
# 2 = Internal + SW
# 3 = External + Internal + SW
# ------------------------------------------------------------------------------
TriggerMode      1
```

This parameter selects the source or combination (OR) of sources providing the trigger for the acquisition.

Dwell Time

```
# ------------------------------------------------------------------------------
# Dwell Time (period of the internal trigger) in usec
# ------------------------------------------------------------------------------
DwellTime        100000
```

If the internal trigger source is selected through the *TriggerMode* parameter, this setting programs the period of the internal trigger (in units of µs).

Event Settings

```
# Save time tag in the event data (0=disabled, 1=enabled)
# Ch_Mask, TimeTag_64 and CVcounter_64 are meaningful only when V2495_Payload is set to 1
# ------------------------------------------------------------------------------
TimeTag          1
Ch_Mask          1
TimeTag_64       0
Counter_64       0
V2495_Payload    1
```

This is a set of information regarding the event format.

- *V2495_Payload* configures the legacy, V1495 compliant event format (value = 0) or the V2495 new event format (value = 1).

> **IMPORTANT**
>
> When connected to a V1495 board with FW1495SC firmware, whatever the *V2495_Payload* value, the software configures the V1495 compliant event format.

- *TimeTag* = 1 makes the time tag information to be added to the event structure.
- *Ch_Mask*, *TimeTag_64, Counter_64*:

> **IMPORTANT**
>
> *Ch_Mask, TimeTag_64* and *Counter_64* are meaningless in case of V1495.

Input Port G1

```
# ------------------------------------------------------------------------------
# Input Port G1:
# 0 = inhibit
# 1 = counter reset
# 2 = test
# ------------------------------------------------------------------------------
G1Mode          0
```

G1Mode parameter must be used to set the function of the G1 front panel port.

G Ports Type

```
# ------------------------------------------------------------------------------
# G Ports type:
# 0 = NIM
# 1 = TTL
# ------------------------------------------------------------------------------
GPortType       0
```

GportType sets the electrical level of G0 and G1 front panel ports: NIM or TTL.

Readout Settings

```
# ------------------------------------------------------------------------
# Readout Options
# ReadoutMode:   0 = Poll event size and read one event in block mode;
#                1 = Read a chunk of data (256KB). Block transfer is terminated
#                    prematurely if data queue empties.
# ------------------------------------------------------------------------
ReadoutMode     0
```

This sections allows to manage the readout mode. In the polling mode (*ReadoutMode* = 0), if an event is present, the program reads out the event size and then reads out the whole event in a single block transfer. Otherwise (*ReadutMode* = 1), the program reads out a block of fixed size (256 KB); if the data (e.g. events) size is lower than the block size, a Bus Error is returned after the event data only.

IMPORTANT

Readout options are implemented starting form VME FPGA firmware **revision 1.6**.

Output file Saving

```
# ------------------------------------------------------------------------------
# Enable saving to output File. The file can be chosen at runtime
# ------------------------------------------------------------------------------
SaveToFile      0
```

Setting the *SaveToFile* parameter to 1 before to run the program, enables the output stream from the V1495 to be saved in binary format. The user will be asked to enter the file name at runtime.

IMPORTANT

Due to the lack of information on the enabled channel mask, when connected to a V1495 board equipped with FW1495SC firmware, the saved files cannot be analyzed offline by the V2495scaler_daq demo. The user can anyway process the files developing a customized code.

Test Clock

```
# Enable 50 MHz clock output on port C (all channels, can be used to test counters)
TestClock       1
```

IMPORTANT

The Test Clock feature is not supported by the V1495 equipped with FW1495SC firmware.

Plot Options

```
# ------------------------------------------------------------------------
# Plot Options
# OpenPlot:   0 = plot disabled;   1 = plot enabled
# PlotChan: channel to be plotted in the count vs time graph
# PlotPoints: number of points on the X axis of the plot
# RefreshTime: Seconds between two counter consecutive counter reading in loop mode
# ReadingTime: Seconds between two consecutive counter printouts
# PrintCounters: activate the on-screen counter display after each VME access
# ------------------------------------------------------------------------
OpenPlot        1
PlotChan        0
PlotPoints      100
RefreshTime     1
PrintCounters   1
ReadingTime     0
```

In this section, it is possible to enable (*OpenPlot*) the simultaneous counter histogram and Counts vs Time plot, of *PlotChan* (ranging from 0 up to 159; please remember to activate the related channel in the output stream), the maximum number of points to be collected in the Counts vs Time plot (*PlotPoints*), the time in seconds between two consecutive counter readings when the loop mode is enabled (periodic software trigger by DOS shell), the possibility to display the readout data (*PrintCounters*) in the DOS shell, nd the refresh time of the readout data being displayed (if *PrintCounters* = 1).

Demo Commands

```
Options:
[h] print instructions
[m] manual controller (read/write registers)
[p] Print Counters of active channels (no VME readout)
[t] Software trigger
[T] Software trigger (periodic)
[r] Reset Counters
[f] Analyze binary file (previously saved)
[q] quit
```

Fig. 4.2: Command set

Launching the Demo program, a set of accepted keyboard commands is shown (see **Fig. 4.2**):

- Key 'h' displays the command list
- Key 'm' enter the register read/write sub-menu; type 'w' to write or 'r' to read, followed by the register offset.
- Key 'p' prints the counters content related to the latest readout event.
- Key 't' issues a single trigger by software.
- Key 'T' issues a periodic software trigger (loop mode, whose frequency is set by the *RefreshTime* parameter in the configuration file). In loop mode, the counters are reset at each trigger period.
- Key 'r' resets the counters.
- Key 'f':

> **IMPORTANT**
>
> The 'f' command is not supported by the V1495 equipped with FW1495SC firmware.

- Key 'q' quits the program.

Example

This section shows how to perform single event reading and saving by software trigger from a V1495 board (VME Base Address 32100000) running FW1495 firmware, receiving pulses on CH0 and CH8 of the A connector.

1. Configure the V2495scaler_Config file (see **Fig. 4.3**).

```
# ******************************************************************************
# ------------------------------------------------------------------------------
# V2495 Scaler Config File
# ------------------------------------------------------------------------------
# ******************************************************************************

# ------------------------------------------------------------------------------
# Base Address of the V2495 (hex 32 bit)
# ------------------------------------------------------------------------------
BaseAddress      32100000

# ------------------------------------------------------------------------------
ChEnableA        00000101
ChEnableB        00000000
ChEnableD        00000000
ChEnableE        00000000
ChEnableF        00000000

# ------------------------------------------------------------------------------
# Counter autoreset (0=disabled, 1=enabled)
# ------------------------------------------------------------------------------
AutoReset        0

# ------------------------------------------------------------------------------
# Trigger Source
# 0 = SW only
# 1 = External + SW
# 2 = Internal + SW
# 3 = External + Internal + SW
# ------------------------------------------------------------------------------
TriggerMode      0


# ------------------------------------------------------------------------------
# Dwell Time (period of the internal trigger) in usec
# ------------------------------------------------------------------------------
DwellTime        1000000

# ------------------------------------------------------------------------------
# Save time tag in the event data (0=disabled, 1=enabled)
# Ch_Mask, TimeTag_64 and CVcounter_64 are meaningful only when V2495_Payload is set
# ------------------------------------------------------------------------------
TimeTag          1
Ch_Mask          1
TimeTag_64       0
Counter_64       0
V2495_Payload    1

# ------------------------------------------------------------------------------
# Input Port G1:
# 0 = inhibit
# 1 = counter reset
# 2 = test
# ------------------------------------------------------------------------------
G1Mode           2


# ------------------------------------------------------------------------------
# G Ports type:
# 0 = NIM
# 1 = TTL
# ------------------------------------------------------------------------------
GPortType        0


# ------------------------------------------------------------------------------
# Readout Options
# UseBerr:       0 = Berr disabled; 1 = Berr enabled (stop BLT after N events)
# NumEventBlock: Max. number of event to transfer during a BLT cycle
# ------------------------------------------------------------------------------
UseBerr          0
NumEventBlock    1

# ------------------------------------------------------------------------------
# Enable saving to output File. The file can be chosen at runtime
# ------------------------------------------------------------------------------
SaveToFile       1
# Enable 50 MHz clock output on port C (all channels, can be used to test counters
TestClock        0
# ------------------------------------------------------------------------------
# Plot Options
# OpenPlot:   0 = plot disabled;   1 = plot enabled
# PlotChan: channel to be plotted in the count vs time graph
# PlotPoints: number of points on the X axis of the plot
# RefreshTime: Seconds between two counter consecutive counter reading in loop mod
# ReadingTime: Seconds between two consecutive counter printouts
# PrintCounters: activate the on-screen counter display after each VME access
# ------------------------------------------------------------------------------
OpenPlot         1
PlotChan         0
PlotPoints       100
RefreshTime      1
ReadingTime      5
PrintCounters    1
```

Whatever the value, the software sets the V1495 compliant event format

Fig. 4.3: Configuration text file

2. Make sure that the requirements described at § **4** are satisfied.
3. Check the hardware cabling and make sure your setup is powered and ready.
4. Launch V2495scaler Demo from the DOS shell:

```
C:\Program Files (x86)\CAEN\VME\V2495Scaler\bin>V2495scaler_daq.exe V2495scaler_Config.txt
```

5. Type a name for the output binary file (e.g. “Test.bin”) and press Enter.

```
C:\Users\test>cd "C:\Program Files (x86)\CAEN\VME\V2495Scaler\bin"

C:\Program Files (x86)\CAEN\VME\V2495Scaler\bin>V2495scaler_daq.exe V2495scaler_Config.txt
Config file opened
please enter the binary output file name
Test.bin
```

6. The Demo connects to the V1495 retrieving the firmware release number and showing the commands menu.

```
C:\Program Files\CAEN\VME\V2495Scaler\bin>V2495scaler_daq.exe V2495scaler_Config
.txt
Config file opened
please enter the binary output file name
Test.bin
output will be copied in file Test.bin
A connection with the VME bridge has been established
Scaler firmware revision: 80.03

Daughterboard mod. A395D detected in slot D. Only the first 8 channels can be us
ed, the others will be masked
Daughterboard mod. A395A detected in slot E
Daughterboard mod. A395A detected in slot F

 Options:
 [h] print instructions
 [m] manual controller (read/write registers)
 [p] Print Counters of active channels (no VME readout)
 [t] Software trigger
 [T] Software trigger (periodic)
 [r] Reset Counters
 [f] Analyze binary file (previously saved)
 [q] quit
```

7. Type ‘t’ to issue a single software trigger. The event data will be displayed in the DOS shell and the counter histogram and Counters vs Time plots open up.

```
V1495 packet format detected
Event number: 1
Time Tag = 4EC6DDEF
                port A          port B          port D          port E
F
CH   0       43410383               *               *               *
*
CH   1              *               *               *               *
*
CH   2              *               *               *               *
*
CH   3              *               *               *               *
*
CH   4              *               *               *               *
*
CH   5              *               *               *               *
*
CH   6              *               *               *               *
*
CH   7              *               *               *               *
*
CH   8       43410383               *               *               *
*
CH   9              *               *               *               *
*
CH  10              *               *               *               *
*
CH  11              *               *               *               *
*
CH  12              *               *               *               *
*
CH  13              *               *               *               *
*
CH  14              *               *               *               *
*
CH  15              *               *               *               *
*
CH  16              *               *               *               *
*
CH  17              *               *               *               *
*
CH  18              *               *               *               *
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CH  19              *               *               *               *
*
CH  20              *               *               *               *
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CH  21              *               *               *               *
*
CH  22              *               *               *               *
*
CH  23              *               *               *               *
*
CH  24              *               *               *               *
*
CH  25              *               *               *               *
*
CH  26              *               *               *               *
*
CH  27              *               *               *               *
*
CH  28              *               *               *               *
*
CH  29              *               *               *               *
*
CH  30              *               *               *               *
*
CH  31              *               *               *               *
*
```

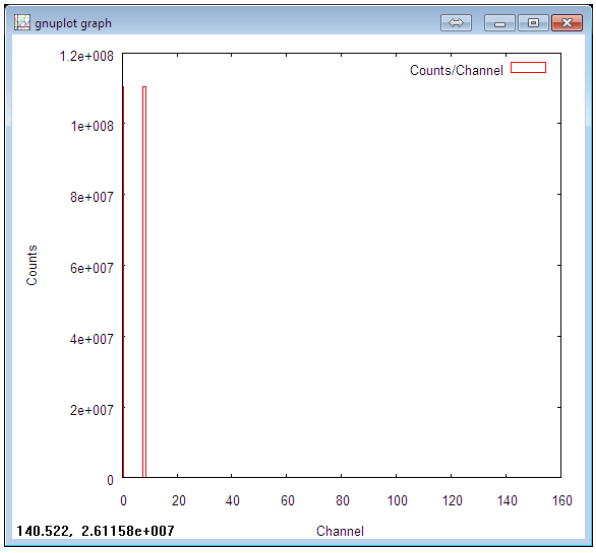

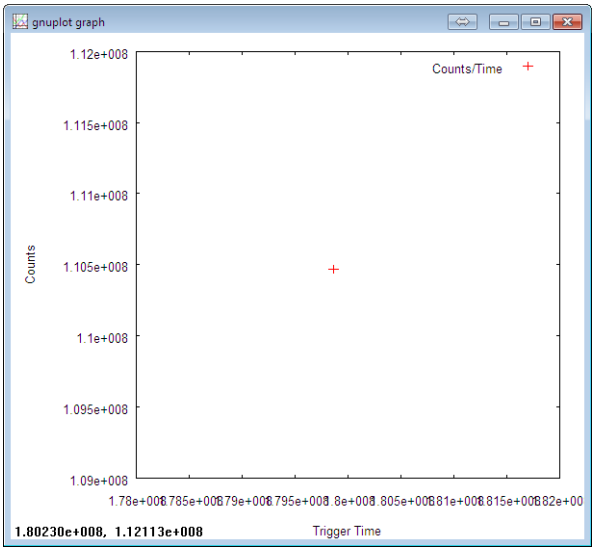

8. Type ‘q’ to quit the program; the output file will be saved in the program folder.

IMPORTANT

Due to the lack of information on the enabled channel mask, when connected to a V1495 board equipped with FW1495SC firmware, the saved files cannot be analyzed offline by the V2495scaler_daq demo. The user can anyway process the files developing a customized code.

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