Rev. 02 - 01/06/2012

SY2791

TPC Readout System

CAEN
Tools for Discovery

User Manual

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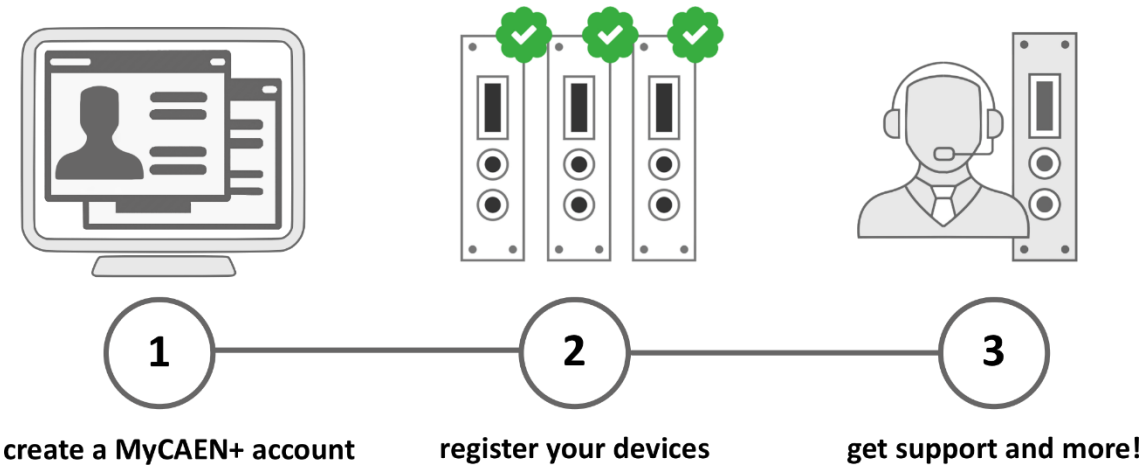

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Technical Information Manual

Revision n. 2

01 June 2012

MOD. SY2791
TPC READOUT SYSTEM
MANUAL REV.2

NPO:
00121/06:2791x.MUTx/02

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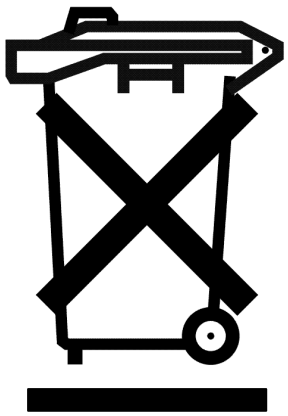

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Ordering Options

Ordering code	Model	Description
WSY2791XAAAA	SY2791	Chassis of the SY2791 (crate 4U)
WA2792XAAAAA	A2792	32ch 12Bit 2 MHz ADC mainboard for SY2791 (without preamplifiers)
WA2793XAAAAA	A2793	Power Supply for SY2791
WA2818XAAAAA	A2818	PCI Optical Link
WAY2705XAAAA	AY2705	5 m duplex patch cord with one duplex LC connector on one side and two simplex LC connectors on the other side
WAY2720XAAAA	AY2720	20 m duplex patch cord with one duplex LC connector on one side and two simplex LC connectors on the other side
WAI2705XAAAA	AI2705	5 m simplex patch cord with one simplex LC connector on both sides
WAI2720XAAAA	AI2720	20 m simplex patch cord with one simplex LC connector on both sides
WAI2703XAAAA	AI2703	30 cm simplex patch cord with one simplex LC connector on both sides

1 General Description

Fig. 1.1: SY2791 complete detector readout system

The ***SY2791*** is a complete detector readout system, ideally suited for liquid Argon TPC (Time Projection Chamber), but easily customizable for a wide variety of detectors. The system is housed in a 19" 4U crate that contains the AC/DC power supply unit ***A2793*** and eight acquisition modules ***A2792***, with 32 channels each. In total, one SY2791 can read up to 256 channels.

The analog signals coming from the detector can feed directly the inputs of the A2792s, in which the ***preamplifiers*** are arranged in arrays of plug-in hybrid circuits (2 channels each) and enclosed in a metal shielding box. This solution allows the preamplifier, which is detector and application dependent, to be re-designed or adapted to match the specific requirements. The user can chose in a list of different models provided by CAEN or develop a custom version of the preamplifier to be used on the empty motherboard of the A2792. The preamplifier outputs are digitized by 12 bit 2.5MS/s flash ADCs and processed by the internal acquisition logic, implemented in a programmable FPGA, which provides the trigger logic, the data storage in local memory buffers and the readout through a proprietary optical link, controlled by the PCI board ***A2818***.

Thanks to this compact and modular solution, the readout electronics can be positioned very close to the detector, giving the best performances in terms of noise and resolution. The optical fiber allows the system to be connected to the host PC as far as few hundred meters; the fiber guarantees easy cabling and absence of ground loops. One PCI card A2818 can control up to eight A2792s (that is one full crate) connected in daisy chain with the fibers. Typically, one PC can host four A2818s, which means 1024 channels controlled and readout from a single commercial PC.

The system has been designed for the scalability: growing from a single crate with 256 channels up to experiments with thousands of channels is made easy by the ***TT-Link***. This is a single wire bus (over a coaxial cable) connecting as many crates as needed, that distributes the same sampling clock to all the ADCs of the whole system and the same global commands, like triggers, start/stop acquisition, reset, etc. thus keeping all the acquisition boards synchronized.

From the output of the preamplifier, the system operates as a waveform digitizer: the 32 serial outputs of the ADCs are connected to one FPGA which continuously reads the digital samples and writes them, in parallel for all the channels, into an array of circular memory buffers (Multi Event Buffer). When a channel is triggered, the FPGA keeps writing the programmable number of samples that belong to the post trigger window and then saves the current buffer (i.e. an acquisition window) of that channel; such event data are completed by a header and a time tag. The acquisition can continue without dead-time in a new circular buffer. Each channel operates independently from the others and is triggered when the relevant input signal crosses a programmable digital threshold. It is possible to propagate the trigger of one channel through the TT_Link and create regions in which one channel over threshold “alerts” the other channels that can decide to lower their threshold and let a very small signal trigger the acquisition. As an alternative to the threshold crossing, a global trigger common to all the channels can be issued using software commands or an external signal.

The data throughput of the SY2791 is directly proportional to the sampling and trigger rates; in theory, it is possible to perform the acquisition of the analog signals in continuous mode. For this purpose, the system features an internal *autotrigger* whose period is such that the acquisition windows are concatenated and the waveform digitizing becomes continuous. However, the data throughput of this operating mode can exceed the maximum readout speed allowed by the bandwidth of the optical link. Algorithms for the zero suppression and/or data compression can be added to the firmware of the FPGA in order to reduce the amount of data to transfer. It is also possible to implement on-line data processing for the extraction of the energy and/or the time of the digitized pulses and drastically reduce the data throughput. For the moment, CAEN doesn’t provide firmware releases that implement such features. However, thanks to the capability of upgrading the firmware of the FPGA through the optical link (see § 4.1), new functionalities can be easily added in the future.

CAEN provides a software package that contains the drivers for the PCI board A2818, the libraries (both in C and LabView) for the access to the optical link and some demos and examples of readout programs. Windows and Linux are both supported.

1.1 Rack mounting

The ***SY2791*** is an equipment for BUILDING-IN: it must be installed in a 19” ventilated equipment rack.

2 Technical Specifications

2.1 Mechanics

The SY2791 is a modular system housed in a standard 19” 4U crate, 296 mm deep. It houses 8 acquisition units (8 TE wide each) and one power supply box (20 TE wide).

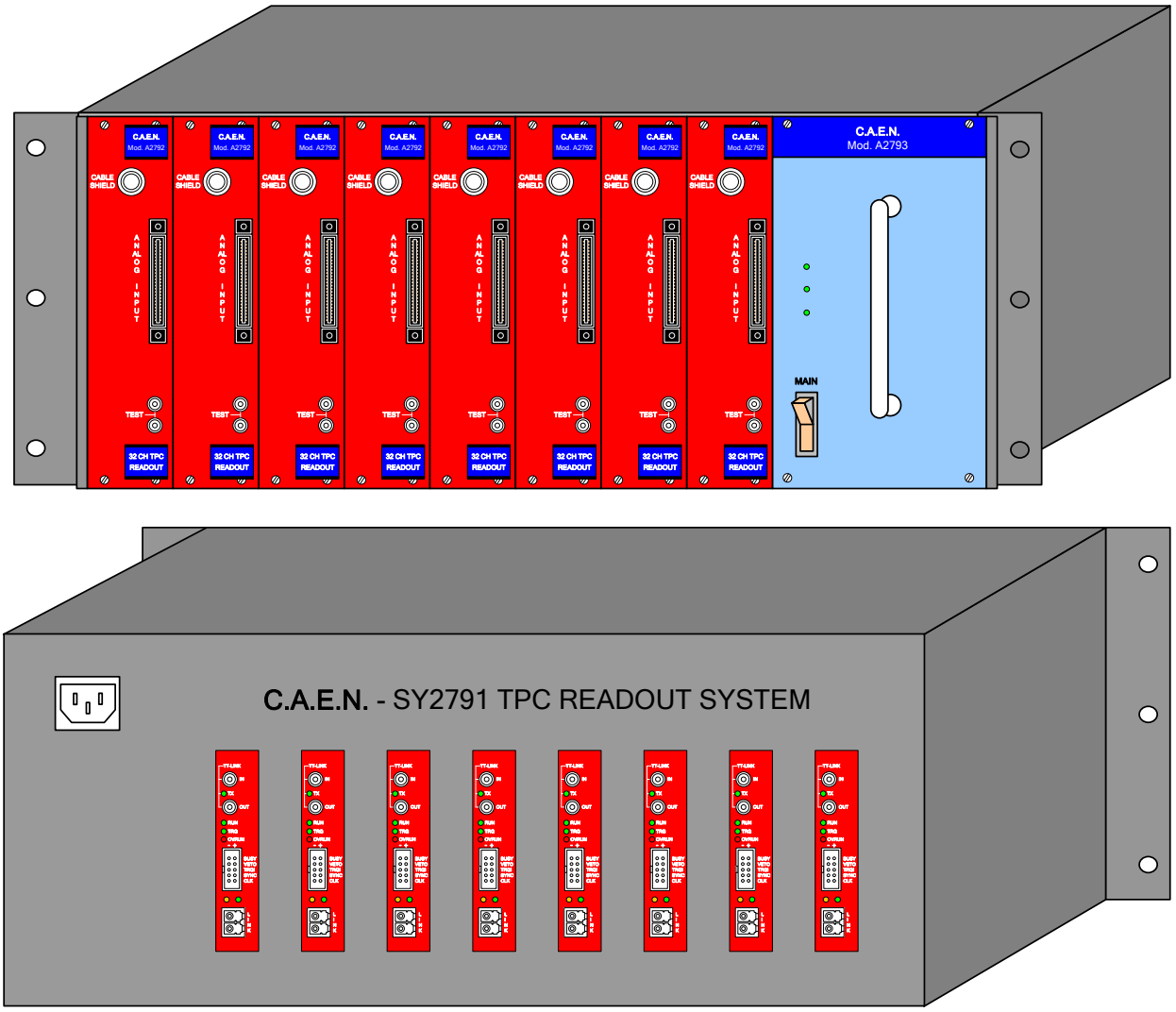

Fig. 2.1: Front and Rear views of the SY2791

The units can be inserted/extracted from the front side of the crate. The A2791 has two panels: the front panel is a standard 4U, 8 TE panel on which there are the connectors for the analog and test inputs and a banana connector for the cable shield. On the rear panel there are the digital I/Os, the LEDs and the duplex LC connector for the optical fibers. Actually, the rear panel of the A2792 is a 20x95 mm frame that appears, when the board is slid in, inside a common panel fixed to the crate, that covers the whole rear face.

The power lines, coming from the power supply unit, are distributed inside the crate through a backplane that is mounted on the internal side of the rear panel. The backplane distributes also some control signals, as the internal TT-Link, generated by the board in the slot 0 (the rightmost on the rear panel) and received by the others.

The analog parts of the board are enclosed in a metal shielding box connected to the analog ground; in order to avoid cross talk between channels, it is also possible to separate the hybrid circuits one by one by metal covers internal to the box.

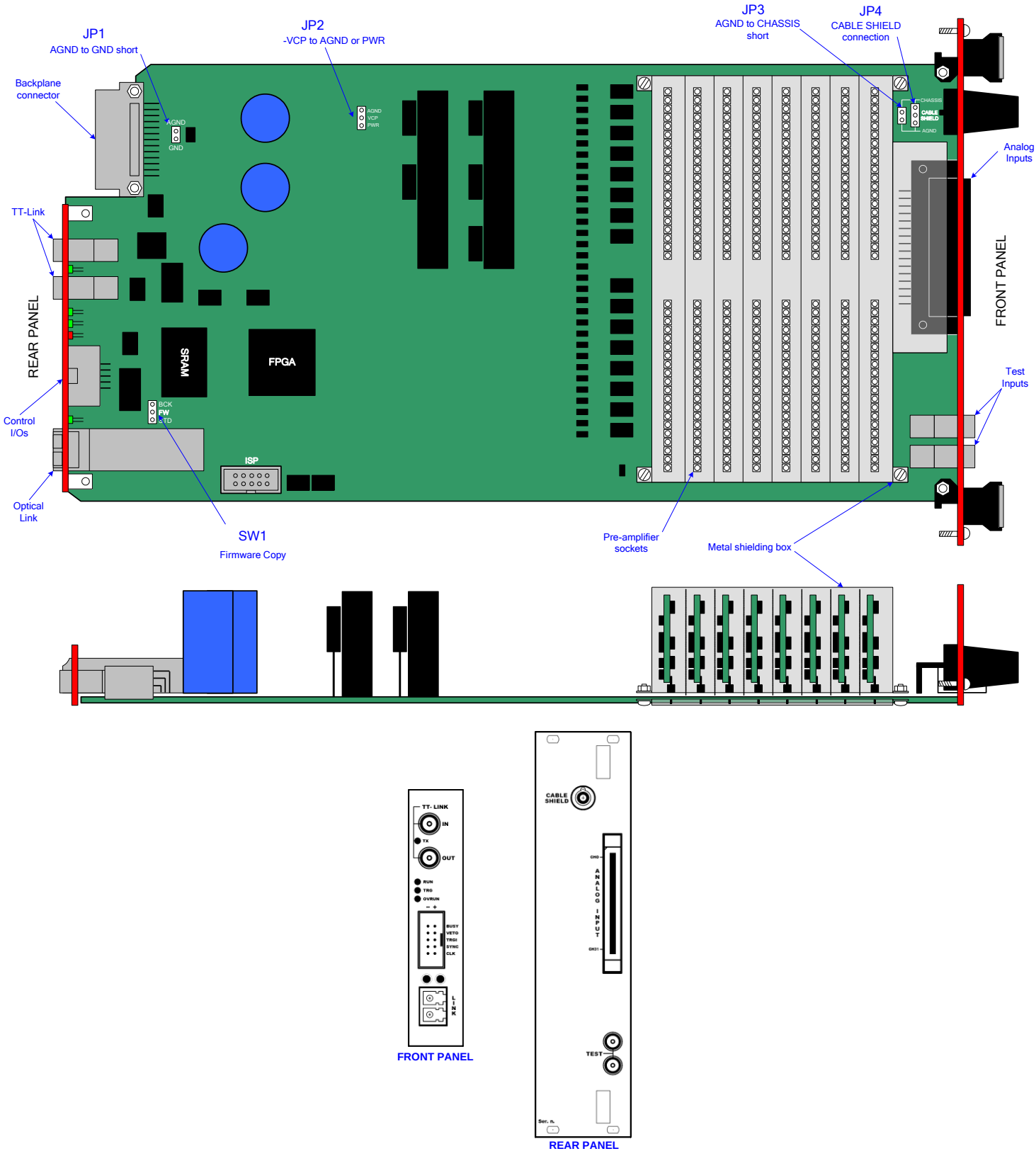

Fig. 2.2: A2792 layout and panels

2.2 Inputs and Outputs

2.2.1 Front Panel (analog section)

Analog Inputs

The signals coming from the TPC chamber enter the SY2791 through a 68 pin plug connector model ***3M*** *P50E-068P1-SR1-EA* (or equivalent) on the front panel. The pin-out of the connector (see Tab. 2.1) is such that signals and grounds are interleaved when a .025" pitch high density ribbon cables (crimped to a wiremount socket connector type ***3M*** *P25E-068S-EA* or equivalent) is used.

WARNING: using two 0.5" pitch ribbon cables crimped to a wiremount socket P50E-068S-EA (or equivalent) is possible but may cause cross talk between adjacent channels due to the incorrect distribution of the signals on the flat cables.

It is strongly recommended to use twisted pair shielded cables. The shield of the cable can be connected to the chassis of the SY2791 or to the analog ground of the A2791 through the banana connector on the front panel of the A2791.

Pin #	1	3	5	7	9	...	63	65	67
	agnd	ch0	ch1	ch2	ch3		ch30	ch31	agnd
	agnd	agnd	agnd	agnd	agnd		agnd	agnd	agnd
Pin #	2	4	6	8	10		64	66	68

Tab. 2.1: Pinout of Analog Input connector

The analog inputs directly feed the preamplifiers; therefore their electrical characteristics (coupling, dynamic range, etc…) depend on the type of the preamplifier which is used. Normally, they are terminated to 50Ω on the hybrid circuit.

External Test Input

Two bridged LEMO connectors (high impedance input) can feed the test input of the preamplifiers. In order to avoid unwanted ground connection through the test input, the signal is AC coupled with a transformer and the metal case of the LEMOs is floating. The test signal, after the transformer, is AC coupled to all the 32 analog inputs through a 1 *pF* capacitor. Sending a voltage step of $\boldsymbol{V_t}$ *mV*, either positive or negative, to the test input (when enabled) causes a charge injection $\boldsymbol{Q_t} = \boldsymbol{V_t}$ *fC* into the preamplifiers.

NOTE: the bridged LEMOs allow the test signal to be daisy chained between several modules. The line must be terminated with 50Ω plugged into one of the two LEMOs on the last module in the chain.

Cable Shield

This banana female connector is in contact with either the chassis of the SY2791 or the analog ground of the A2792. The selection is done by means of the 2-way jumper JP4 (see Fig. 2.2). It is worth noticing that the chassis and analog ground can also be shorted when the jumper JP3 is closed (see § 2.5). In this case, the two positions of the jumper JP3 are equivalent.

2.2.2 Rear Panel (digital section)

TT-Link

Input: LEMO connector, TTL or LVTTL signal, 50Ω input termination, AC coupled: the metal case of the connector is floating.
Minimum pulse width = 25 ns.

Output: LEMO connector, LVTTL signal, can drive 50Ω, DC coupled. The metal case of the connector is connected to the digital ground.

See § 3.5 for the functional description of the TT-Link.

Control I/Os

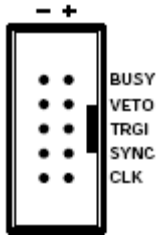

Fig. 2.3: A2792 Control I/Os

Five auxiliary control I/Os (4 inputs + 1 output) are provided mainly for test purposes. The 10 pin connector is a ***3M*** *7610-5002*. The signals are fully differential, thus no ground loop is caused by the connection of these I/Os to other boards. The inputs are terminated with 100Ω and can accept LVDS, ECL, PECL and LVPECL signals. The output is LVDS driving 100Ω. All the signals are active high. These signals are connected to the FPGA and may have the functionality described in the table below. They are not implemented in firmware versions < 2.01. With the 2.01 release, only the TRGI input is enabled to accept an external signal to trigger the board as well as to propagate it to the other boards in the crate.

NAME	Direction	Function
BUSY / TRGOUT	OUT	The busy is asserted when the module is not able to accept any new trigger because the memory buffer (of one channel or for all channels) is full. Optionally, this output can be used as a Trigger Output.
VETO	IN	When the VETO is asserted, the board doesn't accept any trigger.
TRGI	IN	Global Trigger input.
SYNC	IN	The sync signal allows the boards to be synchronized, i.e. to reset the internal counter for the time stamp.
CLK	IN	External sampling clock for the ADCs

Tab. 2.2: Control I/Os

Optical Link (CONET)

The physical layer of the *CONET* optical link is a bi-directional 1.25 Gbit/s optical transceiver. The connector is a Duplex LC. The fiber is a **Multimode 62.5/125µm** and the maximum length is about 200 m. The network topology foresees a CONET master (A2818 or A2818) and from one to eight slaves (A2792) connected in daisy chain. In case of a single A2792, a duplex crossed patch cord is used to connect the master to the slave, while for a daisy chained solution, it is necessary to have simplex patch cords connecting the output of one A2792 to the input of the next one (see Fig. 2.4). CAEN provides 5 types of patch cords, as listed in the table below.

Ordering code	Model	Length	Type of patch cord
WAY2705XAAAA	AY2705	5 m	Duplex patch cord with one duplex LC connector on one side and two simplex LC connectors on the other side
WAY2720XAAAA	AY2720	20 m	Duplex patch cord with one duplex LC connector on one side and two simplex LC connectors on the other side
WAI2705XAAAA	AI2705	5 m	Simplex patch cord with one simplex LC connector on both sides
WAI2720XAAAA	AI2720	20 m	Simplex patch cord with one simplex LC connector on both sides
WAI2703XAAAA	AI2703	10 cm	Simplex patch cord with one simplex LC connector on both sides

Tab. 2.3: Fiber optical patch cords

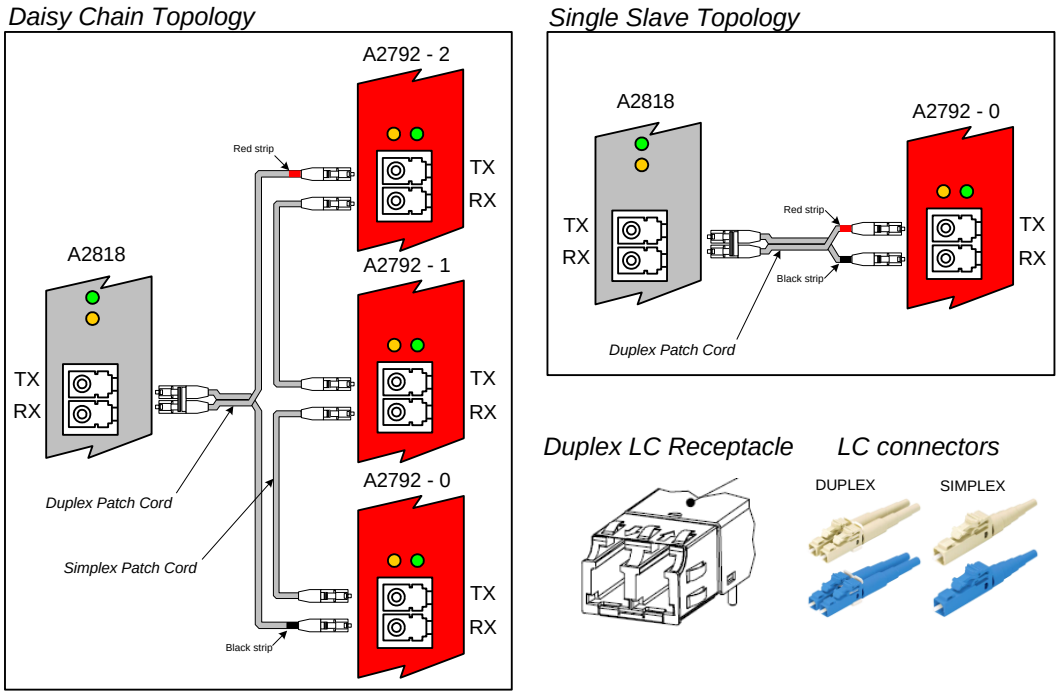

Fig. 2.4: CONET topologies and LC connectors

For the moment, the proprietary protocol implemented over the physical layer is able to transfer data up to 80MB/s. Actually, it has the potentiality to reach 125 MB/s, but this requires a new protocol development (that is a new firmware for both the A2792 and A2818) which is not in planned in the next future.

2.3 LEDs

There are 6 LEDs on the rear panel of the A2792.

NAME	Color	Function
TT-Link	Green	Steady lit when the A2792 is master of the TT-Link; blinking when the A2792 is slave and receives the TT-Link signal.
RUN	Green	Blinking when the acquisition is running. The blinking frequency is a submultiple of the sampling clock. This helps to check the synchronization of the A2792s.
TRG	Green	Lights up when a trigger is accepted.
OVRUN	Red	Lights up when a trigger is rejected because there is not a free buffer for one channel.
OL-SD	Green	Steady lit when the optical link detects the signal from the CONET.
OL-COMM	Yellow	Lights up when there is data transfer activity on the optical link.

Tab. 2.4: Rear Panel LEDs

Besides the rear panel LEDs, there is an SMD green LED, labelled CONF, in the middle of the PCB of the A2792. This LED must light up soon after the power up, thus indicating that the FPGA has been correctly configured (i.e. programmed). When the LED remains off, the firmware stored into the flash memory may be corrupted. In this case, try to move the jumper JP4 to the position BCK (backup copy of the firmware) and cycle the power. If the CONF LED is still off, contact CAEN.

2.4 Power Supply Unit

The AC line input connector, the fuse are located on the rear panel of the system; the power switch is on the front panel. The AC line can be either 230 or 110V, 50/60Hz. The unit provides three supplies, two for the analog circuits (+9V, max 11A, -9V, max 2A) and one for the digital part (+3.3V, max 9A). The table below reports typical power requirements:

Power requirements	A2792 motherboard (without preamplifiers) +3.3V: 1000mA +9V: 150mA -9V: 40 mA	A2792 with preamplifiers +3.3V: 1000mA +9V: 1400mA -9V: 320mA (The values indicated refer to the preamplifiers developed by ETH Zurich)

Tab. 2.5: Power requirements

2.5 Ground and shields

The acquisition board has separated analog and digital grounds (see Fig. 2.5). However, the two grounds can be connected on the A2792 in three different ways:

- close to the power connector (JP1)
- directly on the backplane inside the crate (jumpers indicated with 'A' in the figure)
- with a soldering point close to the ADC's (see Fig. 2.5)

Usually, the best performances can be achieved connecting the ground of the detector to the analog ground of each acquisition unit. However, in order to avoid ground loops, it is necessary to keep the analog grounds of the A2792s separated from the ground of the I/O digital signals. For this reason, the TT-Link input signal is decoupled by means of a transformer and the metal case of the LEMO connector is isolated from both the digital ground and chassis.

The mechanical assembly of the SY2791 box and the front/rear panels of the A2792 are normally isolated from the analog ground, with the option of being connected to it through the jumper JP3. The AC power earth will be connected to the case of the power supply unit and, by default, to the chassis of the SY2791; the latter connection can be removed cutting the wire indicated with 'F'.

WARNING: the SY2791 is provided with the chassis connected to the earth (connection F closed), according to safety normatives of the electrical equipments. CAEN declines all responsibility for electrical shocks due to the earth connection removal.

At the rear side of the power supply unit a screw with a wing nut (or equivalent) is installed to ground the SY2791 chassis to the TPC cryostat (connection 'E'). On the front panel of each acquisition board there is a banana female connector for the cable shield which can be in contact to either AGND or the chassis through the 2-way jumper JP4 (see § 2.2.1)

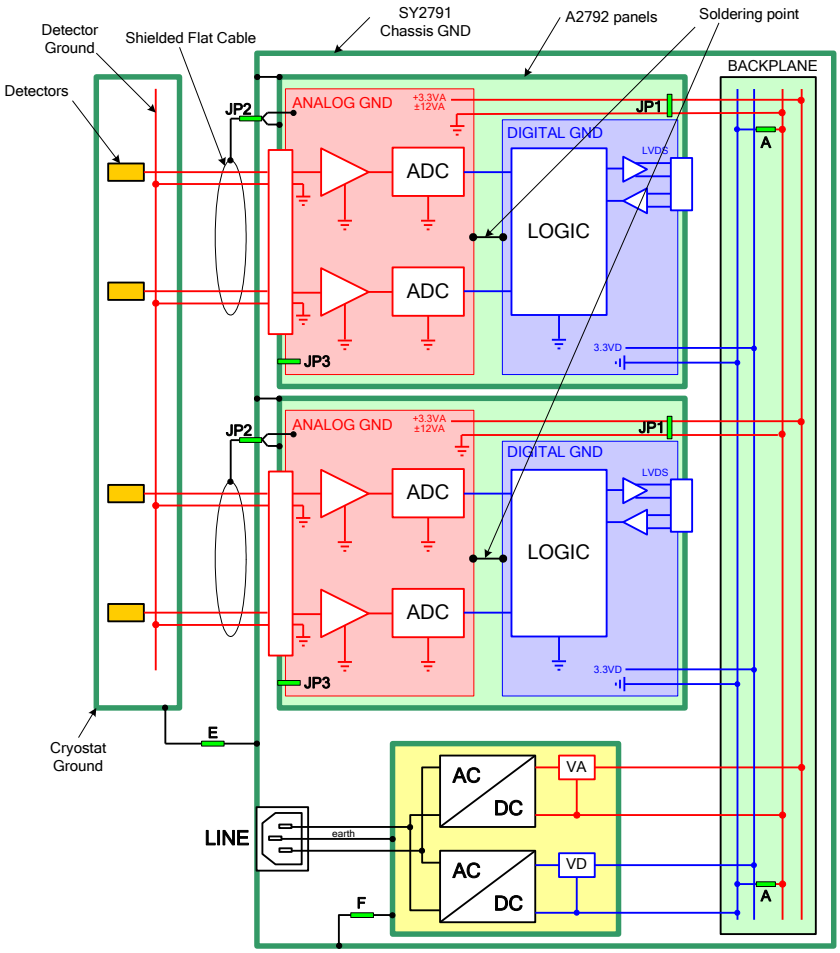

Fig. 2.5: Power Supply and Ground layout with a possible scheme of ground connections to the detector.

2.6 Preamplifiers

The motherboard of the A2792 has 16 sockets (20 pin single female strip line type *PRECI-DIP 315-91-120-41-003001* or equivalent); each socket can host a 5x3 cm hybrid circuit with two channels of preamplifier. This circuit can be adapted to the specifications of the detector. The mechanical constraints and the pin-out of the circuit are showed in Fig. 2.6 and Tab. 2.6.

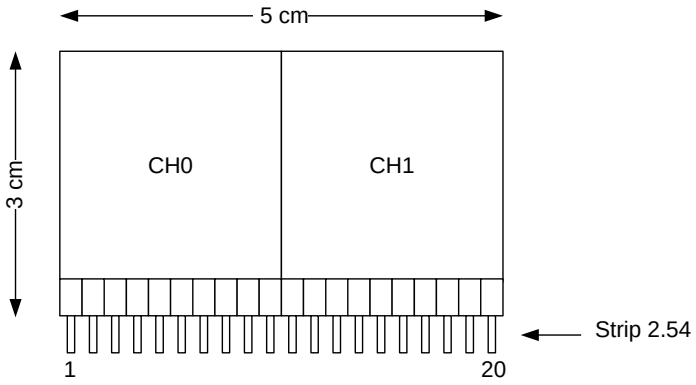

Fig. 2.6: preamplifier hybrid mechanical constraints

PIN #	NAME	DESCRIPTION
1	AGND	Analog Ground
2	AGND	Analog Ground
3	AGND	Analog Ground
4	IN0	Input Channel 0
5	+7V	Positive supply for the input stage (the voltage level can be adjusted)
6	-7V	Negative supply for the input stage (the voltage level can be adjusted)
7	DAC	Voltage level for the output offset adjust (from the DAC on the Mother Board)
8	V-	Negative supply for the output OpAmp (-2.5V or AGND; the voltage level can be adjusted via JP2 jumper, see fig.2.2)
9	OUT0	Output Channel 0
10	AGND	Analog Ground
11	AGND	Analog Ground
12	OUT1	Output Channel 1
13	V+	Positive supply for the output OpAmp (Typ 3.3V, the voltage level can be adjusted)
14	TEST	Test Signal
15	-7V	Negative supply for the input stage
16	+7V	Positive supply for the input stage
17	IN1	Input Channel 1
18	AGND	Analog Ground
19	AGND	Analog Ground
20	AGND	Analog Ground

Tab. 2.6: preamplifier pin-out

By default, the power supplies of the preamplifiers are ±7V for the charge integrator and +3.3V/-2.5V for the output opamp. However, it is possible to change these levels by replacing the resistors of the adjustable linear regulators (ask CAEN for more details).

N.B.: the hybrid circuit preamplifiers are sold separately from the SY2791 System.

2.7 Specification Table

Number of Channels	32 for one A2792; 256 for the full crate.
Preamplifier	Plug-in hybrid circuits with two channels each. See § 2.6 for the specifications.
Output Offset Adjust	Two programmable 16 bit DACs (ch. [0:15] and [16:31]) for the DC offset adjust of the preamplifiers output
Test Pulse	External from a double bridged LEMO. Internal with programmable voltage step (from 0.5 mV to 1V), positive or negative, shot control from TT-Link or SW command.
ADC resolution	12 bit (FSR = 3.3V, 1 LSB = 0.805 mV)
Sampling frequency	Programmable from ~40KHz to 2.5MHz.
Memory	1 MB (corresponding to 16K samples per channel). Expandable to 8 MB.
Number of buffers	From 2 (8K samples) to 1024 (16 samples) per channel. Maximum number of buffers (all channels): 4096
Trigger	Independent trigger channel by channel (threshold crossing); global trigger for all the channels coming from the TT-Link, Control I/O connector or SW command.
Trigger Time Stamp	32 bit counter synchronous with the sampling clock. Range of 2147 sec. @ 2MS/s.
Optical Link	Daisy chainable from 1 to 8 A2792s. Maximum data throughput = 80MB/s.
Power requirements	A2792 motherboard (without preamplifiers): +3.3V: 1000mA +9V: 150 A -9V: 40 mA A2792 with preamplifiers (*) +3.3V: 1000mA +9V: 1400mA -9V: 320mA

(*) The total power requirements for an A2792 depends on the type of preamplifiers. The values indicated refer to the preamplifers developed by ETH Zurich.

Tab. 2.7: A2792 specification table

3 Functional description

3.1 Block diagram

The Fig. 3.1 shows the block diagram of the A2792, *32 channel TPC readout board*. The analog and digital sections are indicated in red and blue respectively.

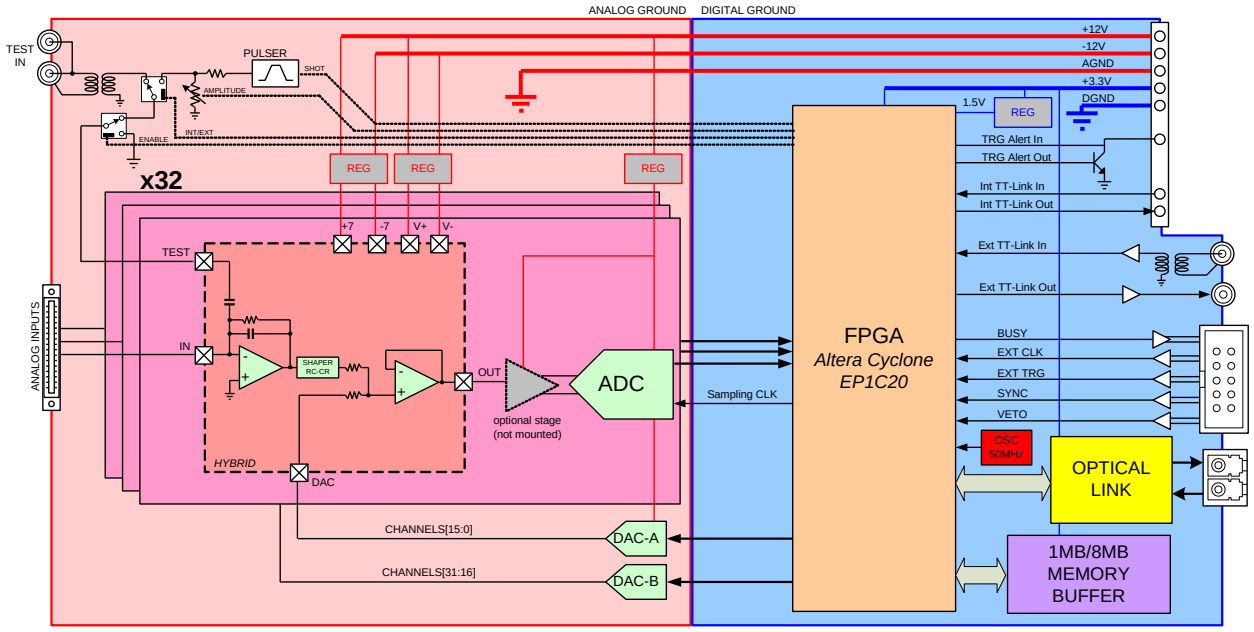

Fig. 3.1: A2792 block diagram

3.2 Analog Section

The analog signals coming from the detector are directly connected to the inputs of the preamplifiers that are housed in plug-in circuits. These are mounted over 20 pin sockets. The characteristics of the preamplifiers are described in § 2.6.

A ***test signal*** is routed to the pin 14 of each socket; both channels of the preamplifier AC couple the test signal to the input through a 1 pF capacitor. Usually the tolerance of this capacitor is very poor (50%), thus the amount of the charge injected into the preamplifier cannot be calculated precisely. For this reason, the test signal is not suitable for the calibration of the channels. When not used, the test signal must be connected to ground acting on the relevant relay. When enabled, the test signal can come from the external LEMO connectors or from the internal programmable pulser. The latter can generate a voltage step (positive or negative) with ~1us rise/fall time, by using a 16bit DAC.

Two programmable 16 bit DACs, ranging from 0 to 3.3V, allow the output of the preamplifiers to be shifted by a DC offset. The DAC 'A' serves the channels from 0 to 15, while DAC 'B' serves the channels from 16 to 31.

The output of the preamplifier goes down to the motherboard where the 32 output signals are routed to the ADC chips. It is possible to add another amplification stage between the output of the preamplifier and the ADC input; it can be used to adjust the dynamic range or to introduce another shaping amplifier. By default, this stage is not mounted.

3.3 A/D conversion

Each output of the preamplifiers is converted by a 12 bit ADC *Analog Device AD7276BUJZ*; a 14 bit pin to pin compatible version is also available. The sampling clock for the ADCs is provided by the FPGA; the

sampling clock period is *N* times the period of the TT-Link signal (100 ns), where *N* is to the content of the bits [24:16] of the ***Control Register***. This gives the following formula for the ADC sampling frequency:

F_{SCLK} *= 10MHz / N (with 4 <= N < 256)*

When the TT-Link is used in *"Trigger Mode"* (see § 3.5), the sampling clock is obtained from an internal 10 MHz signal (1/5 of the local oscillator). In this case, the synchronization of the A2792s cannot be achieved and each board (32 channels) has an independent sampling clock.

The ADC has a serial readout interface; this is handled by the FPGA that reads the serial data outputs with a fixed 45.45 MHz clock (10/11 of the 50 MHz local oscillator). Inside the FPGA, the ADC data are converted from serial to parallel and transferred to the memory interface that continuously writes the samples in the SRAM memory buffers. The data throughput from the ADCs to the memory (with F_{SCLK} = 2 MHz) is *12 x 32 x 2 = 768 Mbit/s = 96 MB/s*.

For test purposes, the FPGA can replace the ADC samples with fixed ***Test Pattern*** going from 0x000 to 0xFFF and back to 0x000. This corresponds to a Full Range triangular wave whose frequency is F_{SCLK} / *8192*. To enable the test pattern, the bit [8] of the ***Control Register*** must be set.

3.4 Acquisition Logic

The A2792 operates as a waveform digitizer: when the acquisition is running, the ADC samples are continuously written (in parallel for all the channels) into the **MEB,** a Multi Event circular memory Buffer. Each channel uses one circular buffer and operates independently from the others. When a channel is triggered, N_{post} more samples are written in the current buffer, where N_{post} is the content of the ***Post Trigger Register***, and then the buffer is saved and made available for the readout together with a header and a trigger time tag added by the acquisition logic; header, time tag and samples form one **event**. The acquisition on the channels that has been triggered continues, without any dead-time, switching to a new buffer, unless there is not any free available buffer; in this case, the acquisition on that channel is stopped.

The size of the circular buffers can be programmed by means of the bits [3:0] of the **Control Register** (see Tab. 4.2)

3.4.1 Starting and Stopping the acquisition

After the power-on or a hardware reset, the A2792 is in ***idle mode***; this means that the acquisition is not running. No data are written into the MEB and the data coming from the ADCs are discarded. In a system made of several A2792s, it is important to start the acquisition simultaneously in all the boards. For this reason, the Start of Run Command (**SOR**) is normally delivered through the TT-Link: when the Master of the TT-Link receives the start command from the Optical Link (Single Shot Commands, see § 4.2.6), it propagates the SOR to all the boards (including itself) starting the acquisition. In a similar way, the acquisition can be stopped simultaneously by the command End of Run (**EOR**).

It is also possible to start and stop the acquisition of one single board by setting/clearing the bit [4] of the ***Control Register*** (see § 4.2.2). This must be used when the TT-Link is in "Trigger Mode" and cannot send the SOR/EOD commands.

As the acquisition starts, the MEB is cleared (all data previously stored are lost) and the Trigger Time Tag is initialized. During the run, it is possible to send periodical SOR commands with the only effect of restarting the Trigger Time Tag; this is recommended in case the acquisition lasts for a long time and the boards could occasionally lose the time reference. As soon as the run is stopped, no further trigger can be accepted; however, the events previously acquired and still present in the MEB are not cleared and can be readout after the EOR.

3.4.2 Trigger Logic

As mentioned above, the acquisition is based on the trigger that defines a temporal window in which the waveform is acquired, saving N_{pre} samples of *Pre Trigger* and N_{post} samples of *Post Trigger* (where N_{post} is programmable and N_{pre} comes as *BufferSize* - N_{post}). Normally, the trigger of one channel (independent from the others) occurs when the digitized signal crosses a programmable threshold, either on the rising or falling edge. When the threshold is zero (or 0xFFF for negative signals), it is disabled and no trigger can be generated on that channel. From here on, we will consider positive signals.

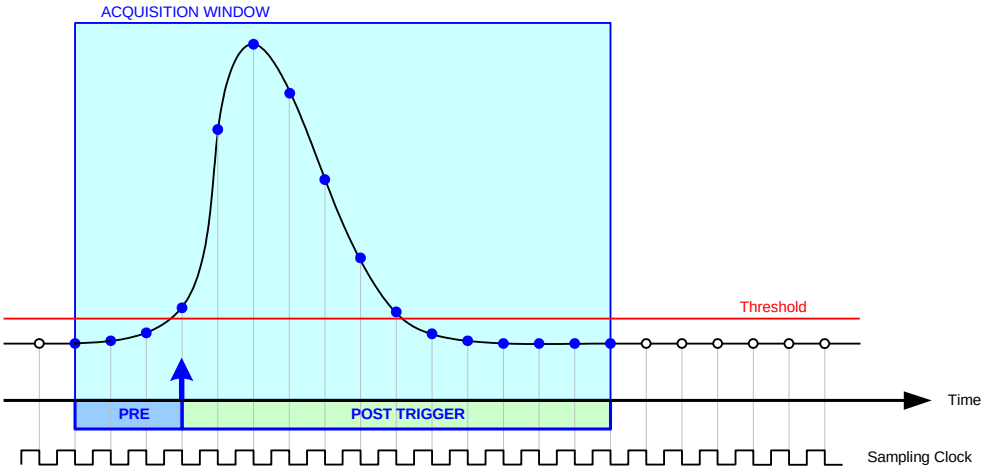

Fig. 3.2: Example of acquisition window with Buffer Size = 16 and Post Trigger = 12

If the time separation (in terms of number of samples) of two consecutive triggers is less than the buffer size, the two relevant acquisition windows will be overlapped (see Fig. 3.3). In this case, the Pre-Trigger of the second acquisition window contains less than N_{pre} samples. It is important to notice that in case of overlapping triggers the event size is not constant.

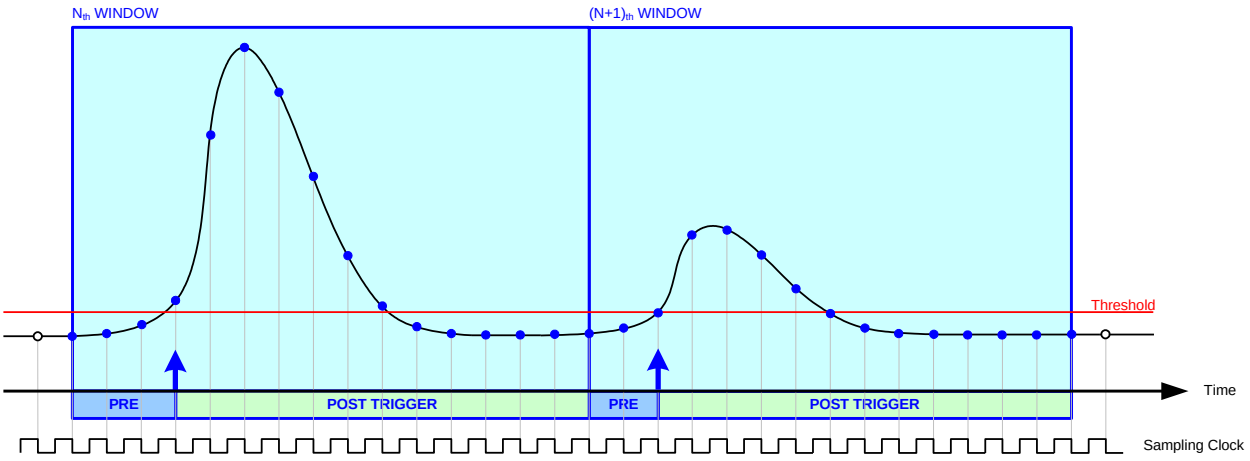

Fig. 3.3: Two overlapping acquisition windows caused by two separated pulses (threshold crossed twice)

If instead the signal is over the threshold at the end of the acquisition window, then the acquisition will be extended, meaning that a new complete buffer will be saved. This allows a large pulse (pile-up) to be recorded as long as there are free buffers to write (see Fig. 3.4). The buffer extension is stopped when the signal returns under the threshold or the buffers are all occupied.

A trigger arming mechanism is foreseen in order to prevent one channel to save buffers continuously because it stays always over the threshold (for example when the threshold is not properly set): when the run starts, all the channels are not armed by default. When the signal goes under the threshold, the trigger on that threshold is armed. As soon as it goes over the threshold, a trigger is generated, the trigger itself is disarmed and one buffer is saved (or more buffers in case of extension). The trigger will remain disarmed until the signal goes back under the threshold.

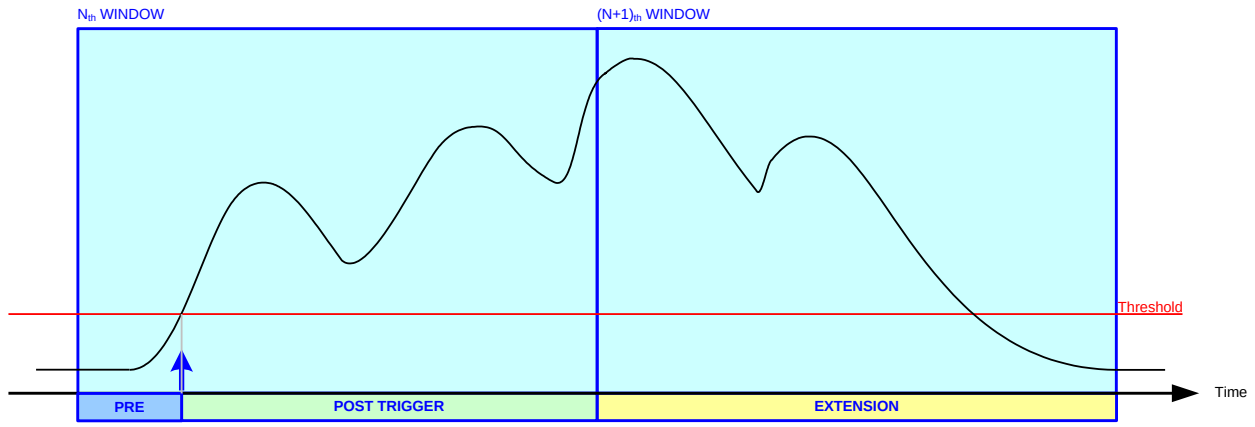

Fig. 3.4: Buffer extension caused by the pile-up

The main problem to face when triggering the channels with a simple digital threshold is that in most cases the signal coming from the output of the preamplifier is rather noisy, thus it is necessary to find a compromise between having a low threshold and get false triggers and setting a higher threshold and lose good pulses. There are many digital algorithms that can be applied to the signal in order to filter the noise and make the trigger more efficient. However, at least for the first prototypes of the A2792, we don't want to implement any digital processing inside the FPGA, although it would be possible. Conversely, we have decided to follow a different approach, which is based on the assumption that we are interested in detecting a very small pulse on one channel only whether this is a "side effect" of a larger charge collection occurred on some other channel close to it. In fact, when one particle passes through the detector, the amount of charge released is distributed over several channels, but it is much more evident in one (or few) channel. So the idea is to "alert" a group of channels belonging to a certain region as soon as a "significant" pulse has been detected in one channel within the region; when alerted, the other channels lower their threshold and allow even a very small pulse to trigger the acquisition.

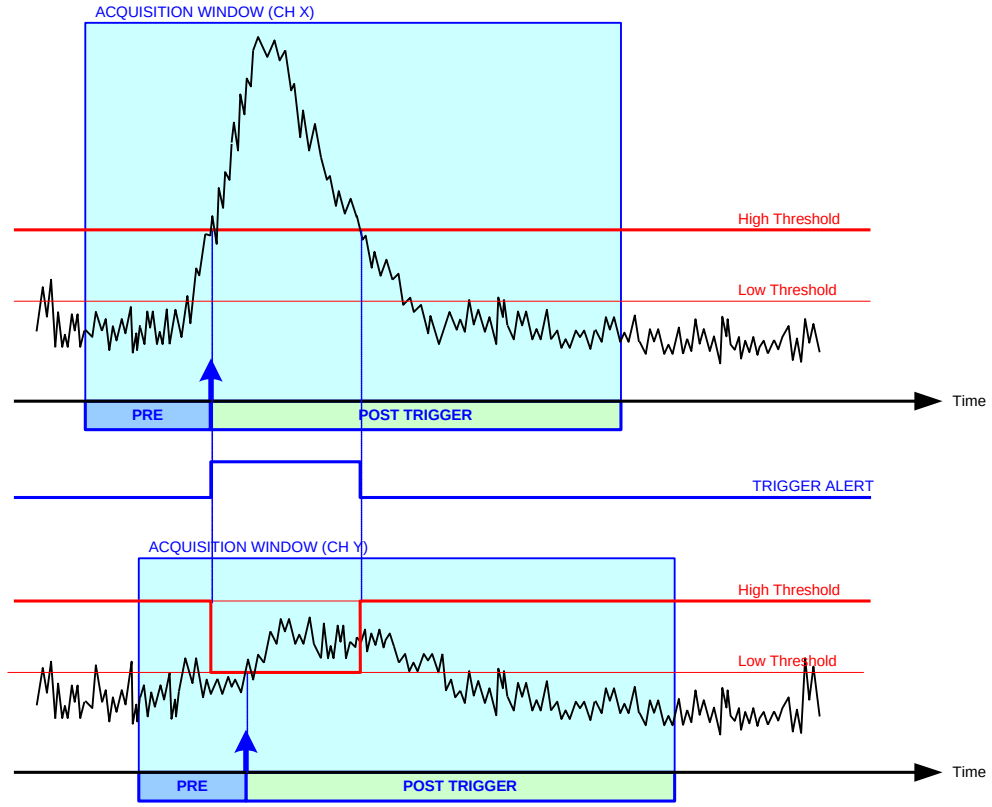

Fig. 3.5: Example of trigger on the 'Low Threshold' of channel Y when the 'Trigger Alert' has been asserted by the channel X

From the hardware point of view, the trigger alerting can be implemented at *board level* (over 32 channels) just providing it in the firmware of the FPGA, at *crate level* (over 256 channels) using the ***Trigger Alert*** signal on the backplane, which is an open collector signal (active low) that can be asserted by any A2792 or at *system level*, propagating the Trigger Alert signal of one crate to the whole system through the TT-Link. In principle, it is also possible to associate a channel, board or crate identifier to the alert signal, so that each part of the system can decide whether to react or not to an alert coming from another part, thus bringing to the definition of regions within which the channels are cross related. For the moment, the firmware of the FPGA provides only a Trigger Alert within the crate, which is asserted when at least one channel between the 256 is over the High Threshold. Both High a Low Thresholds are programmable. If the Low Thresholds are zero, then all the channels are triggered as soon as one channel exceeds the High Threshold. **N.B.. Trigger Alert has a ~5 samples latency!**

Besides the independent triggers generated by the channels, the A2792 provides a ***Global Trigger*** that causes the acquisition of one event for every enabled channel. The Global Trigger can come from a SW command (see § 4.2.6) of from the TT-Link. If one channel is already saving a buffer (i.e. the global trigger arrives within the post trigger window), it will be ignored.

3.4.3 Continuous acquisition (Auto Trigger)

In some applications or for test purposes it is required a continuous acquisition of the input signals. However, it is not convenient to manage a continuous data stream during the readout from the Optical Link. For this reason, the continuous acquisition is made possible still keeping the acquisition based on the events: in this case, the trigger is a periodical signal generated inside the FPGA in such a way that the acquisition windows are concatenated ($F_{TRG} = F_{SCLK} / N_S$, where F_{TRG} is the auto trigger frequency, F_{SCLK} is the sampling frequency and N_S is the number of samples of the acquisition window, according to the buffer size set in the Control Register). It is clear that the acquisition will be actually continuous only under the condition that the data throughput rate can be sustained by the readout from the Optical Link; as mentioned above, when the 32 channels are all enabled, the throughput rate is 96 MB/s with a sampling rate of 2 MS/s. For the moment, this rate exceeds the bandwidth of the Optical Link, thus it is necessary to decrease the sampling rate or to disable some channels.

3.4.4 Zero Suppression and Data Compression

The data readout in a system like the SY2791 becomes unmanageable very quickly as soon as the number of channels increases. Usually, the pieces of signal that contain useful information are a small part of the whole digitized waveforms. In order to significantly reduce the throughput rate and, above all, the amount of data that must be saved and processed by the DAQ system, it is convenient to reduce the data before transferring them to the PC. Basically there are two approaches, one not excluding the other:

Zero Suppression: it can be defined and implemented a zero suppression algorithm that allows the FPGA to discard a part of the samples belonging to the acquisition window. For example, one can decide to suppress the tail of the pulse, that is all the samples following the point in which the signal returns under the threshold.

Data Compression: there are many compression algorithms, either lossless or not. In the case of the A2792, a good compromise can be achieved storing only the difference between consecutive samples (***Delta***) instead of the absolute values: representing that difference over 4 bits and putting 4 samples (instead of 1) in a 16 bit word, the data are compressed of a factor 4. In most cases, this compression is lossless because the actual bandwidth of the signal is usually much lower than the Nyquist frequency and the probability to have a Delta greater than 16 LSB is quite low. However, it is possible to prevent this compression to lose information just allowing it to store the full four 12 bit samples when one of them overflows the 4 bit representation.

For the moment, neither the Zero Suppression nor the Data Compression are implemented in the firmware of the FPGA.

3.5 TT-Link

The TT-Link of the A2792 can be used in two different modes, as explained in the following paragraphs.

3.5.1 TT-Link Normal Mode

The SY2791 is a fully scalable system; this means that it is possible to add as many channels as needed and keep them synchronized during the acquisition. As already mentioned, the TT-Link is used to distribute the sampling clock and a set of real time commands to all the boards connected through it.

The TT-Link is a 1 wire serial bus on which one A2792 master sends a 10 MHz clock with a modulated duty cycle.

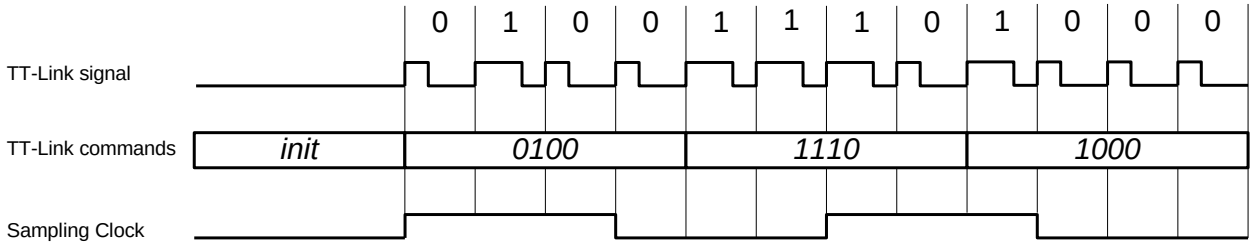

Fig. 3.6 TT-Link signals

The modulation allows the encoding of one bit in each clock period, thus a 10 Mbit transmission can be implemented over the TT-Link. The bit stream is grouped in frames of 4 bits; one frame corresponds to an *opcode* that represents a particular command. During the reset of the A2792 master board, the TT-Link signal is kept low for at least 100 ns (***initialization***); this permits to the slave boards to initialize the state machines that receive the TT-Link and decode the commands. The first rising edge on the TT-Link corresponds to first bit of the first frame. The TT-Link can be reinitialized from time to time in order to recover from a synchronism loss.

Up till now, 6 commands have been defined:

NOP	0000	No Operation (IDLE state)
SOR	0001	Start of Run
EOR	0010	End of Run
GTRG	0011	Global Trigger
TRGALERT	0100	Trigger Alert
TPULSE	0101	Test Pulse (one shot from the internal test pulse generator)

Tab. 3.1: TT-Link command opcodes

Besides the commands, the TT-Link is also used to synchronize the ADC sampling clocks of the whole system; the sampling clock is obtained dividing of the TT-Link signal by a programmable factor (bits [23:16] of the Control Register). The maximum frequency is 2.5 MHz which is obtained dividing by 4. The initialization of the TT-Link guarantees the correct phase of the sampling clocks after the frequency division.

The Fig. 3.7 shows the distribution of the TT-Link signal over the system. Each A2792 is able to drive and receive the TT-Link through two ports, one on the rear panel (two LEMO connectors, see § 2.2.2) and the other one on the backplane connector.

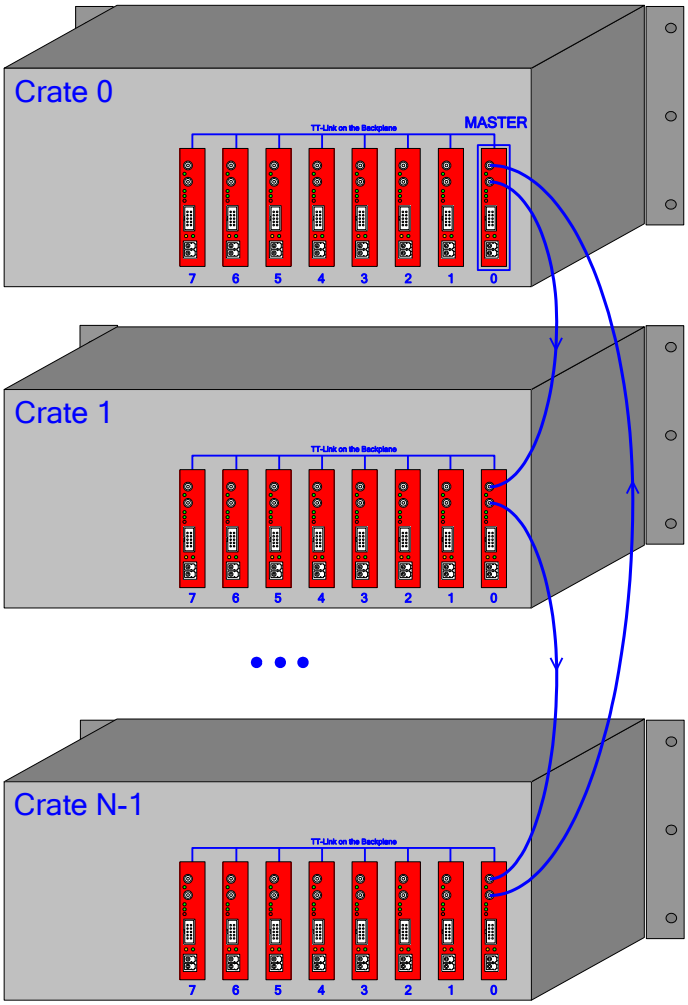

Fig. 3.7 TT-Link distribution between boards and crates

The distribution of the TT-Link between crates is done through a coaxial cable connecting in daisy chain all the boards plugged in the slot 0 (that is the rightmost slot, looking from the rear panel); the output of the last board is connected to the input of the first one, thus makes a closed loop. There must be only one A2792 master in this ring; the master encodes the commands and generates the 10 MHz TT-Link signals. All the A2792s in the slot 0, including the master, propagate the TT-Link signal inside their crate through the backplane, so that all the boards in the crate can receive the signal.

3.5.2 TT-Link Trigger Mode

For test purposes, the TT-Link can be used only for sending and receiving a global trigger. This mode, much simpler than the normal mode, doesn't foresee any encoding; the signal is the pure trigger pulse (TTL or LVTTL, active high, min. width = 30 ns), which is distributed to all the A2792s exactly as in the normal mode described above, with the difference that in this case the "master" of the link (that is the trigger pulse generator) can be any instrument external to the system.

4 User Interface

4.1 Optical Link

The Optical Link of the A2792 is a bi-directional communication channel called *CONET* (**C**hainable **O**ptical **NET**work), able to transfer data up to 80 MB/s. The CONET is controlled by a PCI board, the A2818, that acts as a master of the communication, meaning that every transaction, but the interrupt request, is always started by a request sent by the A2818 to one A2792, that acts as a slave, and closed by the response sent by that A2792. It is possible to connect up to eight A2792s in daisy chain; see § 2.2.2 for the possible network topologies of the CONET and the relevant connecting instructions.

There are three modes to access the A2792:

- **Single Read**: read one long word (32 bit) from the A2792, either the content of an internal register or one datum from the MEB.
- **Single Write**: write one long word (32 bit) to the internal registers of the A2792.
- **Block Transfer Read**: read a block of long words (32 bit) from the MEB. With this type of access, it may happen that the MEB has less data than what requested; in this case, the slave transfers all the available data and then terminate the transaction prematurely. The number of words actually transferred is returned by the BLT function.

It is possible to pack several requests (for example a list of write accesses) and let the A2818 send them to the slave with a single transmission packet and then wait for the reception of all the responses. This reduces the protocol overhead and increases significantly the data throughput of the single accesses. Such transactions are called ***MultiRead*** and ***MultiWrite***; it is worth noticing that a MultiRead is not the same as a Block Transfer Read, since the first allows the access to different addresses and can be done for both registers and MEB data. However, it does not make sense to read the MEB using the MultiRead function, because it is always slower than the Block Transfer Read.

The CONET supports the interrupt request from one slave (A2792) to the host PC through the IRQ lines of the PCI bus. When enabled, the A2792 can generate an interrupt request (see § 4.3), which is propagated through the Optical Link up to the A2818; this is the only case in which the transaction is started by the slave without the explicit request of the CONET master. As soon as the A2818 receives the interrupt request from one slave, it asserts the interrupt on the PCI bus. The propagation latency is of the order of 10-20 μs. It is care of the drivers and software to handle this interrupt request.

As already mentioned, with the present firmware revision, the optical link has a bandwidth of about 80 MB/s (this could be increased up to ~125 MB/s with a firmware upgrade that is not available for the moment). However, such a throughput rate can be reached only with transfers that involve large blocks of data (see Fig. 4.1). In fact, there is a fixed latency due to the transmission of the request packet and the reception of the data. When few bytes are transferred, the latency is much bigger than the real transfer time and the resultant throughput drops drastically.

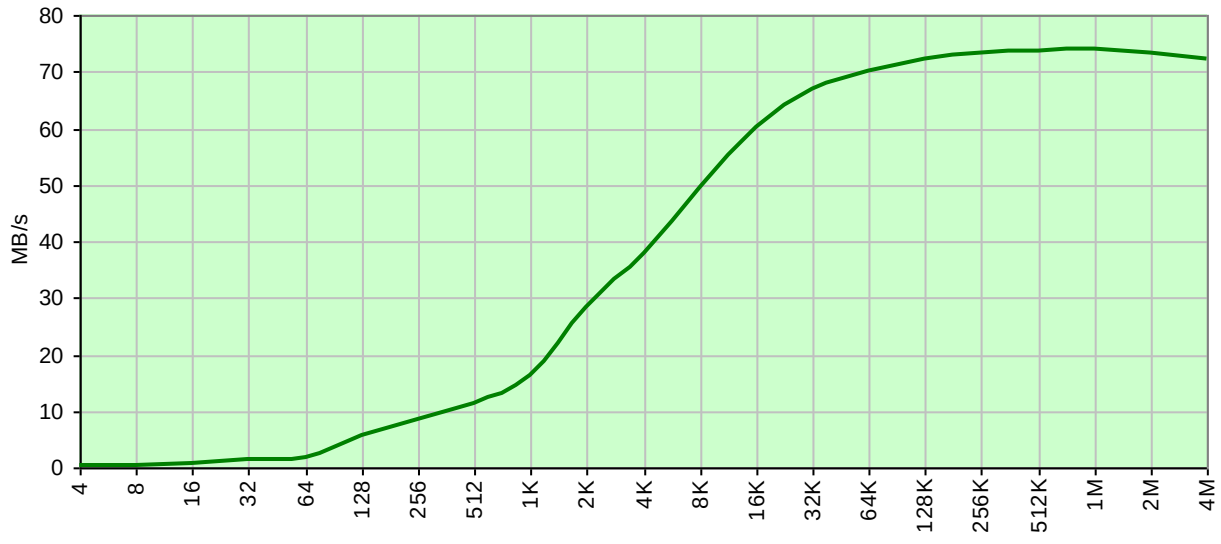

Fig. 4.1: Throughput Rate vs BLT Block Size

4.2 Register Description

The A2792 has a certain number of 32 bit registers that can be read and/or written through the optical link. The following table reports the register address map, indicating also the register access **Type** (**R** = read only, **W** = write only, **R/W** = read and write), the number of significant bits, whether the register is initialized or not after a **Reset** (power ON, LinkReset or SW reset) or after a **Clear** (SW clear of Start of Run), the **Default** value after the initialisation and the **Function** of the register.

Address	Register	Type	#bit	RES	CLR	Default	Function
0x0000	MEB	R	32	♦	♦	-	MEB readout data
0x1000	CONTROL	R / W	32	♦		0x00050001	Control Register
0x1004	CONTROL_SET	R / W	32			-	Control Register (Set Mode Write)
0x1008	CONTROL_CLR	R / W	32			-	Control Register (Clear Mode Write)
0x100C	STATUS	R	4			-	Status Register
0x1010	FW_REVISION	R	32			-	Firmware Revision
0x1014	TEST	R / W	32	♦		0xAAAAAAAA	Test Register
0x1018	SINGLESHOT_CMD	W	20			-	Single Shot SW commands
0x101C	CH_ENABLE	R / W	32	♦		0xFFFFFFFF	Channel Enable Mask
0x1020	NEVSTORED	R	16	♦	♦	-	Number of events stored in the MEB
0x1024	NEVREAD	R / W	16	♦		0x0001	Max. num. of events to read in a BLT
0x1028	POST_TRG	R / W	13	♦		0x0008	Post Trigger Register
0x102C	ENFLASH	R / W	1	♦		0x1	SPI Flash Enable
0x1030	SPIDATA	R / W	8			-	SPI read and write data
0x1034	DAC_A	R / W	16	♦		0x0000	CH0..15 DC offset
0x1038	DAC_B	R / W	16	♦		0x0000	CH16..31 DC offset
0x103C	DAC_PULSE	R / W	16	♦		0x0000	Test pulse amplitude
0x1100 + CH * 4	THR_LOW	R / W	12	♦		0xFFF	Low Thresholds (32 values)
0x1200 + CH * 4	THR_HIGH	R / W	12	♦		0xFFF	High Thresholds (32 values)
0xF000 – 0xF100	CONF_ROM	R	8			-	Configuration ROM

Tab. 4.1: Register Map

4.2.1 MEB

Address: 0x0000
Bits: [31:0]
Access Mode: Read Only

A read access to the MEB address, either in single mode or block transfer, causes the readout of the data from the Multi Event Buffer. See § 4.3 for more details about the access to the MEB.

4.2.2 CONTROL

Address: 0x1000, 0x1004 (BitSet), 0x1008 (BitClear)
Bits: [31:0]
Access Mode: Read and Write

There are three ways to write the content of the Control Register:

- Normal Write (at address 0x1000): the content of the register is fully overwritten by the new data.
- Bit Set Mode (at address 0x1004): writing '1' in one bit, will set that bit; writing '0' leaves the bit unchanged.
- Bit Clear Mode (at address 0x1008): writing '1' in one bit, will clear that bit; writing '0' leaves the bit unchanged.

The use of the Bit Set/Clear modes are recommended when concurrent processes can access the register; this prevents a process to operate on the content of the register while another process has already changed it. The read access to the Control Register can be done at any address.

[3:0] 0x0000000F Default: 1	**Buffer Organization**: number of buffers per channel in which the memory is divided (see Tab. 4.2).
[4] 0x00000010 Default: 0	**Force Acquisition Run**: normally, the acquisition is started at the same time in all the A2792s by means of a command sent through the TT-Link (see § 3.4.1). However, it is possible to force one board to start the acquisition setting this bit. **0:** The acquisition start/stop is controlled by TT-Link. **1:** The acquisition is forced to be running.
[5] 0x00000020 Default: 0	**TT-Link Mode** (see § 3.5). **0:** **Normal Mode.** The TT-Link is used to propagate the sampling clock and the commands. **1:** **Trigger Mode**. The TT-Link is used only for global triggers.
[6] 0x00000040 Default: 0	**TT-Link Master** (see § 3.5). **0:** The board is a slave of the Rear Panel TT-Link (however it can be the master of the TT-Link on the backplane when it is plugged in the slot 0). **1:** The board is the master of the Rear Panel TT-Link. It must be also the master of the TT-Link on the basckplane, thus this board must be plugged in the slot 0 of the crate.
[7] 0x00000080 Default: 0	**Internal Test Pulse Polarity** (see § 3.2). **0:** Negative voltage step. **1:** Positive voltage step.
[8] 0x00000100 Default: 0	**Test Pattern Enable** (see § 3.3). **0:** Test pattern is disabled. Data are real samples coming from the ADCs. **1:** Test Pattern is enabled: Data from the ADCs are replaced by a triangular wave ranging from 0x000 to 0xFFF and back to 0x000. The frequency of the test pattern is $F_{SCLK}/8192$, where F_{SCLK} is the sampling frequency.
[9] 0x00000200 Default: 0	**Test Pulse Enable** (see § 3.2). **0:** Test Signal is connected to the analog ground. No test pulse can be injected into the preamplifiers. **1:** Test Signal connected to either the External Test Input or the Internal Pulse Generator (see bit [10])
[10] 0x00000400 Default: 0	**Test Pulse Internal/External** (see § 3.2). **0:** Test Signal from the External Test Input on the rear panel. **1:** Test Signal from the Internal Pulse Generator.
[11] 0x00000800 Default: 0	**Auto Trigger (Continuous Acquisition)** (see § 3.4.3) **0:** Auto Trigger disabled. **1:** A periodical global trigger is internally generated with a frequency.
[12] 0x00001000 Default: 0	**Trigger Edge Low Channels [15:0]** (see § 3.4.2) **0:** Trigger on the rising edge of the input signal. **1:** Trigger on the falling edge of the input signal.
[13] 0x00002000 Default: 0	**Trigger Edge High Channels [31:15]** (see § 3.4.2) **0:** Trigger on the rising edge of the input signal. **1:** Trigger on the falling edge of the input signal.
[14] 0x00004000 Default: 0	**Auto Trigger Inhibit** **0:** Auto Trigger Inhibit disabled **1:** Auto Trigger Inhibit enabled
[15] 0x00008000 Default: 0	**External Trigger Inhibit** **0:** Ext. Trigger Inhibit disabled **1:** Ext. Trigger Inhibit enabled
[23:16] 0x00FF0000 Default: 5	**Sampling Frequency**: set the frequency of the sampling clock according to the formula $\boldsymbol{F_{SCLK} = 10MHz / N}$ where N is the content of the bit [23:16]. The minimum value allowed for N is 4, which corresponds to $F_{SCLK} = 2.5MHz$.
[27:24] 0x0F000000 Default: 0	**Disable ADC octet**: reserved
[31:28] 0xF0000000	Not Used

The standard version of the A2792 has 1 MB of memory. One sample takes 2 bytes. This means that each channel has 16K samples in total. The memory is organized in a certain number of circular buffers, according to the following table:

Bit [3:0]	# of buffers	Buffer Size (in samples)	
		1 MB version	8 MB version
0	1	16K	64K
1	2	8K	32K
2	4	4K	16K
3	8	2K	8K
4	16	1K	4K
5	32	512	2K
6	64	256	1K
7	128	128	512
8	256	64	256
9	512	32	128
10-15	not allowed		

Tab. 4.2: Buffer Organization Table

4.2.3 STATUS

Address: 0x100C
Bits: [4:0]
Access Mode: Read Only

[2:0] 0x00000007	**Slot ID**: slot number in which the board is plugged (from 0 to 7). 0 is the rightmost slot in the crate (looking the rear panel)
[4] 0x00000008	**Acquisition Running**: **0:** The acquisition is stopped. **1:** The acquisition is running.

4.2.4 FW_REVISION

Address: 0x1010
Bits: [31:0]
Access Mode: Read Only

[15:0] 0x0000FFFF	**Firmware Revision**: the format if **XX.YY**, where XX and YY are the major and minor Revision Numbers (2 bytes each)
[31:16] 0xFFFF0000	**Realization Date**: The format is **YMDD**, where Y is the year (8 stands for 2008), M is the month (from 0x1 to 0xC) and DD is the day (hex number that must be interpreted as a decimal). Example: 0x8214 is the 14th of February 2008.

4.2.5 TEST

Address: 0x1014
Bits: [31:0]
Access Mode: Read and Write

The Test Register may have different meanings:

- It can be used as a 32 bit scratch register to verify the regular access from the Optical Link to the A2792.
- Setting of the Internal Test Pulse amplitude (this is not yet completely defined).

4.2.6 SINGLESHOT_CMD

Address: 0x1018
Bits: [19:0]
Access Mode: Write Only

This register is used to send SW commands to the A2792. Each bit of the register corresponds to a specific action; writing a word to this register causes the execution of the actions related to those bits that are ‘1’ in the word. It is possible to set multiple bits, thus giving the possibility to cause the simultaneous

execution of multiple actions. For example, writing 0x0000000C to the Single Shot Register, it is possible to send a test pulse and a global trigger to all the channels of the A2792 at the same time.

The bits above 16 are dedicated to send commands through the TT-Link. These bits must be used only in the board that is Master of the TT-Link. Using them in the others boards, won't have any effect.

[0] 0x00000001	**Reset**: this command causes the following actions: • Stops the acquisition (if it is running); • Clears all data and counters; • Reset the Trigger Time Tag; • Set to their default value all the registers with '♦' in the column **RES** of the Tab. 4.1.
[1] 0x00000002	**Clear**: this command causes the following actions: • Stops the acquisition (if it is running); • Clears all data and counters; • Reset the Trigger Time Tag.
[2] 0x00000004	**Global Trigger**: send a global trigger to all the channels of the A2792.
[3] 0x00000008	**Test Pulse**: send a test pulse from the Internal Pulse Generator. The polarity (step up/down) depends on the bit [7] of the Control Register. Once toggled, the output of the internal pulse generator returns to the idle state after about 10 ms. The test pulse will actually arrive to the 32 channels of the A2792 only if the test pulse is enabled and switched to "Internal" (bit [9] and [10] of the Control Register).
[15:4]	**Reserved.**
[16] 0x00010000	**TT-Link Start of Run (SOR)**
[17] 0x00020000	**TT-Link End of Run (EOR)**
[18] 0x00040000	**TT-Link Global Trigger**
[19] 0x00080000	**TT-Link Test Pulse**

4.2.7 CH_ENABLE

Address: 0x101C
Bits: [31:0]
Access Mode: Read and Write

The **Channel Enable Register** allows the user to enable/disable the channels of the A2792. The channel *n* is enabled when the relevant bit *n* of this register is set. Disabled channels don't accept triggers, thus they don't contribute to the readout data.

4.2.8 NEVSTORED

Address: 0x1020
Bits: [15:0]
Access Mode: Read Only

The value of the **NEVSTORED Register** (16 bits) corresponds to the number of events stored in the MEB and available for readout.

4.2.9 NEVREAD

Address: 0x1024
Bits: [15:0]
Access Mode: Read and Write

The value of the **NEVREAD Register** (16 bits) corresponds to the maximum number of events that are transferred in a Block Transfer. After the last word of the n_{th} event (where *n* is the content of the register), the A2792 terminates the block transfer, whatever is the size actually requested by the readout program. If the MEB contains less than *n* events, the transfer will be terminated after the last available word. The default setting is 1.

4.2.10 POST_TRG

Address: 0x1028
Bits: [12:0]
Access Mode: Read and Write

The **Post Trigger Register** (13 bits) allows the user to set the position of the trigger inside the acquisition window, that is the number of samples following the trigger (see § 3.4.2). Since the memory chip of the

A2792 is 32 bit wide, the data flow from and to the SRAM is based on couples of samples; therefore, the Port Trigger is expressed in couples of samples. It can be converted in time, according to the following formula:

$T_{post} = (N_{post} + 1)* 2 / F_{SCLK}$ *(1 sample uncertainty; minimum value = 1)*

where T_{post} is the length of the Post Trigger window in μs, N_{post} is the content of this register and F_{SCLK} is the frequency of sampling clock in MHz.

4.2.11 ENFLASH

Address: 0x102C
Bits: [0]
Access Mode: Read and Write

This register is used to upgrade the firmware of the board and is managed by the ***CLupgrade*** tool. The direct access to it is not allowed.

4.2.12 SPIDATA

Address: 0x1030
Bits: [7:0]
Access Mode: Read and Write

This register is used to upgrade the firmware of the board and is managed by the ***CLupgrade*** tool. The direct access to it is not allowed.

4.2.13 DAC_A

Address: 0x1034
Bits: [15:0]
Access Mode: Read and Write

A write access to the **DAC-A Register** (16 bits) causes the programming of the 16 bit DAC that serves the channels from 0 to 15: this DAC is used to adjust the DC level of the output of the preamplifiers. The output of the DAC can range from 0V (0x0000) to 3.3V (0xFFFF). A read access to this register returns the content of the register as stored in the FPGA (it doesn't corresponds to a real reading of the analog voltage). The default value after a reset or power-on is 0.

4.2.14 DAC_B

Address: 0x1038
Bits: [15:0]
Access Mode: Read and Write

Same as DAC-A, but for channels from 16 to 31.

4.2.15 DAC_PULSE

Address: 0x103C
Bits: [15:0]
Access Mode: Read and Write

A write access to this Register (16 bits) allows the programming of the 16 bit DAC that sets the Test pulse amplitude. A read access to this register returns the content of the register as. The default value after a reset or power-on is 0.

4.2.16 THR_LOW

Address: 0x1100 + CH * 4
Bits: [11:0]
Access Mode: Read and Write

These 32 registers (one per channel) contain the values of the Low Thresholds (12 bits) expressed in ADC counts (1 ADC count = ~0.8 mV). Set the threshold to 0xFFF for positive signals or 0x000 for negative signals if you want to disable it. See § 3.4.2 for the description of the high and low thresholds and the role they play in the trigger logic.

4.2.17 THR_HIGH

Address: 0x1200 + CH * 4
Bits: [11:0]
Access Mode: Read and Write

Same as for Low Thresholds.

4.2.18 CONF_ROM

Address: 0xF000 – 0xF100
Bits: [7:0]
Access Mode: Read Only

The **Configuration ROM** contains information about the model and revision of the board, the manufacturer ID, the serial number, as reported in the table below.

Address	*Data*	*Value*	*Meaning*
0xF024	OUI2	0x00	The OUI (Organization Unique Identifier) is the Company Identification number assigned by IEEE. CAEN's OUI is 00-12-5E. (http://standards.ieee.org/regauth/oui/index.shtml).
0xF028	OUI1	0x12	
0xF02C	OUI0	0x5E	
0xF030	VERSION		Board Version (See Tab. 4.4).
0xF034	BOARD2	0x00	A2792 Identification Number (00-0A-E8).
0xF038	BOARD1	0x0A	
0xF03C	BOARD0	0xE8	
0xF04C	PCB_REV		PCB Revision of the A2792.
0xF080	SERNUM1		A2792 serial number: ***S.N. = SERNUM0 + SERNUM1 * 256***
0xF084	SERNUM0		

Tab. 4.3: Configuration ROM content

Version	*Memory*	*FPGA*	*Premplifier*	*Others*
0	1M	EP1C20	Version 1	
1	1M	EP1C20	Version 2	
2				
3				

Tab. 4.4: A2792 versions

4.3 Event Data Format and Readout Modes

From the functional point of view, the Multi Event Buffer is organized as a FIFO in which each channel can push one event while the acquisition is running. The events will be read out from the Optical Link in the same temporal order in which they have been written.

Fig. 4.2: Event format

The event data are formatted as showed in Fig. 4.2. The first word is the **header** of the event and contains the following information:

- **Event Size**: number of long words (32 bit) including the header
- **Lost Triggers**: number of triggers that have not been accepted on that channel before this event.
- **Channel**: channel identification (0 to 31).
- **Flags**: trigger type (see Tab. 4.5).

The **flags** identify the type of the trigger that caused the buffer saving, according to the table below.

Flags	*Trigger Type*
000	Not allowed
001	Global Trigger
010	Low Threshold crossing
011	Low Threshold crossing and a Global Trigger received during the post trigger
100	High Threshold crossing
101	High Threshold crossing and a Global Trigger received during the post trigger
110	Not allowed
111	Not allowed

Tab. 4.5: Trigger Flags

The **Trigger Time Tag** is the value of a 32 bit time counter that is incremented every sampling clock cycle and latched with the trigger.

The access to the Multi Event Buffer is managed by the FPGA in order to allow simultaneous read and write operations. This means that the data stored in the MEB are ready for the readout while the acquisition logic continues to collect new events. One event is available for reading only when it has been completely written in the MEB.

Although the MEB could be read with Single Read accesses, the Block Transfer is the proper way to read it. The efficiency of the readout (that is the throughput rate that can be sustained) is strongly dependent on the size of the blocks that are read with every Block Transfer Cycle (see § 4.1). For this reason, we suggest to read several events at time, setting a suitable value for the NEVREAD Register (see § 4.2.9). In general, the readout program doesn't know a priori how many events are currently available in the MEB and which is their size; this means that it doesn't know when to launch the Block Transfer Read and how many word to request for. There are two typical approaches:

Register Polling: the readout program polls the EVSTORED register and launch the BLT as soon as there are at least *N* events in the MEB, where *N* is the content of the NEVREAD register. The number of words (32 bit) requested by the BLT will be *N*EventSize*, where *EventSize* is the maximum number of words per event, that is *2+BuffSize/2*, being *BuffSize* the size of the acquisition buffer according to the Tab. 4.2. This is well done and very clear but doesn't achieve the maximum efficiency; in fact, polling the EVSTORED register, which consists in a Single Read access, takes more or less the same time of an empty BLT cycle (i.e. a BLT that doesn't return any data because the MEB is empty). Therefore, it is more convenient to make a simple loop in which the MEB is continuously read by BLT cycles of the size reported above, whatever is the number of events actually available in the MEB. Every BLT may return no data (0 events) or a number of events up to *N*.

Interrupt wake up: the main drawback of the register polling is that the readout program may waste CPU time for polling the register without reading any data. To avoid this, it is necessary to use the interrupts: the A2792 asserts the interrupt request when there are at least *N* events in the MEB, where *N* is still the content of the NEVREAD register. The interrupt request is propagated through the Optical Link to the A2818 (the propagation latency is of the order of few μs) that can assert the interrupt request on the PCI bus (only when enabled). This allows the readout program to sleep until the MEB contains the programmed number of events; at that time, the program can launch the BLT of the same size calculated for the polling mode and read exactly *N* events.

In the typical case where the readout program must handle several A2792s, either connected in daisy chain to a single A2818 or to many A2818s in the same PC, the readout procedures change: for the register polling mode, the only difference is that the readout loop which launches the BLT cycles becomes two nested loops, the inner of which is used to go through each A2792. For the interrupt, it is more complicated; in fact, it does not make sense to sleep waiting for the interrupt from one A2792 because that A2792 could remain empty for a long time while the others have data to read. The problem can be solved using as many threads as the number of A2792 to read; each thread waits for the interrupt coming from the relevant A2792 and the readout of the boards takes place in parallel. It is not the purpose of this document to deal with the issues related to the acquisition software.

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