rev 01 - 26/11/2012

DT5761

1 Channel 10 bit 4 GS/s Digitizer

CAEN
Tools for Discovery

User Manual
UM4271

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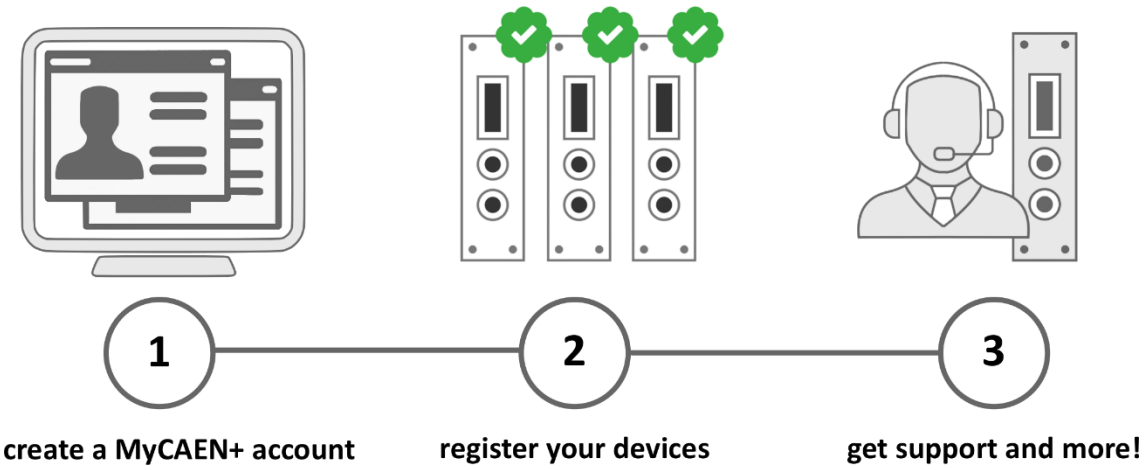

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PRELIMINARY

Technical Information Manual

Revision n. 1

26 November 2012

MOD. DT5761
1 CHANNEL 10 BIT
4GS/S DIGITIZER
MANUAL REV.1

NPO:
00100/09:5761x.MUTx/01

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CAEN declines all responsibility for damages or injuries caused by an improper use of the Modules due to negligence on behalf of the User. It is strongly recommended to read thoroughly the CAEN User's Manual before any kind of operation.

CE

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Disposal of the Product

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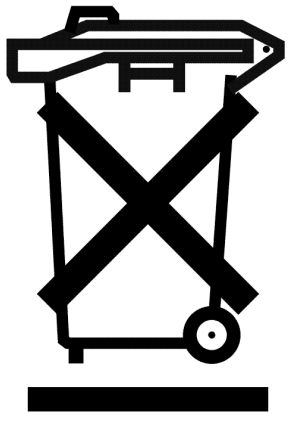

MADE IN ITALY : We stress the fact that all the boards are made in Italy because in this globalized world, where getting the lowest possible price for products sometimes translates into poor pay and working conditions for the people who make them, at least you know that who made your board was reasonably paid and worked in a safe environment. (this obviously applies only to the boards marked "MADE IN ITALY", we can not attest to the manufacturing process of "third party" boards).

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1. General description

1.1. Overview

Fig. 1.1: Mod. DT5761 Desktop Waveform Digitizer

The Mod. DT5761 is a Desktop module housing 1 Channel 10 bit 4 GS/s Digitizer with 1 Vpp dynamic range on single ended MCX coax. input connector.

The DC offset is adjustable via a 16-bit DAC on each channel in the ±0.5V range.

The module features a front panel clock In and a PLL for clock synthesis from internal/external references.
The sampled data are continuously written in a circular memory buffer. When the trigger occurs, the FPGA writes further N samples for the post trigger and freezes the buffer that can be read via USB or optical link. The acquisition can continue without dead time in a new buffer.

The channel has a SRAM memory buffer (7.2 MS/ch) divided in buffers of programmable size (1 - 1024). The readout (from USB or Optical link) of a frozen buffer is independent from the write operations in the active circular buffer (ADC data storage).
Zero suppression and data reduction algorithms allow substantial savings in data amount readout and processing, rejecting samples smaller than programmable thresholds.

Mod. DT5761 supports multi-board synchronization allowing all ADCs to be synchronized to a common clock source and ensuring Trigger time stamps alignment. When synchronized, all data will be aligned and coherent across multiple DT5761 boards.

The trigger signal can be provided via the front panel input as well as via the software, but it can also be generated internally with threshold auto-trigger capability

DT5761 houses USB 2.0 and optical link interfaces. USB 2.0 allows data transfers up to 30 MB/s. The Optical Link supports transfer rate of 80 MB/s, and offer daisy-chain capability. Therefore it is possible to connect up to 8/32 ADC modules to a single Optical Link Controller (Mod. A2818/A3818).

Table 1.1: Available items

Code	Description
WDT5761XAAAA	DT5761 - 1 Ch. 10 bit 4 GS/s Digitizer: 7.2MS/ch, EP3C16, SE
WA654XAAAAAA	A654 - Single Channel MCX to LEMO Cable Adapter
WA654K4AAAAA	A654 KIT4 - 4 MCX TO LEMO Cable Adapter
WA2818XAAAAA	A2818 - PCI Optical Link
WA3818AXAAAA	A3818 - PCIe 1 Optical Link
WA3818BXAAAA	A3818 - PCIe 2 Optical Link
WA3818CXAAAA	A3818 - PCIe 4 Optical Link
WAI2730XAAAA	AI2730 - Optical Fibre 30 m. simplex
WAI2720XAAAA	AI2720 - Optical Fibre 20 m. simplex
WAI2705XAAAA	AI2705 - Optical Fibre 5 m. simplex
WAI2703XAAAA	AI2703 - Optical Fibre 30cm. simplex
WAY2730XAAAA	AY2730 - Optical Fibre 30 m. duplex
WAY2720XAAAA	AY2720 - Optical Fibre 20 m. duplex
WAY2705XAAAA	AY2705 - Optical Fibre 5 m. duplex

1.2. Block Diagram

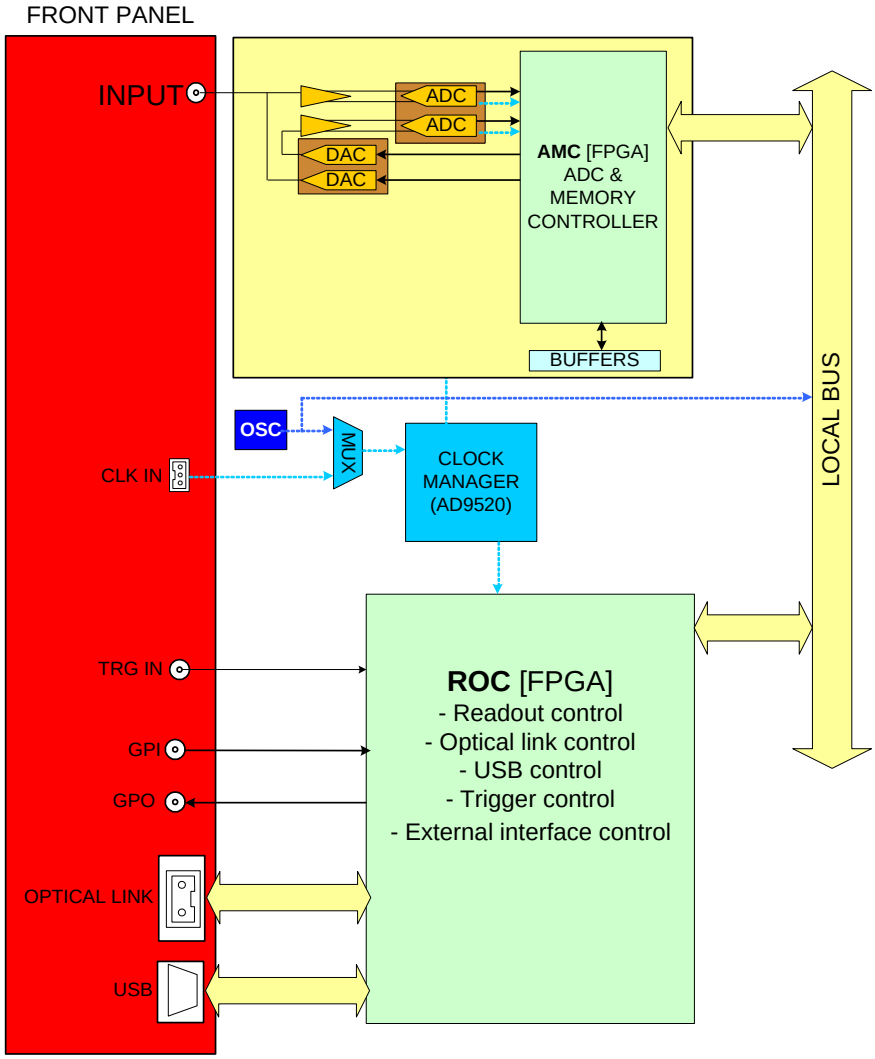

Fig. 1.1: Mod. DT5761 Block Diagram

The function of each block will be explained in detail in the subsequent sections.

2. Technical specifications

2.1. Packaging and Compliancy

The unit is a Desktop module housed in a 154x50x164 mm^3 alloy box.

2.2. Power requirements

The module is powered by the external AC/DC stabilized power supply provided with the digitizer and included in the delivered kit.

2.3. Front and Back Panel

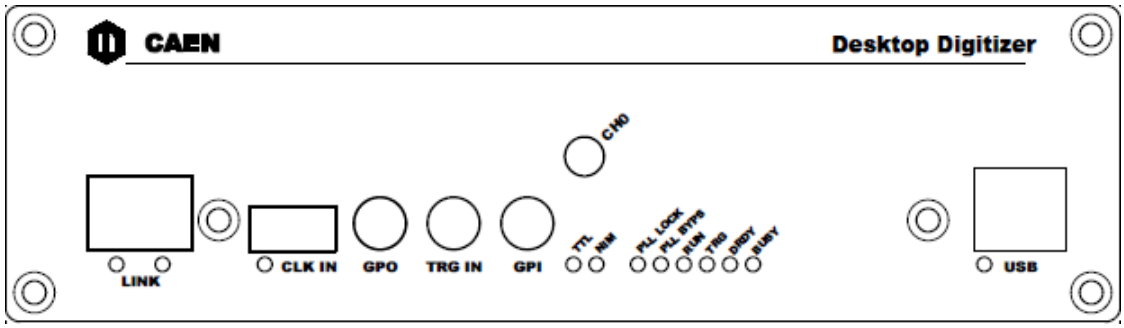

Fig. 2.1: Mod. DT5761 front panel

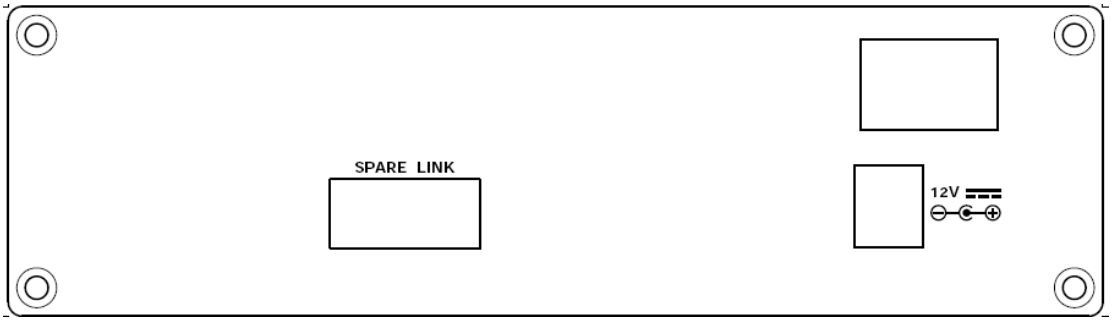

Fig. 2.2: Mod. DT5761 back panel

2.4. External connectors

2.4.1. ANALOG INPUT connectors

Fig. 2.3: MCX connector

Function:
Analog input, single ended, input dynamics: 1Vpp Zin=50Ω
Mechanical specifications:
MCX connector (CS 85MCX-50-0-16 SUHNER)
Absolute max analog input voltage: 3Vpp (with Vrail max +3V or -3V) for any DAC offset in single ended configuration

2.4.2. CONTROL connectors

Function:
TRG IN: External trigger input (NIM/TTL, Zin= 50Ω)
Mechanical specifications:
00-type LEMO connectors

2.4.3. ADC REFERENCE CLOCK connectors

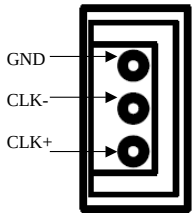

Fig. 2.4: AMP CLK IN Connector

Function:
CLK IN: External clock/Reference input, AC coupled (diff. LVDS, ECL, PECL, LVPECL, CML), Zdiff= 100Ω.
Mechanical specifications:
AMP 3-102203-4 AMP MODUII

2.4.4. Digital I/O connectors

Function:
- GPI: programmable front panel input (NIM/TTL, Zin=50Ω)
- GPO: programmable front panel output (NIM/TTL across 50Ω); used as output for trigger propagation

Mechanical specifications:
00-type LEMO connectors

2.4.5. Optical LINK connector

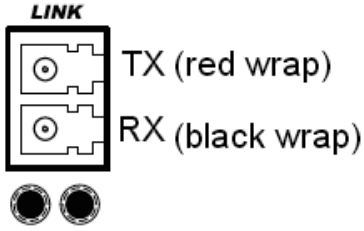

Fig. 2.5: LC Optical Connector

Mechanical specifications:
LC type connector; to be used with Multimode 62.5/125µm cable with LC connectors on both sides
Electrical specifications:
Optical link for data readout and slow control with transfer rate up to 80MB/s; daisy chainable.

2.4.6. USB Port

Mechanical specifications:
B type USB connector
Electrical specifications:
USB 2.0 and USB 1.1 compliant

2.4.7. 12V External

Mechanical specifications:
RAPC722X SWITCHCRAFT PCB DC Power Jack
Electrical specifications:
+12V DC Input

2.4.8. Spare Link

Mechanical specifications:
3M-7610-5002 connector
Electrical specifications:
T.B.D.

2.5. Other components

2.5.1. Displays

The front panel hosts the following LEDs:

Table 2.1: Front panel LEDs

Name:	Colour:	Function:
CLK_IN	green	External clock enabled.
NIM	green	Standard selection for GPO, TRG IN, GPI.
TTL	green	Standard selection for GPO, TRG IN, GPI.
USB	green	Data transfer activity
LINK	green/yellow	Network present; Data transfer activity
PLL _LOCK	green	The PLL is locked to the reference clock
PLL _BYPS	green	The reference clock drives directly ADC clocks; the PLL circuit is switched off and the PLL_LOCK LED is turned off.
RUN	green	RUN bit set (see § 5.18)
TRG	green	Triggers are accepted
DRDY	green	Event/data (depending on acquisition mode) are present in the Output Buffer
BUSY	red	All the buffers are full

2.6. Technical specifications table

Table 2.2: Mod. DT5761 technical specifications

Package	Desktop module, 154x50x164 mm^3 (WxHxD), Weight 680 gr
Analog Input	1 channel (MCX 50 Ohm) Single-ended Input range: 1 Vpp; Bandwidth: 1 GHz. Programmable DAC for Offset Adjust x ch., adjustment range: ±0.5V
Digital Conversion	Resolution: 10 bit; Sampling rate: 4 GS/s; multi board synchronization
ADC Sampling Clock generation	Two operating modes: - PLL mode - internal reference (50 MHz loc. oscillator). - PLL mode - external reference on CLK_IN (±100ppm tolerance).
Digital I/O	CLK_IN (AMP Modu II): - AC coupled differential input clock LVDS, ECL, PECL, LVPECL, CML (single ended NIM/TTL available) - Jitter<100ppm TRG_IN (LEMO 50 Ohm, NIM/TTL) GPI/GPO (LEMO 50 Ohm, NIM/TTL)
Memory Buffer	7.2 MSample/ch; Multi Event Buffer with independent read and write access. Programmable event size and pre-post trigger. Divisible into 1÷ 1024 buffers. Readout of Frozen buffer independent from write operations in the active buffer (ADC data storage)
Trigger	Common Trigger - TRG_IN (External signal) - Software (from USB or Optical Link) - Self trigger (Internal threshold auto-trigger) Daisy chain trigger propagation among boards (using GPO)
Trigger Time Stamp	32bit - 4ns (34s range)
USB interface	USB2.0 compliant Up to 30 MB/s transfer rate
Optical Link	CAEN proprietary protocol, up to 80 MB/s transfer rate, Daisy chainable: it is possible to connect up to 8/32 ADC modules to a single Optical Link Controller (Mod. A2818/A3818).
Upgrade	Firmware can be upgraded via Optical Link or USB interface
Multi Modules Synchronization	Allows data alignment and consistency across multiple modules: - CLK_IN allows the synchronization to a common clock source - GPI ensures Trigger time stamps and start acquisition times alignment
Electrical Power	Voltage range: 12 ± 10% Vdc
Software	General purpose C and LabView Libraries Demo and Software Tools for Windows and Linux

3. Functional description

3.1. Analog Input

Input dynamics is 1V (Zin= 50 Ω). 16bit DAC allow to add up to ±0.5V DC offset to preserve the full dynamic range also with unipolar positive or negative input signals. The input bandwidth ranges from DC to 1 GHz.

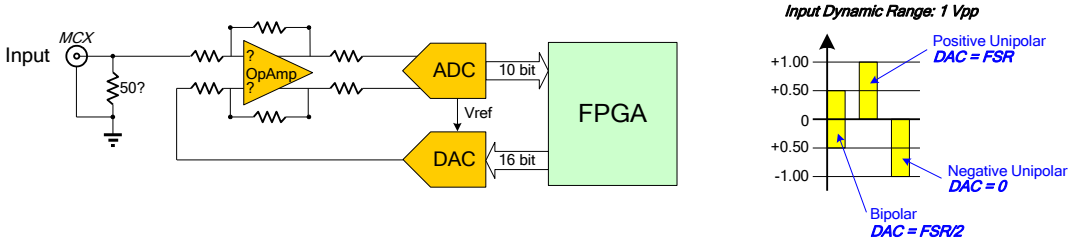

Fig. 3.1: Input diagram

3.2. Clock Distribution

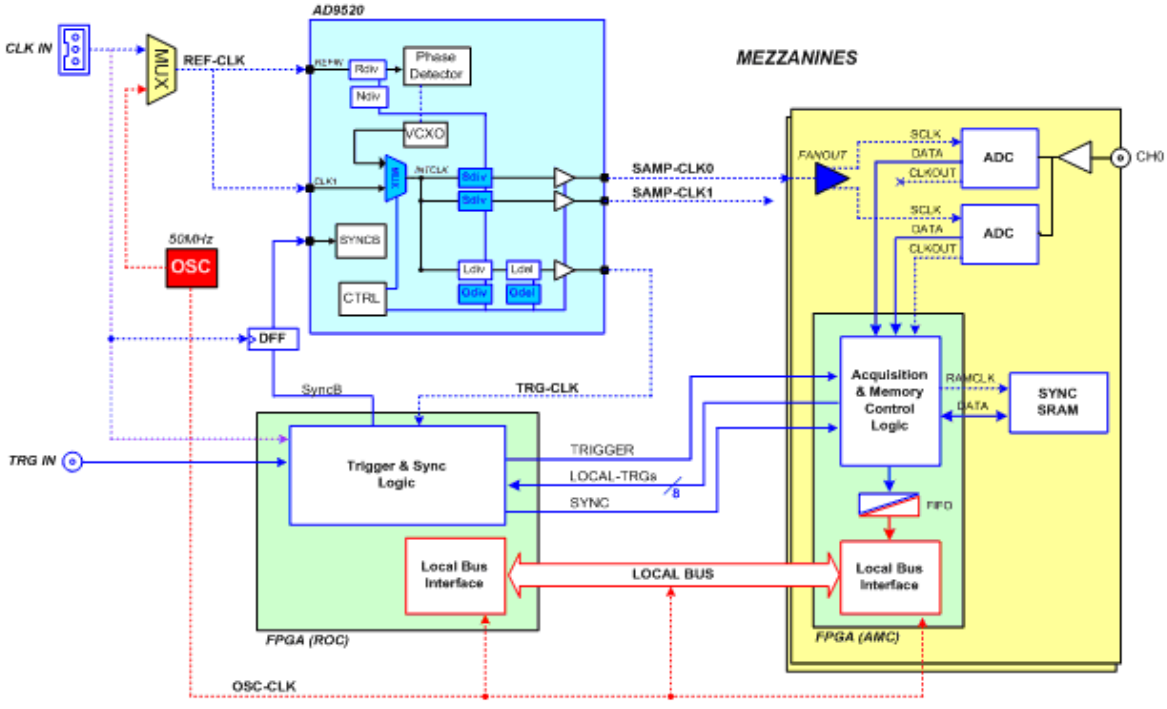

Fig. 3.2: Clock distribution diagram

The module clock distribution takes place on two domains: OSC-CLK and REF-CLK; the former is a fixed 50MHz clock provided by an on board oscillator, the latter provides the ADC sampling clock.
OSC-CLK handles Local Bus (communication between motherboard and mezzanine boards; see red traces in the figure above).
REF-CLK handles ADC sampling, trigger logic, acquisition logic (samples storage into RAM, buffer freezing on trigger) through a clock chain. Such domain can use either an external (via front panel signal) or an internal (via local oscillator) source, in the latter case OSC-CLK and REF-CLK will be synchronous (the operation mode remains the same anyway).
DT5761 uses an integrated phase-locked-loop (PLL) and clock distribution device (AD9520). It is used to generate the sampling clock for ADCs (SAMP-CLK0/SAMP-CLK1) and trigger logic synchronization clock (TRG-CLK).
Both clocks can be generated from the internal oscillator or from external clock input (CLK IN). By default, board uses the internal clock as PLL reference (REF-CLK). External clock can be selected by register access. AD9520 configuration can be changed and stored into non-volatile memory. AD9520 configuration change is primarily intended to be used for external PLL reference clock frequency change:
DT5761 locks to an external 50 MHz clock with default AD9520 configuration.

Please contact CAEN (support.frontend@caen.it) for more information and configuration tools.

Refer also to AD9520 data sheet for more details:
http://www.analog.com/UploadedFiles/Data_Sheets/AD9520.pdf

3.2.1. Trigger Clock

TRG-CLK signal has a frequency equal to 1/8 of SAMP-CLK; therefore a 32 samples "uncertainty" occurs over the acquisition window.

3.3. Acquisition Modes

3.3.1. Channel calibration

Whenever the operating temperature changes significantly, in order to achieve the best performance, a new self calibration procedure should be performed after the ADCs have stabilized their operating temperature.
The calibration is performed through a write access to Broadcast ADC Configuration (see § 5.16).

Self calibration procedure:
- Set Broadcast ADC Configuration register bit [1] = 0;
- Set Broadcast ADC Configuration register bit [1] = 1. The self calibration process will start and the registers 0x1n88 (n = 0,1,2,3) bit [6] will be set to 0. This means that the channels calibration is running;
- Polling on registers 0x1n88 (n = 0,1,2,3) until the bit [6] all of them return to 1 (few milliseconds). This means that the channels calibration is ended;
- Set again the Broadcast ADC Configuration register bit [1] = 0. The self calibration procedure is finished.

3.3.2. Acquisition run/stop

The acquisition can be started in two ways, according to Acquisition Control register bit 0 setting (see § 5.16):
- setting the RUN/STOP bit (bit 2) in the Acquisition Control register (bit 0 of Acquisition Control must be set to REGISTER-CONTROLLED RUN MODE)
- driving GPI signal high (bit 0 of Acquisition Control must be set to 1, GPI CONTROLLED RUN MODE)

Subsequently acquisition is stopped either:
- resetting the RUN/STOP bit (bit 2 in the Acquisition Control register (bit 0 of Acquisition Control must be set to REGISTER-CONTROLLED RUN MODE)
- driving GPI signal low (bit 0 of Acquisition Control set to 1, GPI CONTROLLED RUN MODE)

3.3.3. Acquisition Triggering: Samples and Events

When the acquisition is running, a trigger signal allows to:

- store the 32 bit counter (represents a time reference) of the Trigger Time Tag (TTT), that runs at 1/32 of the sampling clock frequency; actually the capture of the trigger takes place every 2 clock cycles, thus the time resolution of the Trigger Time Tag is 2 clock cycles (16 ns). This means that the LSB of the TTT is always 0.
- increment the EVENT COUNTER (see § 5.25)
- fill the active buffer with the pre/post-trigger samples, whose number is programmable (Acquisition window width, § 5.22), freezing then the buffer for readout purposes, while acquisition continues on another buffer

Table 3.1: Buffer Organization

REGISTER (see § 0)	BUFFER NUMBER	SIZE of one BUFFER (samples)
		SRAM @ 4 GS/s
0x00	1	7.2M
0x01	2	3.6M
0x02	4	1.8M
0x03	8	896k
0x04	16	448k
0x05	32	224k
0x06	64	112k
0x07	128	56k
0x08	256	28k
0x09	512	14k
0x0A	1024	7k

An event is therefore composed by the trigger time tag, pre- and post-trigger samples and the event counter.
Overlap between “acquisition windows” may occur (a new trigger occurs while the board is still storing the samples related to the previous trigger); this overlap can be either rejected or accepted (programmable via software).
If the board is programmed to accept the overlapped triggers, as the “overlapping” trigger arrives, the current active buffer is filled up, then the samples storage continues on the subsequent one.

In this case events will not have all the same size (see figure below).

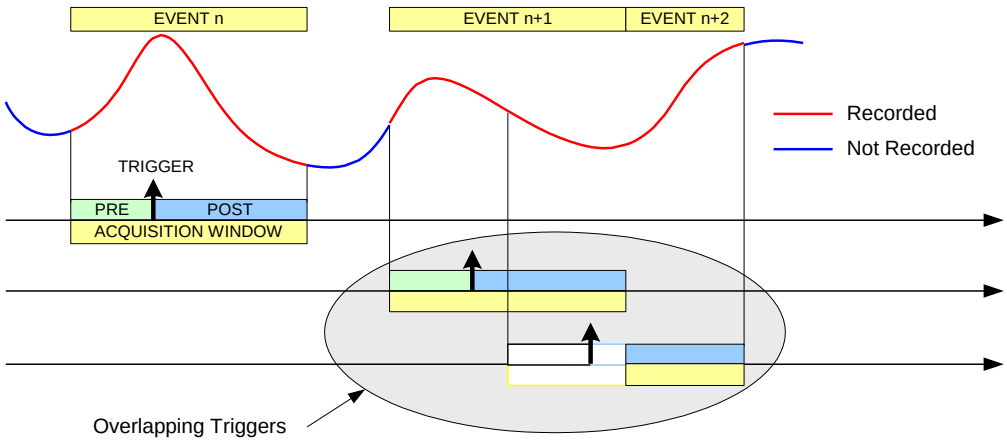

Fig. 3.3: Trigger Overlap

A trigger can be refused for the following causes:
- acquisition is not active
- memory is FULL and therefore there are no available buffers
- the required number of samples for building the pre-trigger of the event is not reached yet; this happens typically as the trigger occurs too early either with respect to the RUN_ACQUISITION command (see § 3.3.2) or with respect to a buffer emptying after a MEMORY_FULL status
- the trigger overlaps the previous one and the board is not enabled for accepting overlapped triggers

As a trigger is refused, the current buffer is not frozen and the acquisition continues writing on it. The Event Counter can be programmed in order to be either incremented or not. If this function is enabled, the Event Counter value identifies the number of the triggers sent (but the event number sequence is lost); if the function is not enabled, the Event Counter value coincides with the sequence of buffers saved and readout.

3.3.3.1. Custom size events

It is possible to make events with a number of Memory locations, which depends on Buffer Organization register setting (see § 0) smaller than the default value. One memory location contains 7 ADC samples and the maximum number of memory locations N_{LOC} is NS = 256K/Nblocks.
Smaller N_{LOC} values can be achieved by writing the number of locations N_{LOC} into the Custom Size register (see § 5.14).
N_{LOC} = 0 means “default size events”, i.e. the number of memory locations is the maximum allowed.
N_{LOC} = N1means that one event will be made of 28*N1.

3.3.4. Event structure

An event is structured as follows:
- Header (4 32-bit words)
- Data (variable size)

The event can be readout either via USB or Optical Link; data format is 32 bit long word.

3.3.4.1. Header

It is composed by four words, namely:
- Size of the event (number of 32 bit long words)
- Bit24; data format: 0
- Event Counter: It is the trigger counter; it can count either accepted triggers only, or all triggers (see § 5.14).
- Trigger Time Tag: It is a 32 bit counter (31 bit count + 1 overflow bit), which is reset as acquisition starts and is incremented at each sampling clock hit. It is the trigger time reference.

3.3.4.2. Samples

Bit [31,30] are useful to acknowledge how many samples are in the last word of an event (1 to 3); example in § 3.3.4.3. shows a case with two samples in the last word.

3.3.4.3. Event format example

The event format is shown in the following figure:

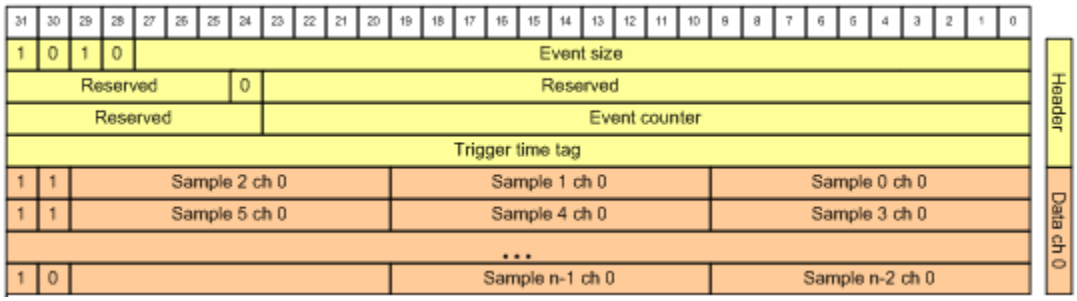

Fig. 3.4: Event Organization

3.4. Trigger management

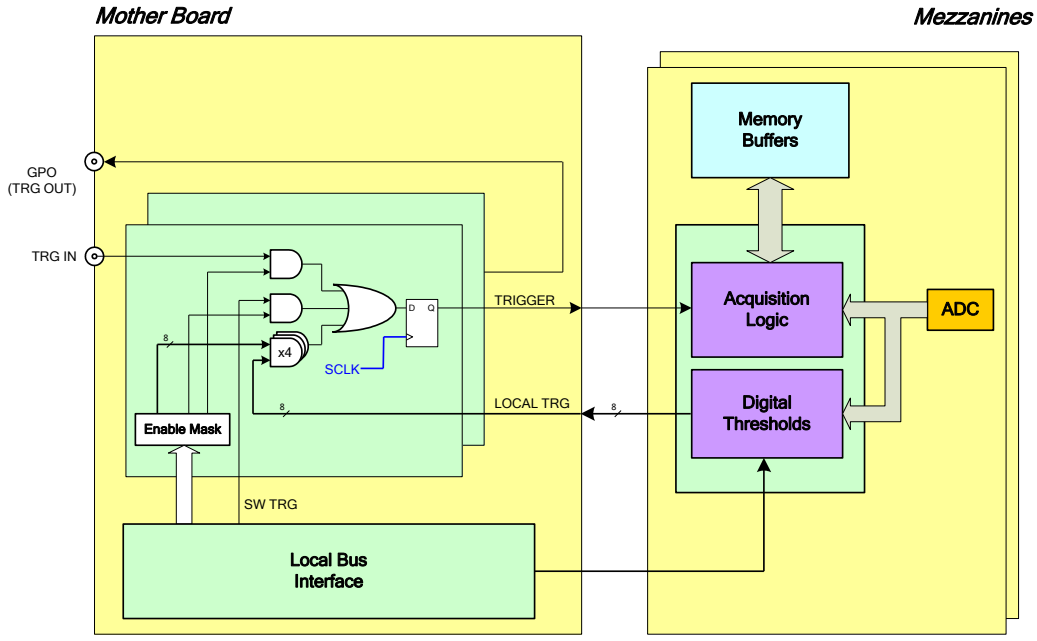

Fig. 3.5: Block diagram of Trigger management

Several trigger sources are available:

3.4.1. External trigger

External trigger can be NIM/TTL signal on LEMO front panel connector, 50 Ohm impedance. The external trigger is synchronised with the internal clock (see § 3.2.1); if External trigger is not synchronised with the internal clock, a one clock period jitter occurs.

3.4.2. Software trigger

Software trigger are generated INTERNALLY (write access in the relevant register, see § 5.19).

3.4.3. Local channel auto-trigger

The channel can generate a local trigger as the digitized signal exceeds the Vth threshold (ramping up or down, depending on Channel Configuration settings see § 5.9). The Vth digital threshold, the edge type are programmable via register accesses, see § 5.3.
N.B.: the local trigger signal does not start directly the event acquisition on the channel; such signal is propagated to the central logic which produces the global trigger (see § 3.4.4).

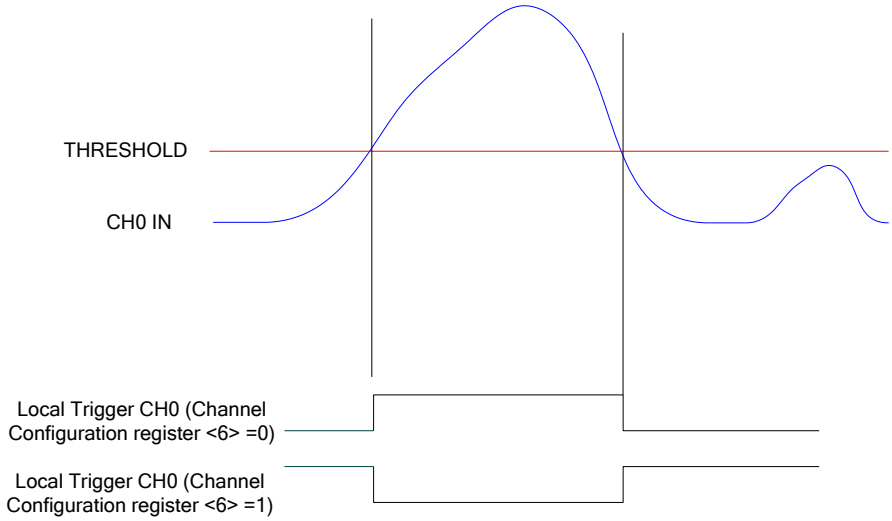

Fig. 3.6: Local trigger generation

3.4.4. Trigger distribution

The OR of all the enabled trigger sources, after being synchronised with the internal clock, becomes the global trigger of the board and is fed in parallel to the channel, which stores an event.
A Trigger Out is also generated on the relevant front panel GPO connector (NIM or TTL), and allows to extend the trigger signal to other boards.
For example, in order to start the acquisition as the channel ramps over threshold, the Local Trigger must be enabled as Trigger Out, the Trigger Out must then be fed to a Fan Out unit; the obtained signal has to be fed to the External Trigger Input of all the boards in the set up (including the board which generated the Trigger Out signal).

3.5. Data transfer capabilities

The board can be accessed by using software drivers and libraries developed by CAEN. Single 16/32 register read/write cycles, multi read cycles and block transfers are supported by the provided library (please consult the relevant documentation for details)
Sustained readout rate is up to 60 MB/s for optical link, using block transfers, and up to 30 MB/s for a USB 2.0 link, using block transfers as well.

3.6. Events readout

Event readout is done by accessing the Event Readout Buffer (see § 5.1), a FIFO (First-In First-Out) memory that can be accessed into the 0x0000-0x0FFC address space.
Data transfer is always aligned to the programmed number N of events; let X the size of the event expected or read from dedicated register:

- If the event size is known, a read cycle equal to N*X will return all data without interruptions.
- If the number of data read from the Event Readout Buffer is higher than N*X, transfer will be terminated anyway by DT5761 at the end of N*X data.
- If the event size X is unknown (for example in case of overlapping triggers), there are two cases:
  - data transfer ≤ N*X : all data will be returned.
  - data transfer > N*X : only N*X data will be returned.

Once an event is read, the corrisponding acquisition buffers are available to store new data.
During readout, the board can continue to store events in memory up to the maximum number of programmed buffers available; the acquisition process is therefore "dead-timeless": event storage is only interrupted if the combination of trigger and readout rate causes a memory full situation: all acquisition buffers are used and they have not been read yet.
In order to exploit the maximum readout rate allowed by the communication path (USB or optical link), it is suggested to perform block transfer read cycles of at least N*X data with N set to its maximum value, whether possible.

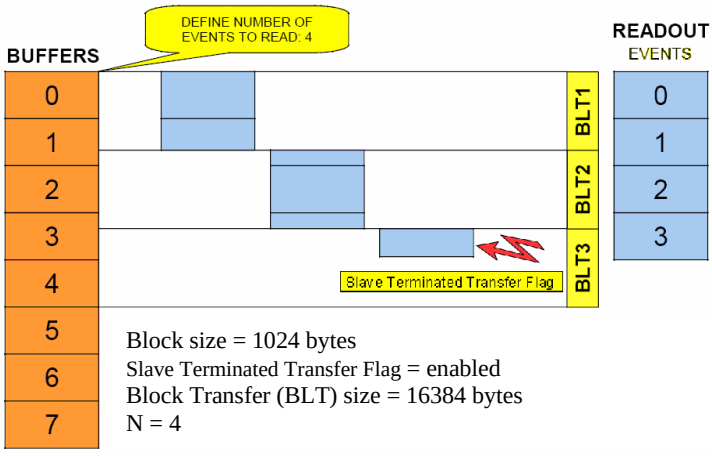

Fig. 3.7: Example of block transfer readout

3.7. Optical Link and USB access

The board houses a USB2.0 compliant port, providing a transfer rate up to 30 MB/s, and a daisy chainable Optical Link able to transfer data at 80 MB/s; the latter allows to connect up to eight DT5761 to a single Optical Link Controller: for more information, see www.caen.it (path: Products / Front End / PCI/PCIe / Optical Controller)
The parameters for read/write accesses via optical link are Address Modifier, Base Address, data Width, etc; wrong parameter settings cause Bus Error.
Control Register bit 3 allows to enable the module to broadcast an interrupt request on the Optical Link; the enabled Optical Link Controllers propagate the interrupt on the PCI bus as a request from the Optical Link is sensed.

4. Software tools

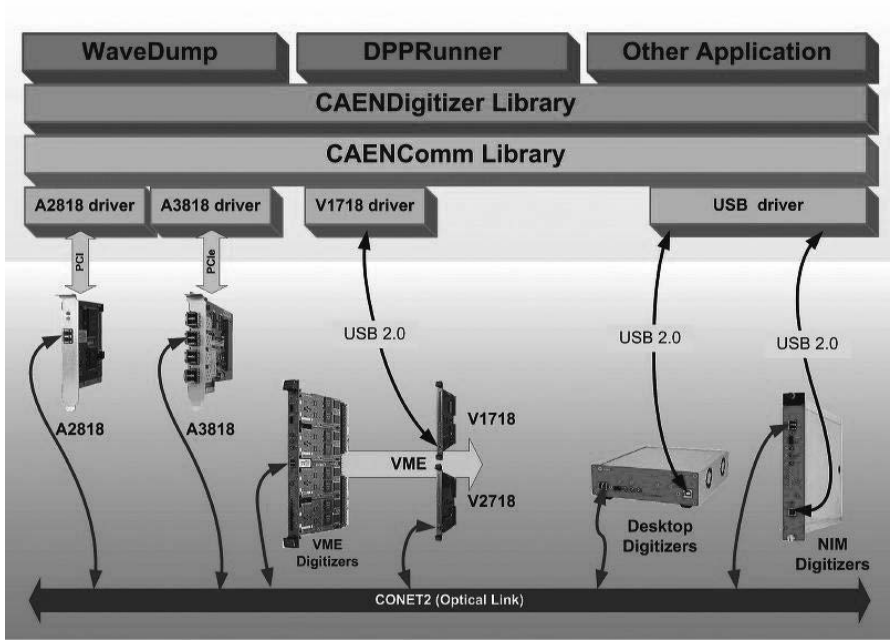

Fig. 4.1: Block diagram of the software layers

CAEN provides drivers for both the physical communication channels (USB and the proprietary CONET Optical Link managed by the A2818 PCI card or A3818 PCIe cards; see § 6.4), a set of C and LabView libraries, demo applications and utilities. Windows and Linux are both supported. The available software is the following:

- **CAENComm** library contains the basic functions for access to hardware; the aim of this library is to provide a unique interface to the higher layers regardless the type of physical communication channel. The CAENComm requires the CAENVMELib library to be installed even in the cases where the VME is not used.
- **CAENDigitizer** is a library of functions designed specifically for the digitizer family and it supports also the boards running special DPP (Digital Pulse Processing) firmware. The purpose of this library is to allow the user to open the digitizer, program it and manage the data acquisition in an easy way: with few lines of code the user can make a simple readout program without the necessity to know the details of the registers and the event data format. The CAENDigitizer library implements a common interface to the higher software layers, masking the details of the physical channel and its protocol, thus making the libraries and applications that rely on the CAENDigitizer independent from the physical layer. The library is based on the CAENComm library that manages the communication at low level (read and write access). CAENVMELib and CAENComm libraries must be already installed on the host PC before installing the CAENDigitizer; however, both CAENVMELib and CAENComm libraries are completely transparent to the user.

- **WaveDump** is a Console application that allows to program the digitizer (according to a text configuration file that contains a list of parameters and instructions), to start the acquisition, read the data, display the readout and trigger rate, apply some post processing (such as FFT and amplitude histogram), save data to a file and also plot the waveforms using the external plotting tool "gnuplot", available on internet for free. This program is quite basic and has no graphics but it is an excellent example of C code that demonstrates the use of libraries and methods for an efficient readout and data analysis. **NOTE:** WaveDump does not work with digitizers running DPP firmware. The users who intend to write the software on their own are suggested to start with this demo and modify it according to their needs. For more details please see the WaveDump User Manual and Quick Start Guide (Doc nr.: UM2091, GD2084).

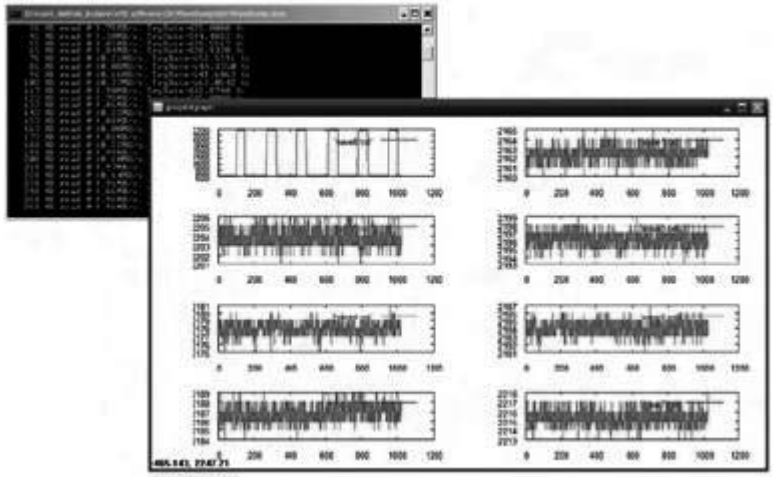

Fig. 4.2: WaveDump output waveforms

- **CAENScope** is a fully graphical program that implements a simple oscilloscope: it allows to see the waveforms, set the trigger thresholds, change the scales of time and amplitude, perform simple mathematical operations between the channels, save data to file and other operations. CAENscope is provided as an executable file; the source codes are not distributed. **NOTE:** CAENScope does not work with digitizers running DPP firmware and it is not compliant with x742 digitizer family. For more details please see the CAENScope Quick Start Guide GD2484.

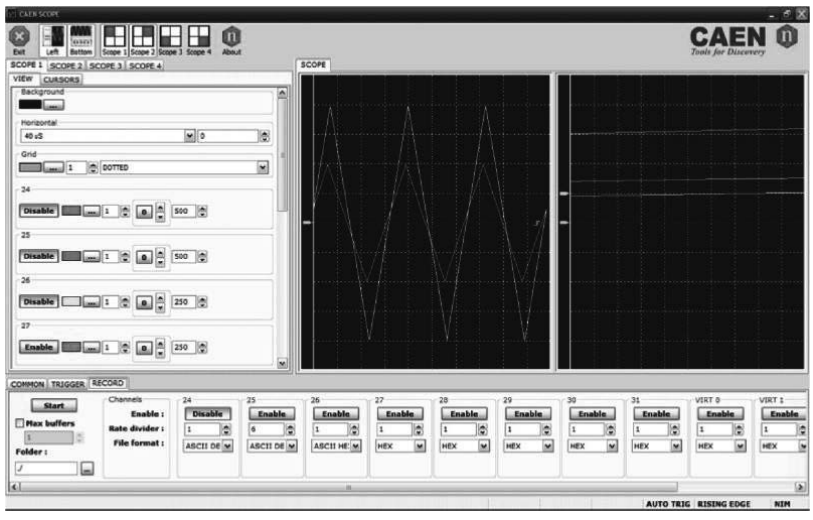

Fig. 4.3: CAENScope oscilloscope tab

- **CAENUpgrader** is a software composed of command line tools together with a Java Graphical User Interface (for Windows and Linux OS). CAENUpgrader allows in few easy steps to upload different firmware versions on CAEN boards, to upgrade the VME digitizers PLL, to get board information and to manage the firmware license. CAENUpgrader requires the installation of 2 CAEN libraries (CAENComm, CAENVMELib) and Java SE6 (or later). CAENComm allows CAENUpgrader to access target boards via USB or via CAEN proprietary CONET optical link.

Fig. 4.4: CAENUpgrader Graphical User Interface

- **DPP Control Software** is an application that manages the acquisition in the digitizers which have DPP firmware installed on it. The program is made of different parts: there is a GUI whose purpose is to set all the parameters for the DPP and for the acquisition; the GUI generates a textual configuration file that contains all the parameters. This file is read by the Acquisition Engine (**DPPrunner)**, which is a C console application that programs the digitizer according to the parameters, starts the acquisition and manage the data readout. The data, that can be waveforms, time stamps, energies or other quantities of interest, can be saved to output files or plotted using gnuplot as an external plotting tool, exactly like in WaveDump. NOTE: so far DPP Control Software is developed for Mod. x724 and Mod. x720 digitizer series.

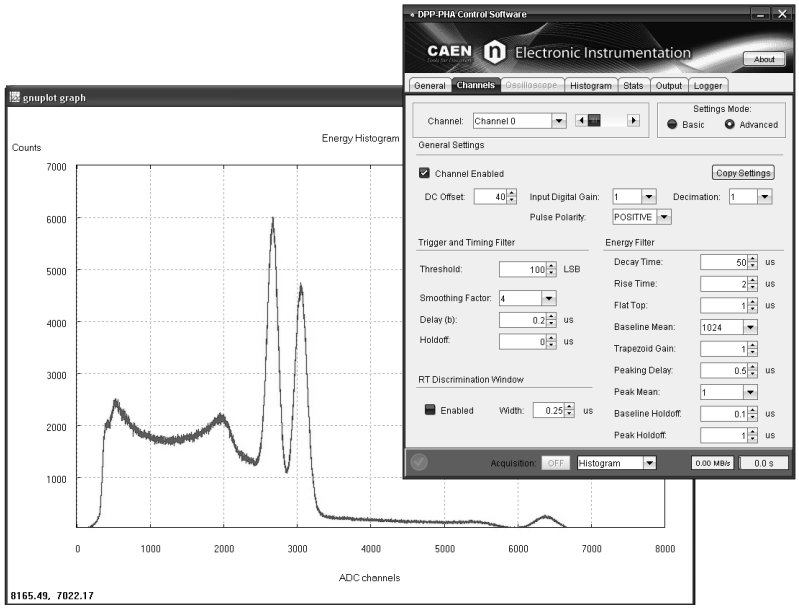

Fig. 4.5: DPP Control Software Graphical User Interface and Energy plot

5. Board internal registers

The following sections will describe in detail the registers (accessible via software in D32 mode) content.
N.B.: bit fields that are not described in the register bit map are reserved and must not be over written by the User.

5.1. Registers address map

Table 5.1: Address Map for the Model DT5761

REGISTER NAME	ADDRESS	MODE	H_RES	S_RES	CLR
EVENT READOUT BUFFER	0x0000-0x0FFC	R	X	X	X
Channel THRESHOLD	0x1080	R/W	X	X	
Channel STATUS	0x1088	R	X	X	
Channel AMC FPGA FIRMWARE REVISION	0x108C	R			
Channel BUFFER OCCUPANCY	0x1094	R	X	X	X
Channel DAC	0x1098	R/W	X	X	
Channel ADC CONFIGURATION	0x109C	R/W	X	X	
Channel TEMPERATURE MONITOR	0x10A8	R/W	X	X	
CHANNEL CONFIGURATION	0x8000	R/W	X	X	
CHANNEL CONFIGURATION BIT SET	0x8004	W	X	X	
CHANNEL CONFIGURATION BIT CLEAR	0x8008	W	X	X	
BUFFER ORGANIZATION	0x800C	R/W	X	X	
BUFFER FREE	0x8010	R/W			
CUSTOM SIZE	0x8020	R/W	X	X	
BROADCAST ADC CONFIGURATION	0x809C	R/W	X	X	
ACQUISITION CONTROL	0x8100	R/W	X	X	
ACQUISITION STATUS	0x8104	R			
SW TRIGGER	0x8108	W			
TRIGGER SOURCE ENABLE MASK	0x810C	R/W	X	X	
FRONT PANEL TRIGGER OUT ENABLE MASK	0x8110	R/W	X	X	
POST TRIGGER SETTING	0x8114	R/W	X	X	
FRONT PANEL I/O CONTROL	0x811C	R/W	X	X	
ROC FPGA FIRMWARE REVISION	0x8124	R			
EVENT STORED	0x812C	R	X	X	X
BOARD INFO	0x8140	R			
EVENT SIZE	0x814C	R	X	X	X
CONTROL	0xEF00	R/W	X		
STATUS	0xEF04	R			
INTERRUPT STATUS ID	0xEF14	R/W	X		
INTERRUPT EVENT NUMBER	0xEF18	R/W	X	X	
BLT EVENT NUMBER	0xEF1C	R/W	X	X	
SCRATCH	0xEF20	R/W	X	X	
SW RESET	0xEF24	W			
SW CLEAR	0xEF28	W			
FLASH ENABLE	0xEF2C	R/W	X		
FLASH DATA	0xEF30	R/W	X		

REGISTER NAME	ADDRESS	MODE	H_RES	S_RES	CLR
CONFIGURATION RELOAD	0xEF34	W			
CONFIGURATION ROM	0xF000-0xF088	R			

5.2. Configuration ROM (0xF000-0xF088; r)

The following registers contain some module's information, they are D32 accessible (read only):

- **OUI**: manufacturer identifier (IEEE OUI)
- **Version**: purchased version
- **Board ID**: Board identifier
- **Revision**: hardware revision identifier
- **Serial MSB**: serial number (MSB)
- **Serial LSB**: serial number (LSB)

Table 5.2: ROM Address Map for the Model DT5761

Description	Address	Content
checksum	0xF000	*0xA4*
checksum_length2	0xF004	0x00
checksum_length1	0xF008	0x00
checksum_length0	0xF00C	0x20
constant2	0xF010	0x83
constant1	0xF014	0x84
constant0	0xF018	0x01
c_code	0xF01C	0x43
r_code	0xF020	0x52
oui2	0xF024	0x00
oui1	0xF028	0x40
oui0	0xF02C	0xE6
vers	0xF030	0x60
board2	0xF034	0x02
board1	0xF038	0x16
board0	0xF03C	0x81
revis3	0xF040	*0x00*
revis2	0xF044	*0x00*
revis1	0xF048	*0x00*
revis0	0xF04C	*0x00*
sernum1	0xF080	
sernum0	0xF084	
VCXO type	0xF088	0x00 (AD9520-3)

These data are written into one Flash page; at Power ON the Flash content is loaded into the Configuration RAM, where it is available for readout.

5.3. Channel Threshold (0x1080; r/w)

Bit	Function
[9:0]	Threshold Value for Trigger Generation

The channel can generate a local trigger as the digitized signal exceeds the Vth threshold. This register allows to set Vth (LSB=input range/10bit); see also § 3.4.3

5.4. Channel Status (0x1088; r)

Bit	Function
[8]	Over temperature flag 0 = Ch temperature OK 1 = Ch Over temperature
[7]	Power down flag 0 = Ch Power OK 1 = Ch Power Down
[6]	Calibrating: 1 = calibration done 0 = calibration in progress
[5]	Buffer free error: 1 = trying to free a number of buffers too large
[3,4]	reserved
[2]	Channel DAC / ADC bus Busy (see § 5.7) 1 = Busy 0 = Ready
[1]	Memory empty
[0]	Memory full

5.5. Channel AMC FPGA Firmware (0x108C; r)

Bit	Function
[31:16]	Revision date in Y/M/DD format
[15:8]	Firmware Revision (X)
[7:0]	Firmware Revision (Y)

Bits [31:16] contain the Revision date in Y/M/DD format.
Bits [15:0] contain the firmware revision number coded on 16 bit (X.Y format).
Example: revision 1.3 of 12th June 2007 is: 0x7612103

5.6. Channel Buffer Occupancy (0x1094; r)

Bit	Function
[10:0]	Occupied buffers (0..1024)

5.7. Channel DAC (0x1098; r/w)

Bit	Function
[15:0]	DAC Data

Bits [15:0] allow to define a DC offset to be added the input signal in the ±0.5V range. When Channel n Status bit 2 is set to 0, DC offset is updated (see § 5.4).

5.8. Channel ADC Configuration (0x109C; w)

Bit	Function
[1]	Calibration
[0]	Power Down configuration 0 = Ch Power OK 1 = Ch Power Down

This register allows to pilot the relevant ADC signal.

5.9. Channel Temperature Monitor (0x10A8; r)

Bit	Function
[7:0]	Monitored Temperature (°C)

This registers allow to monitor the temperature of ADC chips.

5.10. Channel Configuration (0x8000; r/w)

Bit	Function
[6]	0 = Trigger Output on Input Over Threshold 1 = Trigger Output on Input Under Threshold allows to generate local trigger either on channel over or under threshold (see § 5.3)
[5]	reserved
[4]	0 = Memory Random Access 1 = Memory Sequential Access
[3]	0 = Test Pattern Generation Disabled 1 = Test Pattern Generation Enabled
[2]	reserved
[1]	0 = Trigger Overlapping Not Enabled 1 = Trigger Overlapping Enabled Allows to handle trigger overlap (see § 3.3.3)
[0]	reserved

This register allows to perform selective set/clear of the Channel Configuration register bits writing to 1 the corresponding set and clear bit at address 0x8004 (set) or 0x8008 (clear) see the following § 5.11 and 5.12. Default value is 0x10.

5.11. Channel Configuration Bit Set (0x8004; w)

Bit	Function
[12:0]	Bits set to 1 means that the corresponding bits in the Channel Configuration register are set to 1.

5.12. Channel Configuration Bit Clear (0x8008; w)

Bit	Function
[12:0]	Bits set to 1 means that the corresponding bits in the Channel Configuration register are set to 0.

5.13. Buffer Organization (0x800C; r/w)

Bit	Function
[3:0]	BUFFER CODE

The BUFFER CODE allows to divide the available Output Buffer Memory into a certain number of blocks, according to the table in § 3.3.3.
A write access to this register causes a Software Clear, see § 5.35. This register must not be written while acquisition is running.

5.14. Buffer Free (0x8010; r/w)

Bit	Function
[11:0]	N = Frees the first N Output Buffer Memory Blocks, see § 0

5.15. Custom Size (0x8020; r/w)

Bit	Function
[31:0]	0= Custom Size disabled N_{LOC} (≠0) = Number of memory locations per event (1 location = 28 samples @ 4GS/s)

This register must not be written while acquisition is running.

5.16. Broadcast ADC Configuration (0x809C; w)

Bit	Function
[1]	Calibration
[0]	Power Down; must always be 0

This register allows to pilot all the relevant ADC signal.

5.17. Acquisition Control (0x8100; r/w)

Bit	Function
[3]	0 = COUNT ACCEPTED TRIGGERS 1 = COUNT ALL TRIGGERS allows to reject overlapping triggers (see § 3.3.3)
[2]	0 = Acquisition STOP 1 = Acquisition RUN allows to RUN/STOP Acquisition
[1]	Reserved (set to 0)
[0]	0 = REGISTER-CONTROLLED RUN MODE 1 = GPI CONTROLLED RUN MODE

Bit [2] allows to Run and Stop data acquisition; when such bit is set to 1 the board enters Run mode and a Memory Reset is automatically performed. When bit [2] is reset to 0 the stored data are kept available for readout. In Stop Mode all triggers are neglected.
Bit [0] descritpion:
0 = REGISTER-CONTROLLED RUN MODE: multiboard synchronisation via GPI front panel signal

- RUN control: start/stop via set/clear of bit[2]
- GATE always active (Continuous Gate Mode)

1 = GPI CONTROLLED RUN MODE: Multiboard synchronisation via GPI front panel signal

- GPI works both as SYNC and RUN_START command
- GATE always active (Continuous Gate Mode)

5.18. Acquisition Status (0x8104; r)

Bit	Function
[8]	Board ready for acquisition (PLL and ADCs are synchronised correctly) 0 = not ready 1 = ready This bit should be checked after software reset to ensure that the board will enter immediatly run mode after RUN mode setting; otherwise a latency between RUN mode setting and Acquisition start might occur.
[7]	PLL Status Flag (see § 2.5.1): 0 = PLL loss of lock 1 = no PLL loss of lock NOTE: flag can be restored to 1 via read access to Status Register
[6]	PLL Bypass mode (see § 2.5.1): 0 = No bypass mode 1 = Bypass mode
[5]	Clock source: 0 = Internal 1 = External
[4]	EVENT FULL: it is set to 1 as the maximum nr. of events to be read is reached
[3]	EVENT READY: it is set to 1 as at least one event is available to readout
[2]	0 = RUN off 1 = RUN on
[1:0]	*reserved*

5.19. Software Trigger (0x8108; w)

Bit	Function
[31:0]	A write access to this location generates a trigger via software

5.20. Trigger Source Enable Mask (0x810C; r/w)

Bit	Function
[31]	0 = Software Trigger Disabled 1 = Software Trigger Enabled
[30]	0 = External Trigger Disabled 1 = External Trigger Enabled
[29:1]	*reserved*
[0]	0 = Channel 0 trigger disabled 1 = Channel 0 trigger enabled

This register enables the channel to generate a local trigger as the digitised signal exceeds the Vth threshold (see § 3.4.3).
EXTERNAL TRIGGER ENABLE (bit30) enables the board to sense TRG-IN signals
SW TRIGGER ENABLE (bit 31) enables the board to sense software trigger (see § 5.19).

5.21. Front Panel Trigger Out Enable Mask (0x8110; r/w)

Bit	Function
[31]	0 = Software Trigger Disabled 1 = Software Trigger Enabled
[30]	0 = External Trigger Disabled 1 = External Trigger Enabled
[29:1]	*reserved*
[0]	0 = Channel 0 trigger disabled 1 = Channel 0 trigger enabled

This register Bit0 enables the channel to generate a TRG_OUT front panel signal on GPO output as the digitised signal exceeds the Vth threshold (see § 3.4.3).
EXTERNAL TRIGGER ENABLE (bit30) enables the board to generate the TRG_OUT
SW TRIGGER ENABLE (bit 31) enables the board to generate TRG_OUT (see § 5.19).

5.22. Post Trigger Setting (0x8114; r/w)

Bit	Function
[31:0]	Post trigger value

The register value sets the number of post trigger samples. The number of post trigger samples is
$N_S = 4[(N_{PV} + N_{DEL}) \cdot 16 \pm 15]$
N_S = number of post trigger samples.
N_{PV} = PostTriggerValue = Content of this register.
N_{DEL} = ConstantLatency = constant number of samples added due to the latency associated to the trigger processing logic in the ROC FPGA; N_{DEL} is 4 with external trigger and 8 with internal trigger.

5.23. Front Panel I/O Control (0x811C; r/w)

Bit	Function
[15:2]	*reserved*
[1]	0= panel output signals (GPO) enabled 1= panel output signals (GPO) enabled in high impedance
[0]	0 = GPI/GPO/TRG-IN are NIM I/O Levels 1 = GPI/GPO/TRG-IN are TTL I/O Levels

5.24. ROC FPGA Firmware Revision (0x8124; r)

Bit	Function
[31:16]	Revision date in Y/M/DD format
[15:8]	Firmware Revision (X)
[7:0]	Firmware Revision (Y)

Bits [31:16] contain the Revision date in Y/M/DD format.
Bits [15:0] contain the firmware revision number coded on 16 bit (X.Y format).

5.25. Event Stored (0x812C; r)

Bit	Function
[31:0]	This register contains the number of events currently stored in the Output Buffer

This register value cannot exceed the maximum number of available buffers according to setting of buffer size register.

5.26. Board Info (0x8140; r)

Bit	Function
[15:8]	Memory size code (DT5761: 0x02)
[7:0]	Board Type (DT5761: 0x06)

5.27. Event Size (0x814C; r)

Bit	Function
[31:0]	Nr. of 32 bit words in the next event

5.28. Control (0xEF00; r/w)

Bit	Function
[7]	Reserved; must be set to 0, Release On Register Access (RORA) Interrupt mode
[6]	Reserved, must be set to 0
[5]	Reserved, must be set to 0
[4]	Reserved, must be set to 1
[3]	0 = interrupt disabled 1 = interrupt enabled
[2,1]	Reserved
[0]	Reserved (must be set to 0)

Interrupt request can be removed by accessing this register and disabling the active interrupt level

5.29. Status (0xEF04; r)

Bit	Function
[2]	0 = Slave Terminated Transfer Flag: no terminated transfer 1 = Slave Terminated Transfer Flag: one transfer has been terminated by DT5761 (unsupported register access or block transfer prematurely terminated in event aligned reaout)
[1]	0 = The Output Buffer is not FULL; 1 = The Output Buffer is FULL.
[0]	0 = No Data Ready; 1 = Event Ready

5.30. Interrupt Status ID (0xEF14; r/w)

Bit	Function
[31..0]	This register contains the STATUS/ID that the module places on the data stream during the Interrupt Acknowledge cycle

5.31. Interrupt Event Number (0xEF18; r/w)

Bit	Function
[9:0]	INTERRUPT EVENT NUMBER

If interrupts are enabled, the module generates a request whenever it has stored in memory a Number of events > INTERRUPT EVENT NUMBER

5.32. Block Transfer Event Number (0xEF1C; r/w)

Bit	Function
[15:0]	This register contains the number of complete events which has to be transferred via Block Transfer (see § 3.6).

5.33. Scratch (0xEF20; r/w)

Bit	Function
[31:0]	Scratch (*to be used to write/read words for test purposes*)

5.34. Software Reset (0xEF24; w)

Bit	Function
[31:0]	A write access to this location allows to perform a software reset

5.35. Software Clear (0xEF28; w)

Bit	Function
[31:0]	A write access to this location clears all the memories

5.36. Flash Enable (0xEF2C; r/w)

Bit	Function
[0]	Reserved for Firmware upgrade tool

5.37. Flash Data (0xEF30; r/w)

Bit	Function
[7:0]	Data to be serialized towards the SPI On board Flash

This register is handled by the Firmware upgrade tool.

5.38. Configuration Reload (0xEF34; w)

Bit	Function
[31:0]	A write access to this register causes a software reset, a reload of Configuration ROM parameters and a PLL reconfiguration.

6. Installation

6.1. Power ON sequence

To power ON the board follow this procedure:

1. connect the 12V dc power supply to the DT5761
2. power up the DT5761

6.2. Power ON status

At power ON the module is in the following status:

- the Output Buffer is cleared;
- registers are set to their default configuration

6.3. Firmware upgrade

The DT5761 firmware is stored onto on-board non-volatile memory. The board hosts one FPGA on the mainboard and two FPGAs on the mezzanine. The channel FPGAs firmware is identical. A unique file is provided that will updated all the FPGA at the same time.
The programming file has the extension .CFA (CAEN Firmware Archive) and is a sort of archive format file aggregating all the standard firmware files compatible with the same family of digitizers.
CFA and its name follows this general scheme:

x761_revX.Y_W.Z.CFA

where:

- x761 are all the boards the file is compliant to all the models of the 720 family (see Table 1.1).
- X.Y is the major/minor revision number of the mainboard FPGA.
- W.Z is the major/minor revision number of the channel FPGA.

CAEN provides a firmware upgrade tool (see § 4) that can be used with either USB or optical link paths. Firmware updates are available in the Digitizer web page, while the software package, application notes and user manual are available in the CAENUpgrader web page at www.caen.it; follow the instructions for installation and usage.

WARNING: in case of programming failures, the board hosts a backup image of factory firmware. Please contact CAEN at support.frontend@caen.it for instuctions in order to restore the backup image.

Once the board is successfully powered with backup firmware, the standard firmware image can be reprogrammed.

6.4. Drivers

DT5761 needs CAEN USB driver to be installed in order to use the USB communication channel:

- **Download** the driver package compliant to your Operating System (Windows or Linux) on CAEN web site in the 'Software/Firmware' area at the digitizer page.
- **Uncompress** the package to your host.
- **For Windows users:**
  - **Installer option:** with the hardware not connected, run the single installer file and complete the installation Wizard. Then, connect the hardware and the driver will be automatically find by the OS.
  - **Driver files option:** connect the hardware; then, perform the driver installation by pointing Windows to the folder where driver files have been extracted.
- **For Linux users:** follow the installation instructions inside the README file in the package.

The detailed procedure for Windows is described in the document "First Installation Guide to Desktop Digitizers & MCA" downloadable at www.caen.it in the digitizer web page.

Concerning the OPTICAL LINK communication channel, please refer to A2818 PCI card or A3818 PCIe cards User Manual for driver installation.

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