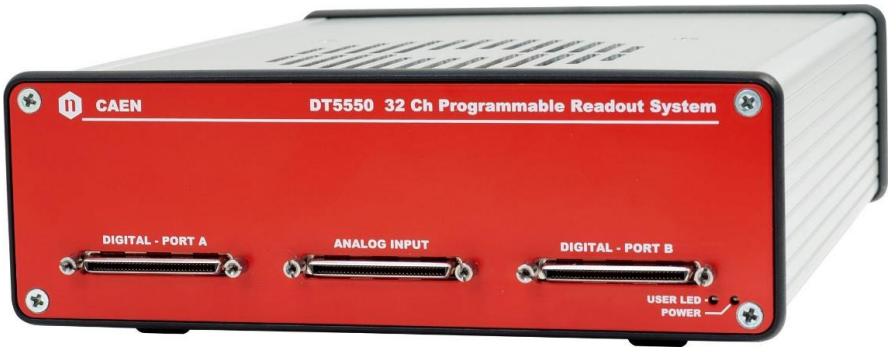
rev. 2 - June 5th, 2020

DT5550

32 Channels DAQ System with User Programmable FPGA and Sequencer



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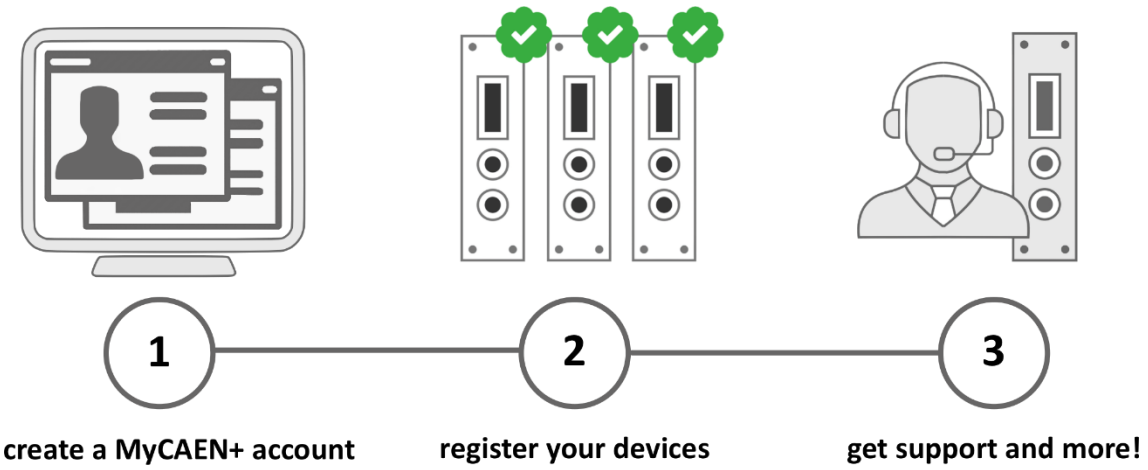

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Purpose of this User Manual

This User Manual contains the full description of the DT5550 32-Channels Programmable Readout System and a brief guide to the SCI-55X0 Readout Software.

Change Document Record

Date	Revision	Changes
August 31st, 2018	00	Initial release
February 6th, 2019	01	Modified **Settings Tab** Sec. and **Technical Support** Chap.
June 5th, 2020	02	Revised Chap. **SCI-55X0 Readout Software**

Symbols, abbreviated terms and notation

ADC	Analog to Digital Converter
FPGA	Field Programmable Gate Array
OS	Operating system

Reference Document

[RD1] GD6520 - SCI-Compiler Quick Start Guide

[RD2] UM6519 - SCI-Compiler User Manual

[RD3] DS6521 – DT5550AFE Datasheet

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1 Introduction

The DT5550 is a **Programmable 32-channel Digital Acquisition System** for physics application. It is one of the CAEN programmable board designed to help users in building a customized acquisition system fitting the needs of their detectors and experimental conditions. The applications of the DT5550 range from nuclear spectroscopy to ASICs readout, from neutron physics to Silicon Photmultipliers detection systems. The firmware, the readout software and some design files are distributed for free and open source so that the user can easily customize them in order to implement a full and complex experimental readout system on a single board.

The DT5550 is capable to manage simultaneously a large number of **digital** and **analog** signals to implement many functionalities required by physics experiments: signal digitization, complex trigger logic, Pulse Height Analysis with MCA capabilities, Time Tagging, Pulse Shape Discrimination, Scaler, Counters and so on. The large number of digital I/O and analog inputs make the DT5550 a solution suitable to readout most of the ASICs commonly used in physic, allowing the user to minimize the effort in designing a readout system (only a simple adapter board between the ASIC and the DT5550 I/O connectors is needed). It is possible, for example, to use a DT5550 to readout up to 8 WeeROC Petiroc (analog readout) or up to 8 WeeROC Catiroc.

The DT5550 can be used for the following applications:

- Readout of the following detectors:
  - HPGe, Segmented germanium detector
  - Array/matrix of PMTs
  - Multi anode PMTs
  - Array/Matrix of SiPMs
  - Position sensing detectors (for application like gamma camera) with realtime position reconstruction
  - APD, SPAD, SiPIN and SDD
  - Silicon detectors, CCD
  - CdTE and CZT detector
  - Neutron Detector (^{3}He tubes, position sensing tubes)
  - Neutron scintillator detectors with Gamma Neutron discrimination
- Readout of mixed signals ASICs
- Nuclear Spectroscopy
- High Energy Physics
- Imaging with multichannel detectors

The DT5550 is fully supported by **SCI-Compiler,** a Windows-based graphical development system for **easy FPGA programming**. This tool allows to develop and compile the firmware code using graphical blocks which represents the functionalities needed for firmware implementation (for example oscilloscope, TDC, MCA, charge integration, etc). SCI-Compiler automatically generates the VHDL firmware code starting only from logic blocks and virtual instruments that can be connected together in the GUI and, moreover, it generates C/C++/C#/Python Libraries for custom software development in Windows, Linux, MacOS, Android OS (refer to **[RD1]** for more details).
A complete, ready to use default firmware is provided for free and open source. The default firmware manages the basic waveform digitization and charge integration and it is preloaded on the board. The user can open the default firmware in SCI-Compiler and modify it in order to customize, for example, the trigger logic, the data online processing or integrate it in a larger system.
The SCI-Compiler license and one-year upgrade is included with the DT5550.

The **SCI-55X0 Readout Software** is the free and open source Windows-based software developed to perform acquisitions with the DT5550. It works in conjunction with the DT5550 default firmware and it can be modified by the user according to the custom functions implemented in the firmware and for any other need.

Available board models and accessories are listed below.

Board	Description	Product Code
DT5550	DT5550 – 32 ch DAQ System with Programmable FPGA and Sequencer	WDT5550XAAAA
Accessories	**Description**	**Product Code**
DT5550AFE	DT5550AFE –Single-Ended to Differential Input Adapter for DT5550	WDT5550AFEXA

Table 1.1: table of available board models and accessories.

2 Block Diagram

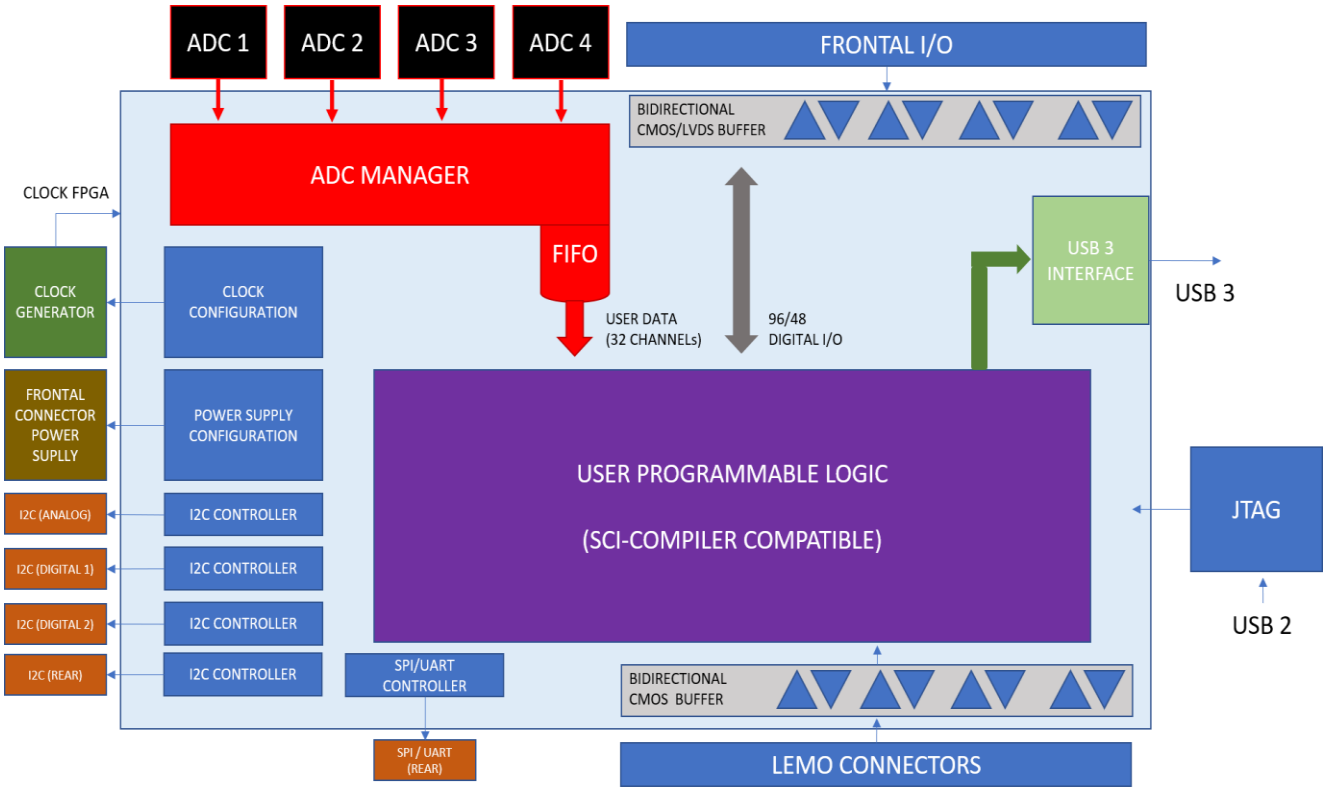


Figure 2.1: DT5550 block diagram.

3 Technical Specifications

GENERAL	**Form Factor** 163x50x226 mm^3 (WxHxD) Desktop		
POWER CONSUMPTION	2 A @ 12 V (Typ.)		
ANALOG INPUT	**Channels** 32 channels Differential **Impedance** Z_{diff} = 100 Ω	**Connector** VHDCI **Full Scale Range** 2 V_{pp}	**Bandwidth** 31 MHz
DIGITAL INPUT	**Channels** 2 x 24 channels Differential **Impedance** Z_{diff} = 100 Ω	**Connector** 2 x VHDCI **Coupling** AC	**Signal Type** CMOS 3.3V LVCMOS 1.8V LVDS BLVDS
DIGITAL CONVERSION	**Resolution** 14 bits	**Sampling Rate** 80 MS/s Simultaneously on each channel	
CLOCK GENERATION	Clock source: internal/external On-board programmable PLL provides generation of the main board clocks from an internal (25 MHz local Oscillator) or external (rear panel CLK-IN connector) reference		
LEMO DIGITAL I/O	**CLOCK-IN (LEMO)** Z_{in} = 50 Ω Single-ended, 25 MHz, 3.3V **CLOCK-OUT (LEMO)** R_t = 50 Ω Single-ended, 25 MHz, 3.3V, 50mA	**GPIO 1…8 (LEMO)** General purpose programmable digital I/Os Single-ended, Z_{in} / R_t = 50 Ω	
MEMORY	16 kS/ch		
TRIGGER	**Trigger Source** *Internal/External*: managed by the default firmware *Complex trigger logic*: implementable by the user on the open FPGA	**Trigger Propagation** Through programmable LEMO GPIO 1…8 **Trigger Time Stamp** *Default FW*: 32-bit counter, 12.5 ns resolution, 50 s range; *Custom FW*: defined by the firmware design	
SYNCHRONIZATION	**Clock Propagation** LEMO CLOCK IN/OUT connectors	**Acquisition Synchronization** Through programmable LEMO GPIO 1…8	
FPGA	**Open FPGA** Xilinx XC7K160T (Kintex-7 family)		
COMMUNICATION INTERFACE	**USB 3.0** USB 2.0 back compatibility Up to 240 MB/s transfer rate		
FIRMWARE	**Default** Waveform recording and Charge Integration	**Custom** Use SCI-Compiler to develop your own firmware! LICENSE INCLUDED	
FIRMWARE UPGRADE	Firmware can be upgraded via USB 3.0 or mini-USB debugger (on-fly)		
SOFTWARE	- **SCI-55X0 Readout Software** to manage the default firmware - **SCI-Compiler** for custom firmware development		

Table 3.1: technical specifications for the DT5550.

4 Packaging and compliancy

The DT5550 is a Desktop board housed in a 163x50x226 mm^3 (WxHxD) alloy box.

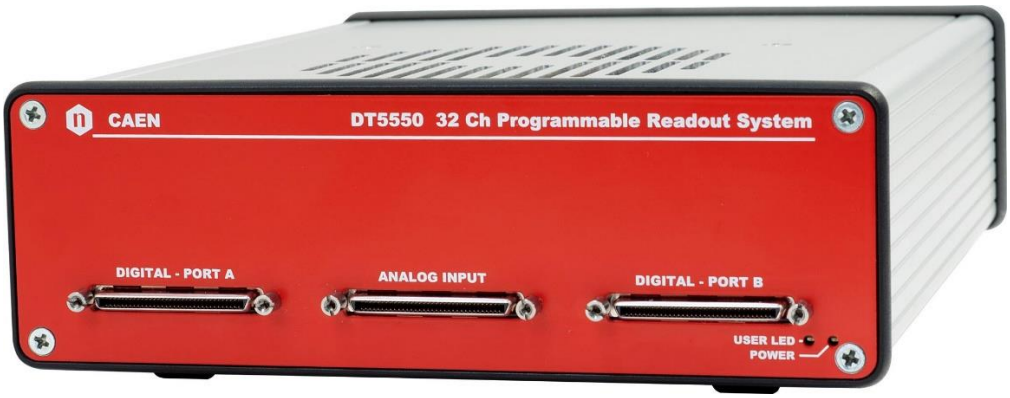


Figure 4.1: general view of the DT5550.

The user is equipped with a USB 3.0 communication cable and a micro-USB programmer cable for the FPGA.

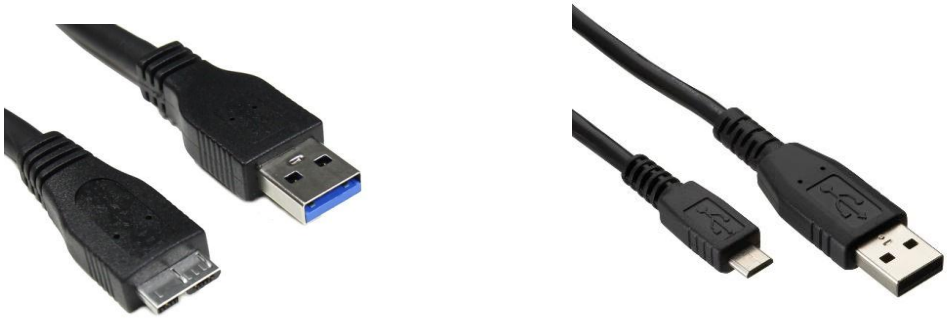


Figure 4.2: USB cables included in the delivered kit.

CAUTION: to manage the product, consult the operating instructions provided.

A POTENTIAL RISK EXISTS IF THE OPERATING INSTRUCTIONS ARE NOT FOLLOWED!

CAEN provides the specific document "Precautions for Handling, Storage and Installation" available in the documentation tab of the product web page that the user is mandatory to read before to operate with CAEN equipment.

SCI-Compiler License

Purchasing a DT5550, the user receives, included in the price, a full working license for SCI-Compiler, the CAEN ***firmware generator*** for ***easy FPGA programming*** developed in collaboration with Nuclear Instruments S.R.L.

SCI-Compiler full version works upon a license and a physical USB Dongle to be plugged in the PC during software usage. The license allows to use SCI-Compiler with no time limit, while the software upgrade is limited to a certain software release which is indicated while running SCI-Compiler. All the software releases, up to the last available for your license, are downloadable from www.scicompiler.cloud.
The license provided with the DT5550 unlocks all the features of SCI-Compiler and includes **one year of free upgrade**.

Note: in order to extend your license for further upgrade, contact CAEN or info@scicompiler.cloud

Note: a trial version setup for evaluation is available for free on the CAEN website or at www.scicompiler.cloud. It has no time limit but does not generate code and does not allow to save your design

Full version of SCI-Compiler is activated with the SERIAL NUMBER and an ACTIVATION key provided together with the USB Dongle.

Figure 4.3: SCI-Compiler USB Dongle and keys for license activation.

The user needs to create an account at www.scicompiler.cloud and add the serial number and activation key in the "MySciCompiler" area, in order to unlock the license and access the download area. Refer to **[RD1]** for more details.

Note: user is not allowed to use the code generated by the SCI-Compiler on boards different from DT5550. Using also a small part of the code generate by the SCI-Compiler on a custom design board or other products is an explicit violation of the license terms and it is an offense against CAEN S.P.A and Nuclear Instruments S.R.L.

5 Power Requirements

The DT5550 is powered by an external 220V-12V AC/DC stabilized power supply provided with the board and included in the delivered kit.

Note: using a different power supply source, like battery or linear type, it is recommended the source to provide +12 V and 2A; the power jack is a 2.1 mm type, a suitable cable is the RS 656-3816 type (or similar)

WARNING: the maximum operating voltage is 12.8V while the minimum is 9V.

Figure 5.1: AC/DC power supply wall adapter provided with the module.

6 Safety Notices

CAEN recommends to always operate the DT5550 within the following safe limits.

WARNING: the two digital front connector lines are directly connected to the FPGA I/Os. Violation in maximum absolute rating illustrated in this document will likely destroy the FPGA. There is no buffer or protection on this line. That is necessary because we want to preserve the possibility to operate at different voltages and with both single ended and differential signals: front Digital I/O can operate at 1.8 or 3.3V and can be configured as LVDS.

The following operating limits must be respected:

Connector	Net class	Unit	Min	Max
DC IN	Power Supply	Voltage	9 V	13 V
LEMO [all]		Voltage	-0.1 V	3.6 V
DIGITAL I/O	Digital 3.3V	Voltage (3.3 V I/O bank selected)	0 V	3.5 V
		Current		10 mA
	Digital 1.8V	Voltage (1.8 V I/O bank selected)	0 V	1.95 V
		Current		10 mA
	LVDS	Voltage	0.5 V	2.3 V
		Current		10 mA
		Common Mode	0.9 V	1.75 V
	I2C/Serial	Voltage	0	3.5 V
	Analog Differential Input	Voltage		2 Vpp
		Common Mode	0.5 V	3.8 V
		V+,V- Absolute Range	0.5 V	3.8 V
	Power 5V	Current		2 A
	Clock Output	Differential Impendance	80 Ω	120 Ω

Table 6.1: operating limits for DT5550 connectors.

7 Cooling Management

The DT5550 board can operate in the temperature range -20 + 50 °C.

On the alloy box is installed a fan on top face. The user must take in care to provide a proper cooling to the board with external fan if the board is used in an enclosure or if the board is installed in a setup with poor air flow.
Excessive temperature will, in first instance, reduce the performance and the quality of the measurements and can also damage the board.

If the board is stored in cold environmental, please check for water condensation before power on.

The board has not been tested for radiation hardness. High energy particle can be source of soft error and can damage the FPGA. If used in strong proton or neutron beams, arrange proper shielding or remote the sensor with a custom cable.

8 Panels Description

Figure 8.1: Front panel view

Figure 8.2: Rear panel view

Front Panel

ANALOG INPUT

FUNCTION

68-pin connector carrying 32 differential input analog signals and one I2C (3.3V)

ELECTRICAL SPECS

Differential Input dynamic: 2 V_{pp}

Z_{diff}: 100 Ω

MECHANICAL SPECS

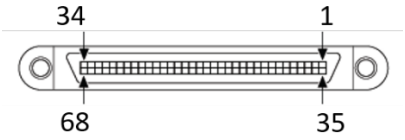
Series: VHDCI connector.

Type: 71430-0008
Manufacturer: TE Connectivity

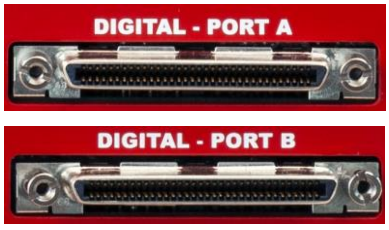
Suggested plug: 68-pin VHDCI

Suggested cable: SCSI-5 type.

PINOUT



DIGITAL -PORT A/B



FUNCTION

68-pin connector carrying 24 differential digital lines, one low jitter clock, one I2C for low speed device configuration and one 2 A programmable voltage power supply

ELECTRICAL SPECS

Sign. type: differential (CMOS 3.3V, LVCMOS 1.8V, LVDS, BLVDS).

Coupling: AC.

Z_{diff}: 100 Ω.

MECHANICAL SPECS

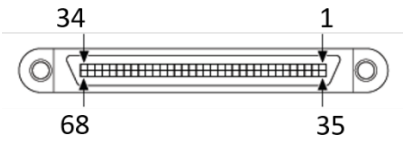
Series: VHDCI connector.

Type: 71430-0008
Manufacturer: TE Connectivity

Suggested plug: 68-pin VHDCI

Suggested cable: SCSI-5 type.

PINOUT



LEDs

FUNCTION

User LED: user firmware output LED (customizable)

POWER: power state on

ELECTRICAL SPECS

Not available

MECHANICAL SPECS

Not available

Rear Panel

DC INPUT

FUNCTION

Input connector for the DT5550 main power supply from the external AC/DC adapter.

ELECTRICAL SPECS

Typ. Input voltage: +12 VDC.

MECHANICAL SPECS

Series: CC power supply connectors

PINOUT

ON/OFF SWITCH

FUNCTION

Panel switch for module power supply ON/OFF:

O → power supply OFF.

I → power supply ON.

ELECTRICAL SPECS

Not available.

MECHANICAL SPECS

Not available.

IDENTIFYING LABEL

FUNCTION

Board's identifying label indicating its serial number (S/N)

CLOCK IN/OUT

FUNCTION

Digital I/O connectors to synchronize the internal clock PLL with an external clock source.

ELECTRICAL SPECS

CLOCK IN: 25 MHz, 3.3V, 50 Ω impedance

CLOCK OUT: 25 MHz, 3.3V, 50 mA

GPIO 1…8

FUNCTION

General purpose digital I/O connectors. Their function is defined at firmware level

ELECTRICAL SPECS

Signal level : NIM or TTL

Input impendace (Z_{in}) : 50 Ω

USB 3.0

FUNCTION

USB connector for data readout and flow control

ELECTRICAL SPECS

Standard : compliant with USB 3.0

Transfer rate: up to 240 MB/s

SERIAL

FUNCTION

Auxiliary connector to expose I2C, UART and SPI interfaces.

MOSI B: SPI master output (DT5550) slave input
MISO B: SPI master input (DT5550) slave output
CLK B: SPI clock output
CS B: SPI chip select
SCL B: I2C serial clock (DT5550 is the master)
SDA B: I2C serial data (DT5550 is the master)
VDSUB: input to be powered between 1.2 V and 3.6 V.

I2C has an internal 1.2 kΩ pull-up to VDSUB.

ELECTRICAL SPECS

Not available

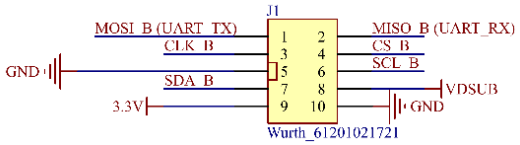
MECHANICAL SPECS

Series: 10 ways male header

Type: 61201021721

Manufacturer: Wurth

PINOUT



DEBUGGER

FUNCTION

Connector for direct FPGA access in order to perform fast firmware download and FPGA signals monitor and probing

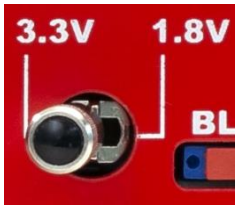
ELECTRICAL SPECS

Standard: compliant with micro-USB

MECHANICAL SPECS

Series: USB Micro type.

VOLTAGE SELECTOR



FUNCTION

Switch to select between 3.3 V and 1.8 V bank voltage for digital I/Os

ELECTRICAL SPECS

Not available.

WARNING: always remove the power before moving the switch

BOOT MODE SWITCH

FUNCTION

Switch to force the FPGA to boot in bootloader mode in order to upgrade the firmware

ELECTRICAL SPECS

Not available.

9 Functional Description

Analog Input Stage

The DT5550 is a flexible and compact board meant to be used as a fully-programmable DAQ system for different applications which require to control both analog and digital signals.

The DT5550 has 32 differential analog inputs and hosts 4 ADCs operating in simultaneous sampling at 80 MS/S - 14 bit. Differential signals are used in order to minimize the crosstalk between channels and allows the system to operate minimizing the noise even with long cables carrying the analog inputs from detectors.

It is possible to connect the DT5550 to both single ended and differential output detector pre-amplifier. Differential output pre-amplifier can be connected directly to the DAQ while single ended detector requires the an analog frontend adapter board in order to achieve the best performance in terms of noise, linearity and resolution. CAEN suggest to use one of the following detector analog front end boards:

- **DT5550-AFE**: a 32 channels analog front end voltage mode amplifier (for PMTs, HPGe, etc). The board **converts the pre-amplified single ended signal from the detector in a differential signal.**

- **DT5550-AFES**: a 64 channels analog **front end transimpedance charge amplifier designed for SiPMs** application, with integrated High Voltage bias with channel by channel fine tuning. The DT5550-AFES board is equipped with a ready to use detector board for an 8x8 Hamamatsu SiPM matrix and it can be connected to one or two DT5550 to realize a complete system for waveform recording, imaging and spectroscopy.

The DT5550 has three frontal VHDCI (ULTRA-SCSI) connectors to carry analog and digital signal. The central connector is used for analog signals input. VHDCI connectors and cables are a very common industrial standard and allow connecting a large number of differential interconnection using single shielded cable. Each VHDCI connector carries up to 68 single ended wires or 34 differential couples.

The pinout of the frontal analog connector is shown in figure. Differential analog lines are indicated in red and the polarity is marked by the "_P" and "_N" label in the pin name.

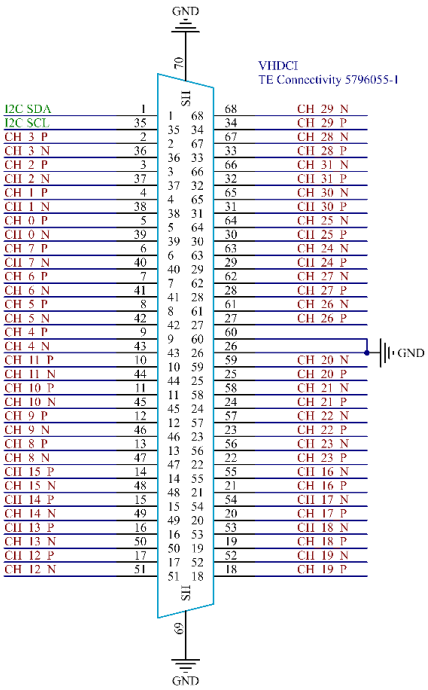


Figure 9.1: front panel analog connector pinout.

The DT5550 analog connector pins are connected to the analog front-end. An LTC6405 fully differential operational amplifier is used in order to buffer the input signals. The OPAmp is not used only as simple buffer but has also the function of common mode isolation. While the ADC require exactly 0.95V as common mode, the front-end can accept any common mode between 0.5V and 3.8V. Moreover, wiring correctly the V_P and V_N terminals, the front-end is capable to accept both single ended and differential signals (see subsections below for more details)

The analog front-end has the following characteristics:

- Bandwidth: 31 MHz
- Gain: 1 V/V
- Differential Input Dynamic: 2 V_{pp}
- Single Ended Dynamic: +/- 1 V (with V_N terminals grounded), 2V (with V_N terminals connected to 1V source)
- Any common mode voltage is accepted if within the absolute maximum rating
- Absolute Input Dynamic: 0.5 V … 3.8 V
- Differential Input Impedance: 100 Ω
- Single Ended Impedance: 75 Ω
- 50µV integrated noise

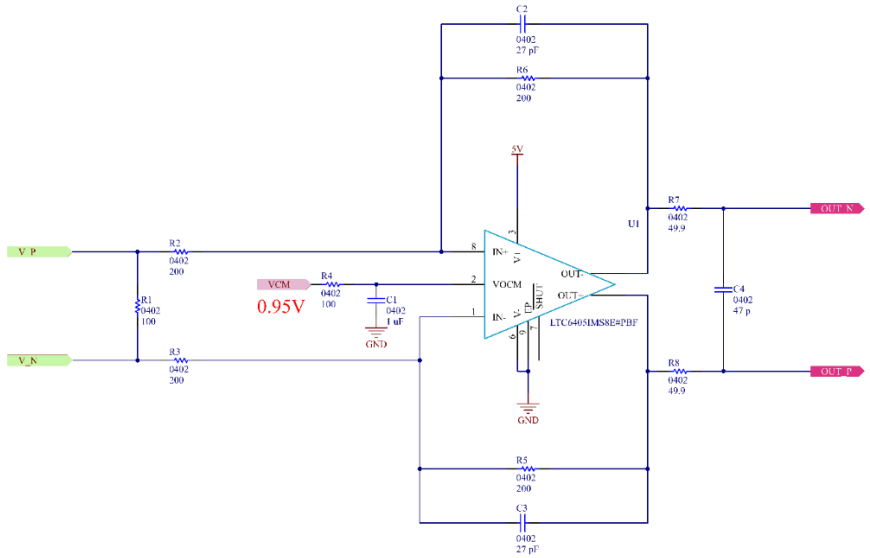


Figure 9.2: scheme of the analog input stage.

As previously said, the DT5550 accepts as input differential analog signal, which have several advantages:

- Immune to common mode noise
- Immune to channel cross-talk
- Immune to RF noise
- Immune to ground-loops
- Immune to ADC clock coupling
- With limited signal swing it is possible to achieve a larger input dynamic

However, if you have single-ended analog signals, CAEN suggests one of the connection explained below in order to adapt the single ended signals to the DT5550

Differential Signal Input

Differential signal can be directly connected to the DT5550 input. Both V_P and V_N must be connected.

SYMBOL	DESCRIPTION	MIN	MAX
VCM	Input common mode	0.5	3.5
VDIFF	Input Differential signal	0	2Vpp
V_P	Input positive terminal	0.5	3.5
V_N	Input negative terminal	0.5	3.5
RIN	Input impedance		100Ω

Table 9.1: differential parameters for the DT5550 analog input.

Modern ASICs are designed to have directly a differential signal output.

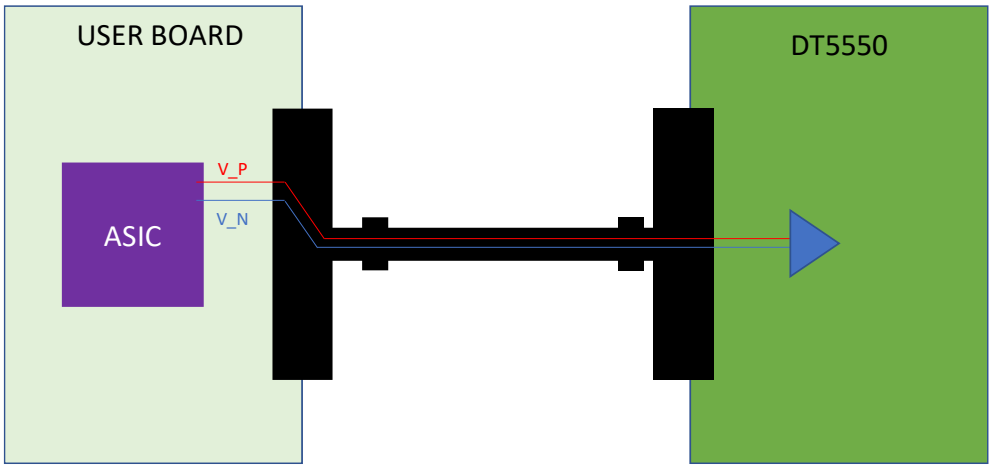


Figure 9.3: connection of differential outputs of an ASIC to the DT5550.

DT5550AFE: Single-Ended to Differential conversion

The **DT5550AFE** is an analog front-end board specifically designed for the DT5550, in order to convert single-ended signals into differential ones. It has 32 analog inputs on MCX connectors and analog differential outputs on a single VHDCI connector. In this way, the converted signals can be carried out by a single VHDCI cable directly to the DT5550 analog input. Thanks to the DT5550AFE it is possible to easily connect detectors to the DT5550 for digitization and pulse processing purposes, as shown in **Figure 9.4.** Refer to **[RD3]** for more details on the DT5550AFE board.

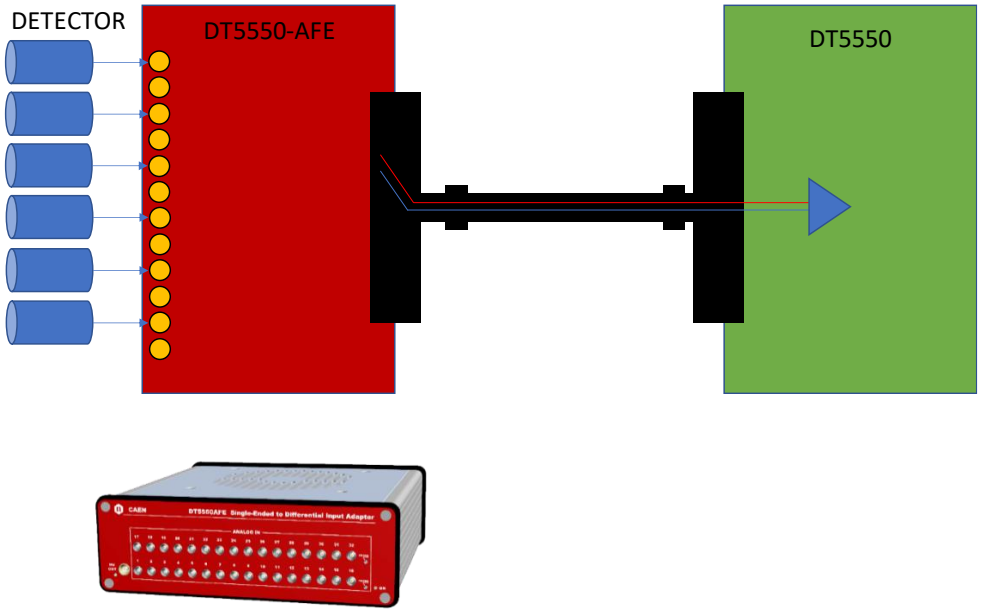
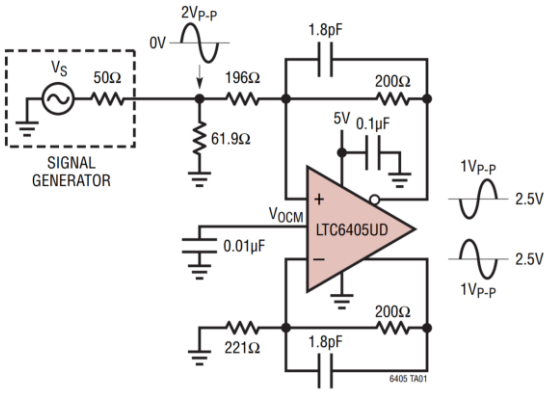


Figure 9.4: connection of single-ended signals using the DT5550AFE.

Active Single-Ended to Differential conversion

Single ended signals can be used as input of the DT5550 using active single ended to differential converter. Single ended to differential converter use a fully differential op-amp in the following configuration:



This configuration works perfectly even with higher resistors (multiply every value x10) in order to increase the input impedance.

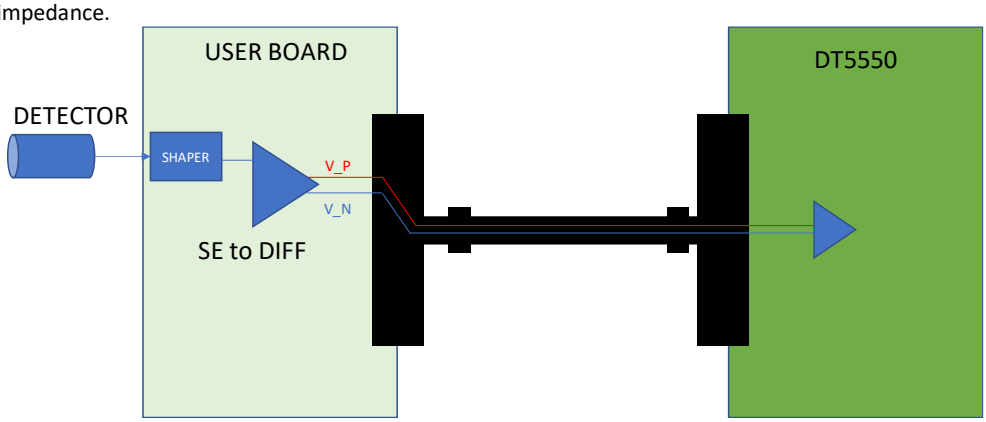


Figure 9.5: connection of single-ended signals using an active single-ended to differential conversion.

The input of the single ended to differential converter can be a discrete shaper output or an analog output of an ASIC (this is the recommended solution to readout ASICs like Weeroc PETIROC, CITIROC, MAROC, etc.)

The user must take care of respecting the differential output parameters explained in **Table 9.1**

AC-coupled passive Single-Ended to Differential conversion

A coupled inductor can be used in order to transform a single ended signal in a differential one. The advantage in using a passive transformer is that no extra power is required for the conversion and no noise is added to the input signal. The drawback is that the signal is AC coupled, that means that baseline information will be lost and the baseline fluctuations will depend on the rate.
A central tap on the transformer is mandatory in order to add the common mode to the differential signal

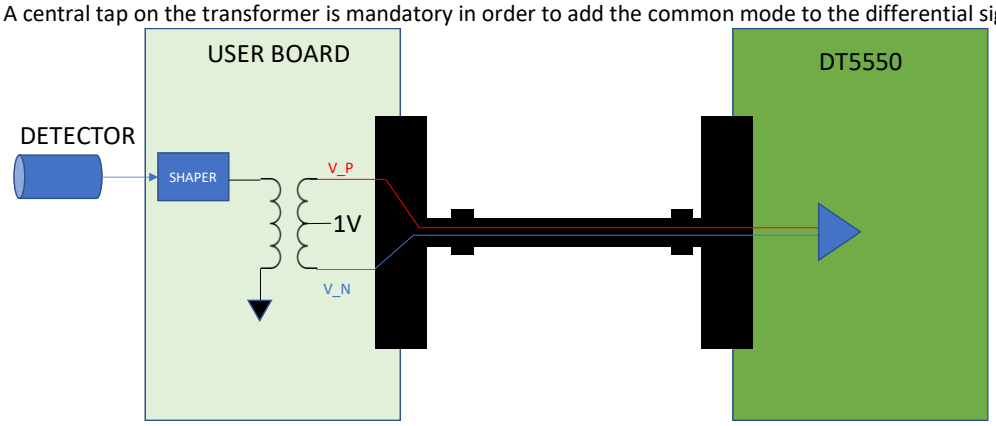


Figure 9.6: connection of single-ended signals using an AC-coupled passive single-ended to differential conversion.

DC-coupled passive Single-Ended to Differential conversion

Several existing ASICs have a single channel dedicated to the analog output. Usually this ASICs have a single ended output in order to reduce the ASIC pinout.

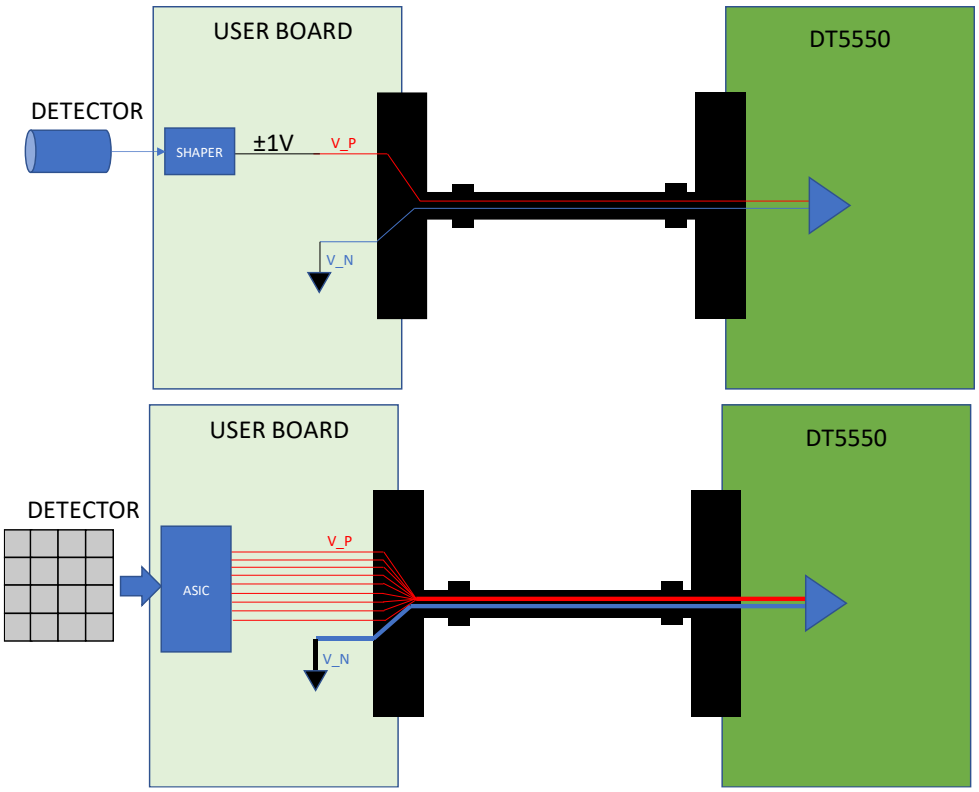


Figure 9.7: connection of single-ended signals using a passive single-ended to differential conversion.

The user should ground (or connect to a fixed power supply) all the negative (V_N) terminal of all channels used in single-ended mode. Please take note that with this solution all benefit of differential signal will be lost.

We suggest (if possible) to ground the V_N terminals as close al possible to the DT5550. It is possible to design a small PCB with a VHDCI male connector on one side and a STRIP ribbon cable connector on the other side. On that PCB all V_N must be connected to GND or 1V. We also suggest to use a shielded ribbon cable when single ended signal are carried on the cable. We suggest to alternate one signal and one ground on the ribbon cable in order to reduce the cross talk

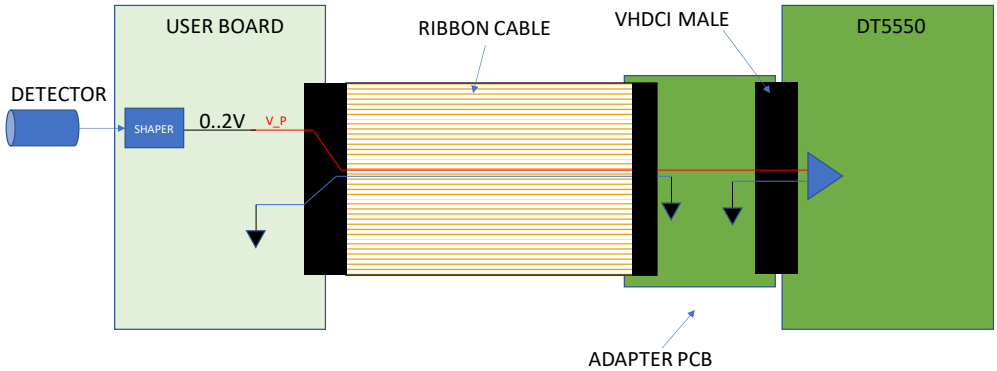


Figure 9.8: connection of single-ended signals using a passive single-ended to differential conversion and grounding optimization.

Digital Input Stage

The DT5550 hosts two VHDCI connectors for digital inputs/outputs on the front panel. Each connector carries:

- 24 differential lines supporting the standards CMOS 3.3V, LVCMOS 1.8V, LVDS, BLVDS (or PSEUDO LVDS)
- one low jitter clock
- one I2C for low speed device configuration
- one 2 A programmable voltage power supply

The pinout of the digital VHDCI connector is shown below.

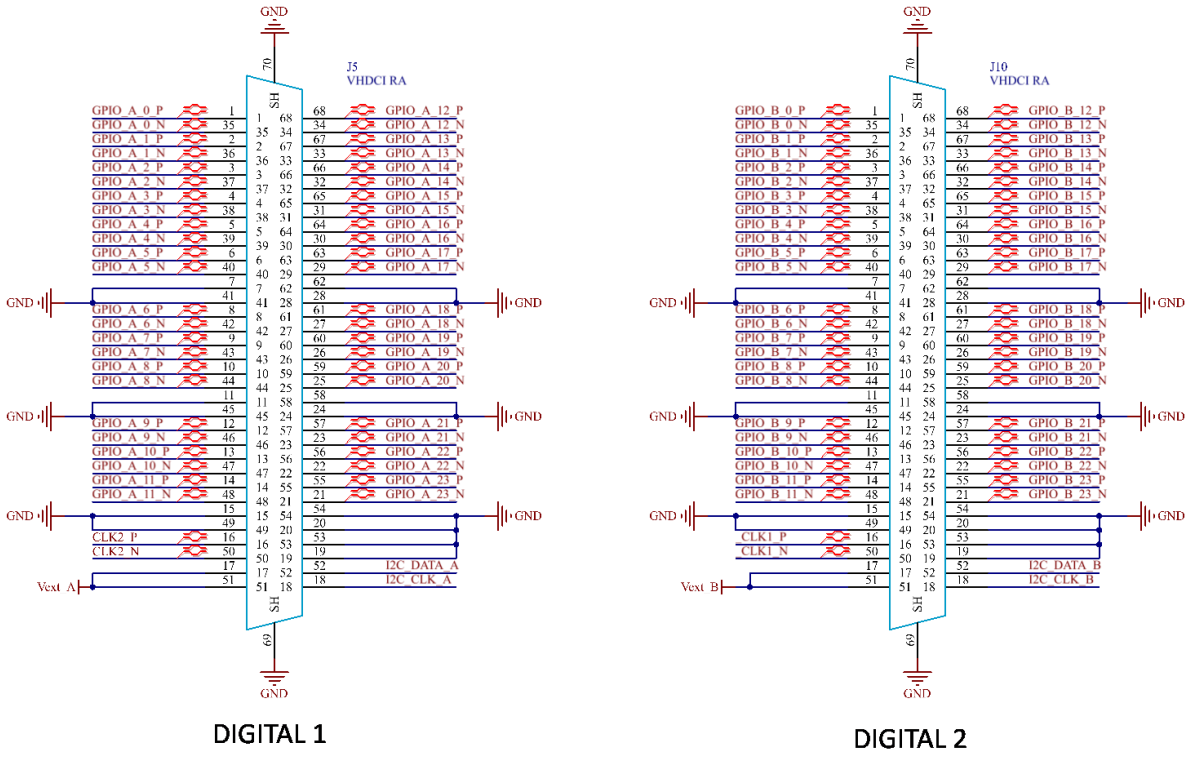


Figure 9.9: pinout of the digital connectors of the DT5550.

Digital I/O can be used for several applications, for example:

- Input for triggers/veto
- Input from photon counting detector / ASIC
- Readout of digital ASIC both with serialized output or parallel output
- Control of the readout process of analog ASIC
- Direct interconnection between multiple DT5550 to extend processing algorithm

Using SCI-Compiler, is possible to select the I/O standard and the pin direction (IN/OUT). Pin direction and signal standard must be selected at configuration time and can not be changed in real-time.

A switch on the back side of the DT5550 allows to select the operational voltage for all digital I/Os. The switch can be moved only when the instruments is off.

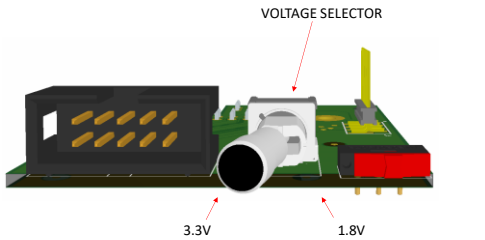


Figure 9.10: DT5550 voltage selector switch for digital I/Os.

WARNING: Do not change the bank voltage of the I/O connector while the instruments is powered. It could damage the board and the connected detector system. In order to minimize the risk of unwanted voltage changes a security switch is used.

LVDS signals can be used both with 3.3V and 1.8V bank power supply. The LVDS common mode is 1.65V when 3.3 V is selected while when is 0.9V if 1.8 V is selected. Both common modes are within the LVDS specifications.
The clock signal is driven directly by the clock generator, indeed is not possible to select the voltage. The clock signal is always an LVDS with 1.25V common mode.
When CMOS signal is used we recommend connecting together all ground pin at board level.

Clock Distribution

The DT5550 has a versatile clock distribution net. A Texas Instruments CDCE62005 clock generator is used in order to generate the clock for all devices on the board. Two clocks (fixed at 80 MHz) are provided to the ADCs. The others three clocks are connected to the front panel digital connectors and to the FPGA. By default, the chip is configured to generate the ADC clock at 80 MHz and at 320 MHz LVDS to the FPGA, while the clock on front panel connectors is disabled.

WARNING: The user is not allowed to reprogram the clock generator, since the FPGA has no other clock source except one. If the FPGA clock is disabled, there will be no way to restore a clock to the FPGA. User can change on-fly the configuration of the clock generator without writing it in the EEPROM.

SCI-Compiler clock manager allows the user to configure the Clock Generator frontal connector frequency. This setting will be not stored in the clock generator EEPROM but in the firmware. When the firmware boot-up it will override the default configuration of the EEPROM writing in in the volatile memory.

An eventual external clock input signal must be a 25MHz, low jitter, 3.3V CMOS input. The external clock output is a CMOS 3.3v 25 MHz square wave. The clock output is able to drive a 50Ω terminated cable.

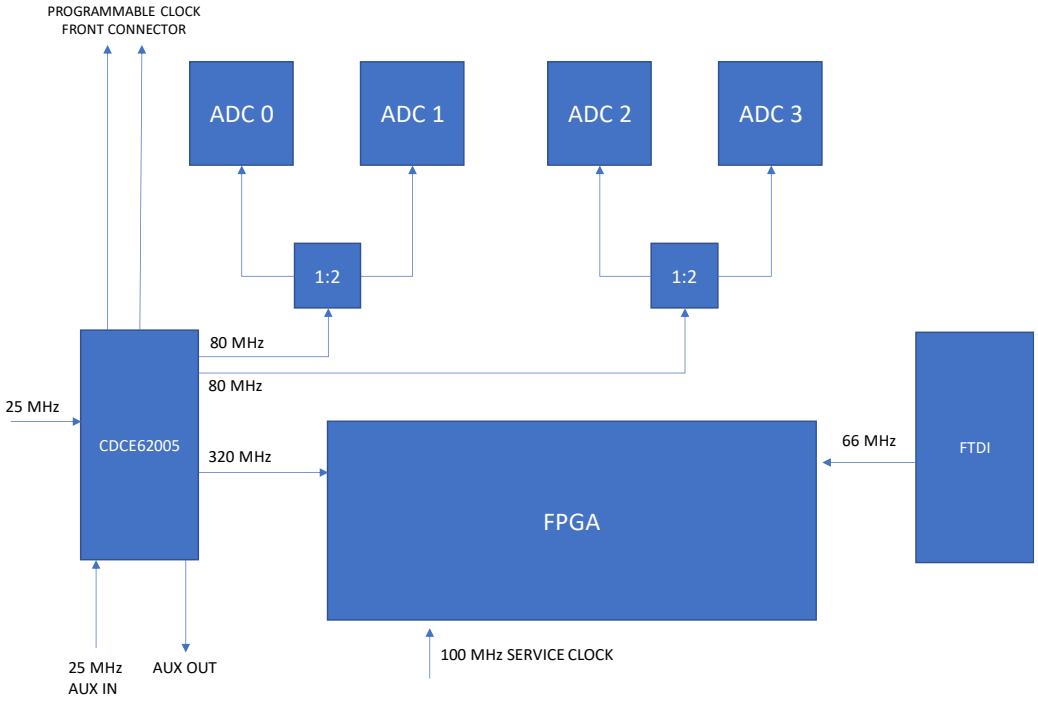


Figure 9.11: scheme of the clock distribution on the DT5550.

10 Drivers & Libraries

The DT5550 uses the standard FTDI FT60X driver (D3XX Driver) for USB 3.0 connection. We decided not to customize the device driver in order to preserve the portability of the driver on Windows/Linux/MacOS/Android OS. Drivers for these operating systems can be downloaded from FTDI web page:

http://www.ftdichip.com/Drivers/D3XX.htm

Follow the FTDI driver installation guide to install the device driver.

Note: upon installation of SCI-Compiler or SCI-55X0 Readout Software, the drivers for DT5550 will be automatically installed in your Windows OS.

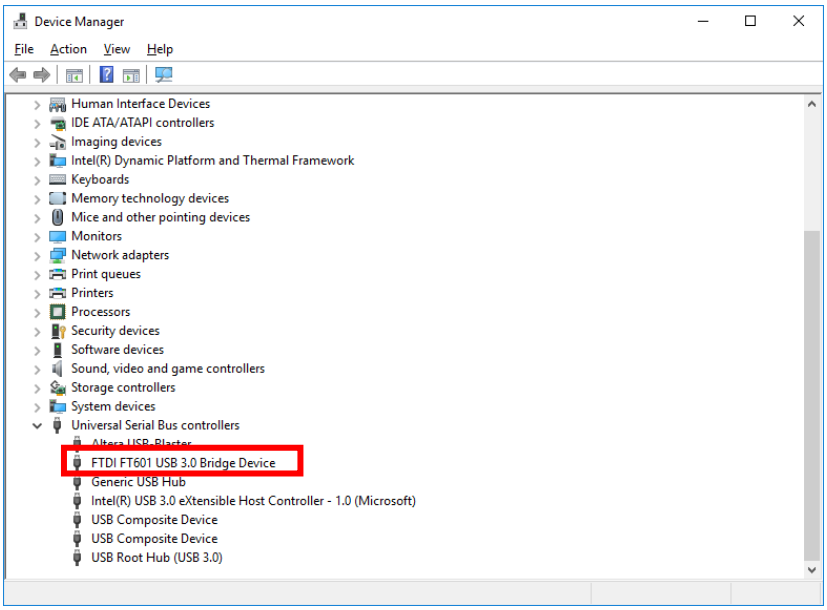


Figure 10.1: the Windows Device Manager showing up the DT5550 as FTDI FT601 USB3.0 Bridge Device

Libraries for C/C++/C#/Python are generated by SCI-Compiler when firmware code is compiled. The libraries can be used for custom software development on Windows/Linux/MacOS/Android. Libraries related to the default firmware are provided within the SCI-55X0 Readout Software open source code.

11 Firmware and Upgrade

The DT5550 is a programmable platform and it is designed in order to encourage the user to develop its own custom firmware using **SCI-Compiler** to generate and compile the firmware code.
However, a full working default firmware is provided: this is a fully featured solution and it is developed not as a basic example to start developing with SCI-Compiler but as a full DAQ readout system firmware. The DT5550 comes with the default firmware already uploaded. In any case the firmware can be downloaded from CAEN website and easily installed on the board with the OpenHardware – Firmware Upgrader tool (see Sec. **Firmware Upgrade**)

The **default firmware** implements typical features of Waveform Recording Digitizers and QDC algorithms and it is fully managed by the free-downloadable and open-source SCI-55X0 Readout Software. In more details, the default firmware implements the following pulse processing features:

- Waveform digitization of all analog channels
- Leading edge or derivative trigger
- 32 independent channels digital charge integration for energy calculation (QDC)
- Time stamping with 12.5 ns resolution
- Different readout modes: independent channels, frame trigger (OR of all channels trigger), external trigger
- External veto and trigger on programmable LEMO GPIO
- List readout mode
- Interface with DT5550AFE
- Rate meter with dead time calculation on each channel

In general, a firmware for the DT5550 is divided in two parts:

- FRAMEWORK: a set of non-configurable blocks (or configurable with some limitations) that implements low level functionalities like ADC management, USB3 communication, I/O buffers, etc.

- PROCESSING CORE: firmware developed by the user (the block diagram in SCI-Compiler tool) with all processing algorithms to analyze and process the acquired data.

Firmware Framework Structure

All firmware for DT5550 have a common structure called framework. The framework contains the building blocks which are mandatory for the board correct working. The framework should not be edited by the user but can be configured with some limitations using SCI-Compiler tool. The framework is like the kernel of an OS and manage the low-level interfacing with hardware peripherals. The main structures are:

- ADC manager: configures the ADCs, deserialize data and provide them as a data vector synchronous to the acquisition clock.
- Clock configuration: configures the clock generator with user-defined configuration after bootstrap.
- Frontal Connector Power Supply: configures the voltage on the power supply pins of the frontal connector
- I2C Interface: Map on USB or allow direct firmware access to all the physical I2C interfaces
- SPI/UART Interface: Map on USB or allow direct firmware access to the rear SPI/UART interfaces; it allows to select between UART/SPI at designing time
- I/O buffers: allows to select the standard (CMOS/LVDS) and the direction (input/output) of all programmable I/Os.
- USB 3 interface: implements the USB 3 to local bus conversion

SCI-Compiler masks all physical VHDL interconnection automatically placing and configuring the blocks above. The configurable parameters can be set set in the project property page. See SCI-Compiler documentation for further details

Firmware design: the processing core

The DT5550 processing core is a Xilinx Kintex7 FPGA. The FPGA can be programmed in several ways:

- VHDL/Verilog: this is the typical language for developing processing system in FPGAs. It is based on basic operation (logic/arithmetic/conditional processing/sequential element) connected each other to build component. Component are then connected together in order to create more complex designs.

- C: a C/C++ program is automatically converted in a VHDL design by a software tool.

- Design with high level blocks: the user connects together a series of pre-designed building block in order to obtain the desired processing system.

SCI-Compiler is a set of very high level blocks which implement the functionalities of the most common instrumentation used in physics experiment: digitizer, MCA, TDC, Time Over Threshold, trigger, scaler, etc.

Sci-Compiler is designed to work at best with DT5550 and CAEN suggests to use this firmware generator and compiler tool since it focuses the attention only on the functional blocks of the application to be implemented and does not require a deep knowledge of the device in use. The user is free to develop a firmware in VHDL without using the SCI-Compiler. We suggest to use the default framework to correct initialize the board components. Framework source code is partially encrypted in order to protect our IP and avoid unauthorized copy of the board.
The framework code is available inside the installation folder of SCI-Compiler.

SCI-Compiler generates VHDL code and Vivado Project. If the user wants to add custom functionalities that are not implementable with SCI-Compiler, he can use the SCI-COMPILER to develop some parts of the design and then open the project in Vivado to add missing function writing in VHDL and then compile as a standard Vivado Project.

The DT5550 can be used for different application, requiring different firmware (for example multichannel analog digitization, readout of mixed signal ASICs, direct readout of shaped signals).
In the following we describe the default firmware of the DT5550.

Default firmware for DT5550

The DT5550 has a default firmware pre-programmed from factory. The default firmware implements a 32-channels digitizer with waveform recording and charge integration.
The default firmware is designed to work with SCI-55X0 Readout Software. It is fully developed in SCI-Compiler and can be easy modified by the user. SCI-55X0 Readout Software is distributed open source in VB.NET. The user can start from the firmware and software project to create his own custom application.
The default firmware works with both differential and single-ended signals. SCI-55X0 Readout Software can directly control the DT5550AFE single-ended to differential adapter board to set the offset and the input impedance.

Charge integration

The basic structure of the firmware is the following: the trigger identifies the signal and calculate the sum of all digitized data. The baseline is calculated as moving average of the input signal. The baseline calculation is suspended during the charge integration. The energy is calculated as the difference between the charge and the baseline. The data are then transmitted to the computer as a list of time and energy. The SCI-55X0 Readout Software receives the list and calculates the energy spectrum for each channel; it also displays data as bidimensional heatmap (image from the detector)

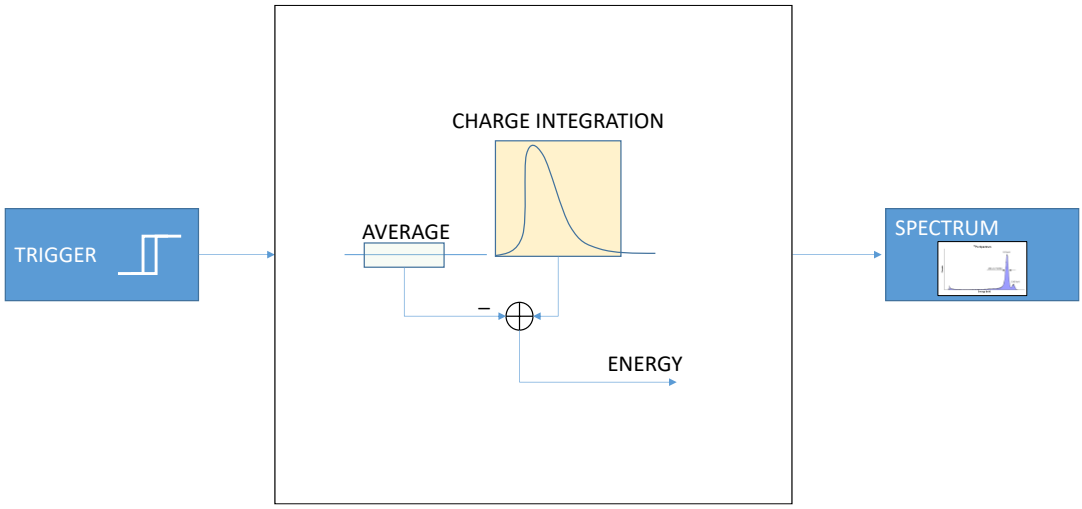


Figure 11.1: scheme of the default firmware for the DT5550.

The firmware diagram above is developed in SCI-Compiler and implements the single channel processing logic. The SCI-Compiler project is then designed in a hierarchic way. Multiple processing blocks calculate the energy and timestamp of each channel: this processing blocks are connected together at the top of the project.

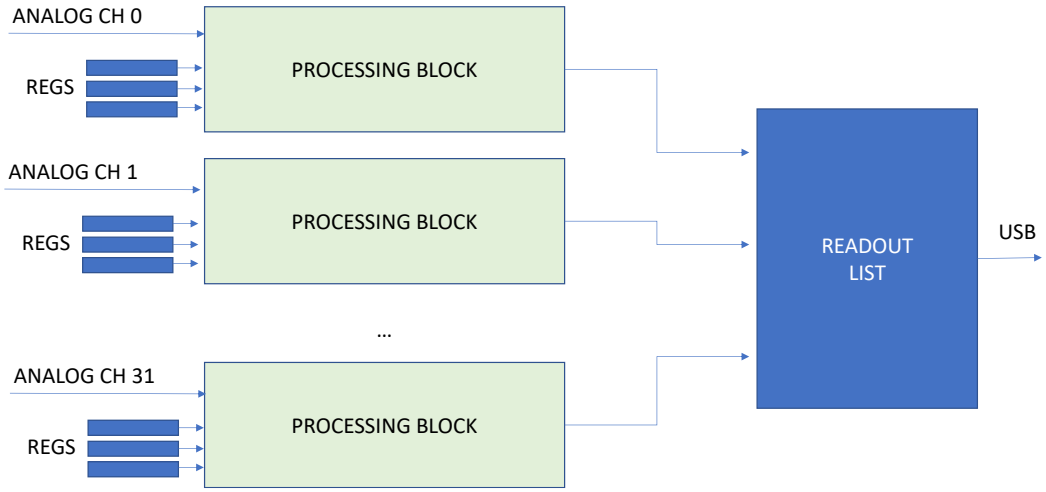


Figure 11.2: Firmware hierarchic structure in SCI-Compiler.

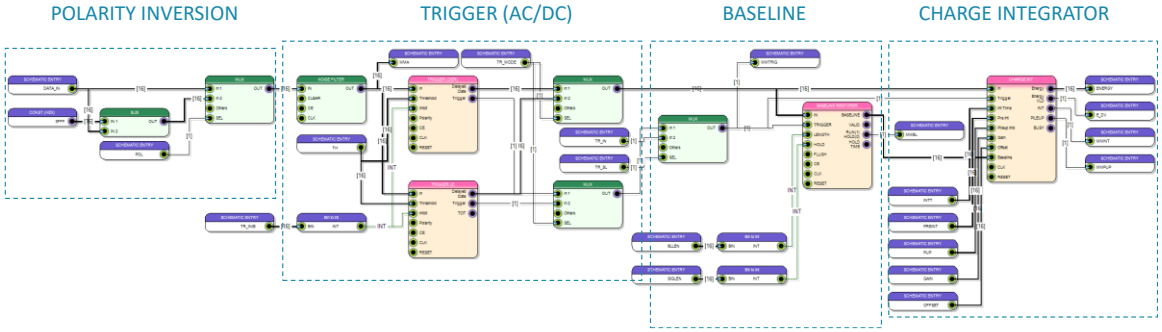


Figure 11.3: SCI-Compiler scheme for single channel data processing in the default firmware.

The SCI-Compiler scheme of the single channel processing block is shown in **Figure 11.3**. Different main parts can be distinguished in this block diagram:

- **Polarity inversion** chain allows to accept both polarity signal. The signal is inverted calculating (0x3FFF – signal). A multiplexer selects between positive (no operation) and negative (inverted) polarity.
- The **trigger** can operate with both leading edge and derivative trigger. The trigger mode to be used can be selected in the SCI-55X0 Readout Software. Two multiplexer are used: the first selects between leading and derivative trigger, while the second selects between internal and external trigger.
- The **baseline** is calculated by averaging the signal values for a certain amount of time. The baseline calculation starts when the TRIGGER is high and the time interval indicated at the HOLD input has been passed. The output of the "Baseline Restorer" SCI-Compiler block contains the baseline value.
- The **charge integration** is managed in SCI-Compiler by the "Charge Int" block and it is performed on the input signal delayed by the trigger. It is possible to specifiy in input the integration gate, the pre-gate, the pile-up rejection time and the baseline value. The result of the integration process, i.e. the area of the input signal, is provided at the ENERGY output pin of the "Charge Int" block. The PILEUP output signal indicates if the considered input signal has been characterized by a pileup event. The BUSY output is high if the integration calculation is occurring.

The single channel processing block shown in **Figure 11.3** can be represented by a unique block, the PRCORE block shown in **Figure 11.4**. Inside this block there are all sub-blocks illustrated before. The PRCORE is connected to the Analog Input and to the registers for the configuration. Moreover, the PRCORE can accept an external trigger signal coming from LEMO 0 (see again **Figure 11.4** , bottom part).

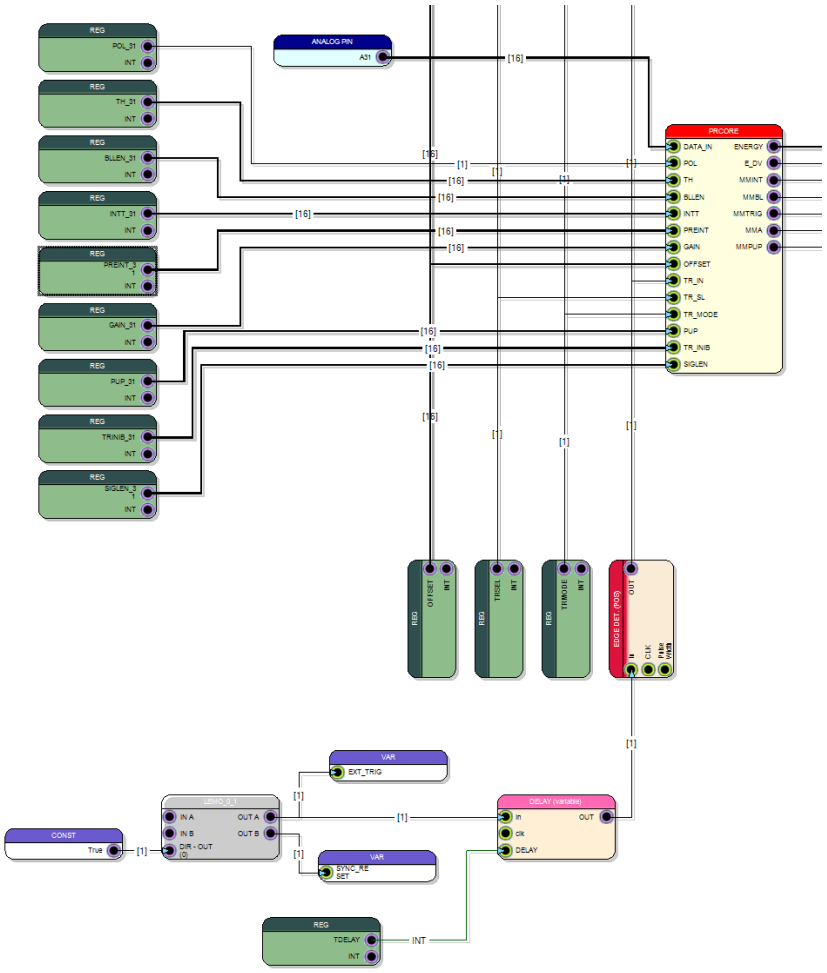


Figure 11.4: SCI-Compiler scheme of the whole charge integration process for a channel of the DT5550.

The registers used for charge integration settings are listed below (see also green blocks in **Figure 11.4** for reference). These registers can be used by the user to configure the data acquisition when developing a custom application to control the DT5550

Register Name (XX= channel number)	Address (HEX)	Bits	Description
POL_XX	[0x10000 : 0x1001F]	32	Polarity of the input signal. 0: input signal is positive 1: input signal is negative
TH_XX	[0x10020 : 0x1003F]	32	Trigger threshold. If derivative trigger is selected this is the slope of the signal, if leading edge trigger is selected this is the value of the input signal height that fires the trigger
INTT_XX	[0x10040 : 0x1005F]	32	Length in samples of the integration window.
BLLEN_XX	[0x10060 : 0x1007F]	32	Length in samples of the baseline (1 sample = 12.5ns)
SIGLEN_XX	[0x10080 : 0x1009F]	32	Length of the whole signal used for the baseline calculation hold-off.
PREINT_XX	[0x100A0 : 0x100BF]	32	Length in samples of the pre-integration window; the pre-integration window integrates the part of the signal before the trigger
GAIN_XX	[0x100C0 : 0x100DF]	32	Gain of the charge integrator. Usually this number should be equal to 1/INTT*65535. It is possible to increase the gain and the measure resolution multiply by an arbitrary value the previous number
TRINIB_XX	[0x100E0 : 0x100FF]	32	Length of the trigger inhibit. Trigger inhibit avoid to double trigger a signal.
PUP_XX	[0x10100 : 0x1011F]	32	Length in samples of the pileup window. The pileup window opens after the end of the integration window. An event occurs in the integration window both events (the integrating event and the piled up one) are discarded. If event occurs in the pileup event only the second event is discarded
TRMODE	0x10120	1	Trigger mode 0: derivative 1: leading edge
TRSEL	0x10121	1	Trigger select 0: internal 1: external trigger (LEMO 0)
OFFSET	0x10122	1	Digital offset enabled/disabled
TDELAY	0x10124	1	Delay applied on the external trigger. External trigger usually should be delayed in order to compensate the DT5550 pipeline (about 200ns)

Table 11.1: registers description of the charge integrator module.

In the full SCI-Compiler project, all channels outputs (energy) are connected to the frame transfer module. The frame transfer module is able to transfer all channels together when one triggers. It is also possible to operate in list mode: energy, time, channel information is transferred as soon as a specific channel trigger.

Waveform recording

An oscilloscope module is also available in SCI-Compiler and it allows to inspect the input signal and digitize the waveform. The oscilloscope allows the user to digitize the analog input signal synchronously with four digital tracks:

- Integration probe: the signal is high when integration is in process.
- Trigger
- Baseline: the signal is high when baseline calculation is in progress.
- Pileup: the signal marks events discarded by the pileup rejector

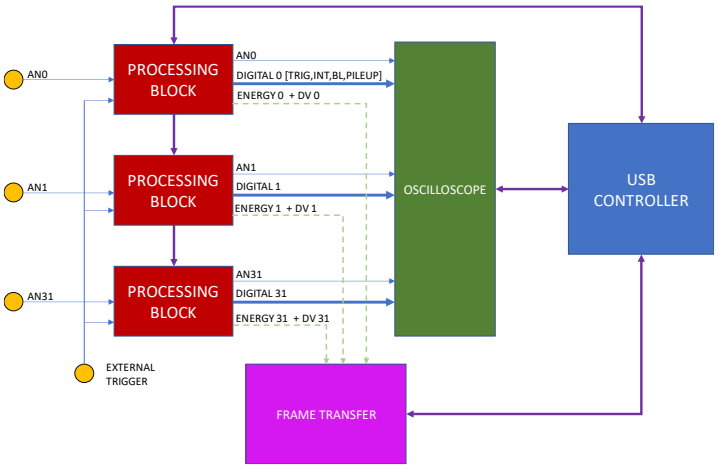


Figure 11.5: scheme of the oscilloscope module available in the default firmware for the DT5550.

In the graphical interface of the Oscilloscope tool (available directly in SCI-Compiler) the user can set the following parameters: the trigger source (external, internal or the specific channel), the trigger mode (automatic, single shot), the trigger level, the acquisition window and the position of the triggered signal in the acquisition window. These parameters, together with the oscilloscope status and the waveform data can be controlled through some registers automatically generated during the block creation. The register addresses are available in the .json file generated during the firmware compilation. These registers can be used by the user to configure the data acquisition when developing a custom application to control the DT5550. Below the registers for the oscilloscope module are listed:

CONFIG_ARM
A transition from 0 to 1 of the value of this register enables the oscilloscope measurement.

CONFIG_DECIMATOR
The value set with this register represents the decimation factor for the output data.

CONFIG_TRIGGER_MODE
This register sets all the information of the data acquisition trigger. The first three bits of the value written in the register specify the trigger acquisition mode:
000 -> external trigger
010 -> software trigger
001 -> analog signal trigger
100 -> digital 0 signal trigger
101 -> digital 1 signal trigger
110 -> digital 2 signal trigger
111 -> digital 3 signal trigger
The fourth bit, that has to be specified for the analog channel trigger mode, represents the trigger edge: 0 is a rising edge (to be set for positive signals) and 1 is a falling edge (in case of negative signals). For the software trigger mode the seventh bit has to be set to 1 to trigger the data acquisition. In all the cases of the analog and digital trigger modes the channel can be specified from the eight to the fifteenth bit.

CONFIG_PRETRIGGER
This register allows to specify the trigger position from the opening of the acquisition window in number of samples.

CONFIG_TRIGGER_LEVEL
For the analog signal trigger mode the level of the trigger can be set through this register in lsb.

READ_STATUS
If the value read from this register is 0 the oscilloscope is not able to provide data, if it is 1 it will be possible to read data.

READ_POSITION
This register contains the information of the trigger position of each event in number of samples.

The waveform data can be obtained by reading at the oscilloscope Address register (written in the .json file) a number of values equal to the number of points in the waveform signal (nsamples).

Example: Use the software trigger with negative signals and set 0 as decimation factor and 800 samples as pre trigger.

```
set_register(CONFIG_DECIMATOR, 0)
set_register(CONFIG_PRETRIGGER, 800)
set_register(CONFIG_TRIGGER_MODE, 0000000010001010)
set_register(CONFIG_ARM, 0)
set_register(CONFIG_ARM, 1)
Read Data
```

Example: Use the analog signal trigger of the fifth channel (number 4 starting from 0) with positive signals and set 3 as decimation factor, 800 samples as pre trigger and 12000 lsb as trigger level.

```
set_register(CONFIG_DECIMATOR, 3)
set_register(CONFIG_PRETRIGGER, 800)
set_register(CONFIG_TRIGGER_MODE, "0000010000000001")
set_register(CONFIG_TRIGGER_LEVEL, 12000)
set_register(CONFIG_ARM, 0)
set_register(CONFIG_ARM, 1)
Read Data
```

Example: Read data

```
if (read_register(READ_STATUS) ==1)
  {
     data = read_register(Address, nsamples)
     position = read_register(READ_POSITION)
     fix_position = position - pre_trigger
     for (i=0, i=nsample, i++) {
         analog_data(k) = data(i) and 65535
         digital0_data(k) = data(i) >> 16 and 1
         digital1_data(k) = data(i)  >> 17 and 1
         digital2_data(k) = data(i)  >> 18 and 1
         digital3_data(k) = data(i)  >> 19 and 1 }
  }
```

Imaging module

The imaging module available in SCI-Compiler, implements frame transfer functionalities, allowing to transfer the input data and associate a time code to each transferred event. It is similar to a list mode transfer, except that it is possible to configure it to transfere entire frame each time a trigger on a channel is fired. This is useful to implement imaging system where the information is partially cointained also in the under-threshold pixels. As the input data is the event energy information, the block allows to reconstruct the energy spectrum by counting the occurrences of each transferred energy value, and to perform an imaging analysis by considering the event by event and/or the cumulative energy information of various channels. The user can specify the number of channels during the block creation in SCI-Compiler. The ENERGY input signal represents the input energy data for each channel. The correspondent TRG input signal is the trigger signal that is HIGH to indicate when energy data is valid. The block can be configured to transfer data with different trigger logics: the OR of all the TRG input signals (if one energy is valid, all the channel energies are transferred), the AND of all the TRG input signals (all the channel energies has to be valid in order to transfer the data) and the external trigger. The CE input signal enables the transfer of data, while the BUSY output signal notifies that the block is transferring the data. In presence of data coming from different boards it is mandatory to synchronize the operations on the data: the SYNC CLK IN provides the common signal clock, which is replicated at the SYNC CLK OUT signal. The same is done for the reset signal with the SYNC RESET IN and the SYNC RESET OUT signals. The SYNC TRIG IN is a trigger signals counter, which is incremented at each event and is reported as an output signal. The acquisition parameters, together with the block status and the data can be controlled through some registers automatically generated during the block creation. The register addresses are available in the .json file generated during the firmware compilation. These registers can be used by the user to configure the data acquisition when developing a custom application to control the DT5550. Below the registers for the imaging module are listed:

CONFIG_ARM
Enable the module

CONFIG_WAIT
The value that can be set in this register determines the number of clock cycles that the block waits before transferring the data.

CONFIG_SYNC
Set synchronization parameters

CONFIG_T0_MASK
This register can be used to select the active channels: a 1 in a bit enables the correspondent channel.

CONFIG_TRIGGER_MODE

This register sets the trigger acquisition mode:
010 -> external trigger
001 -> OR trigger between the enabled channels
000 -> AND trigger between the enabled channels

READ_STATUS
The first bit of this register is 0 when there are some available data. The second bit of this register contains the first bit of the CONFIG_ARM register.

The data can be obtained by reading the Frame Transfer Address register written in the .json file. The data can be transferred in packets, each one characterized by a structure described in the read data example.

Example: one board with an OR trigger between the first four enabled channels.

set_register(CONFIG_SYNC, 0)
set_register(CONFIG_WAIT, 0)
set_register(CONFIG_TRIGGER_MODE, "001")
set_register(CONFIG_T0_MASK, "1111")
set_register(CONFIG_ARM, 2)
set_register(CONFIG_ARM, 0)
set_register(CONFIG_ARM, 1)
Read Data

Example: Read data

Each data packet is composed by a series of value transmitted with a state machine.
The first value is "FFFFFFFF" (in hexadecimal notation). The second value is "12345678" (in hexadecimal notation). The third value represents the event time-code from bit 63 to bit 32, while the fourth value contains the event time-code from bit 31 to bit 0. In the fifth and the sixth values is reported in the same way the number of trigger signals (number of events). The next two values contain the number of transmitted data packets. The ninth value represents an information related to the trigger: each bit corresponds to a channel and is equal to 1 if the channel has triggered the event (the information is provided by the TRG inputs of the block). If the ninth value contains at least a 1 the event is considered to be valid and the next information could be received. This last information consists in an array of energies, one value for each channel (the information is provided by the ENERGY inputs of the block). The spectrum of each channel can be reconstructed by incrementing of a unit the bin corresponding to the transferred energy value.

Firmware Upgrade

It is possible to change the flahs firmware using the firmware upgrade tool *(OpenHardware – Firmware Upgrader),* included both in SCI-Compiler and SCI-55X0 Readout Software setup. The firmware upgrade tool interfaces with the FPGA bootloader via USB 3.0 port in order to load the firmware in the DT5550 flash memory. In order to access the FPGA in bootloader mode, the **boot mode switch** on the rear panel of the DT5550 must be switched from "Normal" to "Bootloader" (see **Figure 11.6** for reference). Toggle the boot mode switch only with the board switched off.

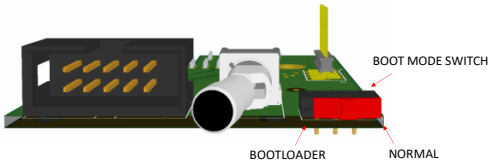


Figure 11.6: DT5550 Boot Mode Switch positions.

The DT5550 mounts a QSPI 512 Mbit flash S25FL512S. The first 4 Mbytes are used for the bootloader. At startup bootloader is always loaded. If the bootloader mode is not selected with the switch, the bootloader reconfigures on fly the FPGA to load the firmware at address 0x40 0000.
The firmware size depends on the complexity of the project. Always enable bitstream compression: this option is by default enabled in SCI-Compiler standard firmware.

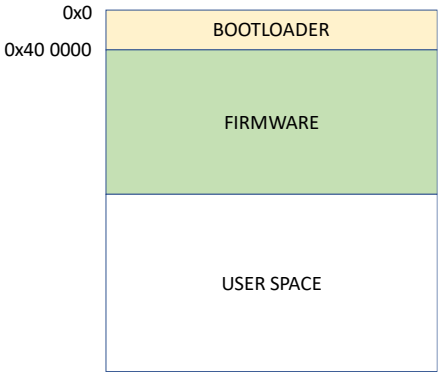
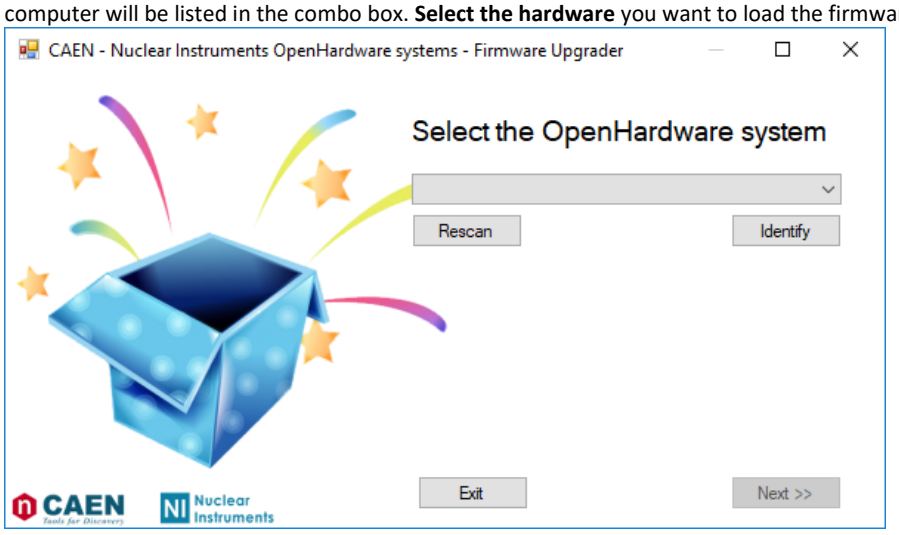


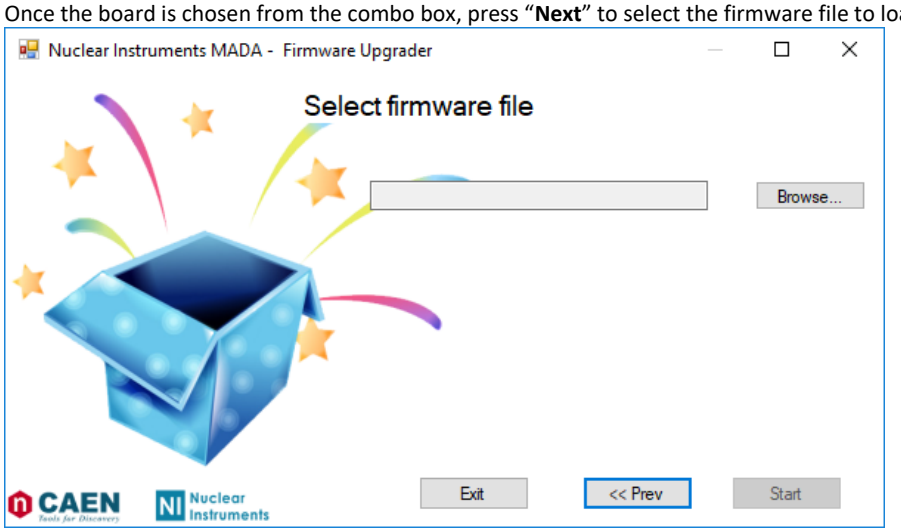
Figure 11.7: scheme of the DT5550 FPGA memory usage.

In order to upgrade the firmware, follow the steps below:

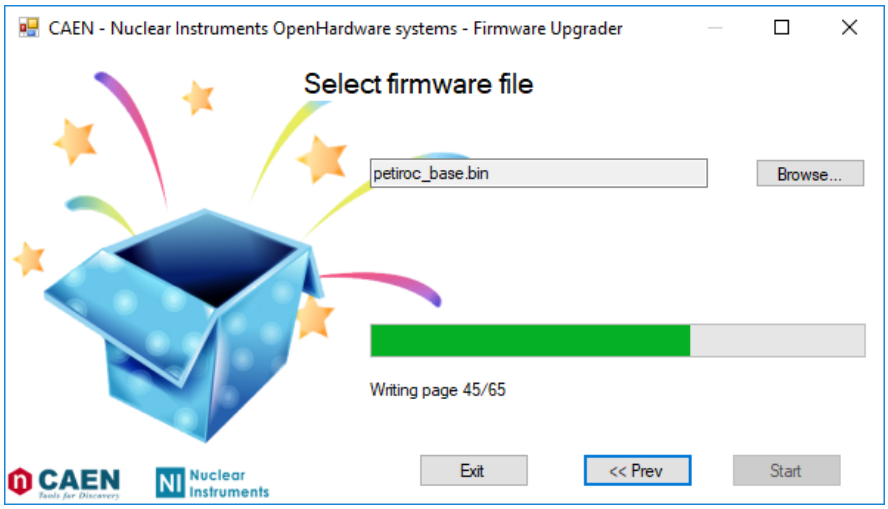
- **Switch the Boot Mode Switch to "Bootloader"** with the board switched off.
- Connect the board to the PC via USB 3.0 communication port and power on.
- Open the ***OpenHardware Firmware Upgrader,*** which is automatically installed with SCI-Compiler or SCI-55X0 Readout Software.
- A wizard will guide you in the firmware upgrade process. All supported hardware connected by USB to the computer will be listed in the combo box. **Select the hardware** you want to load the firmware on.



- Once the board is chosen from the combo box, press "**Next**" to select the firmware file to load.



- **Load the .bin file** (or .NIU in case of the default firmware available on CAEN website), cointaining the firmware code and press the "**Start"** button.



- When the firmware is fully loaded a message invites the user to **power cycle the board** in order to load the new firmware.

- Remember to **switch the Boot Mode Switch to normal operation mode** in order to allow the board to run in standard mode and load the firmware from the flash memory.

WARNING: There is no way for the system to recognize if a firmware is correct for a particular hardware. For example, a firmware designed for another board can be loaded on a DT5550 but it can damage the board. User must check the hardware target for a specific firmware BEFORE load it on the flash memory.

Note: the latest release of the DT5550 default firmware is available on CAEN website at the relative product page. You can load it on the board using the OpenHardware -Firmware Upgrader, following the procedure described above.

Note: it is possible to upgrade the firmware in the volatile FPGA memory, using SCI-Compiler and the "Debugger" micro-USB port on the DT5550 rear panel (refer to **[RD2]** for more details). In this way it is possible to connect directly to the FPGA and perform a **fast firmware upgrade**. Using the "Debugger" port, the firmware is written in a volatile way directly into the FPGA in a couple of seconds (against about few minutes with bootloader flash tool): a power cycle will reload the firmware stored in the flash memory. This can be useful during development time.

12 SCI-55X0 Readout Software

SCI-55X0 Readout Software is a **free and open-source** software developed for Windows OS to operate **in conjunction with the default firmware** of the DT5550, in order to provide a ready-to-use solution.

The software implements typical features needed to acquire and process data in nuclear spectroscopy and particle physics:

- Waveform monitor with common or independent channel trigger
- List mode readout (energy, time) in channel independent mode and in frame mode (all channels readout after a common trigger)
- Energy Spectrum plot for all channels
- Bidimensional heatmap visualization for imaging, with configurable detector shape
- DT5550AFE configuration to control signals coming from detectors (offset, input impedance, HV control/monitor, BIAS compensation)
- Spectrum fitting and energy calibration
- Data saving with waveform dump on file

The software is distributed both as compiled application and as source code. The source code is written in VB.NET and C# and it can be easily customized by the user to adapt to a custom firmware and for any other need. In order to recompile the SCI-55X0 Readout Software, a free version of Visual Studio .NET 2015 or later must be installed on the user's PC.

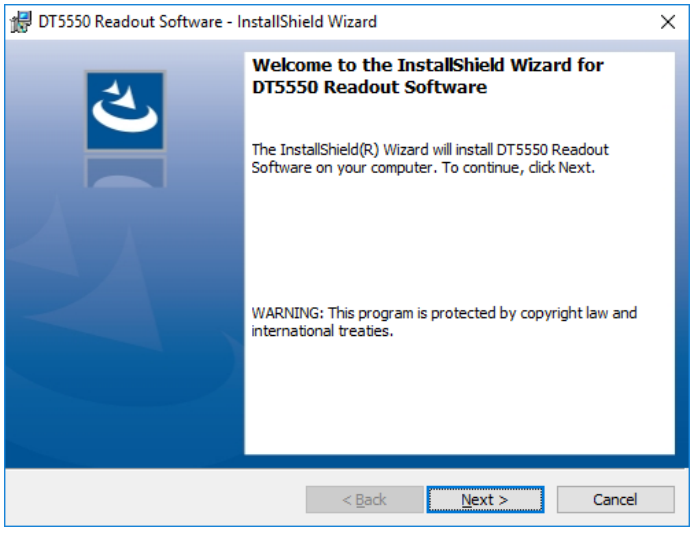
Software installation

SCI-55X0 Readout Software is compliant with Windows 7 or later.

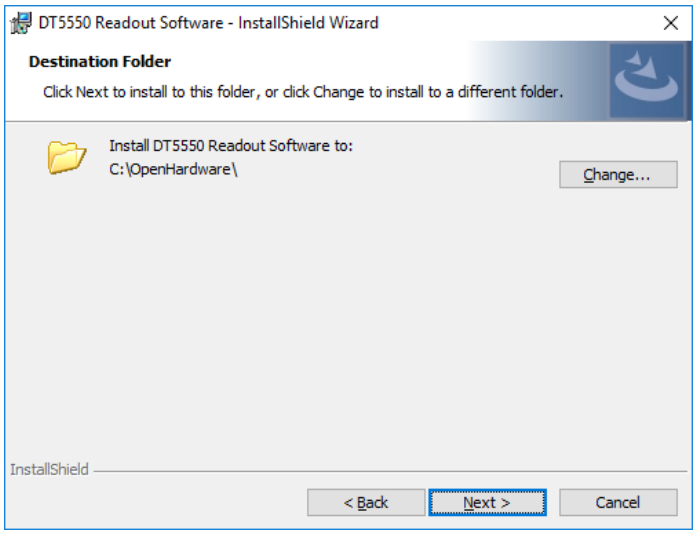
Note: The software is standalone and does not require the prior installation of any library. The installation setup also installs the Open Hardware Firmware Upgrader tool.

In order to install the SCI-55X0 Readout Software and the Open Hardware Firmware Upgrader, follow the steps below:

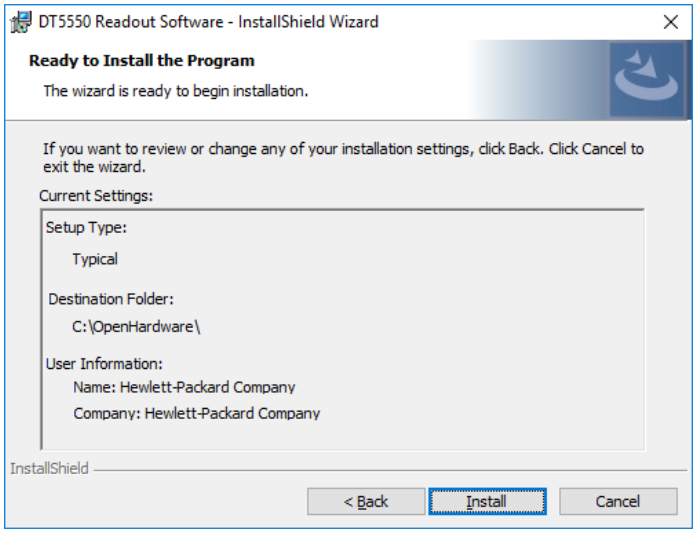
- Download the software package from the DT5550 product page on the CAEN website (**login required**)
- Unzip and run the executable.
- A setup wizard will start. **Press "Next" to continue.**



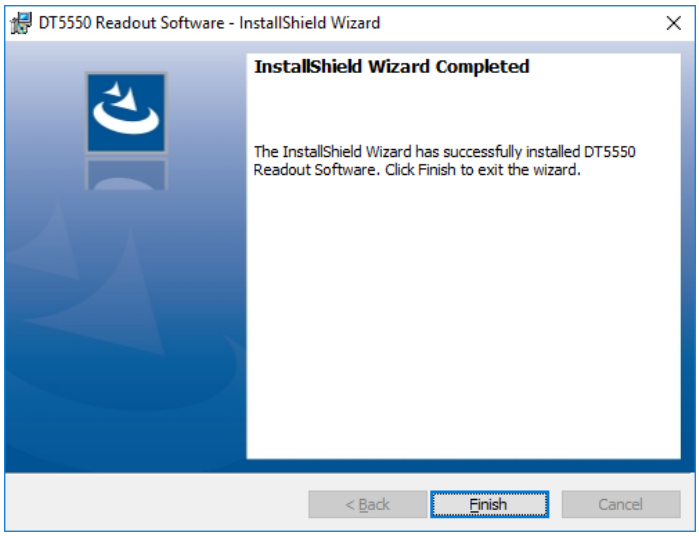
- Choose the destination folder and **press "Next".** By default, the readout software is installed in C:\OpenHardware\DT5550 and the firmware upgrader in C:\OpenHardware\FirmwareUpgrader



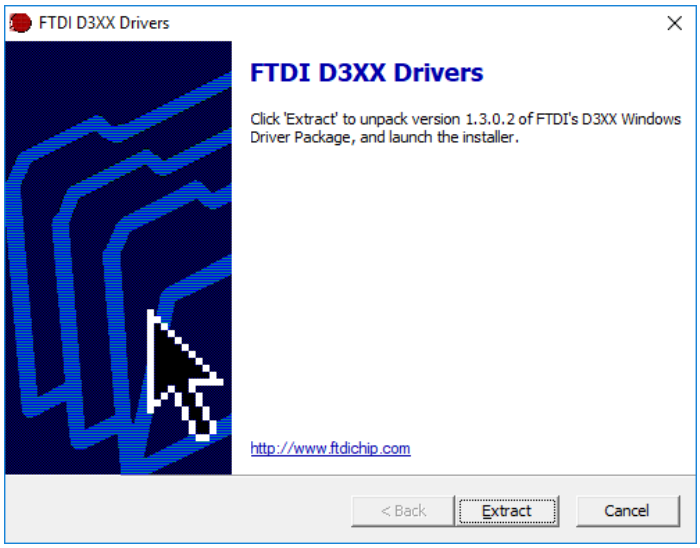
- **Click "Install"** to complete software installation.



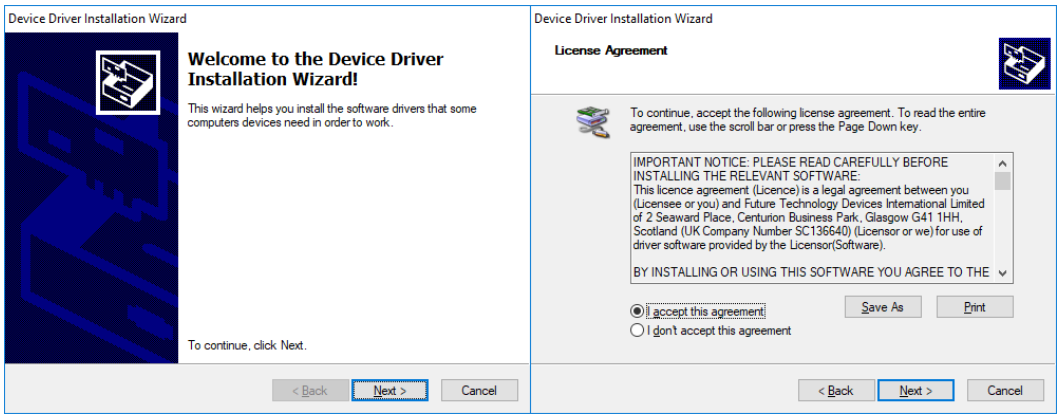
- Wait until installation is completed and press "**Finish**" to complete the setup.



- Once SCI-55X0 Readout Software installation is complete, the Wizard will ask to extract and install FTDI USB Drivers for the DT5550. Press "**Extract**" to continue.



- **Press "Next"** in the following window to continue and **accept the License Agreement**.



- The driver will then be installed. **Press "Finish"** to exit the Wizard.
- Now it is possible to launch the software.

Note: the software is open source: it is possible to find the software VB.NET source code and the default firmware project (developed with SCI-Compiler) in the installation folder, to allow user customization.

Board connection

After launching the software, the "Connection" window will open and the user is asked to connect a board specifying the connection parameters:

- *Firmware Type*: selection between "Standard", if connecting a board with the default firmware loaded, or "Custom" if the board is equipped with a user-developed firmware. If the user recompiles the deafult firmware using the SCI-Compiler, "Custom" must be selected under firmware type.
- *Select Json File*: in case of "Custom" firmware, here the path of the register file in .json format must be specified. When using SCI-Compiler to compile a firmware code, a file called RegisterFile.json is generated. The file contains a full description of all registers and USB mapped blocks available in the firmware project.
- *Connection Type*: only USB supported
- *Serial Number*: select the serial number of the board to be connected. The serial number is written on the rear panel of the instrument (see Sec. **Rear Panel**)

Figure 12.1: the "Connection" window at startup of the SCI-55X0 Readout Software

After the connection parameters has been set, the user can press the "Connect" button to initialize the software GUI.

Software GUI Description

After successful connection, the main window will appear. The window is divided in four areas:

- Control bar: here there are all the buttons needed to control the acquisition process.
- Main working area: all tabs like "Settings", "Spectrum" and "Oscilloscope" are shown here.
- Imaging module: the 2D image of the channels energies is reconstructed in the two heatmap (one for the single frame view and the other for the cumulative view).
- Log Area: all messages related to the user actions are displayed in the history log.

All panels can be undocked and rearranged also outside the main window in order to organize the software layout on multiple monitors.

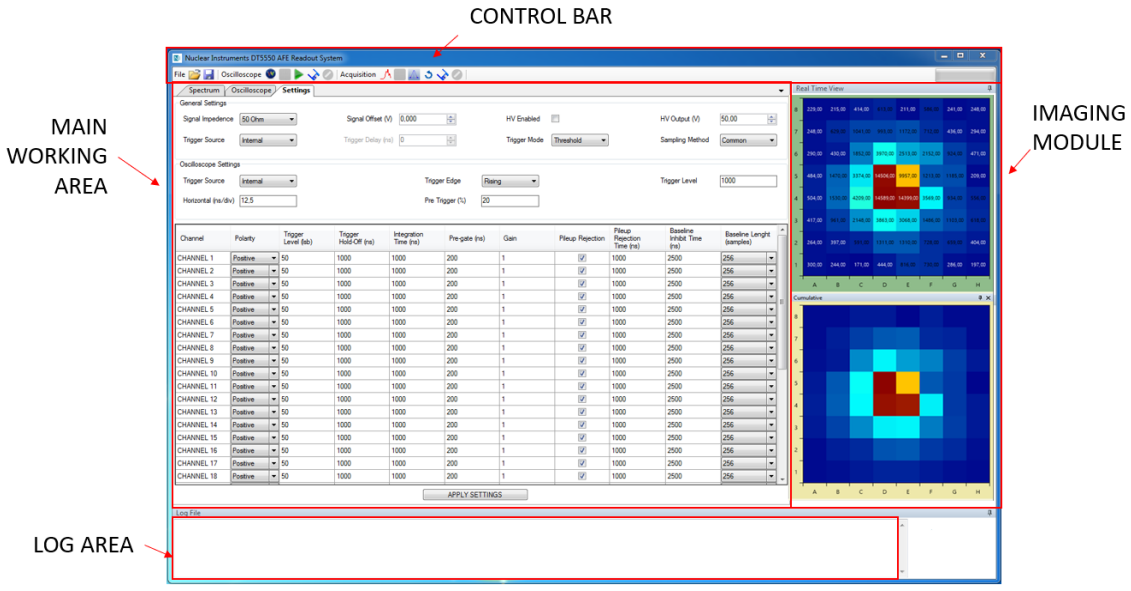


Figure 12.2: the main window of the SCI-55X0 Readout Software. The main areas are highlighted**.**

Control Bar

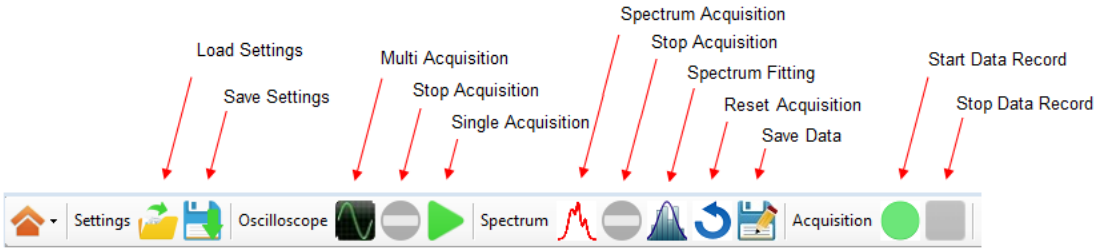
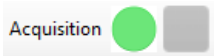


Figure 12.3: the Control Bar of the SCI-55X0 Readout Software.

The "Control Bar" contains the following buttons:

- 
  - **Spectrum**: change the visualization features of the spectrum (semi-logarithmic or linear on Y axis, rebinning on the X axis, graphical plot type)
  - **View**: select the zoom type
  - **File**: export and print plots
- 
  - **Load** settings from file
  - **Save** Settings to file
- 
  - **Multi Acquisition**: start to acquire waves until stop acquisition button is pressed
  - **Stop Acquisition**: abort waves acquisition
  - **Single Acquisition**: acquire a single waveform every time the button is pressed
- 
  - **Spectrum Acquisition**: start spectrum and image acquisition process
  - **Stop Acquisition**: abort spectrum acquisition
  - **Spectrum Fitting**: open the fitting tool window
  - **Reset Acquisition**: reset spectrum and image
  - **Save Data**: save on disk the spectrum for each channel and the cumulative images
- 
  - **Start Data Record**: open the data dump window to configure and start saving data (waves or energy) event by event
  - **Stop Data Record**: stop current data dump process

Settings Tab

The Settings Tab allows to configure all digitizer parameters. It is divided in three areas, as shown in **Figure 12.4**:

- **General Settings**: it includes all parameters common to all channels like trigger mode and source and sampling method (list/frame transfer). It also includes settings for the DT5550AFE adapter board, like input impedance and offset
- **Oscilloscope settings**: it allows to select the trigger source for the oscilloscope, the time scale on the plot and the length of the pre-trigger window
- **Channel Specific Settings**: this is a table with a row for each channel containing all configuration parameters for that channel, like trigger threshold, signal polarity, charge integration time, etc.

The user must push the button **APPLY SETTINGS**, at the bottom of the window, in order to let the settings become effective. Settings can not be applied while an acquisition is running.

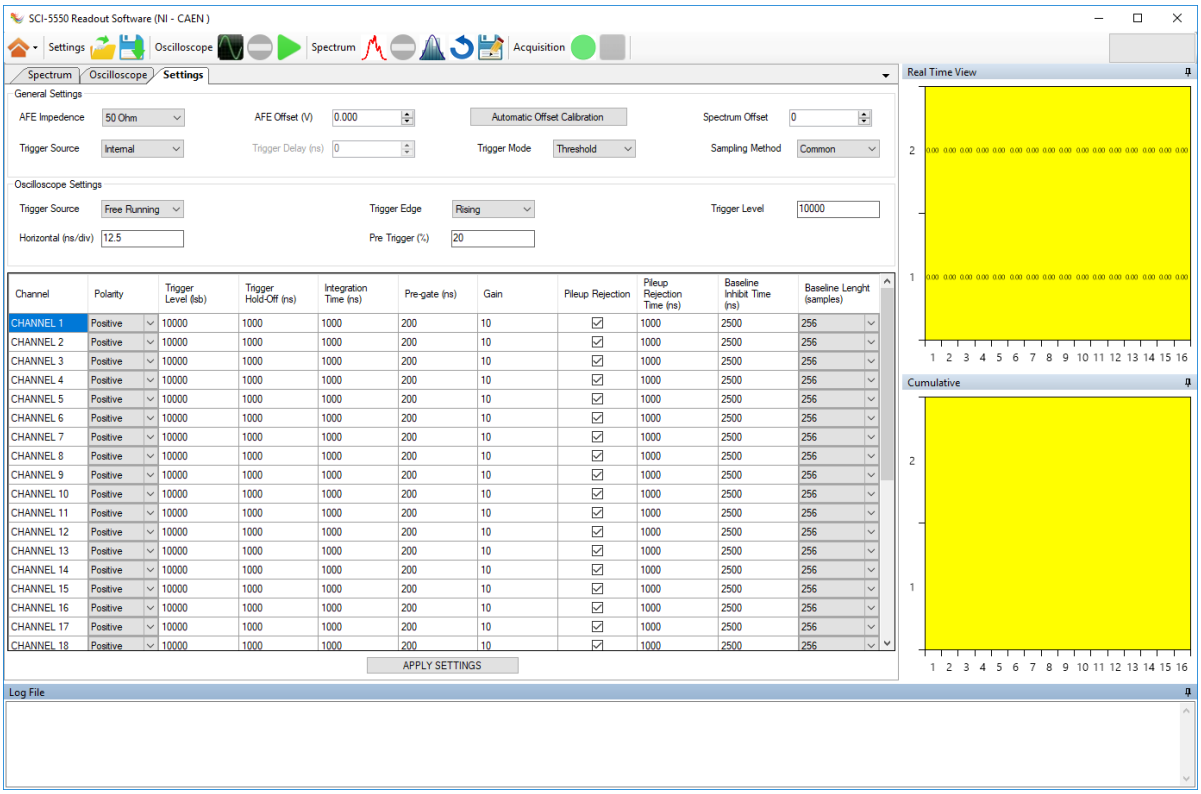


Figure 12.4: the Settings Tab of the SCI-55X0 Readout Software.

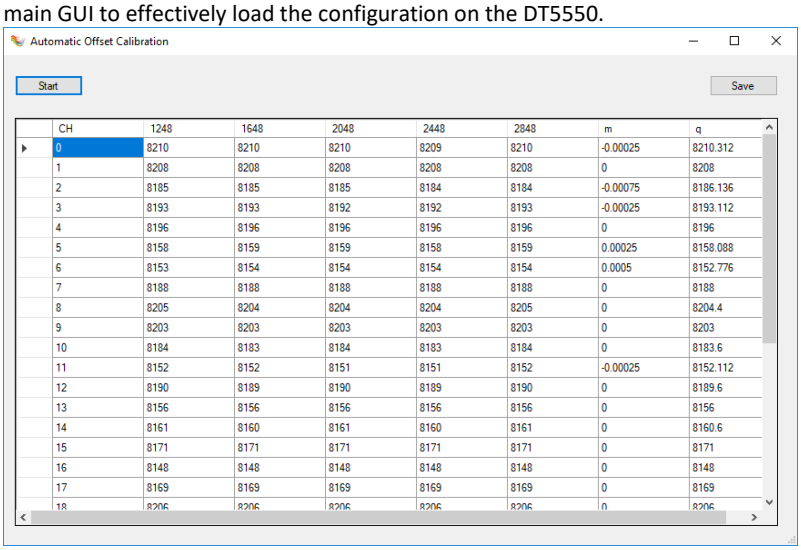
General Settings

These settings are applied identically to all channels of the board

AFE Impedance: when the DT5550 is used in conjunction with the DT5550AFE adapter board, this control selects the input impedance of the single ended frontend. Options are 1KΩ / 50Ω. The two boards communicate between the I2C link present in the analog cable, no connection to the PC is required for the DT5550AFE

AFE Offset: when the DT5550 is used in conjunction with the DT5550AFE, this control allows to add an analog offset to all single ended channels in order to fit at best the ADC input dynamic. The AFE Offset can be adjusted between -0.9 and +0.9 V.

Automatic Offset Calibration: this button allows to perform an automatic procedure to adjust the channels offset when using DT5550AFE. In this way it is possible to minimize the offset spread among different channels. The procedure must be performed with all input signals disconnected. Press “Start” to initialize the procedure. The calculated coefficient values are stored in a table, as shown below. Press “Save” to store the offset configuration and “Apply settings” in the main GUI to effectively load the configuration on the DT5550.



Spectrum Offset: allows to add an offset in the charge integration calculation, common to all channels.

Trigger source: selects between internal trigger (indipendent for each channel) and external trigger (common to all channels). The external trigger is sensible to the rising edge of a signal on the GPIO1 connector.

Trigger delay: allows to add a delay on the external trigger in order to compensate the internal pipeline delay (the internal pipeline delay is about 200ns).

Trigger Mode: allows to select between leading edge ("Threshold") and "Derivative" trigger.

Sampling Method: the "Common" option allows to acquire data in Frame Transfer Mode, transferring all the information when a channel triggers, while the "Independent" option allows to operate in List Mode, transferring the data of the triggering channels only.

Oscilloscope Settings

These settings allow to configure the parameters of the oscilloscope (i.e. of the waveform recording).

Trigger Source: Select the trigger source for the oscilloscope. Options are:

- Internal: the same channel that starts the charge integrator is used as trigger. The trigger level must be set in the "Channel Specific Settings".
- External: the external signal on GPIO1 is used as a trigger for the oscilloscope (the Trigger Source in the General Setting should be set to External, too)
- Free running: the oscilloscope operates without trigger and acquires a waveform as soon as the previous transfer is completed
- Channel n: the oscilloscope acquisition starts when the selected channel n overcomes a programmable threshold (to be set in the *Trigger Level field*)

Trigger Edge: it selects if the oscilloscope triggers on the rising or falling edge of the input signal. It works only in conjunction with "Trigger Mode" = Threshold in the General Settings

Trigger Level: set the absolute threshold of the leading edge trigger. It works only in conjunction with *Trigger Mode* = Threshold in the General Settings

Horizontal (ns/div): Set the time base for the oscilloscope in ns per division

Pre Trigger (%): Specify the portion of the acquisition window dedicated to the pre trigger (signal sampled before the trigger)

Channel Specific Settings

These settings allow to configure the specific parameters of each channel, used by the charge integration firmware:

Polarity: Select between positive and negative polarity according to the input channel

Trigger Level (lsb): Set the absolute trigger level. If leading edge trigger is selected this is the level of the trigger signal on the oscilloscope. If derivative trigger is selected this number represents the slope of the signal: the bigger is this number, the greater should be the difference between consecutive samples of the waveform in order to fire the trigger.

Trigger holdoff (ns): Set the trigger inhibition time after a trigger

Integration Time (ns): Set the charge integration time in ns

Pre-gate time (ns): Set the extra integration time for the part of the waveform before the trigger.

Gain: Multiplication factor for the charge integration result. This allow to recover resolution avoiding to trash away the least significant bits of the charge integration. A low gain reduces the resolution of the measure while a too high gain will saturate the spectrum dynamic.

Pileup Rejection: Enable/Disable the pileup rejector to discard events occurring inside the pileup rejection window, whose width is set in the *Pileup Rejection Time* field.

Pileup Rejection Time (ns): Time window that opens after the integration time in order to reject events too close to a good event. This control is useful to avoid that the tail of an event could interact with the energy measurement of the next event.

Baseline Inhibit Time (ns): Inhibition time for the baseline calculation after the integration window. It avoids that the tail of an event is measured as part of the baseline.

Baseline Length (samples): Length in samples of the window for baseline calculation.

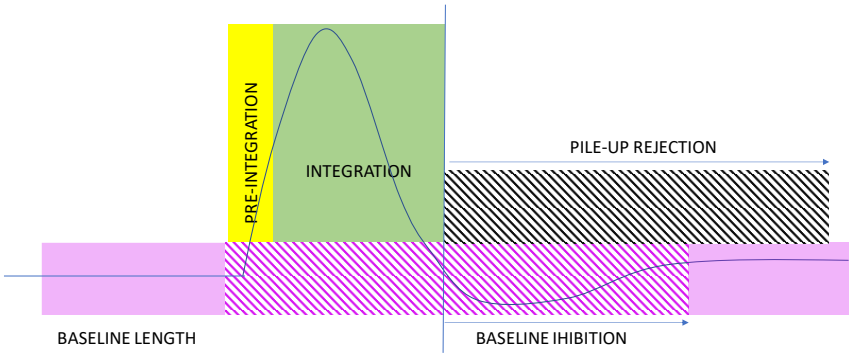


Figure 12.5: scheme of the charge integration firmware parameters to be set in the SCI-55X0 Readout Software.

Oscilloscope Tab

The Oscilloscope Tab allows to monitor on plot all analog input signals and digital probes:

- The ANALOG trace displays the waveform sampled by the ADC
- The INTEGRATION GATE displays the digital signal representing the integration time
- The BASELINE GATE displays the state of the baseline restorer. When high, the baseline restorer is running, when low is holding
- The TRIGGER signal toggles when the trigger identifies a signal
- The PILEUP REJECTOR signal toggles each time an event is discarded due to pileup.

Multiple input channels can be captured and displayed on the same plot by checking the correspondent checkbox from the channels list on the left of the Oscilloscope Tab. All oscilloscope configuration parameters can be set in the Settings Tab.

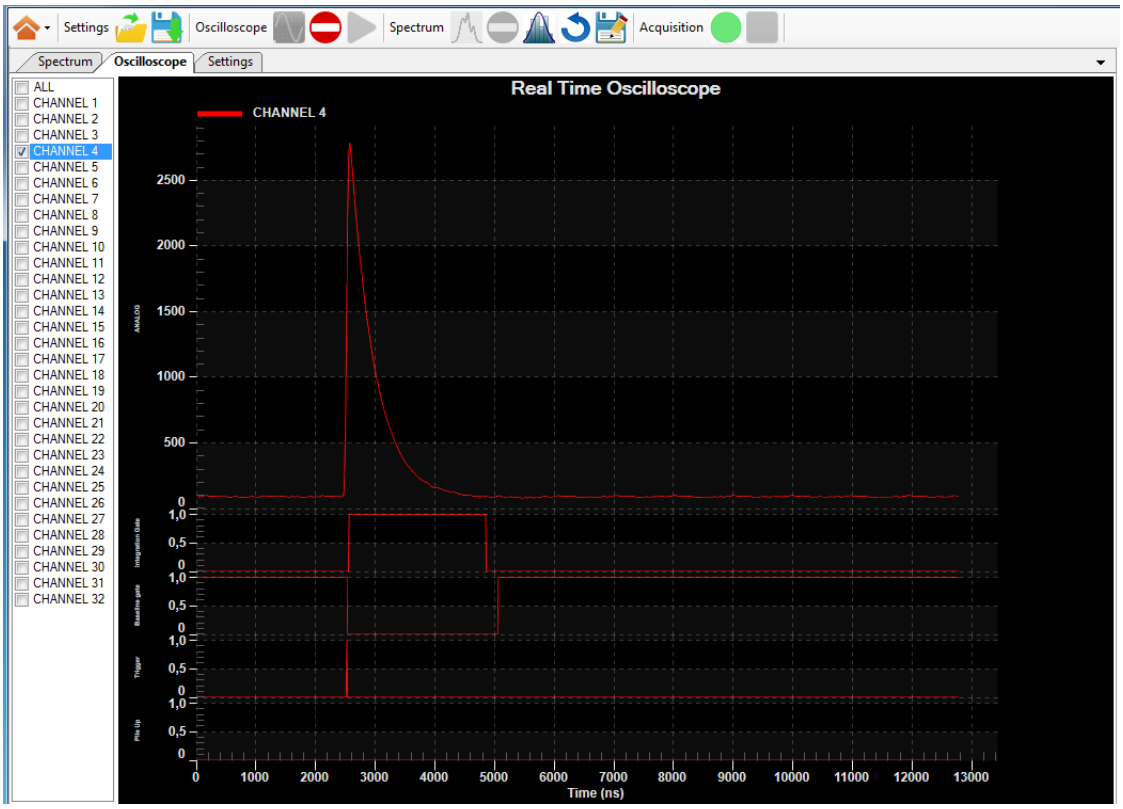


Figure 12.6: the Oscilloscope Tab of the SCI-55X0 Readout Software. Here only signals for channel 4 are displayed.

In order to zoom the waveforms, three zoom modes are available. The zoom mode can be selected pressing a key on your keyboard. The same operation can be done from Menu → View. Options are:

- Area (press Z): enables the zoom on both axes. Drag the mouse to zoom a rectangular area.
- Horizontal Zoom (Press H): enables horizontal zoom. Drag the mouse to zoom on the X-axis.
- Vertical Zoom (Press V): enables vertical zoom. Drag the mouse to zoom on the Y-axis.
- Unzoom (press U): restores the full view of the plot.

The user can:

- print the current view of the plot: Menu → File → Print → Oscilloscope (or press P).
- export the current view of the plot: Menu → File → Export → Oscilloscope (alternatively press X).

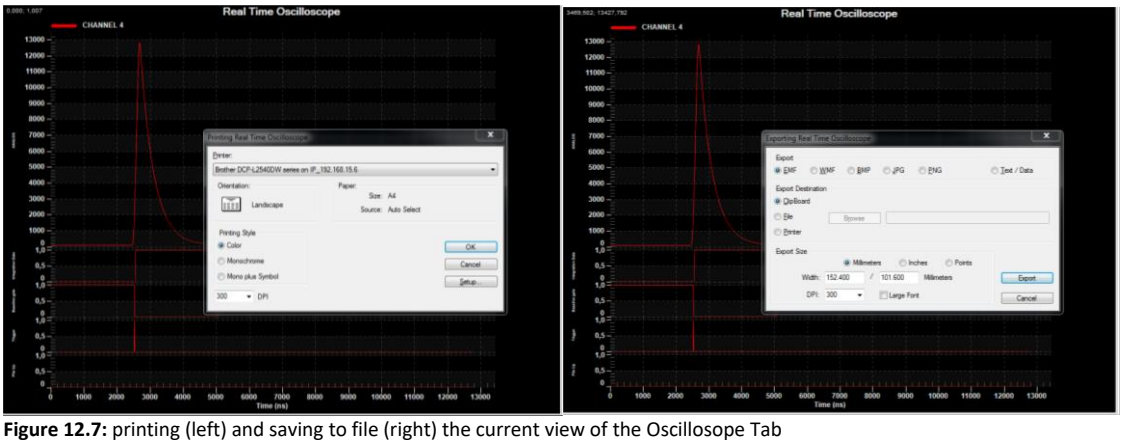


Figure 12.7: printing (left) and saving to file (right) the current view of the Oscillosope Tab

Spectrum Tab

The Spectrum Tab allows to display the cumulative spectrum of each channel calculated in realtime by the board. The charge integration default firmware of the DT5550 generates a 64k bin spectrum for each channel. The rebinning feature can be selected from the Menu → Spectrum → Rebin. The rebinning is applied to all channels.

The spectrum of multiple channels can be displayed on the same plot by checking the relative checkboxes in the channels list on the left of the Spectrum Tab. Each time a channel spectrum is added to the display area, a new label will appear in the legend and a color will be automatically selected for the new spectrum. The plot window is divided in two areas. The main area displays the current zoom of the spectrum. On the bottom area is shown the full view of the spectrum.

In order to zoom the spectrum, three zoom modes are available. The zoom mode can be selected pressing a key on your keyboard. The same operation can be done from Menu → View

- Area (press Z): enables the zoom on both axes. Drag the mouse to zoom a rectangular area.
- Horizontal Zoom (Press H): enables horizontal zoom. Drag the mouse to zoom on the X-axis.
- Vertical Zoom (Press V): enables vertical zoom. Drag the mouse to zoom on the Y-axis.
- Unzoom (press U): restores the full view of the plot.

The spectrum can be displayed in both linear and semi-logarithmic mode. It is possible to switch between Lin/Log mode: Menu → Spectrum → Lin/Log (alternatively Press L).

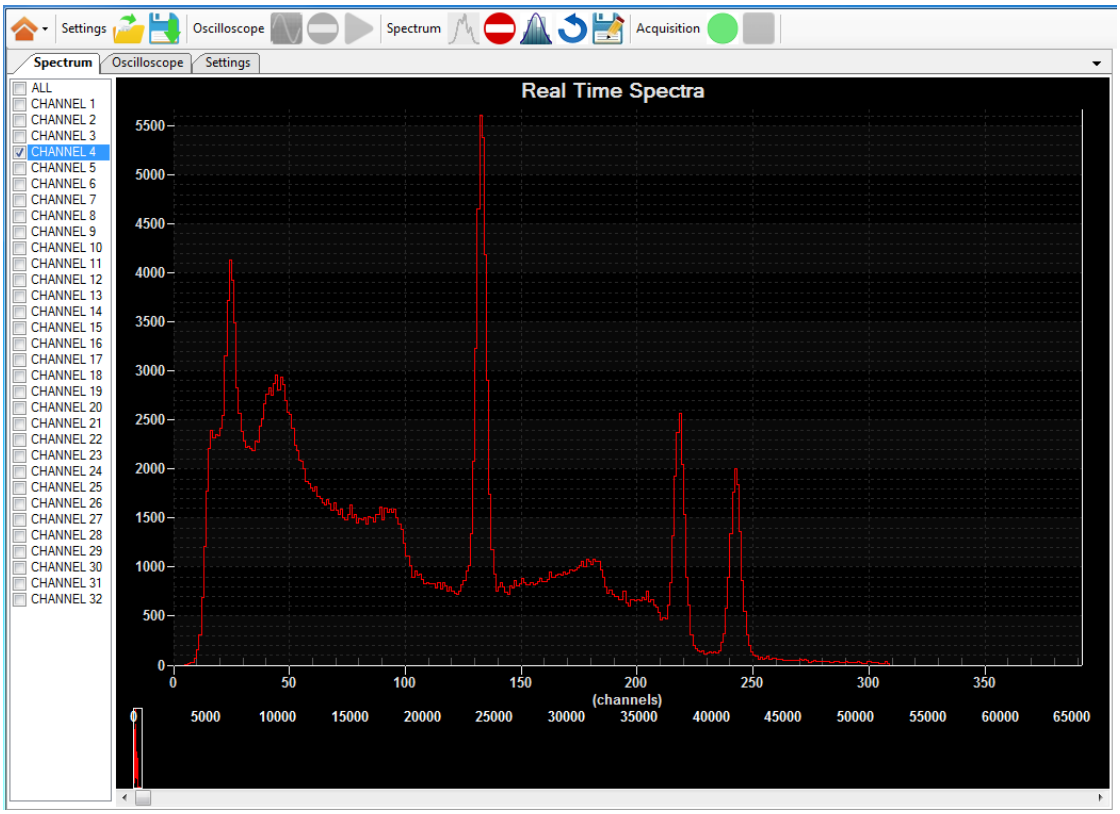


Figure 12.8: the Spectrum Tab of the SCI-55X0 Readout Software. Here only the spectrum for channel 4 is displayed.

It is also possible to change the plot type: Menu → Spectrum → Plot Mode (alternatively press O to cycle between plot modes). Available plot modes are:

- Step
- Line
- Line with interpolation
- Bar
- Area
- Area with interpolation
- Dot
- Dot with Line
- Dot with interpolation

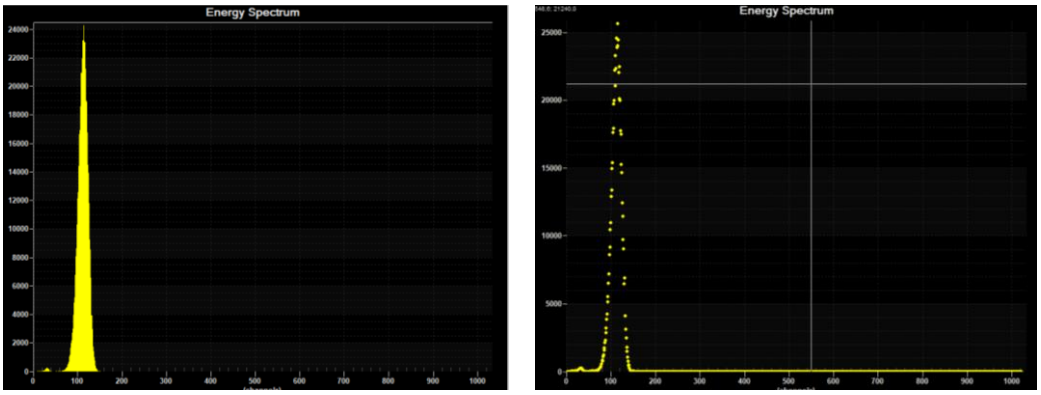


Figure 12.9: spectra shown in different plot modes (left = Area, right = Dot).

The user can:

- print the current view of the plot: Menu → File → Print → Spectrum (alternatively press P).
- save the current view of the plot: Menu → File → Export → Spectrum (alternatively press X).

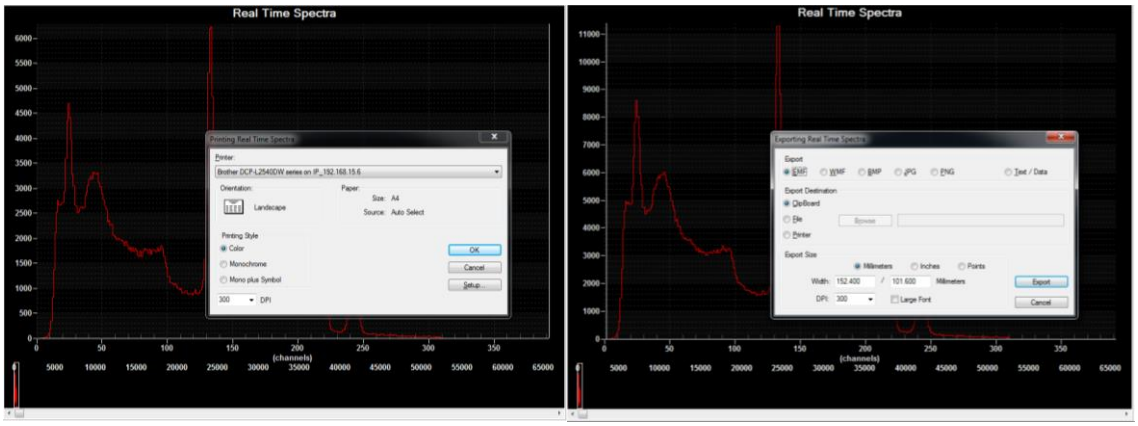
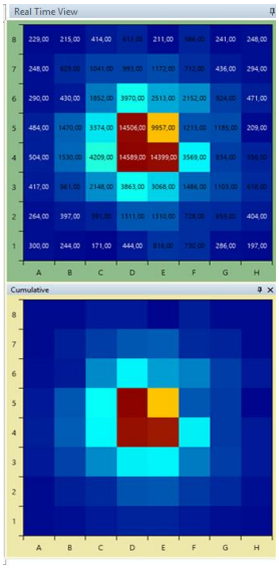


Figure 12.10: printing (left) and saving to file (right) the current view of the Spectrum Tab.

Imaging Module



The Imaging Module displays the realtime and the cumulative 2D heatmaps acquired by the DT5550, basing on the measured energies for each channel. Each pixel of the image is associated to a channel. The user can rearrange the pixels to create a different shape.

The last captured event is displayed on the **realtime view** (top part of the display area). If the frame transfer is selected (Sampling Method = Common, in the general settings), the image displays all pixel captured at the same time.
The bottom part of the display area shows the **cumulative image**.

The acquisition is controlled by the “Start Spectrum” and “Stop Spectrum” buttons in the Control Bar. The “Reset Acquisition” button for spectra in the Control Bar reinitializes also the acquisition of the heatmaps.
The “Save Data” button in the Control Bar allows to save the cumulative energies of all channels in a .csv file whose path can be chosen by the user.

Figure 12.11: the Imaging Module of the SCI-55X0 Readout Software.

How to Perform a Fit

The fitting tool of the SCI-55X0 Readout Software allows to perform gaussian fits of the peaks in the spectrum.

In order to create a new fit, follow the instructions below:

- a channel should be checked in the list of channels on the left of the Spectrum Tab.
- press the “Spectrum Fitting” button in the Control Bar to open the fitting tool at the bottom of the Spectrum Tab.
- insert a value in the Cursor 1 and in the Cursor 2 columns of the table to specify respectively the left and the right boundaries of the fit. On the spectrum the fit boundaries are displayed with white vertical lines and identified with a number corresponding to the table row number. The fit area is shown in green.
- The fitting tool uses the spectrum data between the two cursors to calculate the Mean, the standard deviation (STD) and the Area of the selected region. For each fitted area the results extracted from the gaussian fit are also reported: the mean (Mean Fit), the standard deviation (STD Fit), the full width at half maximum (FWHM), the Resolution (R) and the fitting area (Area Fit).
- A fit can be deleted by selecting the correspondent row in the table and pressing ‘Del’ on your keyboard.

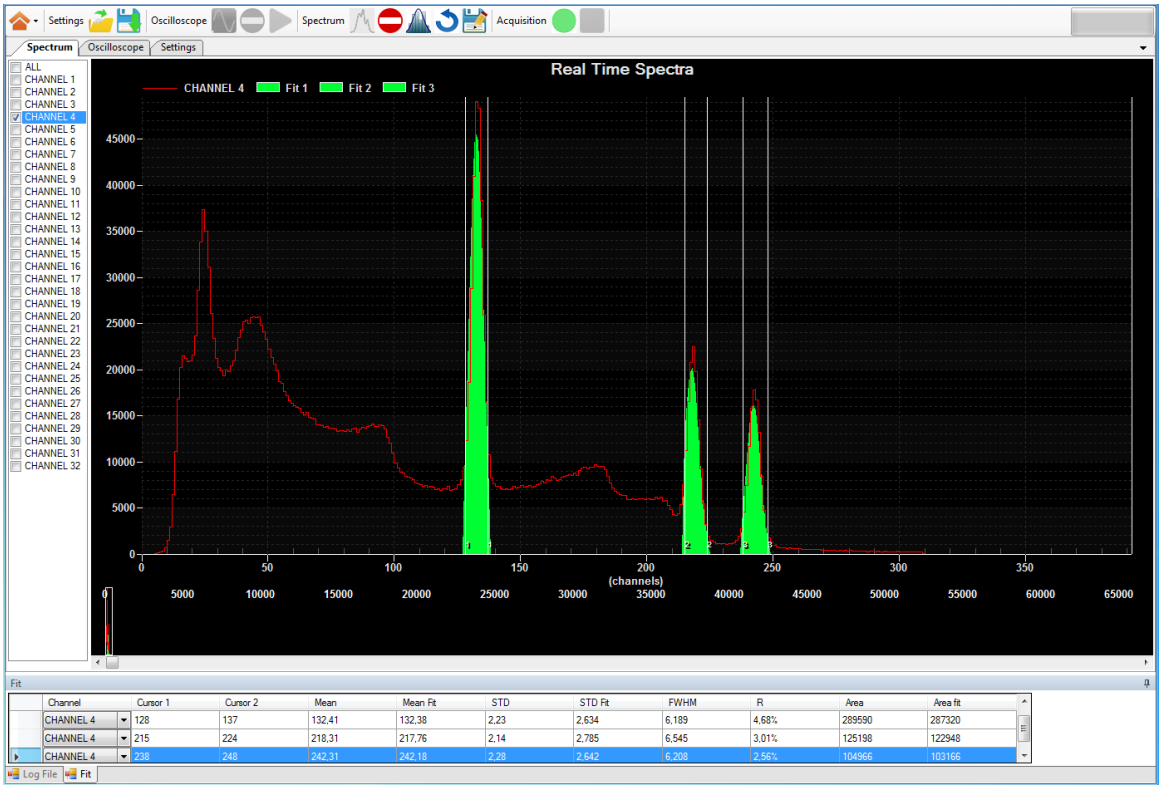


Figure 12.12: the fitting tool of the SCI-55X0 Readout Software.

How to Save Data

The “**Save Data**” button in the Control Bar allows to save both the spectrum and the cumulative image for the enabled channels on the Spectrum Tab. When the button is pressed a first dialog window is visualized to choose the file path for the spectrum data saving. A second dialog window is shown to set the file path for the cumulative image saving.

- The .csv spectrum file is made of a number of rows equal to the number of bin in the spectrum. Each row contains the number of events of the correspondent bin for all the channels visualized in the plot.
- The .csv cumulative image file contains the total energy information for all the channels.

The “**Start/Stop Data Record**” buttons in the Control Bar allow to store on file data from the board.
The “Data Record Configuration” window appears after pressing the “Start Data Record” button. The saved file path can be set by clicking the BROWSE button and the channels data to be saved can be set by checking the correspondent checkboxes in the channel list. The “Data Type” option can be used to choose the type of data to be stored:

- Oscilloscope data: Every time the oscilloscope triggers, the downloaded waveforms from selected channels is dumped on disk (analog and digital)
- Frame data: data from all the channels of the board (channel, energy, time) are stored on the disk event by event, when a trigger signal occurs.

The “Target Mode” option allows to set how to stop data recording:

- Free: record data until “Stop Data Record” button is pressed

- Time: record data for a specified amount of time (not available for the Oscilloscope Data Type)
- Events: record data until a specificied number of events is reached.

The amount of time or the number of events in the respective recording mode can be set in the “Target Value” field.

To start the Oscilloscope or the Frame dumping press the START button.

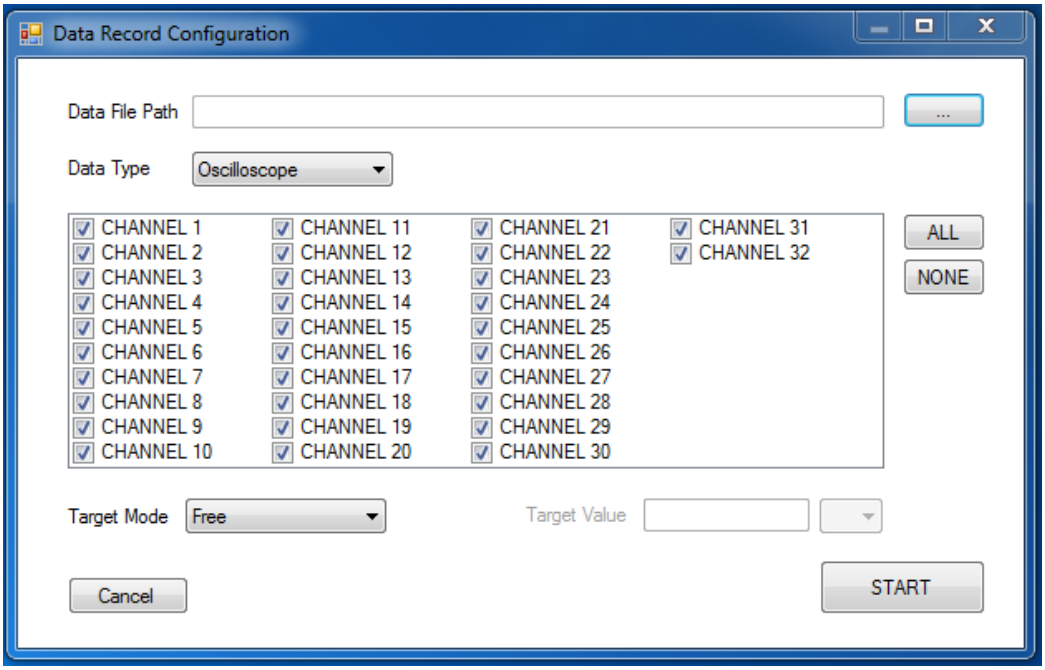


Figure 12.13: the Data Record Configuration window.

Each line of the .csv file for the Oscilloscope Data Type contains the following information:

- Event number;
- Channel number;
- Number of waveform samples;
- Number of waveforms (5: one analog and four digital);
- Waveform values of the five signals.

Each line of the .csv file for the Frame Data Type contains the following information:

- Event id;
- Event timetag;
- Event energy for each channel (energy of not selected channels is zero).

13 Technical Support

CAEN makes available the technical support of its specialists for request concerning the software and the hardware. Use the support form available at the following link:

https://www.caen.it/support-services/support-form/

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