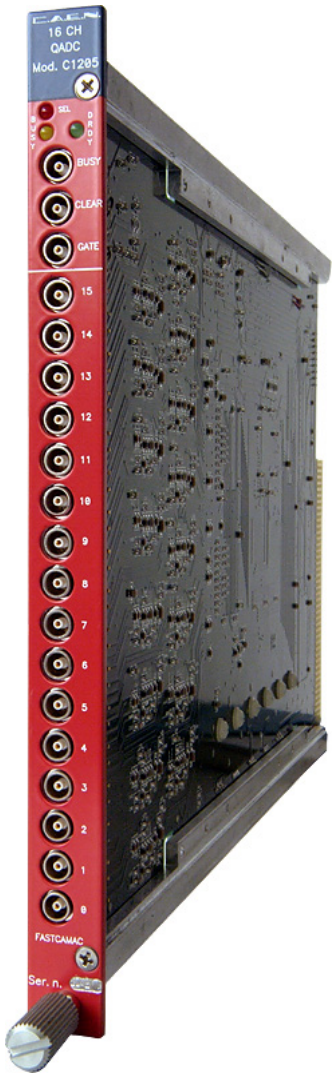
Rev. 05 - 15/10/2009

C1205

16 Channel QDC



CAEN
Tools for Discovery

User Manual

Technical Information Manual

Revision n. 5
13 October 2009

MOD. C1205
16-CHANNEL QDC

NPO:
00116/03:C1205.MUTx/05

CAEN will repair or replace any product within the guarantee period if the Guarantor declares that the product is defective due to workmanship or materials and has not been caused by mishandling, negligence on behalf of the User, accident or any abnormal conditions or operations.

CAEN declines all responsibility for damages or injuries caused by an improper use of the Modules due to negligence on behalf of the User. It is strongly recommended to read thoroughly the CAEN User's Manual before any kind of operation.

CE

CAEN reserves the right to change partially or entirely the contents of this Manual at any time and without giving any notice.

Disposal of the Product

The product must never be dumped in the Municipal Waste. Please check your local regulations for disposal of electronics products.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. Description

1.1. Functional description

The CAEN Model C1205 16-Channel Charge Integrating ADC (QDC) is a single width CAMAC module provided with 16 independent input channels.

The C1205 combines a triple range (the total dynamic range is greater than 17 bits, in three overlapping 12 bit ranges) gated integrator charge to voltage converter, 3 Wilkinson type analog to time converters and a sub nanosecond time digitizer. The result is a high performance, wide dynamic range QDC with low (5.5 μS) dead time.

A clear input and a busy output are also provided. The GATE, clear and busy signals are all NIM levels, with 50 Ohm Lemo style connectors. The 16 inputs are also 50 Ohm Lemo style connectors. The sensitivity at the input connector ranges from 25 fC per count on the low (most sensitive) range, to 1.5 pC per count on the high range. Full scale (on the high range) is greater than 6 nC. Each range extends to at least 4096 counts above the pedestal, providing 12 bit resolution on each range.

This C1205 has been designed for short conversion time and maximum data throughput, as required in state-of-the-art physics experiments. The built in data processing can include sliding scale, pedestal subtraction and threshold suppression to reduce data volume and readout time. The module contains a multiple event buffer that can store up to 51 events. Using FASTCAMAC, this buffer can be read out at up to 30 megabytes/sec.

2. Technical specifications

2.1. Packaging

The Mod.C1205 is housed in 1-unit wide CAMAC module.

2.2. Power requirements

+6 V	2 A
–6 V	2 A
+24 V	450 mA
–24 V	20 mA

2.3. Front panel

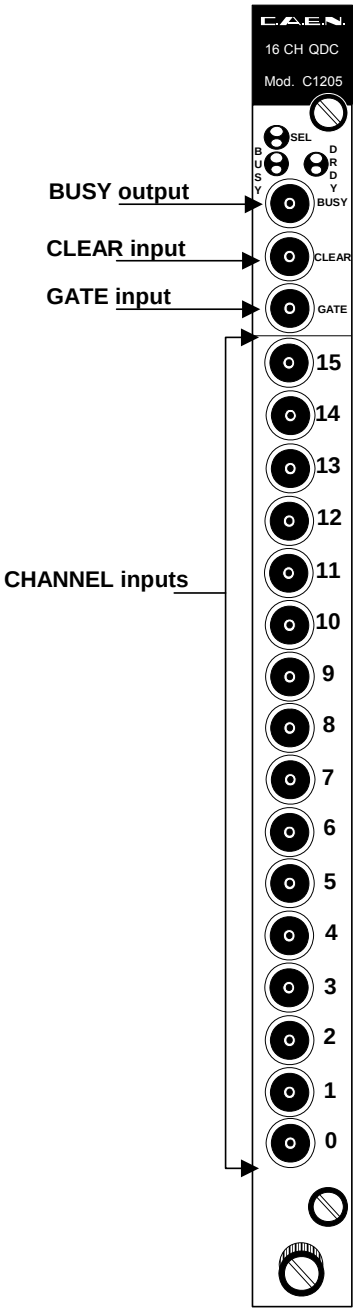


Fig. 2.1 – Mod. C1205 front panel

2.4. External connectors

CLEAR input
Function:
input connector for the CLEAR signal.
Mechanical specifications:
00-type LEMO connector.
Electrical specifications: Std. NIM level signal; 50 Ohm impedance. Width: ≥15 ns.

GATE input
Function:
input connector for the GATE signal.
Mechanical specifications:
00-type LEMO connector.
Electrical specifications: Std. NIM level signal; 50 Ohm impedance. Width: from 10 ns to 500 ns. Timing: the leading edge of the GATE signal must precede the leading edge of the analog input by 10 ns at least.

BUSY output
Function:
output connector for the BUSY signal.
Mechanical specifications:
00-type LEMO connector.
Electrical specifications: Std. NIM level signal. Indicates that the module is BUSY and unable to accept a gate signal.

CHANNEL INPUT connectors
Function:
input connectors for the signals to be converted.
Mechanical specifications:
Sixteen Lemo cable connectors terminated in 50 Ohms +/- 1.5%, clamped at +/- 10 V to accept negative input signals.
Electrical specifications:

Polarity:	negative
Impedance:	50 Ω ± 1.5%
Voltage range for linear response:	0 ÷ -5 V (100 mA input current)
Input sensitivity:	21 fC per count (low range) 160 fC per count (mid range) 1.3 pC per count (high range)
Full scale range:	80 pC full scale (low range) 650 pC full scale (mid range) 6 nC full scale (high range)

2.5. Displays

LEDs:
The yellow led (B) is lighted by BUSY.
The green led (D) is lighted by the event count greater than zero.
The red led (N) is lighted when the module is addressed (N=1).

2.6. Technical specifications table

Table 2.1 – Mod. C1205 technical specifications table

Full Scale Range	80 pC full scale (low range) 650 pC full scale (mid range) 6 nC full scale (high range)
Input sensitivity	21 fC per count (low range) 160 fC per count (mid range) 1.3 pC per count (high range)
Noise	≤1.5 count RMS (high & mid range) low range: from 1.5 counts @ 10 ns Gate to 3 counts @ 500 ns Gate
Input voltage range for linear response	0 ÷ -5 V (100 mA input current)
Integral non linearity	± 5 counts (high & mid range) ± 20 counts (low range)
Interchannel uniformity	2% (typical)
Gate width	From 10 to 500 ns
Conversion time	Typical: 6 µs Worst case: 6.5 µs (3 ranges at the same time)
Fast Clear time	1 µs
Pedestal variation vs GATE width	0.2 counts/ns
Residual pedestal	Non detectable
Thermal stability	+3 counts/C° max

3. CAMAC functions

3.1. CAMAC Function Codes implemented:

C, Z	clear everything, data and registers
F0, A0	Read fifo data, no Q if end of event mark, or no event
F0, A1	read control and status register
F0, A2	read FASTCAMAC control register
F0, A3	read event count
F0, A4	read range select register
F0, A5	read firmware version number
F0, A6	read test counter (read counter, read complement and increment)
F1, A0-15	read channel threshold registers
F2, A0-15	read pedestals for low range
F3, A0-15	read pedestals for mid range
F4, A0-15	read pedestals for high range
F5, A0	FASTCAMAC read
F8, A0	test LAM
F9, A0	clear everything, data and registers
F9, A1	clear data only, not registers
F16, A1	write control and status register
F16, A2	write FASTCAMAC control register
F16, A4	write range select register
F17, A0-15	write channel threshold registers
F18, A0-15	write pedestals for low range
F19, A0-15	write pedestals for mid range
F20, A0-15	write pedestals for high range
F24, A0	disable LAM
F24, A1	disable GATE (hold com FF in reset, busy ON)
F26, A0	enable LAM
F26, A1	enable GATE, release com ff reset
F27, A0	test lam enable/disable status
F27, A1	test gate enable/disable status
F27, A2	test BUSY
F27, A3	test if event ready to read
F30, A0	enter programming mode, see below

3.2. Register descriptions:

3.2.1. Control Register (24 bits)

bit0(lsb)÷7	module ID number (user supplied)
bit8	1 = DC calibration ON, 0 = OFF (default)
bit9÷10	operating mode: 0 = read all range data 1 = auto-range mode 2 = not valid 3 = Sparse data mode (auto range, use channel thresholds)
bit11	1 = enable sliding scale
bit12	1 = enable pedestal subtraction (only valid in auto-range and sparse modes)

bit13	1 = add overflow word only if non zero, 0 = always have overflow word
bit14	1 = diagnostic mode, disable sliding scale subtraction
bit15	1 = block mode, read all complete events in buffer 0 = read one event at a time (default)
bit16	1 = 10 bit resolution mode, 4 μsec dead time 0 = 12 bit resolution mode, 5.5 μsec dead time (default)
bit17	0 = normal Lam, on when any event ready to read (count > 0) 1 = Lam with hysteresis, on when count > 12 (32 in auto range), off count < 6

This register is a 24 bit read/write register and may be used to verify that the CAMAC dataway interface is operational.

3.2.2. FASTCAMAC Control Register (12 bits)

This register follows the FASTCAMAC Control Register and Parameter P specification (version 1.13). the default value for this register is 1, indicating that F5 is a FASTCAMAC level 1 read command.

bit0(lsb)÷1	mode, 0 = normal, 1 = level 1, 2 = level 2, 3 = not valid
bit2	0 = leading edge, 1= both edges
bit3	last word Q response, forced to 0 by module (last word is the end of event marker and contains no data)
bit4÷5	transfer width, forced to 0, ONLY 24 bit width is implemented
bit6	single (0) or multiple module command (1)
bit7÷11	multiple module response order, 0-23

3.2.3. Range Select Register (2 bits)

This register forces the range to the selected range when in AUTO mode. When in sparse mode, the threshold test is performed on the selected range. The default value for this register is 0, which allows normal operation.

bit0(lsb) ÷1	mode, 0= normal, 1= low range, 2= mid range, 3= hi range

3.2.4. Channel threshold registers (12 bits)

This is the sparse data scan threshold for each channel. The data is stored in the fifo only if the data value for the low range is greater than the threshold value. The data is always stored if the range is high or middle. The 16 registers are 12 bits long (0-11), with bit0 the lsb.

3.2.5. Pedestal subtraction registers

This is the value of the pedestal (unsigned 12 bit integer) to be subtracted from the data values. A pedestal value must be provided for each channel and for each of the three ranges (48 values). The resulting data value (after subtraction) is 14 bits long, and is in twos complement notation. The range of data values is from -8190 to +8191. Note that the data value after pedestal subtraction can be negative.

3.2.6. Event Data Record

The complete record consists of the header, up to 48 data words, and the overflow word that contains overflow flags for all 16 channels. If any channel overflows, there will be no data words for that channel, but there will be a bit set in the overflow word. If bit 13 in the

control register is set, the overflow word will only appear in the event record if there is at least one overflow.

3.2.7. Header format (24 bits)

bit0(lsb)÷14	copy of control and status register
bit15	don't care, = 0
bit16-19	event serial number (also used as delay for sliding scale)
bit20-21	don't care, = 0
bit22-23	always =2 (identifies header word)

3.2.8. Data word format (24 bits)

bit0(lsb)÷13	bits 0-13 are the time data (14 bits) from the MTD
bit14÷15	bits 14-15 are the range, low=0, mid=1, high=2, 3=overflow

(during “read all range data” mode, see § 3.2.1, bits14÷15 are meaningless)

bit16÷19	bits 16-19 are the channel number
bit20-22	don't care, = 0
bit22-23	always =0 (identifies data word)

3.2.9. Overflow word format (24 bits)

bit15÷0	overflow flags, =1 if channel is overflowed (no hits in tdc)
bit16÷21	don't care, =0
bit22÷23	always =3 (identifies overflow word)

3.2.10. Separator word format (24 bits)

bit21÷0	always equal to 00FF hex
bit22÷23	always =1 (identifies separator word)

This word separates complete events in the FIFO output buffer and is normally accompanied by Q = 0.
When in block read mode Q = 1, except after the last event in the block, when Q = 0. This word can always be discarded.

3.3. Gate Operation

The gate is a NIM fast level. The pulse length can be as short as 10 ns and as long as 500 ns.

3.4. Dead Time

The start for the ADC run down and the common start for the tdc occur at the end of the gate. The total dead time, including the readout of the tdc is less than 5.5 μsec (from the end of the gate) when in auto range or single range mode. In read all range mode the dead time can be up to 1.6 μsec longer (if no ranges are saturated) longer. Busy is asserted during the dead time (and whenever the ADC is not ready for a gate).
Normally, the firmware program uses a 3.5 μS run down for the TDC. This provides the full 12 bits above pedestal. Setting bit 16 in the control register to 1 shortens the run down time to 2 μsec. This results in only 10 bits above pedestal, 1023 counts instead of 4095. The dead time is shorter by 1.5 μS however, only 4 μS instead of 5.5 μS (when in auto-range or single range mode).

3.5. Lam Operation

The lam is asserted whenever lam is enabled and there is an event in the fifo buffer, ready to be read out. The lam can only be cleared by reading (or clearing) the data. If Lam hysteresis is selected, the Lam is asserted when the event count is > 12 (32 when in single range or auto range mode) and deasserts when the event count is < 6.

3.6. Normal CAMAC readout

Normal CAMAC readout is straightforward. If the event count is zero, the f0, A0 command always returns Q=0. If there is an event stored, the first word to be read (a header) is already at the fifo outputs, waiting to be read. The F0, A0 command gates the data out on to the dataway. The last word of the event is the overflow word. Note that the overflow word is present ONLY if one or more of the channels has overflowed.
Q=1 for the header, the data words and the overflow word. The next read after the overflow (if present) is the separator word, and will always return Q=0. If there is another event stored in the fifo, the next read will return the header of that event, with Q=1. In this mode events are read one at a time, with Q=0 between each event.

3.7. Block mode CAMAC readout

Block mode CAMAC readout is selected by bit 15 in the control register. If the event count is zero, the f0, A0 command always returns Q=0. If there is an event stored, the first word to be read (a header) is already at the fifo outputs, waiting to be read. The F0, A0 command gates the data out on to the dataway. The last word of the event is the overflow word. Note that the overflow word is present ONLY if one or more of the channels has overflowed.
Q=1 for the header, the data words and the overflow word. The next read after the overflow (if present) is the separator word. In Block mode, if there is another event in the buffer waiting to be read, Q=1. If there are no more complete events in the FIFO, Q=0.

3.8. FASTCAMAC readout

FASTCAMAC readout is similar to normal CAMAC, both single event and block mode transfers are implemented. Only 24 bit read transfers are implemented. There are no 48 bit reads, and no FASTCAMAC writes. Level 1 allows transfers at up to 7.5 Mbytes/sec. Level 2 can operate at the maximum rate of 100 ns per transfer, or 30 Mbytes/sec (both S1 edges are used to transfer data), or any other allowed FASTCAMAC rate, either single edge or double edge. Multiple module transfers are also implemented, for both level 1 and level 2.
All FASTCAMAC commands use F5, A0. The FASTCAMAC options are selected by writing to the FASTCAMAC control register.

4. Operating modes

4.1. General information

The Model C1205 16-CHANNEL CHARGE-INTEGRATING ADC allows the analog-to-digital conversion of up to 16 independent charge sources.
The NIM GATE signal is converted to emitter coupled logic (ECL) levels and radially distributed to the 16 ADC channels using high speed ECL logic. The 16 input signals are integrated during the GATE interval. The GATE duration can range from 10 nS to 500 nS. The input signals are integrated and converted to a time interval by a bipolar monolithic integrated circuit. This chip splits the input current into 3 parts in the approximate ratio 64:8:1. Each part is integrated (stored on a capacitor) by an independent (and identical) charge to time converter. At the end of the GATE the charge is removed from the storage capacitor by a 20 μA rundown current. A comparator produces an output signal whose width is the time above threshold of the voltage on the storage capacitor. The time interval between the end of the GATE (when the run down begins) and the trailing edge of the comparator output (when the capacitor voltage returns to its resting value) is the measure of the charge integrated during the GATE.
The basic gain of the bipolar monolithic integrated circuit is 1 nS per 20 fC. The chip requires at least 100 ohm input impedance for best noise performance. In order to provide 50 ohm input impedance at the connector, an impedance matching circuit splits the signal, 2:1, reducing the gain to about 40 fC per nS.
The maximum linear input current at the bipolar monolithic integrated circuit is 50 mA, corresponding to 100 mA (a 5V signal amplitude) at the input connector. The input impedance at the connector is 50 ohms up to 10 V, and about 37 ohms above 10 V, due to clamping circuits that protect the chip.
The outputs of the three charge to time converters are combined with an exclusive OR circuit into one composite signal which is the output to the TDC channel. This signal will have 3 transitions to measure, corresponding to the time over threshold for each of the 3 comparators, one for each range.
The pedestals for the 3 ranges are adjusted so that the high range completes the rundown first, followed by the middle and low ranges. A negative input signal will cause these 3 transitions in the composite signal to spread apart, with the low range being the first to extend beyond the common start time out.
Data words are stored into consecutive locations of a RAM-type memory readable via CAMAC. As soon as the last word has been stored a LAM signal becomes true, and the conversion values can be read performing the appropriate CAMAC-function sequence.

4.2. Operating instructions

4.2.1. Basic Operation

The minimum necessary to operate the module after power up is to clear everything (F9, A0) and enable the GATE (F26, A1). This will give basic multi-range mode with all ranges read out, and the sliding scale disabled.
This will result in 50 data words for each GATE. To reduce the record size, use the control register (F16, A1) to select multi-range mode (control register bit 9, = 512) or select a single range with the range select register (F16, A4). Also select overflow word only if not zero (control register bit 13, = 8192). This will reduce the data record to 17 words. If not all channels are needed, disable individual channels by selecting sparse

mode, and setting the channel thresholds to 0 for each channel in use, and to 4095 for each channel to be disabled. The data record will be reduced to one (the header) plus the number of channels in use.

4.2.2. Reloading the FPGA program from the EEPROM

All of the sequencing and control logic is implemented in the Xilinx 4013 FPGA. The FPGA is RAM based, and must be reloaded each time that power is applied. This is normally transparent to the user, and a few hundred milliseconds after power is applied, the FPGA is ready to use.
The flash memory chip is large enough to store two complete programs for the FPGA, the normal program, and an alternate program. To load the alternate program, follow this sequence of CAMAC instructions.
F30, A0 this enables the FPGA programming mode, with the normal program selected. The FPGA is cleared and a limited set of CAMAC commands are available.
F21, A0 this selects the alternate program, omit this step to reload the normal program
F25, A0 begin programming from the selected part of the EEPROM
F14, A0 test FPGA INIT line, Loop on this command until Q = 1
F13, A0 test FPGA DONE line. Loop on this command until Q = 1
F9, A0 exit programming mode. The special instructions are disabled, except for F30, A0. The CAMAC commands programmed into the FPGA are now operational.
The normal program is the current version. The alternate program is the same. This feature is reserved for future enhancements that may not be compatible with the normal firmware program.
The flash memory chip is in a socket. This allows simple field updates of the firmware by replacing the chip.
Firmware updates, when available will be offered at no charge.

CAEN GmbH
Brunnenweg 9
64331 Weiterstadt
Germany
Tel. +49 (0)212 254 4077
Mobile +49 (0)151 16 548 484
info@caen-de.com
www.caen-de.com

CAEN Technologies, Inc.
1 Edgewater Street - Suite 101
Staten Island, NY 10305
USA
Phone: +1 (718) 981-0401
Fax: +1 (718) 556-9185
info@caentechnologies.com
www.caentechnologies.com

CAEN S.p.A.
Via Vetraia 11
55049 - Viareggio
Italy
Phone +39 0584 388 398
Fax +39 0584 388 959
info@caen.it
www.caen.it

CAENspa INDIA Private Limited
B205, BLDG42, B Wing,
Azad Nagar Sangam CHS,
Mhada Layout, Azad Nagar, Andheri (W)
Mumbai, Mumbai City,
Maharashtra, India, 400053
info@caen-india.in
www.caen-india.in