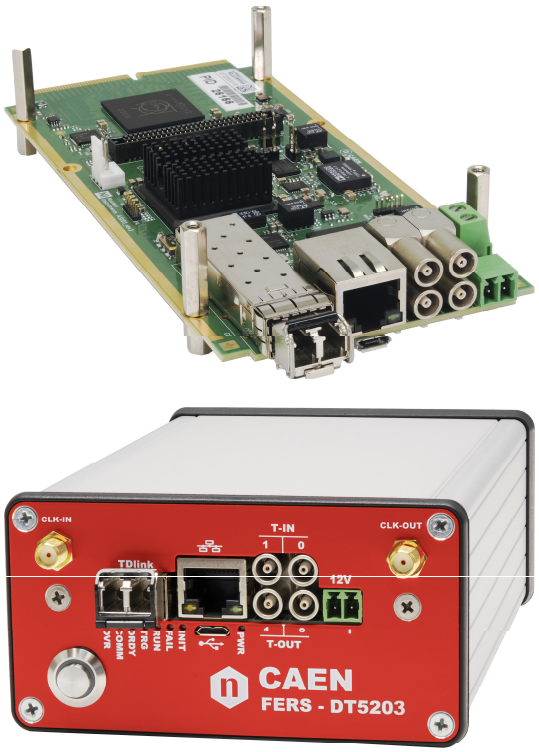
Rev. 0 - Oct 18th, 2023

A5203(B)/DT5203

64/128 Channel picoTDC Unit for FERS-5200



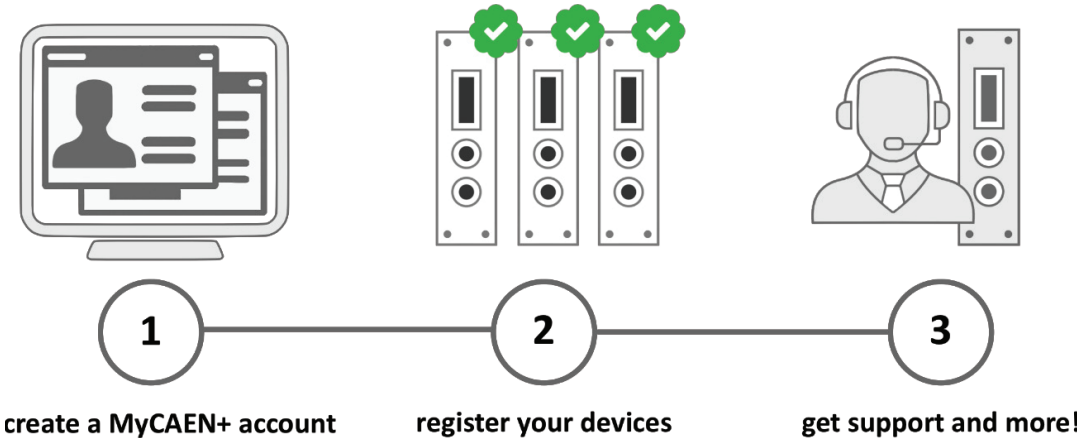
CAEN
Tools for Discovery

User Manual
UM9085

Register your device

Register your device to your **MyCAEN+** account and get access to our customer services, such as notification for new firmware or software upgrade, tracking service procedures or open a ticket for assistance. **MyCAEN+** accounts have a dedicated support service for their registered products. A set of basic information can be shared with the operator, speeding up the troubleshooting process and improving the efficiency of the support interactions.

MyCAEN+ dashboard is designed to offer you a direct access to all our after sales services. Registration is totally free, to create an account go to https://www.caen.it/become-mycaenplus-user and fill the registration form with your data.



https://www.caen.it/become-mycaenplus-user/

Before you Start

- **The A5203B unit does not present heat sinks for the picoTDC chips. As to avoid the board damage, it must be properly ventilated, either with a custom-made fan, or with the A5270 FERS-5200 fan. A5203 units (non-boxed version) do not need an external fan, but ventilation is still recommended.**
- **The A5203(B) edge connector(s) does not allow to directly plug ribbon, or coaxial, cables on the inputs. An adapter is needed.**
  The adapter can be custom made, the A5255 or the A5256 FERS-5200 adapter. The latters can be plugged only on A5203 unit types.
  In case of the A5203B, a custom made adapter must be used. As an alternative, the A5255 or A5256 adapters can be plugged on one of the two edge connectors, but with the drawback of a reduced channel number usable.
- **The A5203(B)/DT5203 channel inputs accept LVDS signals with 1.2 V common mode, and 1.45 V absolute voltage.**
- **The A5203(B)/DT5203 channel inputs do not present any bias, and can toggle when not driven. As to avoid the readout bandwidth saturation, the not-used channels must be disabled.**
- **It is not possible to test the A5203(B) unit without adapters, and no input test signals are available on the unit. As to test/use the board, the minimum setup required should contain:**
  - one adapter
  - at least two LVDS signals (one for the Tref-start, and one for the stop).
- **Take care to not drag nor beat the non-boxed A5203(B) unit. The electronics is not protected, and can easily be torn out.**

Purpose of this Manual

This document contains the hardware description of the A5203(B) and DT5203 FERS-5200 units, their principle of operation as well as all the instructions to start using them in a correct and easy way. This User Manual is compliant with Janus 5203 version 2.5.0 (Beta Release) and A5203(B)/DT5203 FPGA firmware version 1.4 (Build = 7706).

Change Document Record

Date	Revision	Changes
Oct 18th, 2023	00	Initial Release

Symbols, Abbreviated Terms and Notation

ADC	Analog-to-Digital Converter
ASIC	Application Specific Integrated Circuit
DAQ	Data Acquisition
DCR	Dark Count Rate
FERS	Front-End Readout System
FERS-CB	FERS Collector Board
FPGA	Field Programmable Gate Array
FSR	Full Scale Range
GEM	Gas Electron Multiplier
GUI	Graphical User Interface
HG	High Gain
HV	High Voltage
INL	Integral Non-Linearity
LG	Low Gain
LSB	Least Significant Bit
LVTTL	Low Voltage TTL
MUX	Multiplexer
OS	Operating System
PC	Personal Computer
PCB	Printed Circuit Board
PHA	Pulse Height Analysis
QD	Charge Discriminator
RF	Radio-Frequency
RMS	Root-Mean-Square
SiPM	Silicon Photo-Multiplier
TDC	Time to Digital Converter
ToA	Time of Arrival
TCP	Transmission Control Protocol
TD	Time Discriminator
ToT	Time over Threshold
USB	Universal Serial Bus
ZS	Zero Suppression

Reference Documents

[RD1] DS9756 - A52xx Accessories for A5203 FERS-5200 Units

[RD2] PicoTDC, https://kt.cern/technologies/picotdc

[RD3] UM9636 – Janus 5203 CAEN A5203(B)/DT5203 Readout Software User Manual

[RD4] UM8977 - DT5215 User Manual

[RD5] https://www.digikey.it/product-detail/it/xilinx-inc/XC7A75T-1FGG676C/XC7A75T-1FGG676C-ND/5039539

All CAEN documents can be downloaded at:
`www.caen.it/support-services/documentation-area`

Manufacturer Contacts

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Limitation of Responsibility

If the warnings contained in this manual are not followed, CAEN will not be responsible for damage caused by improper use of the device. The manufacturer declines all responsibility for damage resulting from failure to comply with the instructions for use of the product. The equipment must be used as described in the user manual, with particular regard to the intended use, using only accessories as specified by the manufacturer. No modification or repair can be performed.

Disclaimer

The information contained herein has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies. CAEN SpA reserves the right to modify its products specifications without giving any notice; for up to date information please visit www.caen.it.

Made in Italy

We remark that all our boards have been designed and assembled in Italy. In a challenging environment where a competitive edge is often obtained at the cost of lower wages and declining working conditions, we proudly acknowledge that all those who participated in the production and distribution process of our devices were reasonably paid and worked in a safe environment (while this is true for the boards marked ”MADE IN ITALY”, we cannot guarantee for third-party manufactures).

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List of Tables

Safety Notices

N.B. Read carefully the "Precautions for Handling, Storage and Installation document provided with the product before starting any operation.

The following HAZARD SYMBOLS may be reported on the unit:

	Caution, refer to product manual
	Caution, risk of electrical shock
	Protective conductor terminal
	Earth (Ground) Terminal
	Alternating Current
	Three-Phase Alternating Current

The following symbol may be reported in the present manual:

	General warning statement

The symbol could be accompanied by the following terms:

- **DANGER**: indicates a hazardous situation which, if not avoided, will result in serious injury or death.
- **WARNING**: indicates a hazardous situation which, if not avoided, could result in death or serious injury.
- **CAUTION**: indicates a situation or condition which, if not avoided, could cause physical injury or damage the product and / or the surrounding environment.

THIS DEVICE MUST NOT BE USED BY UNTRAINED PERSONNEL

CAUTION: Do Not Operate without a proper shielding (A5203(B) only) or without Covers (DT5203 only).

THE A5203(B) BOARD COMES WITHOUT ENCLOSURE. THE FINAL USER MUST CONSIDER APPROPRIATE SHIELDING TO AVOID ANY ELECTRICAL SHOCK OR FIRE HAZARD.

TO AVOID ELECTRIC SHOCK OR FIRE HAZARD, DO NOT OPERATE THE DT5203 WITH COVERS OR PANELS REMOVED

CAUTION: Do Not Operate in Wet/Damp Conditions

TO AVOID ELECTRIC SHOCK, DO NOT OPERATE THIS PRODUCT IN WET OR DAMP CONDITIONS

CAUTION: Do Not Operate in an Explosive Atmosphere

TO AVOID INJURY OR FIRE HAZARD, DO NOT OPERATE THIS PRODUCT IN AN EXPLOSIVE ATMOSPHERE

CAUTION: Avoid potential hazards

USE THE PRODUCT ONLY AS SPECIFIED.
SERVICE PROCEDURES CAN BE PERFORMED BY QUALIFIED PERSONNEL ONLY

Please, contact the Techincal Support in case Service Procedures are required.

DO NOT OPERATE WITH SUSPECTED FAILURES.
IF YOU SUSPECT THIS PRODUCT TO BE DAMAGED, PLEASE CONTACT THE TECHNICAL SUPPORT

See Chap. **16** for the Technical Support contacts.

IT IS UNDER THE RESPONSIBILITY OF THE CUSTOMER AN IMPROPER USE OF THE PRODUCT

1 Introduction

FERS-5200 is a front-end readout system designed for the readout of large detector arrays, such as SiPMs, multi-anode PMTs, Silicon Strip detectors, Wire Chambers, GEMs, Gas Tubes and others. FERS-5200 is a distributed and scalable system, where each unit is a small card that houses 64 or 128 channels possibly with preamplifier, shaper, discriminator, ADC, trigger logic, synchronization, local memory and readout interface. In most cases, the front-end is based on ASIC chips that allow for high density, cost effective integration of multi-channel readout electronics into small size and low power consumption modules. FERS is a flexible platform: combining the same back-end (i.e. readout architecture and interface) with different types of front-end to fit a wide range of detectors.

The **A5203** (and **DT5203**, which is the boxed version for desktop use) is a member of the FERS-5200 family. It uses the picoTDC chip (produced by CERN) for high-resolution multi-hit time measurements on 64 channels. The **A5203B** houses an additional mezzanine card with a second picoTDC chip, thus implementing a 128 channel TDC module.
Each readout channel accepts LVDS signals[1] and measures the time stamp of the rising egde, or both rising and falling edges, with a programmable LSB with maximum resolution of 3.125 ps. In this way, the unit is able to reconstruct the Time of Arrival (ToA) of signals as an absolute timestamp (Trigger Matching and Streaming acquisition modes) or as a ΔT with respect to a common Tref pulse (Common Start/Stop acquisition modes). The picoTDC can also acquire Time over Threshold (ToT) information and combine it with the edge time stamp. The ToT allows for amplitude estimation, energy spectrum reconstruction, and timing walk correction. The latter permits to achieve optimal timing resolution with no need of Constant Fraction Discriminators (CFDs).

For small setups a single A5203(B)/DT5203 unit can be used stand alone, without any additional hardware, by simply connecting the unit to a PC via USB 2.0 or Ethernet 10/100T. For large readout systems, a flexible and scalable network of units can be created by means of the high speed optical link called TDlink. The TDlink system supports up to 128 FERS units to be connected to and managed by one **DT5215** FERS Data Concentrator Module **[RD4]**. The TDlink supports optical daisy chaining and provides slow control, high speed data readout, synchronization between the units (clock and sync distribution), as well as command broadcasting for triggers, time resets, etc.

The A5203(B)/DT5203 is fully supported by the CAEN **Janus 5203** open source software for Windows® and Linux® **[RD3]**. Janus 5203 can run in console mode (C program, without graphics) or connected to a GUI written in Python. The GUI has configuration and run control panels that simplify the data acquisition management. Both console and GUI modes permits to acquire data from multiple boards, manage the event building and timing histograms (ToA and/or ToT), display data statistics (hit rate, throughput, etc…), plot histograms, and save output, including spectra and list files with the acquired timing data.

[1] Max common mode = 1.2 V Max absolute voltage = 1.45 V

In **Tab. 1.1**, the list of accessories and related products of the A5203(B)/DT5203 boards are reported.

Adapters	Description
A5255	Header adapter for A5203(B)/DT5203: 4 x 34 contacts, 1.27 mm pitch ribbon cables (i.e. 4 x 17 × 2 2.54 mm Headers). Aux LEMO input (NIM/TTL, 50 Ω) for alternative driving of channel 0
A5256	16+1 channel single threshold, 8+1 channel dual threshold fast leading edge discriminator for A5203(B)/DT5203. Accepts positive or negative analog inputs on LEMO 00 connectors, 50 Ω terminated. SW programmable individual threshold (-1.25 V to +1.25 V, 14-bit DACs)
Cables	**Description**
A5260	Remotization cable for FERS-5200 boards - 50 cm
A5260B	Remotization cable for FERS-5200 boards - 100 cm
Rel. Products	**Description**
DT5215	Concentrator Board for FERS-5200
A5270	Fan for FERS-5200 Units

Tab. 1.1: CAEN accessories for the A5203(B)/DT5203 unit.

2 Acquisition Modes Overview

The A5203(B)/DT5203 can work in four ***acquisition modes***:

- **COMMON START**: A signal on channel 0 (default reference channel in Janus 5203 software) identifies the common start of the time measurement, and the hits on the other channels (from 1 to 63, or from 1 to 127) represent the individual stops. Only the first hit of each channel after the start time is taken as individual stop, the following hits in the same trigger window are discarded (see **Fig. 2.1**).
  $\Delta T_{N,start} = T_N - T_0$

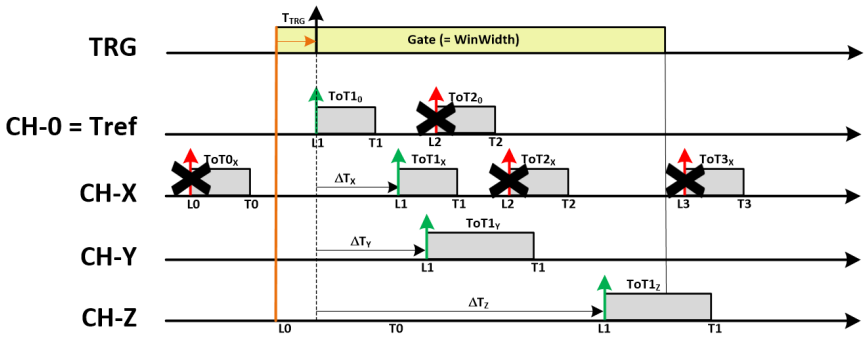


Fig. 2.1: Schematic diagram of Common Start Acquisition Mode: hits 2_0 and 2_X are rejected being multiple hits in the same trigger window, 0_X and 3_X are rejected because outside the trigger window.

- **COMMON STOP**: This mode is symmetric with respect to the COMMON START. Individual starts are acquired on each channel, and a common stop is taken on channel 0. As in the previous acquisition mode, the multi-hit recording is not possible: only the last hit before the common stop is saved.
  $\Delta T_{N,stop} = T_0 - T_N$
- **STREAMING**: the A5203 works as a time stamper, recording the absolute timestamps of all the incoming hits (in the same or more channels), over a dynamic range of 64 bits (i.e. $\sim$1.83 years) and to up to 3.125 ps of picoTDC resolution. For this acquisition mode, no trigger is needed.
- **TRIGGER MATCHING**: Multiple hits, in the same or more channels, inside a trigger window are recorded (see **Fig. 2.2**).
  This acquisition mode presents less constraints than the COMMON START/STOP ones, as the trigger window is not clipped to a reference channel. All time measurements are referred to the Coarse Trigger Time Stamp (LSB = 25.6 ns), while the relative time between the hits keeps the TDC timing resolution (minimum LSB = 3.125 ps).

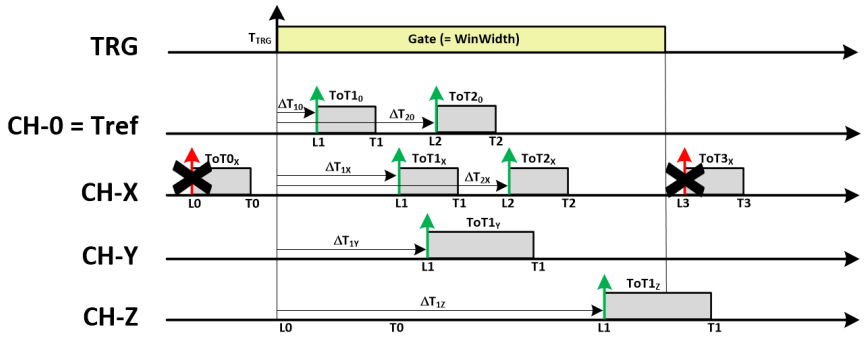


Fig. 2.2: Schematic diagram of Trigger Matching Acquisition Mode: hits 0_X and 3_X are rejected because outside the trigger window.

The trigger can be given via the T0-IN, T1-IN connectors or the edge connector, or can be generated by the FPGA. The timestamps of the hits are given with the FPGA resolution of 25.6 ns on a dynamic of 56 bits. To get high resolution timings, a post processing of the events recorded is needed.

3 Technical Specifications

TDC INPUTS	**A5203/DT5203:** 64 channels (1 edge connector type HSEC8-170) **A5203B:** 128 channels (2 edge connectors type HSEC8-170) Mating connector: Samtec HSEC8-170-01-S-DV Input Type: LVDS signals Input Voltage: Min = -40 mV Max = +1450 mV Common Mode: Min = +70 mV Max = +1200 mV Differential Voltage: Min = +140 mV Max = +450 mV Input Termination: 100 Ω
INPUT ADAPTERS	**A5255:** 4 × 34 contacts, 1.27 mm pitch ribbon cables (i.e. 4 × 17 × 2 2.54 mm Headers). Aux LEMO input (NIM/TTL, 50 Ω) for alternative driving of channel 0 **A5256:** 16+1 channel single threshold, 8+1 channel dual threshold leading edge discriminator. Analog inputs on LEMO 00, 50 Ω, positive or negative. SW programmable individual threshold (-1.2 V to +1.2 V, 12 bit DACs) By default, the desktop version DT5203 comes with an A5255 as front panel.
TIMING RESOLUTION	LSB = 3.125 ps ΔT_{RMS} = ∼5 ps. Tested with LVDS signals, two passive splitters and delay cables. ΔT_{RMS} = ∼7 ps. Tested with pulse generator (1 Vpp, 0.8 ns rise/fall pulses), one passive splitter, delay cables and A5256 fast discriminator ΔT_{RMS} = ∼20 ps with variable amplitude pulses (30 mV to 1 V) and walk correction by ToT
DYNAMIC RANGE	Time measurement dynamic range in picoTDC*: • Leading Edge only: T_{LEAD} = up to 26 bits (FSR = ∼210µs) • Leading + Trailing Edge: T_{LEAD} / T_{TRAIL} = up to 26 bits (FSR = ∼210µs) • Leading + ToT8: T_{LEAD} = up to 19 bits, ToT = 8 bits (LSB size and FSR can be programmed) • Leading + ToT11: T_{LEAD} = up to 16 bits, ToT = 11 bits (LSB size and FSR can be programmed) Coarse time stamp in FPGA con be combined with picoTDC data to extend the full scale range of the time measurement to a maximum dynamic of 64 bit (STREAMING acquisition mode). * dependent on the Header-Trailer selected option (see Sec.**9.6**)
ACQUISITION MODES	**Common Start** Output Data: T_{LEAD} or T_{LEAD}+ToT **Common Stop** Output Data: T_{LEAD} or T_{LEAD}+ToT **Streaming** Output Data: T_{LEAD} or T_{LEAD}+T_{TRAIL} (or T_{LEAD}+ToT, **COMING SOON**) **Trigger Matching** Output Data: T_{LEAD} or T_{LEAD}+T_{TRAIL} or T_{LEAD}+ToT
FPGA TRIGGER TIME STAMP	- 56-bit counter, 25.6 ns step - Up to 128 boards can be synchronized with the DT5215 FERS-CB by sending a time stamp reset signal via TDlink
FRONT PANEL I/Os	**T0-IN, T1-IN**: LEMO-00 connector, NIM or TTL (terminated to 50 Ω) **T0-OUT, T1-OUT**: LEMO-00 connector, TTL (50 Ω termination required) Jumpers for IN-OUT bypass and termination removal (daisy chaining). **Functions (SW programmable)**: Trigger, Acquisition Start/Stop, Sync, Busy, Veto, Signal inspection, etc… T0/T1 inputs can be used to drive TDC - Ch0 = Tref (possible degradation of the resolution because of the FPGA temperature dependence)

FRONT PANEL LEDs	GREEN: Power-ON, Init-Done, Run, Trigger, Data Ready, T0-IN, T1-IN ORANGE: Event Overrun (rejected triggers because received while busy) RED: Failure (missing clock, over-temperature, etc…)	
INTERNAL PULSER	Fast LVDS output (one signal only) with programmable frequency and width, for debug purposes.	
COMMUNICATION INTERFACES	**USB** USB2.0 microUSB connector. Bandwidth = ∼3 MB/s **TDlink** Optical link (∼60 MB/s) with synch distribution. Allows for multi-board synchronization, slow control and data readout. Data Concentrator **DT5215** required.	**Ethernet** Ethernet connector, type RJ-45. Supports 10/100 Mbit/s connection to a PC. Bandwidth = ∼2.5 MB/s
FIRMWARE	Firmware of FPGA upgraded via USB or Ethernet (or TDlink **COMING SOON**) Firmware of µC upgraded via Ethernet only	
SOFTWARE	**Readout SW** Fully controlled by the Janus 5203 open source software for Windows® and Linux®. It can run in console mode (C program, with console commands and gnuplot display for plots) or connected to a GUI (Python) that implements user friendly configuration panels and run controls. Janus 5203 can acquire, plot and save output files with ToA, ToT histograms, as well as list files (trigger timestamp, ToA and ToT for each channel). **Web Interface** Board information and monitoring, Ethernet configuration.	
MECHANICAL	**Dimensions** 73.0 W × 30.0 H × 174.5 L mm^3 73.0 W × 25.0 H × 174.5 L mm^3 106.1 W × 56.1 H × 166.1 L mm^3	**Weight** 140 g (A5203 with spacers mounted) 163 g (A5203B with spacers mounted) 503 g (DT5203)
ENVIRONMENTAL	**Environment**: Indoor use **Operating Temperature**: 0°C to +40°C [1] **Storage Temperature**: –10°C to +60°C **Operating Humidity**: 10% to 90% RH non condensing **Storage Humidity**: 5% to 90% RH non condensing **Altitude**: < 2000m **Pollution Degree**: 2 **Overvoltage Category**: II **EMC Environment**: Commercial and light industrial **IP Degree**: IPX0 Enclosure, not for wet location	
REGULATORY COMPLIANCE	**EMC** CE 2014/30/EU Electromagnetic compatibility Directive	**Safety** CE 2014/35/EU Low Voltage Directive
POWER REQUIREMENTS	Single power supply: +12 V. Accepted voltage range: MIN +7 V, MAX +15 V (110V/220V AC/DC converter provided with Desktop version only.)	
POWER CONSUMPTIONS	700 mA @ +12 V, i.e. ≈ 8.4 W *t.b.d.*	(A5203/DT5203 - 64 channels) (A5203B - 128 channels)

Tab. 3.1: Specification table.

[1] In case of A5203, for T ≥ +25°C, or in case the board is placed in an enclosed environment - like a box without air flow, the user must use an external fan unit to cool down the board temperature.
For the A5203B an external ventilation is required in all environmental conditions.

4 Packaging and Compliancy

4.1 A5203(B)

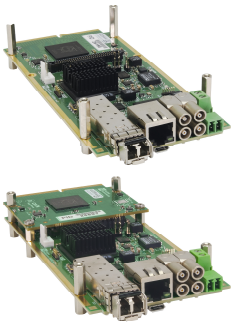
The A5203(B) is available as an electronic board without covers, with metal spacers that make possible to put multiple A5203(B) on top of each other (A5203 module dimensions: 73.0 W $\times$ 30.0 H $\times$ 174.5 L mm^3, A5203B module dimensions: 73.0 W $\times$ 25.0 H $\times$ 174.5 L mm^3). The A5203(B) is mostly intended to be integraded into more complex systems.

WARNING: A5203(B) is an ESD sensitive item. Handling without ESD protective covering shall be performed only into approved ESD Protected Area (EPAs).

WARNING: A5203(B) complies with the EMC directive only if installed in a CE marked system.

The device is inspected by CAEN before the shipment, and it is guaranteed to leave the factory free of mechanical or electrical defects.

The content of the delivered package standardly consists of the part list shown in the table below **Tab. 4.1**.

	Part	Description	Qt
	A5203(B)	64(128) Channel PicoTDC unit for FERS-5200	x1
	Power supply connector	691361300002 WURTH Connector for DC Input	x1
	Ethernet cable	2MTCat6 S-FTP Ethernet Cable	x1
	USB cable	USB 2.0 cable type A to microUSB-B	x1

	Documentation	UM9085 - A5203(B)/DT5203 User Manual	-

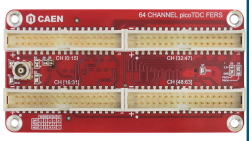
Tab. 4.1: A5203(B) delivered kit content.

4.2 DT5203

The DT5203 is avaiable as a Desktop module housed in an aluminum case and two external stand up rubber frames, one on the front and one on the rear panel (module dimensions: 106.1 W $\times$ 56.1 H $\times$ 166.1 L mm^3).

The device is inspected by CAEN before the shipment, and it is guaranteed to leave the factory free of mechanical or electrical defects.

The content of the delivered package standardly consists of the part list shown in the table below **Tab. 4.2**.

	Part	Description	Qt
	DT5203	64 Channel PicoTDC unit for FERS-5200	x1
	A5255	A5255 FERS-5200 Header Adapter (already mounted)	x1
	DC Input Adapter	DC Input Adapter	x1
	AC-DC Adapter	45W 12V Single Output AC-DC Adapter	x1
	Power Supply Cable	Power Supply Cable	x1
	Ethernet cable	2MTCat6 S-FTP Ethernet Cable	x1

	USB cable	USB 2.0 cable type A to microUSB-B	x1
	Documentation	UM9085 - A5203(B)/DT5203 User Manual	-

Tab. 4.2: DT5203 delivered kit content.

4.3 Unpackaging Instructions

CAUTION: to manage the product, consult the operating instructions provided.

When receiving the unit, the user is strictly recommended to:

- Inspect containers for damage during shipment. Report any damage to the freight carrier for possible insurance claims.
- Check that all the components received match those listed on the enclosed packing list as in **Tab. 4.1** and **4.2**. CAEN cannot accept responsibility for missing items unless any discrepancy is promptly notified.
- Open shipping containers; be careful not to damage contents.
- Inspect contents and report any damage. The inspection should confirm that there is no exterior damage to the unit such as broken knobs or connectors and that the front panel is not scratched or cracked. Keep all packing material until the inspection has been completed.
- If damage is detected, file a claim with carrier immediately and notify CAEN service (see Chap. **16**).
- If equipment must be returned, carefully repack equipment in the original shipping container with original packing materials, if possible. Please contact CAEN service.
- If equipment is not installed when unpacked, place equipment in original shipping container and store in a safe place until ready to install.

DO NOT SUBJECT THE ITEM TO UNDUE SHOCK OR VIBRATIONS

DO NOT BUMP, DROP OR SLIDE SHIPPING CONTAINERS

DO NOT LEAVE ITEMS OR SHIPPING CONTAINERS UNSUPERVISED IN AREAS WHERE UNTRAINED PERSONNEL MAY MISHANDLE THE ITEMS

USE ONLY ACCESSORIES WHICH MEET THE MANUFACTURER SPECIFICATIONS

For a correct and safe use of the module, refer to Chap. **6** and **7**.

5 PID (Product Identifier)

PID is the CAEN product identifier, an incremental number greater than 10000 that is unique for each product. The PID is on a label affixed to the product (**Fig. 5.1** and **5.2**).

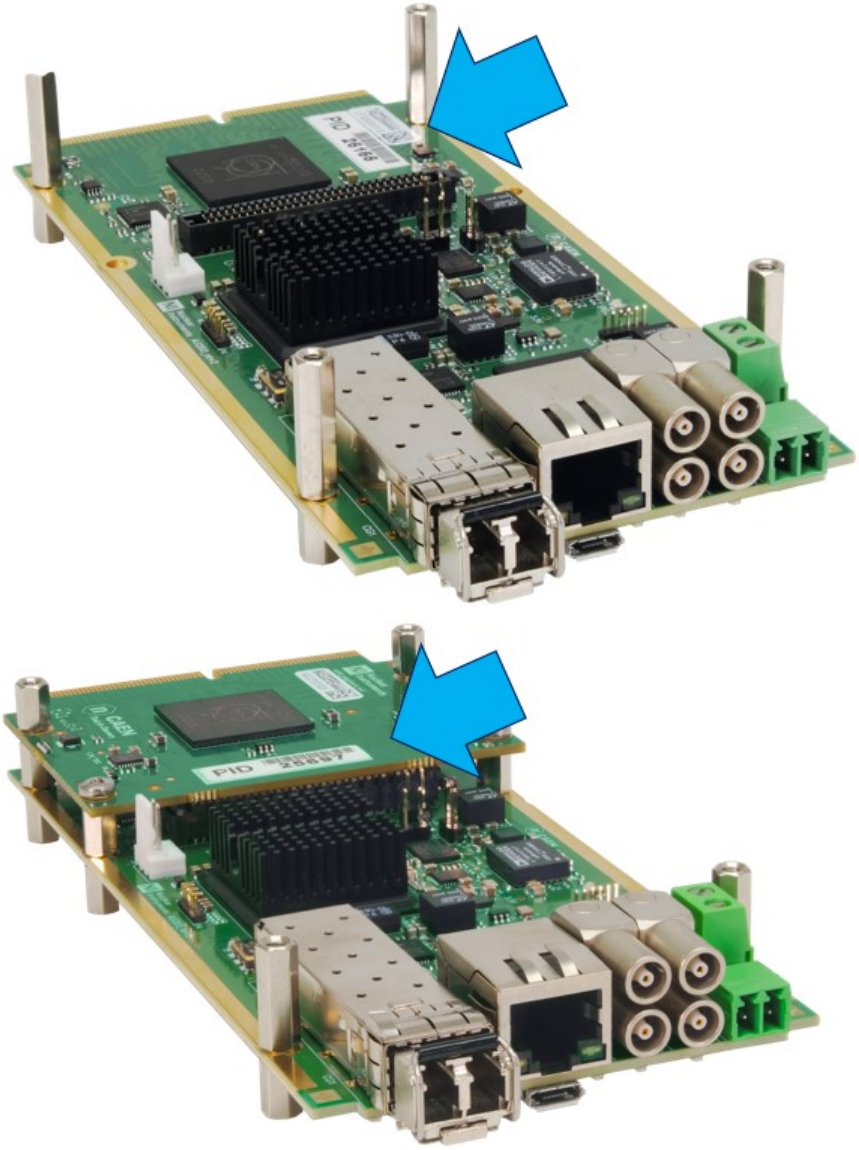


Fig. 5.1: PID location (the number in the picture is purely indicative) on the A5203 (*top*) and on the A5203B (*bottom*).

Fig. 5.2: PID location on DT5203 (the number in the picture is purely indicative) on the front panel of the board (*top*) and on the bottom side (*bottom*).

6 Power Requirements

The CAEN A5203(B) and DT5203 standalone modules are powered by an external 220 V-12 V AC/DC stabilized power supply. The AC/DC power supply is provided with the DT5203 board and included in the delivered kit, together with an adapter cable to easily connect the power supply jack to the DT5203 (see **Fig. 6.1**).
Only a DC connector is provided in the A5203 kit.

Fig. 6.1: AC/DC power supply adapter (left) and the jack cable provided with the DT5203 module (right).

In **Fig. 6.2**, the datasheet of the AC/DC stabilized power supply included in the DT5203 kit is shown.

THE CORRECT FUNCTIONING AND SAFETY OF THE MODULE ARE NOT GUARANTEED IF POWER REQUIREMENTS ARE OUTSIDE SPECIFICATIONS

Switchbox FRA030/045/050 Series

30-50W SINGLE OUTPUT AC/DC DESKTOP ADAPTOR

Features

- Universal input
- IEC320 receptacle 2P or 3P
- Optional output connector
- OVP, OCP, OPP, auto recovery
- CEC compliance

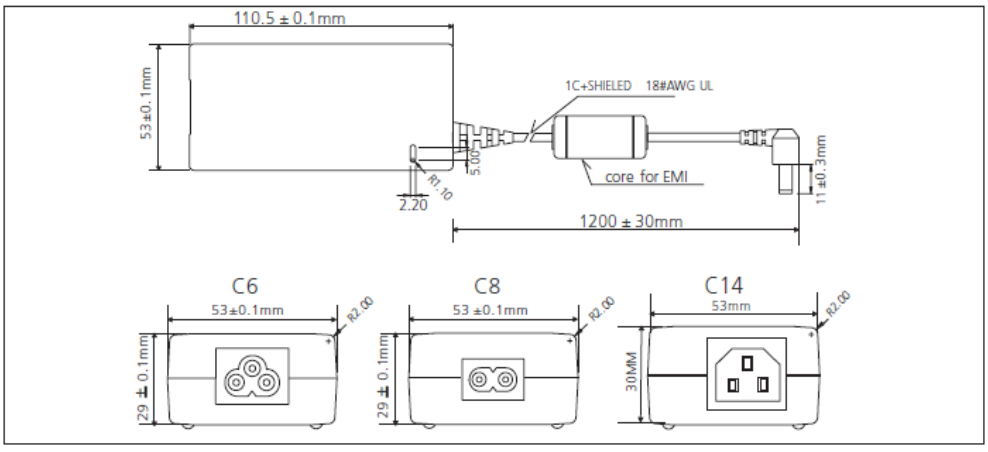
Specifications

INPUT	
Voltage range	100-240VAC.
Inrush current	40A at 115VAC / 80A at 230VAC max.
Dielectric withstand	Input/output 3,000VDC.
OUTPUT	
Output voltage	5-48V.
Ripple and noise	2% p-p max.
Load regulation	±5% max.
No load stand by power	<0.5W @ 230VAC.
Efficiency	>=85% for CEC requirement.
Hold up time	10mS at nominal line.
Protections	OCP, OVP, over power & short circuit.
GENERAL	
Std output connector	Dc barrel jack.
Std output cable/length	UL1185, #18AWG / 5 ft.
ENVIRONMENTAL	
Operating temperature	0°C to +40°C.
Storage temperature	–20°C to +85°C.
STANDARDS	
Safety standards	IEC/UL/EN60950-1, CE, CB.
EMC	EN55022 (CISPR 22) class B, FCC class B.

MODEL NUMBER	OUTPUT VOLTAGE	OUTPUT CURRENT	MAX WATTS	CEC*
FRA030-S05-X	5~7 V	6.00~4.30 A	30 W	
FRA045-S09-X	7~9 V	6.00~5.00 A	45 W	IV
FRA045-S12-X	12~15 V	3.75~3.00 A	45 W	IV
FRA045-S15-X	15~18 V	3.00~2.50 A	45 W	IV
FRA045-S24-X	18~24 V	2.50~1.88 A	45 W	IV
FRA050-S12-X	12~15 V	4.17~3.33 A	50 W	IV
FRA050-S15-X	15~18 V	3.33~2.87 A	50 W	IV
FRA050-S24-X	18~24 V	2.78~2.08 A	50 W	IV
FRA050-S36-X	30~36 V	1.67~1.38 A	50 W	IV
FRA050-S48-X	40~48 V	1.25~1.04 A	50 W	IV

*CEC compliance model provide under customer's request.
*CEC compliance model standby power (@ no load) <0.5W.

Note:
X = Inlet type code
X = 4, IEC320 C14 X = 6, IEC320 C6 X = 8, IEC320 C8



powerbox
www.powerbox.info
20081029

Fig. 6.2: AC/DC power supply provided with the DT5203 module.

7 Cooling Management

The User must take care to provide a proper cooling to the A5203(B)/DT5203 board. DT5203 present a fan inside its box, and theres no need to add further ventilation. The A5203 (64 channels) must be ventilated with an external fan if the board is used in an enclosure, if the board is installed in a setup with poor air flow, or if the environmental temperature exceeds 25 °C. The A5203B (128 channels) must be always ventilated with an external fan. The A5270 fan can be mounted on A5203 and A5203B boards as described in **[RD1]**.

EXTERNAL FANS MUST BE USED WITH THE A5203 BOARD WHEN ENVIRONMENTAL TEMPERATURE EXCEEDS 25 °C, OR WHEN THE BOARD IS PLACED IN AN ENCLOSED ENVIRONMENT - LIKE A BOX WITHOUT AIR FLOW. OVERHEATING MAY DAMAGE THE MODULE AND DEGRADE THE PERFORMANCES

GIVEN THE HIGH CHANNEL DENSITY, THE A5203B MODEL ALWAYS REQUIRES AN EXTERNAL VENTILATION

Excessive temperature will, in first instance, reduce the performance and the quality of the measurements and can also damage the board.

WARNING: The on-board FPGA operates correctly up to a temperature of 85 °C. The user must keep the temperature of the FPGA below this limit (e.g. by using a suitable ventilation system).

If the board is stored in cold environment, please check for water condensation before power on.

The board has not been tested for radiation hardness. High energy particles can be source of errors and can damage the FPGA. If used in strong proton or neutron beams, arrange proper shielding, or remote the sensors with a custom cable.

7.1 Cleaning Air Vents

CAEN recommends to occasionally clean the air vents on all vented sides of the board or crate, if present. Lint, dust, and other foreign matter can block the vents and limit the airflow. Be sure to power off the board and disconnect it from the power by physically detach the power chord before cleaning the air vents and follow the general cleaning safety precautions.

IT IS UNDER THE RESPONSIBILITY OF THE CUSTOMER A NON-COMPLIANT USE OF THE PRODUCT

8 Panels Description

8.1 A5203/A5203B Views

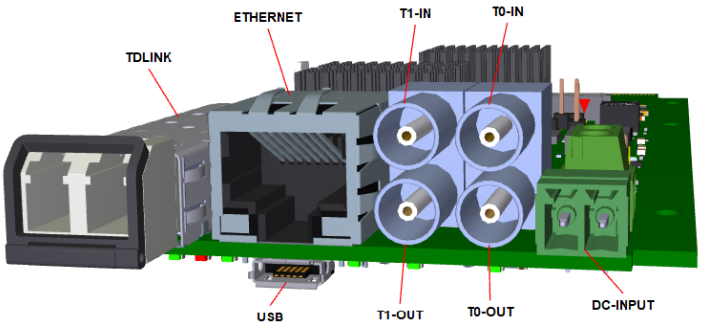


Fig. 8.1: A5203 front panel view.

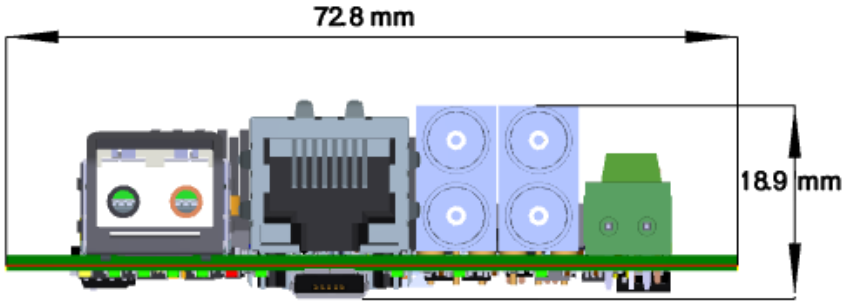


Fig. 8.2: A5203 front panel view with spatial dimensions.

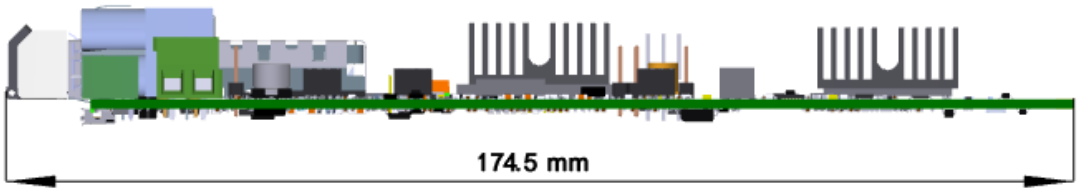


Fig. 8.3: A5203 lateral view with spatial dimensions.

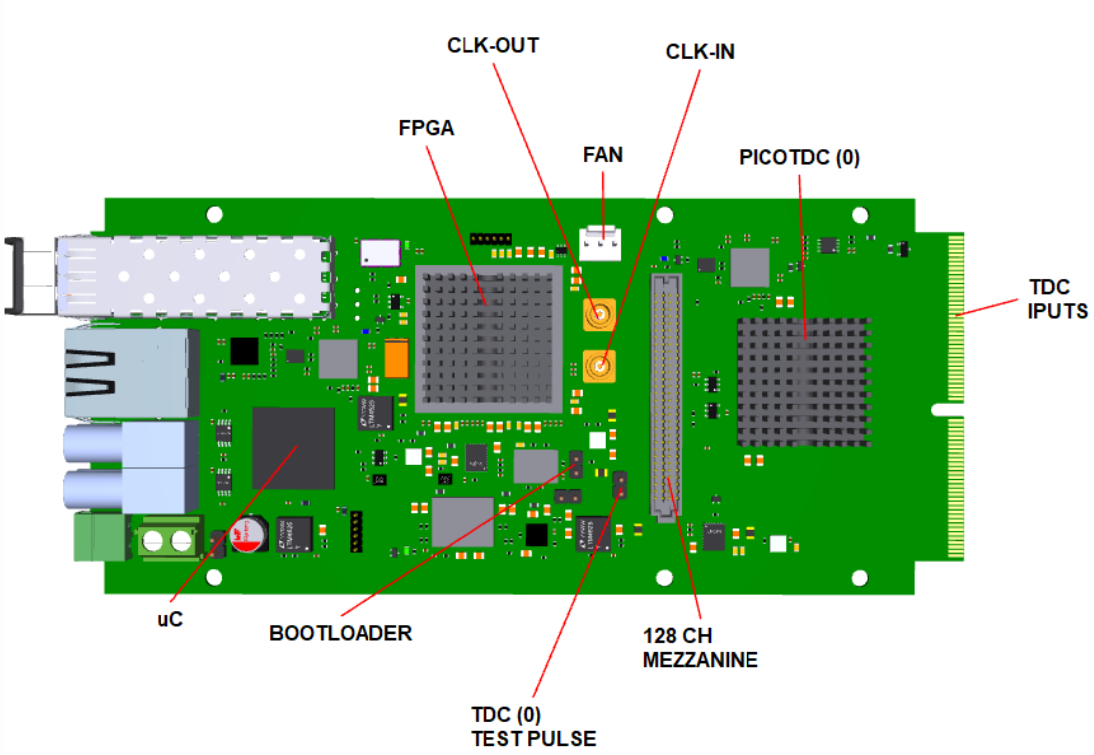


Fig. 8.4: A5203 top view.

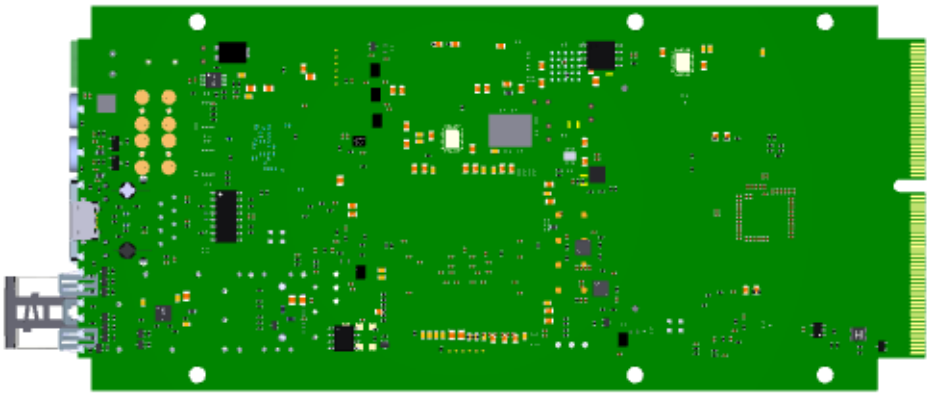


Fig. 8.5: A5203 bottom view.

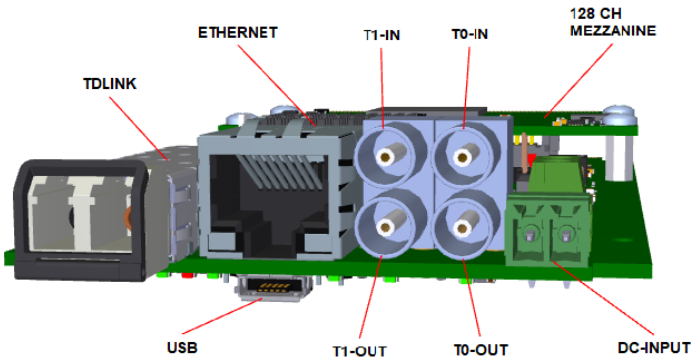


Fig. 8.6: A5203B front panel view.

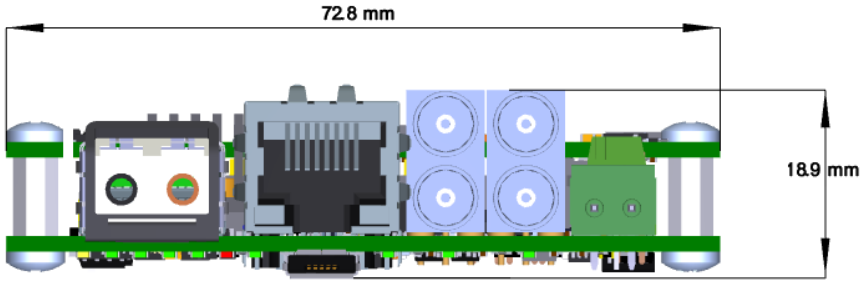


Fig. 8.7: A5203B front panel view with spatial dimensions.

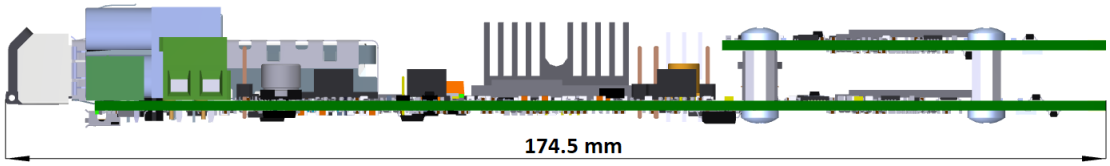


Fig. 8.8: A5203B lateral view with spatial dimensions.

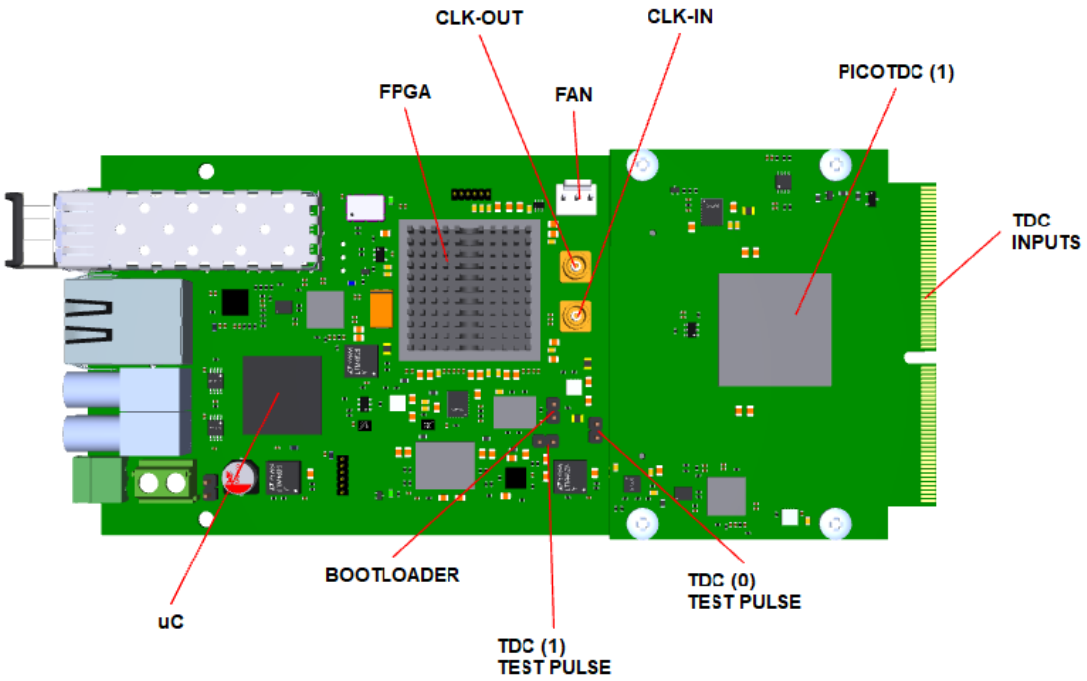


Fig. 8.9: A5203B top view.

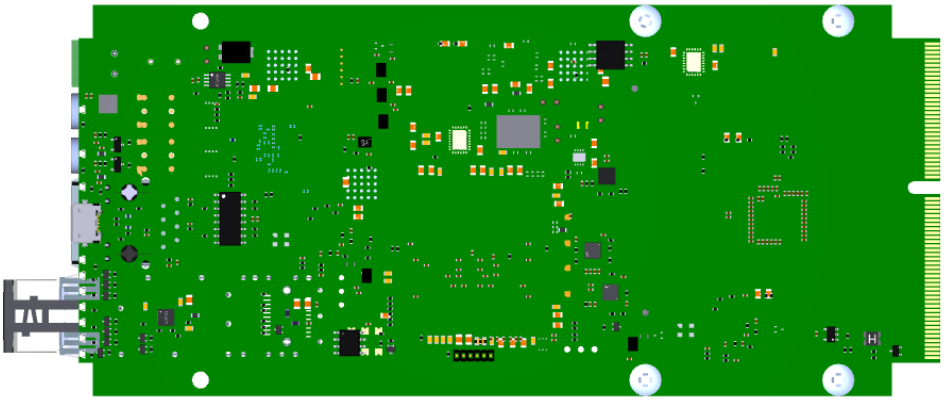
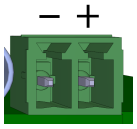
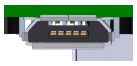


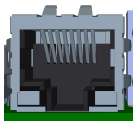
Fig. 8.10: A5203B bottom view.

8.1.1 Panel Views

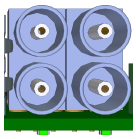
POWER INPUT		
	**FUNCTION** Power connector mating to a 691361300002 WURTH ELEKTRONIK connector (already inserted in the DC input in the A5203(B) kit) **ELECTRICAL SPECS** Typ. Input voltage: +12 V DC	**MECHANICAL SPECS** Manufacturer: WURTH ELEKTRONIK Internal number: 691322310002

USB PORT		
	**FUNCTION** USB 2.0 connector for A5203(B) configuration and data readout **ELECTRICAL SPECS** N.A.	**MECHANICAL SPECS** Series: USB connectors Connector type: Micro USB, type B, reverse Manufacturer: TE connectivity Internal number: 1932788-1

TDLINK		
	**FUNCTION** Optical link connector for data readout and flow control in multiboard configuration. Daisy chainable. Compliant with optical fibers 50/125 µm OM2 and OM3 (back-compliant with 62.5/125 µm OM1) cable featuring LC connectors on both sides **ELECTRICAL SPECS** N.A.	**MECHANICAL SPECS** Series: SFP Transceivers Type: FTLF8524P2BNV (LC connectors) Manufacturer: FINISAR

ETHERNET PORT		
	**FUNCTION** Ethernet connector for A5203(B) configuration and data readout **ELECTRICAL SPECS** N.A.	**MECHANICAL SPECS** RJ45 female connector

DIGITAL I/Os



FUNCTION
Digital software programmable input/output connectors:
- **T0-IN/T1-IN**: global trigger, external time reference, veto source
- **T0-OUT/T1-OUT**: T1-IN input, trigger, run signal, internal periodic signal, busy signal, digital probe, square wave, TDLink clock synchronization signal (if connected to DT5215), run synchronization signal (if connected to DT5215), zero signal

From left to right, from top to bottom (see Fig. **8.1**): T1-IN, T0-IN, T1-OUT, T0-OUT

ELECTRICAL SPECS
Signal level: LVTTL/NIM (input), LVTTL (output).
The two outputs require 50 Ω termination

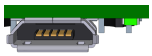
MECHANICAL SPECS
Series: 101 A 004 connectors
Type: DLP 101 A 004-28
Manufacturer: FISCHER
Alternatively:
Type: EPL 00 250 NTN
Manufacturer: LEMO

DIAGNOSTIC LEDs

From left to right:

- **OVR (ORANGE)**: Indicates that the board is in BUSY status. No further trigger can be accepted, and data are lost until the board exits from the BUSY condition.
- **COMM (GREEN)**: Indicates there is activity on the USB, TDLink or Ethernet channel
- **DRDY (GREEN)**: Indicates the event/data is present in the Output Buffer
- **TRG (GREEN)**: Indicates the trigger is accepted
- **RUN (GREEN)**: Indicates the acquisition is running (data taking)
- **FAIL (RED)**: Indicates a severe failure condition: FPGA over-temperature, clock loss, etc.
- **INIT (GREEN)**: Indicates that the connection between the board and the PC or DT5215 concentrator board is established

POWER ON LED



PWR (GREEN): The led turns on as soon as the power supply is connected to the DC input connector

CLK-IN/OUT

FUNCTION
SMA connectors for CLK-IN/CLK-OUT propagation.
CLK-IN: connection for the clock signal to feed to the DT5203
CLK-OUT: connection for the propagation of the clock generated by the DT5203

ELECTRICAL SPECS
Input impedance (Z_{in}): 50 Ω

MECHANICAL SPECS
Series: MCX connectors
Type: SMT PCB jack (female), straight, 5.08
Manufacturer: WURTH ELEKTRONIK
Suggested plug/male: MCX-50-2-16
Suggested cable: RG174 type

8.2 DT5203 Views

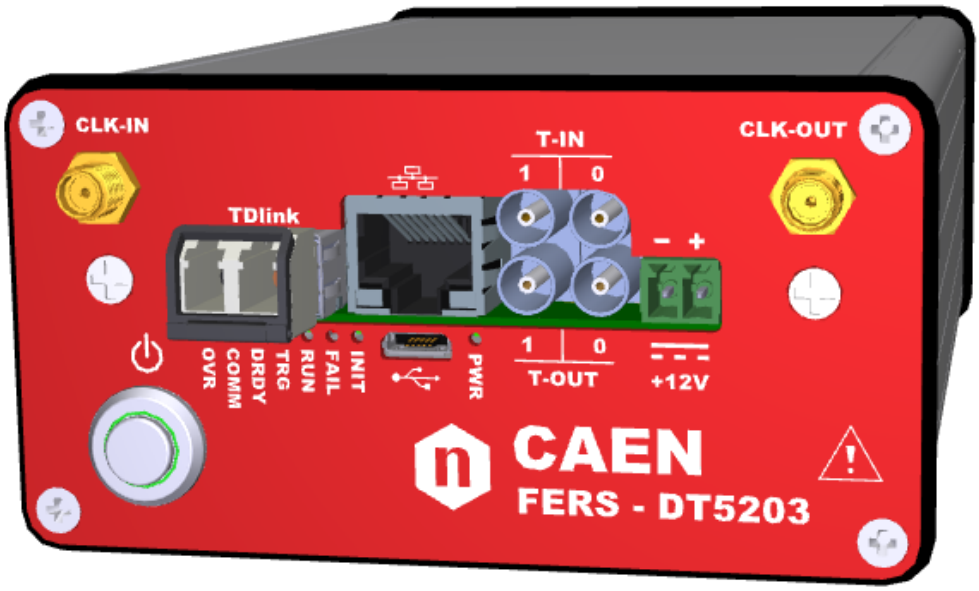


Fig. 8.11: DT5203 front panel view.

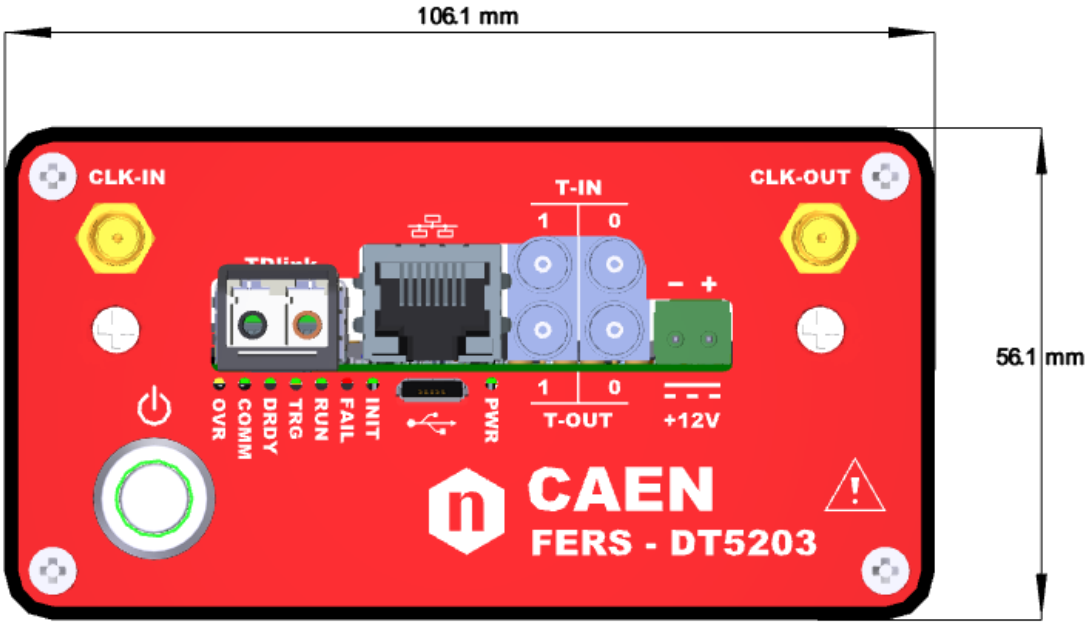


Fig. 8.12: DT5203 front panel view with spatial dimensions.

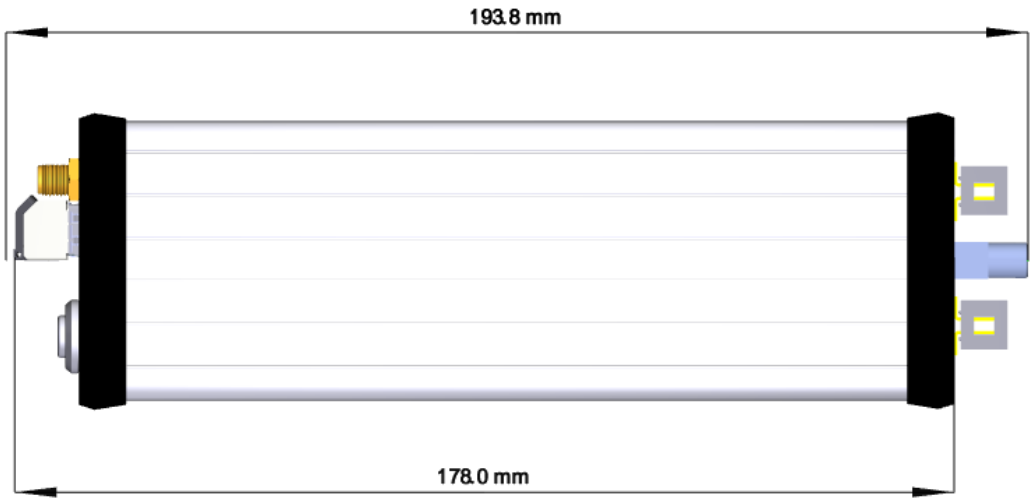


Fig. 8.13: DT5203 lateral view with spatial dimensions.

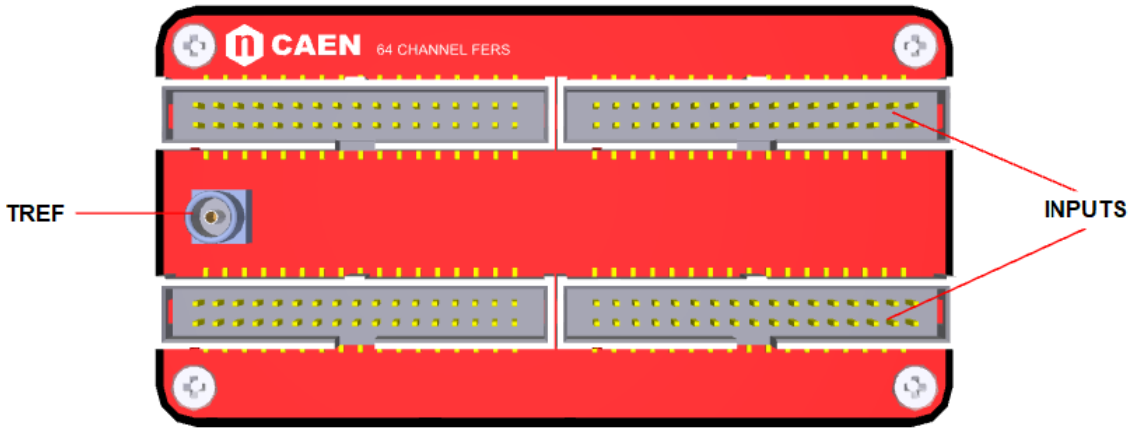


Fig. 8.14: DT5203 back panel view (A5255 adapter mounted **[RD1]**).

8.2.1 Panel Views

POWER INPUT

FUNCTION
Power connector

ELECTRICAL SPECS
Typ. Input voltage: +12 V DC

MECHANICAL SPECS
Manufacturer: WURTH ELEKTRONIK
Internal number: 691322310002

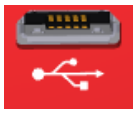
POWER ON BUTTON

FUNCTION
Button allowing the user to power on/off the DT5203 board

ELECTRICAL SPECS
N.A.

MECHANICAL SPECS
N.A.

USB PORT



FUNCTION
USB 2.0 connector for DT5203 configuration and data readout

ELECTRICAL SPECS
N.A.

MECHANICAL SPECS
Series: USB connectors
Connector type: Micro USB, type B, reverse
Manufacturer: TE connectivity
Internal number: 1932788-1

OPTICAL LINK PORT

FUNCTION
Optical link connector for data readout and flow control in multiboard configuration. Daisy chainable. Compliant with optical fibers 50/125 µm OM2 and OM3 (back-compliant with 62.5/125 µm OM1) cable featuring LC connectors on both sides

ELECTRICAL SPECS
N.A.

MECHANICAL SPECS
Series: SFP Transceivers
Type: FTLF8524P2BNV (LC connectors)
Manufacturer: FINISAR

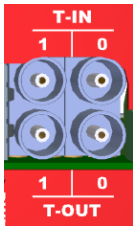
ETHERNET PORT

FUNCTION
Ethernet connector for DT5203 configuration and data readout

ELECTRICAL SPECS
N.A.

MECHANICAL SPECS
RJ45 female connector

DIGITAL I/Os

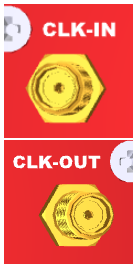


FUNCTION
Digital software programmable input/output connectors:
- **T0-IN/T1-IN**: global trigger, external time reference, veto source
- **T0-OUT/T1-OUT**: T1-IN input, trigger, run signal, internal periodic signal, busy signal, digital probe, square wave, TDLink clock synchronization signal (if connected to DT5215), run synchronization signal (if connected to DT5215), zero signal

ELECTRICAL SPECS
Signal level: LVTTL.
Require 50 Ω termination

MECHANICAL SPECS
Series: 101 A 004 connectors
Type: DLP 101 A 004-28
Manufacturer: FISCHER
Alternatively:
Type: EPL 00 250 NTN
Manufacturer: LEMO

CLK-IN/OUT



FUNCTION
SMA connectors for CLK-IN/CLK-OUT propagation.
CLK-IN: connection for the clock signal to feed to the DT5203
CLK-OUT: connection for the propagation of the clock generated by the DT5203

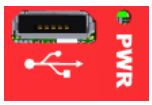
ELECTRICAL SPECS
Input impedance (Z_{in}): 50 Ω

MECHANICAL SPECS
Series: SMA connectors
Type: SMA F BH JCK 50 Ω
Manufacturer: Molex
Suggested plug/male: SMA BH

DIAGNOSTIC LEDs

- **OVR (ORANGE)**: Indicates that the board is in BUSY status. No further trigger can be accepted, and data are lost until the board exits from the BUSY condition.
- **COMM (GREEN)**: Indicates there is activity on the USB, TDLink or Ethernet channel
- **DRDY (GREEN)**: Indicates the event/data is present in the Output Buffer
- **TRG (GREEN)**: Indicates the trigger is accepted
- **RUN (GREEN)**: Indicates the acquisition is running (data taking)
- **FAIL (RED)**: Indicates a severe failure condition: FPGA over-temperature, clock loss, etc.
- **INIT (GREEN)**: Indicates that the connection between the board and the PC or DT5215 concentrator board is established

POWER ON LED



PWR (GREEN): The led turns on as soon as the power supply is connected to the DC input connector

8.3 TDC Input Channels Pin Out

The A5203 has an input edge card connector type HSEC8-170, mating to a Samtec HSEC8-170-01-S-DV. The connector has 140 contacts (0.8 mm pitch) and brings 64 couples, the temperature sensor and several grounds. The A5203 edge connector pin out is presented in **Fig. 8.15** and **Fig. 8.16**.

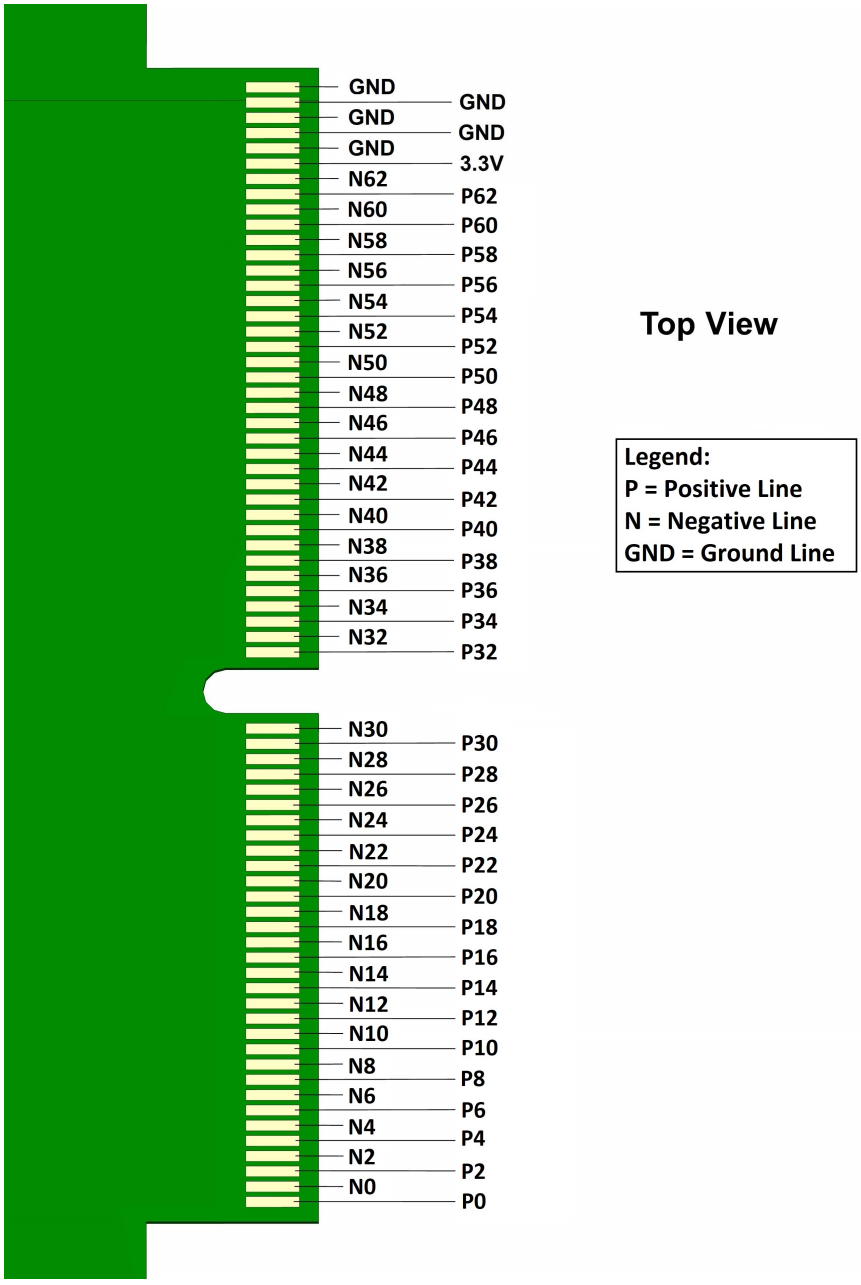


Fig. 8.15: Input edge connectors pin-out (A5203 top view).

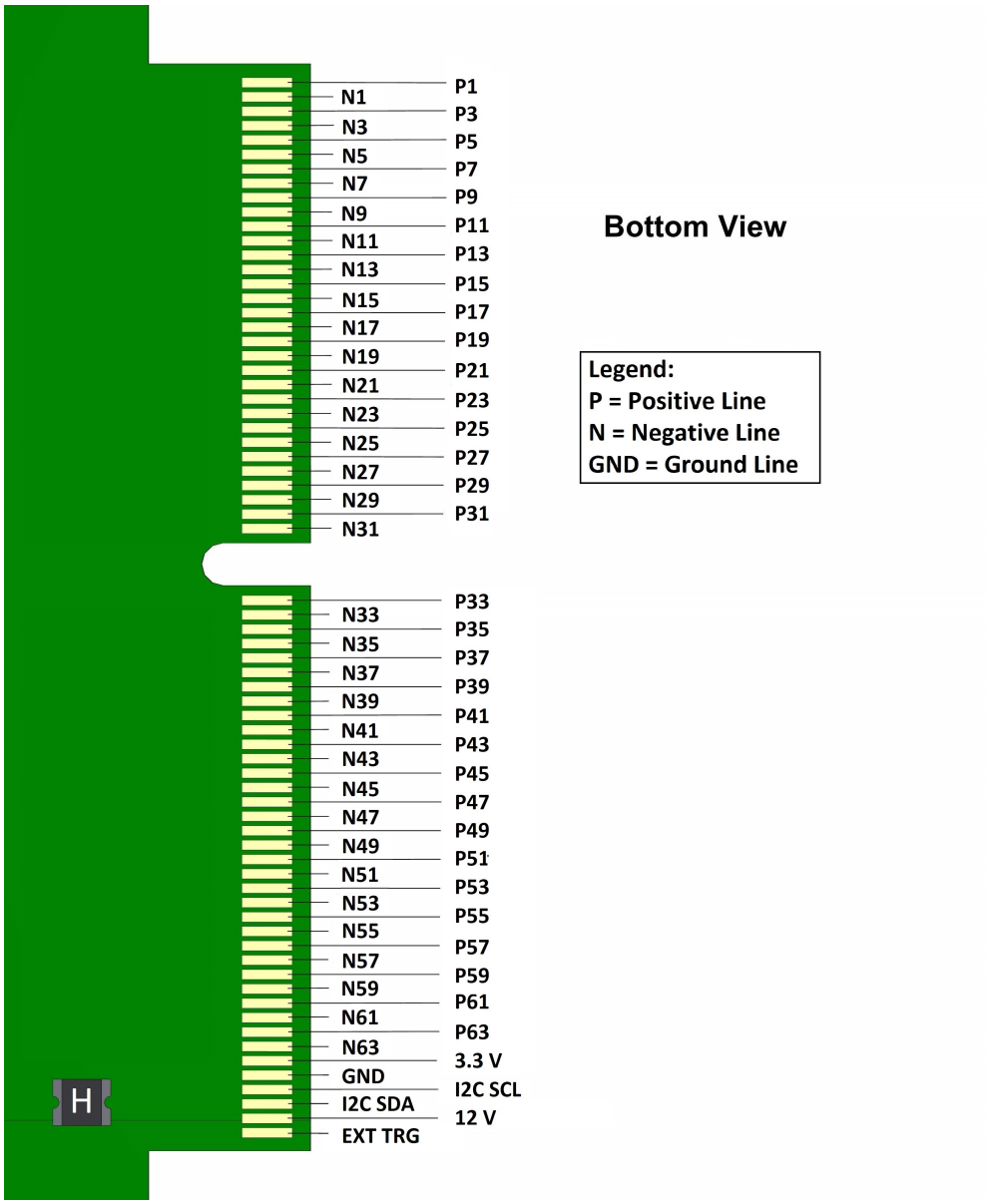


Fig. 8.16: Input edge connector pin-out (A5203 bottom view).

Apart from the TDC input positive, negative and ground lines:

- **I2C SCL** indicates the Serial Clock pin of the I^2C slave bus.
- **I2C SDA** indicates the Serial Data pin of the I^2C slave bus.
- **EXT TRG** indicates the Edge Connector trigger input.

THE PICOTDC CHIP ONLY ACCEPTS REDUCED-LVDS INPUT SIGNALS

In **Tab. 8.1**, the A5203 pin numbering scheme and correspondence with the various lines is presented.

Pin N.	Signal	Pin N.	Signal	Pin N.	Signal	Pin N.	Signal
1	P0	36	N17	71	N34	106	P53
2	P1	37	P18	72	N35	107	N52
3	N0	38	P19	73	P36	108	N53
4	N1	39	N18	74	P37	109	P54
5	P2	40	N19	75	N36	110	P55
6	P3	41	P20	76	N37	111	N54
7	N2	42	P21	77	P38	112	N55
8	N3	43	N20	78	P39	113	P56
9	P4	44	N21	79	N38	114	P57
10	P5	45	P22	80	N39	115	N56
11	N4	46	P23	81	P40	116	N57
12	N5	47	N22	82	P41	117	P58
13	P6	48	N23	83	N40	118	P59
14	P7	49	P24	84	N41	119	N58
15	N6	50	P25	85	P42	120	N59
16	N7	51	N24	86	P43	121	P60
17	P8	52	N25	87	N42	122	P61
18	P9	53	P26	88	N43	123	N60
19	N8	54	P27	89	P44	124	N61
20	N9	55	N26	90	P45	125	P62
21	P10	56	N27	91	N44	126	P63
22	P11	57	P28	92	N45	127	N62
23	N10	58	P29	93	P46	128	N63
24	N11	59	N28	94	P47	129	3.3 V
25	P12	60	N29	95	N46	130	3.3 V
26	P13	61	P30	96	N47	131	GND
27	N12	62	P31	97	P48	132	GND
28	N13	63	N30	98	P49	133	GND
29	P14	64	N31	99	N48	134	I2C SDL
30	P15	65	P32	100	N49	135	GND
31	N14	66	P33	101	P50	136	I2C SCA
32	N15	67	N32	102	P51	137	GND
33	P16	68	N33	103	N50	138	12 V
34	P17	69	P34	104	N51	139	GND
35	N16	70	P35	105	P52	140	EXT TRG

Tab. 8.1: Pin number-electrical line correspondence table.

The pin out of the A5203B mezzanine edge connector is the same of the A5203 edge connector. The only change is at software level, where the channels 0-63 are renamed 64-127.

9 Functional Description

In the following chapter, the operation principles and the functional description of the A5203(B)/DT5203 module are treated in detail. The block diagram of the board is presented in **Fig. 9.1**.

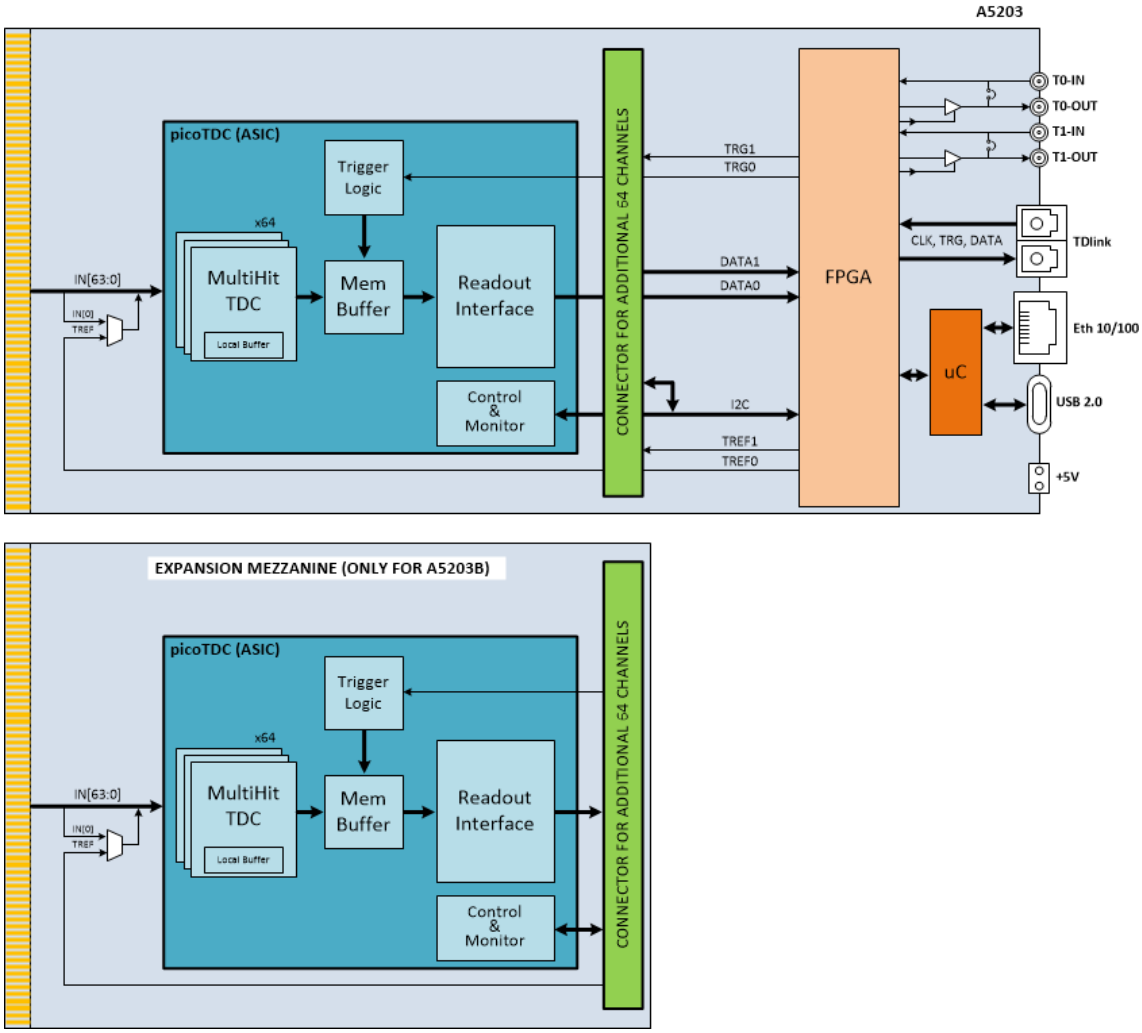


Fig. 9.1: Simplified block diagram of the A5203(B)/DT5203 FERS-5200 unit. The expansion mezzanine is embedded only in the A5203B board type.

The core of the A5203(B)/DT5203 board is a picoTDC ASIC chip **[RD2]**. A single picoTDC chip can acquire timestamps for up to 64 channels contemporaneously, with a maximum time resolution of 3.125 ps and a full time range of 209.7152 µs[1]. Hits are saved in the picoTDC memory buffers, and made available for the FPGA readout following a *trigger matching* logic:

1. The FPGA sends a trigger to the picoTDC. The trigger signal runs at 39.0625 MHz (25.6 ns resolution). It can be generated on board by the FPGA as a periodic trigger with programmable period, or can come

[1]The maximum time range may vary depending on the measurement mode used, and the selected Header-Trailer option. See Sec. **9.6**.

from an external source, passing by the T0-IN, T1-IN LEMO connectors, or by the edge connector. The trigger window width and position are software programmable.

2. The picoTDC selects in its memory buffer the hits falling inside the window (matching the trigger time window), groups them in an event, and stores the event packet in the Readout Interface buffer.
3. The FPGA reads out the event packet in an atomic transaction.

Note: It is possible to define overlapped trigger windows, such as some hits can belong to different trigger windows and be reread multiple times. Hits do not belonging to any trigger trigger window are discarded.

Note: It is not possible to generate a trigger with the hits recorded by the picoTDC, as the picoTDC channels are not accessible by the FPGA.

The A5203(B)/DT5203 can work in different acquisition modes, described in details in Sec. **9.5**: Common Start, Common Stop, Streaming and Trigger Matching. For readout tests and debugging purposes, Test Mode 1 and Test Mode 2 acquisition modes are also available.
In case of Common-Start and Common-Stop modes, a time reference signal with the same time resolution of the recorded hits is needed. The time reference signal then works as trigger for the data readout and as time reference for the recorded hits, being feed to the FPGA as trigger signal and to one of the board's input channels.

Note: Ch0 is the default time reference channel if managing the data acquisition with the Janus 5203 software, and/or if using CAEN adapters for the edge connector **[RD1]**. In case of custom software and/or adapter, the reference channel can be any of the board's input channels.

The reference signal can be:

1. duplicated outside the board, then fed to the T0-IN or T1-IN connectors (as single ended TTL or NIM) for the trigger signal, and to one of the input channels (as differential LVDS) for the time reference signal. See **Fig. 9.2**.

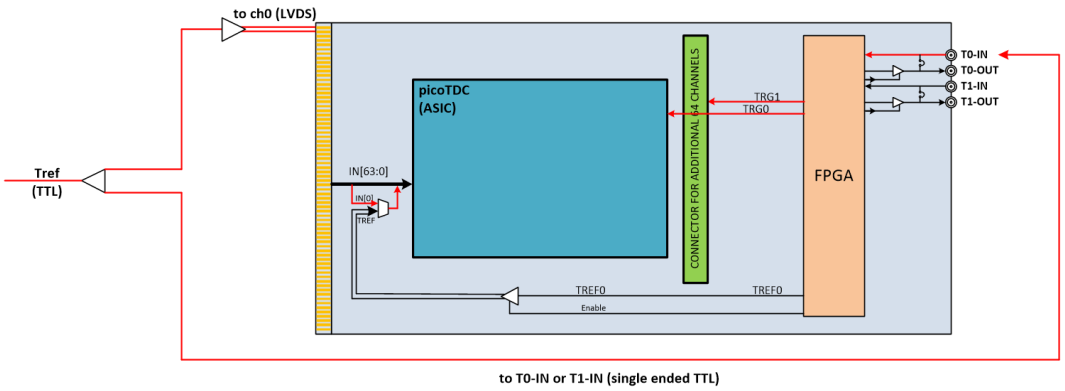


Fig. 9.2: Simplified block diagram of the Tref and trigger connections in case the Tref signal is duplicated outside the board.

2. fed to T0-IN or T1-IN only. The reference signal is then duplicated on board, and sent to the FPGA and to the reference channel (ch0) via an internal driver. See **Fig. 9.3**.

Note: Ch0 on the edge connector must be left open.

Note: In this configuration, the time reference signal on the reference channel present a worst resolution, as it passes by the FPGA which timing is temperature dependent.

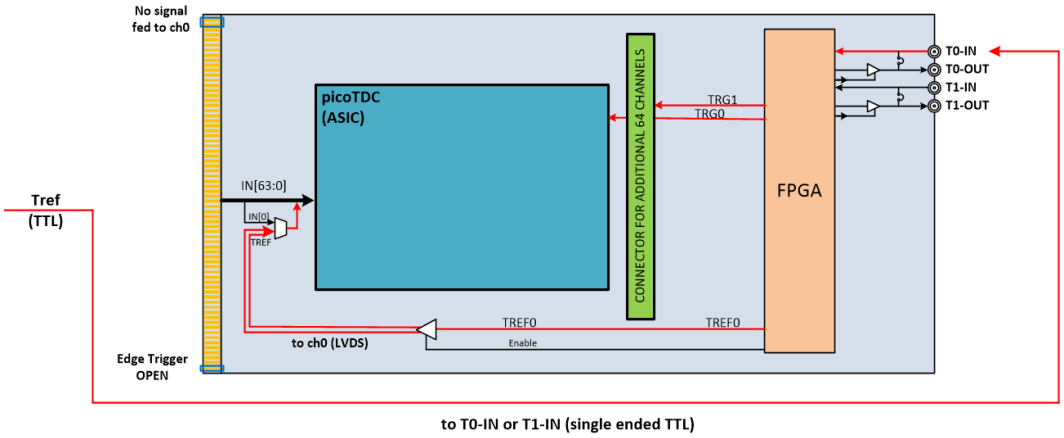


Fig. 9.3: Simplified block diagram of the Tref and trigger connections in case the Tref signal is duplicated inside the board.

3. sent to the reference channel only, via the A5255 or A5256 adapters. The reference signal is then duplicated on the adapter and fed to the FPGA (for triggering) and to the ch0 of the picoTDC chip (for time reference). See **Fig. 9.4**.

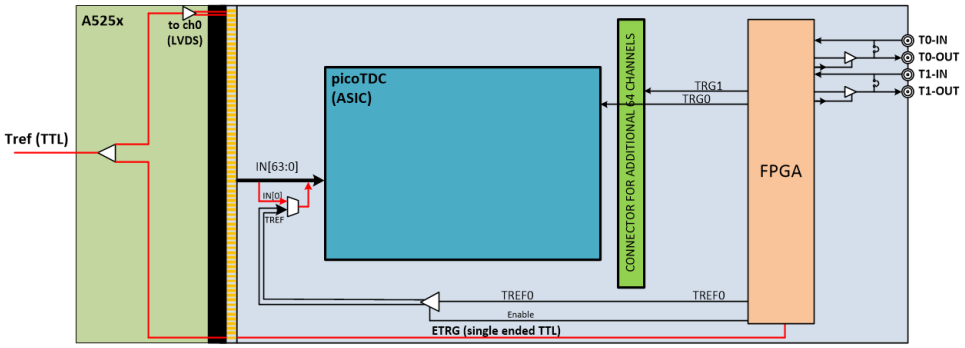


Fig. 9.4: Simplified block diagram of the Tref and trigger connections in case an adapter A525x for the A5203 edge connector is used.

9.1 FPGA Block Diagram

After a description of the main functionalities of the picoTDC chip, in **Fig. 9.5** the Artix XC7A75T-1 FPGA schematic is presented.

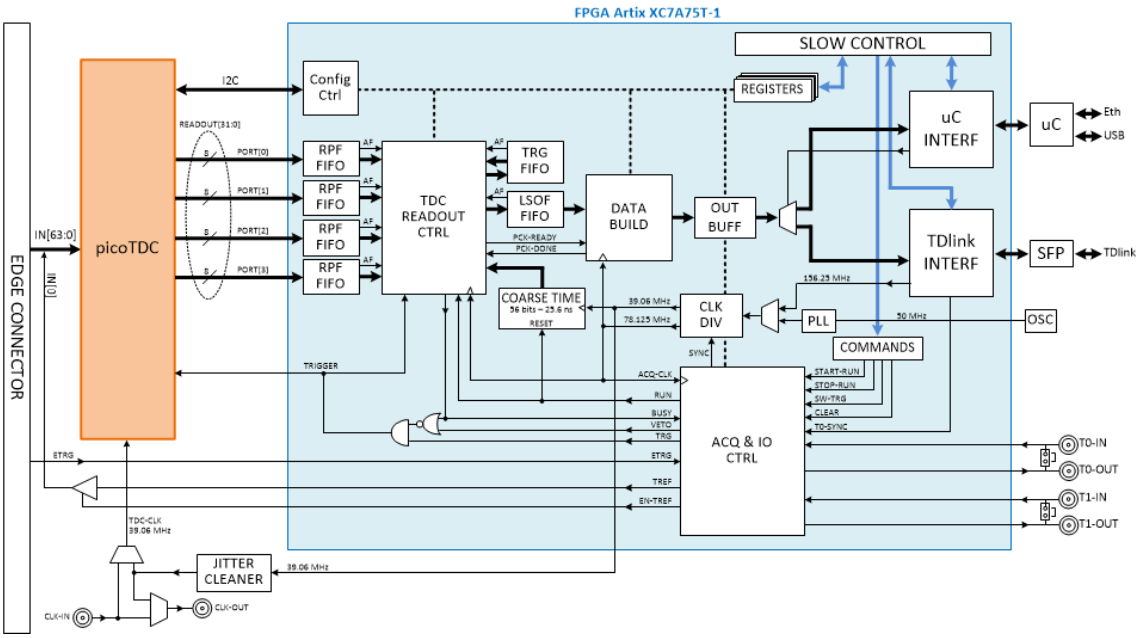


Fig. 9.5: FPGA block diagram.

The data readout from the picoTDC chip is performed, following the trigger matching criterium, via four **FIFO Readout Ports (RPF)**. Each port reads, in parallel to the other ports, the data of 16 picoTDC input channels. Each 16-ch group data packet present an Header and a Trailer containing info regarding that particular data packet. Once acquired, data are ordered and grouped in an event (keeping both header and a trailer, or condenstating them into one single word) inside the **List Output FIFO (LSOF)**. The ready data packet is then sent to the output buffer for the PC event readout. The latter can be directly readout, via the ethernet or USB interfaces (managed by the microcontroller, µC), or via the TDLink, connected to the DT5215 Concentrator Board (see Sec. **10**).

Note: The microcontroller interface is switched off if not used, i.e. if the PC connection is done via the TDLink and DT5215.

The microcontroller interface, or TDLink interface, can read/write board configuration registers and send commands to the board such as: *Start-Run*, *Stop-Run*, and *Clear*. If connected to the DT5215, the TDLink interface sends also the *TD-Sync* command to the board to align the time stamps.
Once received the *Start-Run*, the FPGA manages the data acquisition and controls the Input/Outputs (T0-IN, T0-OUT, T1-IN, T1-OUT). The trigger signal, used for the event acquisition (except for the Streaming acquisition mode), can be: a periodic signal created by the FPGA, or an external signal, from the edge connector or from the T0/T1-IN LEMO 00 connectors. If one of the FPGA memory buffers is (almost) full (AF), a busy signal is asserted to inhibit (veto) the triggers. Any further trigger that arrives while the busy is active will be rejected (see Sec. **9.3**). The veto signal can also be taken from the T0/T1-IN LEMO 00 connectors.

The FPGA works on a main clock of 156.25 MHz frequency, that can be taken from an internal 50 MHz oscillator, or from the TDLink. The acquisition clock (ACQ-CLK) at 79.125 MHz frequency, and the picoTDC clock (TDC-CLK) at 39.06 MHz frequency are derived from the main clock in the clock divider (CLK DIV). The picoTDC clock can also be generated externally, and fed to the picoTDC chip via the CLK-IN connector. The CLK-OUT connector permits to propagate the picoTDC clock to other boards. See Sec. **10.1** for more details

on the picoTDC clock synchronization.

9.2 Control Signals

In this section, a list of the main control signals available for the A5203(B)/DT5203 board is presented, together with a brief explanation of their application:

- **Trigger**. A bunch (i.e. global) trigger signal directed to all channels (64/128) of the board used to define an acquisition window of programmable size. Only the hits belonging to the trigger window are saved in the data packet and read (for all the 64/128 channels simultaneously). In addition to the Edge Trigger (ETRG) and external trigger (coming from the T0-IN or T1-IN connector), the A5203(B)/DT5203 board can generate a periodic trigger whose period is programmed as a 32-bit word. The available values for the period thus range from 25.6 ns to $\approx$ 55 s, i.e. $(2^{32} - 1) \times 12.8$ ns.
- **Time Reference**. As explained at the beginning of this chapter, the time reference (T_{ref}) signal can be taken from different inputs. In case 2, the Tref signal is generated by the FPGA and used to drive the reference channel (ch0 by default). The Time of Arrival (ToA) information is then computed as the time difference between the individual channels hits and the T_{ref} signal. The Time over Threshold (ToT) of the individual hits can also be saved (if working in LEAD_TOT8 or LEAD_TOT11 Measurement Modes, see Sec. **9.6**).
- **Veto**. The Veto signal, as long as it is associated with a high logic level, inhibits all trigger signals.
- **Run**. The Run signal goes high when the Start Run command is executed. The Start Run can be sent by the software to the board via a direct connection (Ethernet or USB), or via the TDLink (through the DT5215 concentrator board), as previously explained. In the second case, the Start/Stop Run commands can be sent in broadcast to all the boards connected to the FERSnet, in order to have a synchronized start/stop.
- **Busy**. The busy signal goes high when one of the buffer memory is full (see the following lines for more details). The trigger signal does not cause the busy signal to go to an high logic level (it only defines the time when the counters are latched and read).

9.3 Data Management

The data acquisition chain in the A5203(B)/DT5203 goes through several buffers and FIFOs implemented in both the picoTDC and the FPGA, as highlighted in **Fig. 9.6** and **Fig. 9.7**.

In the picoTDC, each channel has an input derandomizer, made of four registers that can hold the incoming hits while waiting for the readout logic to transfer them to the memory buffers. These registers are very fast and allow two consecutive pulses to be stored even in the case where they are extremely narrow and close to each other (below 1 ns).
The first memory buffer of the chain is the **TDC Channel Buffer**: it is individual per channel and can store up to 512 hits, but the size can be programmed[2] down to a minimum of 4. Limiting this size allows the user to control the maximum number of hits that one channel can acquire[3]. This is particularly useful when there are noisy signals that may saturate the next buffers.
The hits remain in the TDC Channel Buffer until a trigger signal is sent to the TDC. In that moment the trigger matching algorithm extracts the hits belonging to the trigger window and transfers them to the **ReadOut Buffer (ROB)**. This buffer is common to a group of 16 channels and the maximum size is 512. The size is programmable, but in the Janus 5203 software has been chosen to hard-code it to the maximum value, since there is not a real advantage in making it smaller. The hits belonging to the trigger window exceeding the maximum number of 512 will be discarded by the picoTDC.

[2] The value is fixed and settable via the Janus 5203 software **[RD3]**.
[3] If the number of incoming hits exceeds the maximum size, the exceeding hits are rejected.

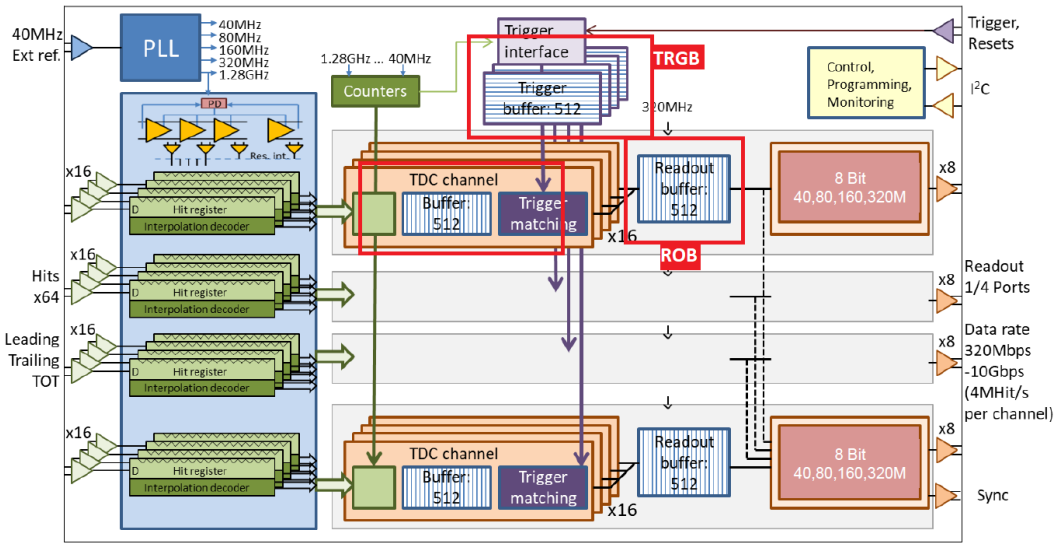


Fig. 9.6: Memory buffers in the picoTDC block diagram.

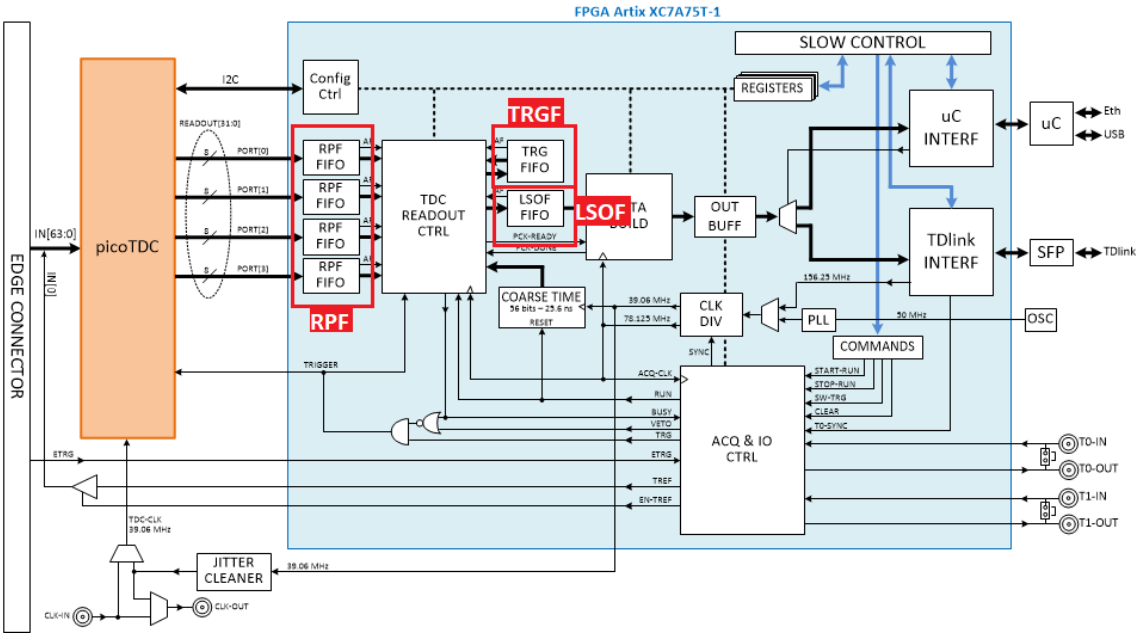


Fig. 9.7: Memory buffers in the FPGA block diagram.

Note: The discarded hits are lost. This may happen when there are particularly noisy channels, and the TDC channel buffer size is set to high values. As to avoid hits loss, the TDC channel buffer size should be low enough, and the ROB maintained to the maximum value.

The picoTDC has also a **Trigger Buffer** (maximum size[4] = 512) to hold the triggers that arrive while the trigger matching logic is still serving a previous trigger. However, the control of the maximum number of pending triggers is implemented by the FPGA, as explained later, so the trigger buffer in the picoTDC should never go full.
Once the trigger has been sent from the FPGA to the picoTDC, the trigger matching mechanism starts and the event data are immediately transmitted by the picoTDC to the FPGA through the four readout ports

[4] Ranging from 4 to 512, set to 16 by default in the Janus 5203 software **[RD3]**.

(one per group of 16 channels). There is no way to stop the data transfer, therefore the FPGA must have enough room to store the incoming data: this is guaranteed by the RPF FIFOs (one per readout port). As soon the free space in one of these FIFOs is less than the maximum event size, the Busy signal is asserted and no further trigger will be accepted by the FPGA. This event is unlikely since the RPF FIFOs are used as temporary transit buffers, being the LSOF FIFO the final destination of the event data packet.
The data acquisition process in the FPGA can be described by the following steps:

1. When a trigger (coming from any possible source) arrives and the board is not busy, the FPGA sends the trigger to the picoTDC and writes the trigger descriptor (time stamp, trigger ID, etc…) into the **Trigger FIFO (TRGF FIFO)**. It is possible to accumulate several "pending" triggers in the TRGF FIFO. These are accepted triggers that are being served but not totally acquired yet.
2. When the trigger is received by the picoTDC, it starts to transmit the hits belonging to the trigger window to the FPGA, that saves the data into the RPF FIFOs. The data being written into the RPFs are immediately transferred to the LSOF FIFO, starting from the port 0 up to the port 3 (or 7 in case of A5203B with two picoTDC chips). Read and write accesses to the RPF take place in parallel. When all data belonging to the trigger have been written into the LSOF, the trigger descriptor is read from the TRGF FIFO and added to the event data. At this point, the event data packet is ready for the transmission to the readout interface of the A5203(B)/DT5203 (optical link, Ethernet or USB). This closes the trigger acquisition: the trigger is no more "pending" as soon as its data packet is ready for reading in the LSOF FIFO.
3. The "Data Build" block checks if there is enough space in the **Output Buffer (OUT BUFF)**; if so, it transfers the event data packet from LSOF FIFO to OUT-BUFF. It is care of the selected readout interface to read the event from the OUT BUFF and send it to the computer or to the concentrator board. This data transfer is independent of the trigger acquisition and it does not act on the Busy logic.
4. If the LSOF FIFO reaches a programmable occupancy level, the Busy signal is asserted to prevent further triggers to be accepted. All the triggers arrived while the Busy is active are rejected and counted in a dedicated counter. The LSOF FIFO almost full level, used to assert the Busy, must be programmed taking into account the maximum size of one event and the maximum number of pending triggers. Typically, this is done automatically by Janus 5203, but the user can set this level manually.
5. Multiple triggers can be accepted and enter the readout pipelines while reading the data of a previous trigger. The maximum number of pending triggers is determined by the almost full level of the TRGF FIFO, that is programmable from 1 to 512. If not programmed or set to 0 in Janus 5203, the FPGA uses the default value = 16. When the number of pending triggers reaches the programmed level, the Busy is asserted and no further trigger is accepted.

To summarize, the Busy signal is asserted when at least one of the following conditions is met:

- The number of pending triggers stored in the TRGF FIFO has reached the programmed threshold;
- The occupancy of the LSOF FIFO exceeds the programmed threshold;
- At least one RPF FIFO is almost full, meaning that there is not enough space to store one full event;
- If the user sets the trigger protection time (super-imposed dead-time after each trigger), the Busy remains asserted for that time
- If the user sets the trigger delay, the Busy remains asserted for the time of the delay

9.3.1 Buffer Occupancy Flags and Data Loss

When the sustained input hit rate is too high, the memory buffers can not store all the incoming hits and data loss will occur at some point of the acquisition chain. This may happen in the picoTDC or in the FPGA. There are several flags indicating the buffer overflow or almost full condition. Janus 5203 configures the picoTDC in order to transmit the *near full* flags in the header word. The FPGA combines all the different flags coming from the picoTDC as well as from its internal buffers and sends them to the readout software in two ways: in the event data trailers or in the service events. The event data trailers can be the same as the picoTDC trailers (they just pass through the FPGA) or can be packed into a single word inserted by the FPGA at the end of the event data packet (one word per chip). The service events are special events that

the FPGA injects in the data flow every second; these events have a special tag that allows the readout software (e.g. Janus 5203) to identify and process them in a separate thread with respect to the normal data. Janus 5203 uses the service events to monitor the flags and inform the user. In JanusC (console mode), short messages appear in the relevant line of the console window; in JanusPy, there are several LEDs that report the flags status. See **[RD3]** for more details.

This is the list of flags:

- **LSOF**: list data FIFO has reached the programmed threshold. When this flag is asserted, data are still flowing without any loss, but the busy is asserted and no further trigger is accepted.
- **Data Loss**: there is a second threshold in the LSOF FIFO , that is hard-coded in the firmware. When the 2nd threshold is reached, the FPGA starts to reject hit data to prevent FIFO overrun; the threshold is set in order to keep enough space to write at least headers and trailers and guarantee the consistency of the event data packets.
- **TRGF**: this flag is asserted when the TRGF FIFO in the FPGA reaches the programmed threshold. When this happens, the busy is asserted and no further trigger is accepted.
- **ROB**: picoTDC readout buffer is almost full. This buffer merges data of 16 channels.
- **RPF**: FPGA Readout Port FIFO; there is one FIFO per TDC port (1 port = 16 channels).
- **TDC Channel Buffer**: each channel in the picoTDC has a local buffer with programmable size. This buffer keeps the hits while waiting for the trigger. If the channel hit rate is too high, this buffer overflows and any further hit will be discarded by the picoTDC. In Janus 5203, the channel buffer flags are showed by coloring the relevant box in yellow in the statistics tab of the GUI.

As said, data loss may happen in different ways:

- The board is busy (for one of the reasons listed above) and the incoming triggers are rejected. In this case, it is not a hit loss (no hit is discarded), it is rather a “complete event loss”;
- The channel buffer fills up and the next incoming hits are not recorded. In this case, the FPGA will not be able to count for the rejected hits since they are discarded by the picoTDC without any communication to the FPGA but the channel full flag in the header;
- RPF overrun: there are some protections in the RPF to prevent data overrun. If the occupancy of this FIFO is too high, hits will be rejected and only headers/trailers are kept. The RPF overrun should never happen.
- LSOF overrun: this FIFO has 2 almost full thresholds; the 1st threshold is used to assert the busy, but no data is discarded when the occupancy exceeds that threshold. The 2nd threshold forces the FPGA to discard hits and keeps only headers and trailers to guarantee the data consistency. The lost hits are counted and a special flag (Data Loss) is asserted, therefore it is possible for the user to monitor the hit loss.

After the LSOF FIFO, no data loss is possible. The next blocks (Data Build, Output Buffer, Readout interfaces, memory buffers in the Data Concentrator) are not allowed to reject data. When any buffer along this chain is getting full, the readout flow is suspended and the “back-pressure” arrives up to the LSOF FIFO that asserts the busy signal. For example, a slow readout from the computer will cause a quick saturation of the buffers and a consequent activation of the Busy signal.

9.3.2 Data Throughput

The data throughput is a function of the trigger rate and event size (that is the average number of hits that belong to a trigger window). For each trigger, there is a fixed payload of 5 words (2 for the time stamp, 2 for the trigger ID, 1 for the size and data qualifier), followed by hit data (normally 1 word per hit, but can be 2 words per hit if leading and trailing edges are acquired separately). The event is completed by headers and trailers: the picoTDC transfer 2 words (1 Header + 1 Trailer) per port, that is a group of 16 channels. The FPGA can propagate the same words to the LSOF FIFO, thus having 8 words per event (16 in case of 128 channel version) or pack them into one single trailer (ONEWORD-trailer), thus having 1 word per event

(2 in case of 128 channel version).
To make an example, let's assume to have a trigger rate of 100 KHz and a trigger occupancy of 5 hits per channel. The board has 64 channels and header/trailer parameter is set to "One-Word" Trailer:

- Event size = (5 + 5 $\times$ 64 + 1) $\times$ 4 = 1304 bytes
- Trigger Rate = 100 kHz
- Data Throughput = 100 kHz $\times$ 1.304 kB = $\sim$130 MB/s

Just to make a simple test aiming to check the readout performances, the FPGA can be programmed to run in TEST mode. In this mode, no trigger is sent to the picoTDC and the event data are artificially produced by the FPGA. There are two test modes called TEST_1 and TEST_2. In mode 1, the FPGA generates one hit per channel, in mode 2 it generates 8 hits per channel. The channel enable mask works in test mode too, so the user can decide which channels are producing data and which channels are quiet. In test mode, there is no individual header/trailer, only the one-word trailer is produced, regardless the relevant setting.

9.4 Front Panel I/Os

The A5203(B)/DT5203 board is provided with four general purpose programmable LEMO I/Os connectors (see **Fig. 8.1**, **8.6** and **8.11**): two of them to be used as input and two of them to be used as output connectors. The description of the available functions of each connector is presented in this section.

9.4.1 Input Connectors

The two LEMO input connectors of the A5203(B)/DT5203 board accept LVTTL/NIM signals whose function is programmable. The two connectors can be programmed independently in order to perform different functions:

- **T0-IN**:
  - *Bunch Trigger Source*: See Sec. **9.2**.
  - *External Time Reference*: See Sec. **9.2**.
  - *Acquisition Start*: The input signal is used to start an acquisition (see "Start Run Mode" parameter inside Janus 5203 User Manual **[RD3]**).
  - *Veto Source*: The veto signal inhibits all bunch trigger signals as long as it is associated with an high logic level (see Sec. **9.2**).
- **T1-IN**:
  - *Bunch Trigger Source*: See T0-IN.
  - *External Time Reference*: See T0-IN.
  - *Acquisition Start*: See T0-IN.
  - *Veto Source*: See T0-IN.

9.4.2 Output Connectors

The two LEMO output connectors of the A5203(B)/DT5203 board allows the user to transmit programmable LVTTL signals. The two connectors can be programmed independently in order to perform different functions that are:

- **T0-OUT**:
  - *T0-IN*: The signal transmitted to the T0-IN connector is propagated, after having being processed by the FPGA, to the T0-OUT connector. This allows the user, when operating in multi-board configuration, to propagate the same signal to all boards, for instance.

  - *Bunch Trigger*: See Sec. **9.2**.
  - *Run*: The signal goes to an high logic level as soon as a new run is started and goes down when the run ends.
  - *Periodic Trigger*: See Sec. **9.2**.
  - *Busy*: See Sec. **9.2**.
  - *Digital Probe*: Different programmable logic signals can be used as digital probes for signal inspection (see Janus 5203 User Manual **[RD3]**).
  - *Square wave*: A periodic square wave having the same period of the internal periodic trigger of the board.
  - *TDL_SYNC*: Signal of synchronism from TDLink. The user can visualize the TDL_SYNC from multiple boards to check that they are all latched together.
  - *RUN_SYNC*: Signal of start run from TDLink. The user can visualize the RUN_SYNC from multiple boards to check that the starts run are all latched together.
  - *Zero*: A low logic level is transmitted (T0-OUT turned off). To be used when performing a daisy chained trigger distribution (see Sec. **9.4.4**).

- **T1-OUT**:
  - *T1-IN*: The signal transmitted to the T1-IN connector is propagated, after having being processed by the FPGA, to the T1-OUT connector. This allows the user, when operating in a multi-board configuration, to propagate the same signal to all boards for instance.
  - *Bunch Trigger*: See T0-OUT.
  - *Run*: See T0-OUT.
  - *Periodic Trigger*: See T0-OUT.
  - *Busy*: See T0-OUT.
  - *Digital Probe*: See T0-OUT.
  - *Square wave*: See T0-OUT.
  - *TDL_SYNC*: See T0-OUT.
  - *RUN_SYNC*: See T0-OUT.
  - *Zero*: See T0-OUT.

9.4.3 Bridged Connection (only for A5203(B))

The T0-IN and T1-IN connectors are, by default, 50 Ω terminated via jumpers. A schematic overview of the default configuration of the TX-IN connectors (with X being 0 or 1) is presented in **Fig. 9.8**.

Note: The jumpers are not available in A5203(B) main board rev.2.

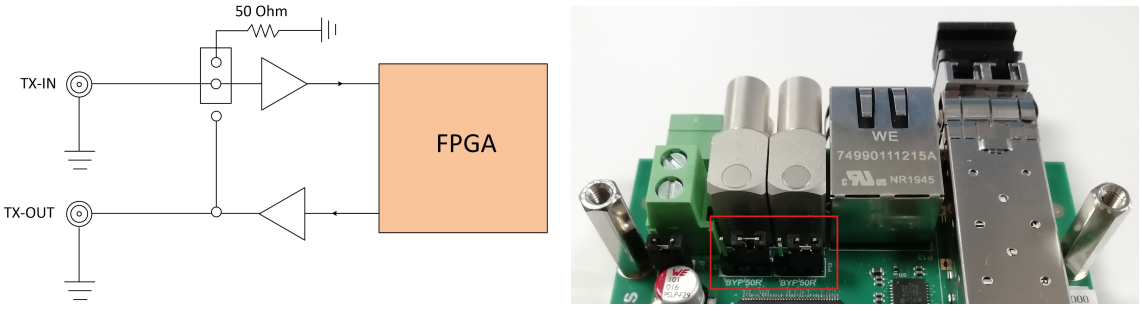


Fig. 9.8: Schematic diagram, on the left, of the TX-IN and TX-OUT connectors with the jumpers in the default position. On the right, an image of the jumpers in the A5203 board: both T1-IN and T0-IN jumpers are 50 Ω terminated.

In this configuration, the input signal on the TX-IN connector can be eventually propagated to the TX-OUT connector, but only after it has been transmitted to the FPGA, which introduces delays on the signal. The output signal from the TX-OUT connector has to be 50 Ω terminated. The TX-IN and TX-OUT connectors are independent in this configuration.

The user can perform a bridged connection by placing the jumper as it is shown in **Fig. 9.9**.

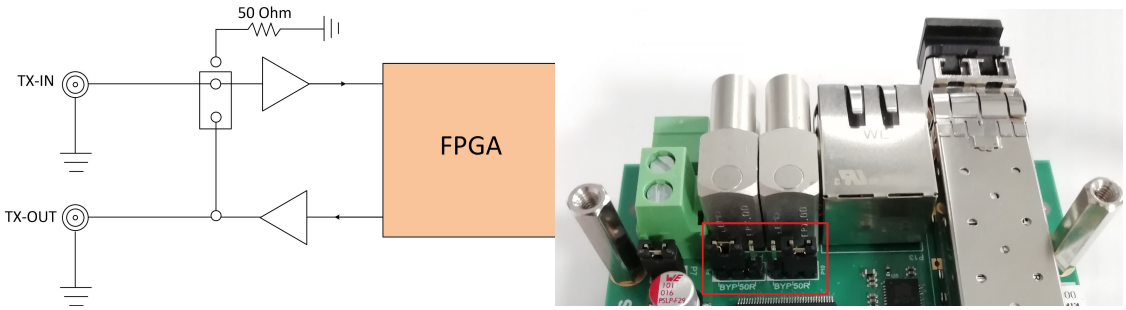


Fig. 9.9: Schematic diagram, on the left, of the TX-IN and TX-OUT connectors with the jumper positioned to form a bridged connection between TX-IN and TX-OUT. On the right, an image of the position of the jumper in the A5203 board: only the T0-IN jumper (on the left) is positioned to form a bridged connection.

In this configuration, a short circuit is created between the TX-IN and TX-OUT lines and the two connectors are no more independent. This second modality is particularly useful in order to perform a **Daisy Chained Trigger Distribution** (see Sec. **9.4.4**) or a **Wired-OR** (see Sec. **9.4.5**) when a system composed by several A5203(B) units is created.

9.4.4 Daisy Chained Trigger Distribution

This modality is particularly useful in case the user may want to propagate a common external trigger to all boards in the FERS-5200 system via the T1-IN/T1-OUT (or T0-IN/T0-OUT) connectors. However, by using a default configuration for the TX-IN jumpers, several delays would be introduced to the trigger signal when connecting in daisy chain TX-IN and TX-OUT connectors of all boards (due to FPGA processing of the signal). For this reason, a bridged connection for all TX-IN/TX-OUT connectors of all boards has to be created moving the jumpers as explained in Sec. **9.4.3**. In **Fig. 9.10**, a schematic overview of a system composed of N A5203 units with a daisy-chained connection of the TX-IN/TX-OUT connectors is presented.

In order to use an external trigger as a bunch trigger source directed to all boards, the user should then:

- Create a daisy chain as in **Fig. 9.10** with an external trigger transmitted to the TX-IN connector of the first board.
- Select as bunch trigger source the signal from the TX-IN connector for all boards.
- Turn off the output from the TX-OUT connector of all boards by selecting the ZERO option (see Sec. **9.4.2**). In this way, no high logic level is transmitted by the FPGA to the TX-OUT connector and that would interfere with the trigger signal transmitted in daisy chain.

As soon as a trigger is asserted, it is transmitted almost contemporary to all boards, with the only delay introduced by the cables connecting the TX-OUT connector of one board to the TX-IN connector of the next board.

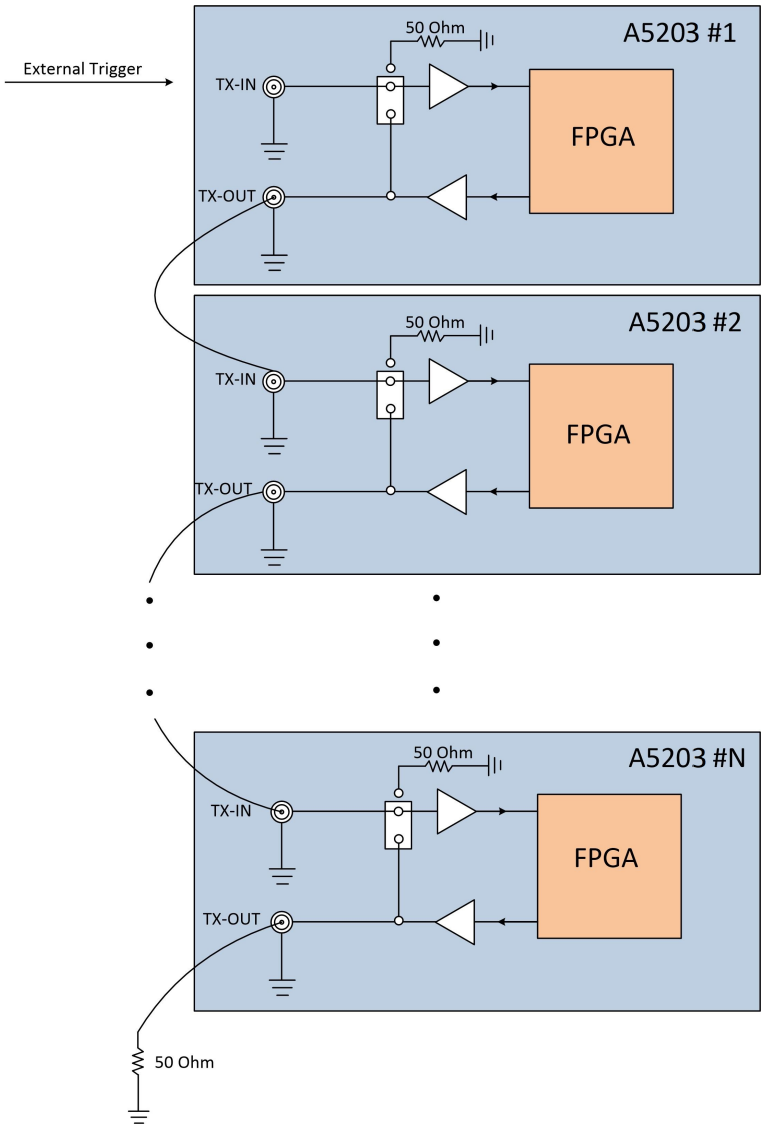


Fig. 9.10: Schematic diagram of a daisy chained trigger distribution.

9.4.5 Wired-OR

By performing slight changes to the system presented in Sec. **9.4.4**, the user can also create a wired-OR connection between all boards composing the FERS-5200 system. In **Fig. 9.11**, a schematic overview of a system composed of N A5203 units with the connection necessary to perform a wired-OR of the TX-IN/TX-OUT connectors is presented.

In order to use the wired-OR connection as a bunch trigger source directed to all boards, the user should then:

- Create a daisy chain connection as in **Fig. 9.11**.
- Select as bunch trigger source the signal from the TX-IN connector of all boards.
- Select the T-OR signal to be transmitted to the TX-OUT connector of all boards.

As soon as a T-OR trigger is asserted by one of the boards, a trigger signal is transmitted almost contemporary to all boards, with the only delay introduced by the cables connecting the TX-OUT connector of one board to the TX-IN connector of the next board.

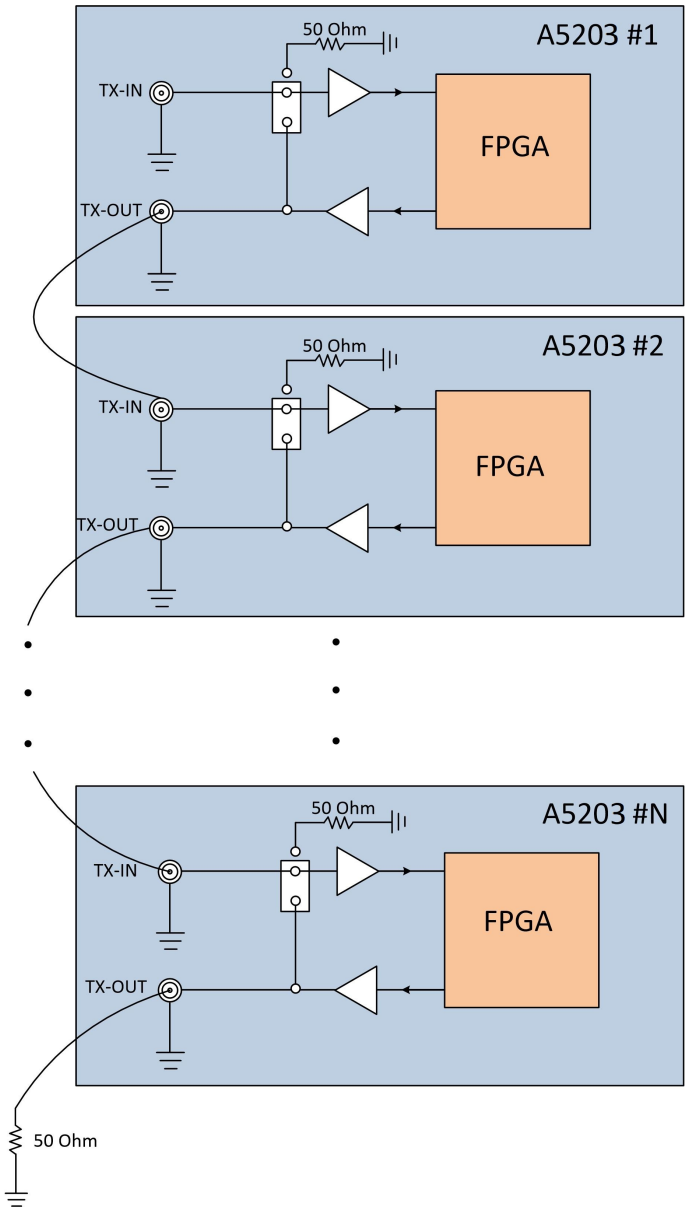


Fig. 9.11: Schematic diagram of a wired-OR connection.

9.5 Acquisition Modes

The data acquisition with the A5203(B)/DT5203 board is controlled by a bunch trigger signal as described in the following lines. It makes exception the Streaming acquisition mode, for which no trigger signal is needed.
The acquisition is simultaneous on the 64 (or 128, only for A5203B) channels of the unit. The trigger can either be local to the unit (e.g. a trigger given by software or by a signal generated by the FPGA), or can come from an external trigger logic.
The T0-IN/T1-IN connectors can be used to transmit (more than the external trigger) a veto signal, allowing to reject particular bunch triggers arriving to the board.

In Sec. **9.4.4** and Sec. **9.4.5**, two examples of trigger distribution for a system composed of several A5203 boards was presented. With the use of the FERS-Concentrator Board DT5215, the OR of the triggers of one chain can be combined with the triggers of other chains or with further external trigger sources. Eventually, the global trigger of the whole system could then be fed back into the T1-IN/T0-IN connectors of all FERS-5200 units. Alternatively, it would also be possible to propagate a global trigger from the DT5215 to the FERS-5200 units through the TDlink, provided that the application can tolerate some jitter and/or delay on the arrival time of the trigger.

The A5203(B)/DT5203 board can acquire data in four Acquisition Modes (plus two test modes), and four Measurement Modes. The former are described in the following lines, the latter are reported in the following section.

9.5.1 Common-Start and Common-Stop

In Common-Start and Common-Stop acquisition modes, a signal on the time reference channel (ch0 by default)[5] is the common start/common stop that open/close the acquisition gate, respectively. All the other N channels (63 in case of A5203/DT5203, or 127 in case of A5203B) provide ΔT time measurements, as shown in the schemes of **Fig. 9.12**:
$\Delta T_{N,start} = T_N - T_0$
$\Delta T_{N,stop} = T_0 - T_N$.
The gate width is programmable by software. Any hit falling outside the gate will be discarded.
Multi-hits acquisitions cannot be performed with these acquisition modes (although all multiple hits will be acquired by the picoTDC): only the first hit after the common start (before the common stop) inside the trigger acquisition window is recorded. The following (previous) hits are discarded.

In Common Start mode the event data are composed by the Trigger ID, the 56 bit coarse time stamp (LSB = 12.8 ns) for the absolute time, the Tref (i.e. Ch 0) fine time stamp (minimum LSB = 3.125 ps) and the list of the ΔT (minimum LSB = 3.125 ps) for the channels from 1 to 63 (only those channels that have been hit). If enabled, ToT is also acquired for all channels, including Ch0 (Tref).

The Zero Suppression (ZS) can be enabled in order to discard those channels that have not recorded any individual stop (individual start) hit during the defined trigger acquisition window. In particular, the advantage of using the ZS is that of reducing the amount of data transmitted from the board to the PC by transferring only significant data.

[5] The common time reference on channel 0 can be driven from the differential LVDS input or from the T0, T1 IN/OUT connectors (NIM or TTL), thus enabling the possibility to distribute the Tref signal among multiple boards through a daisy-chain.

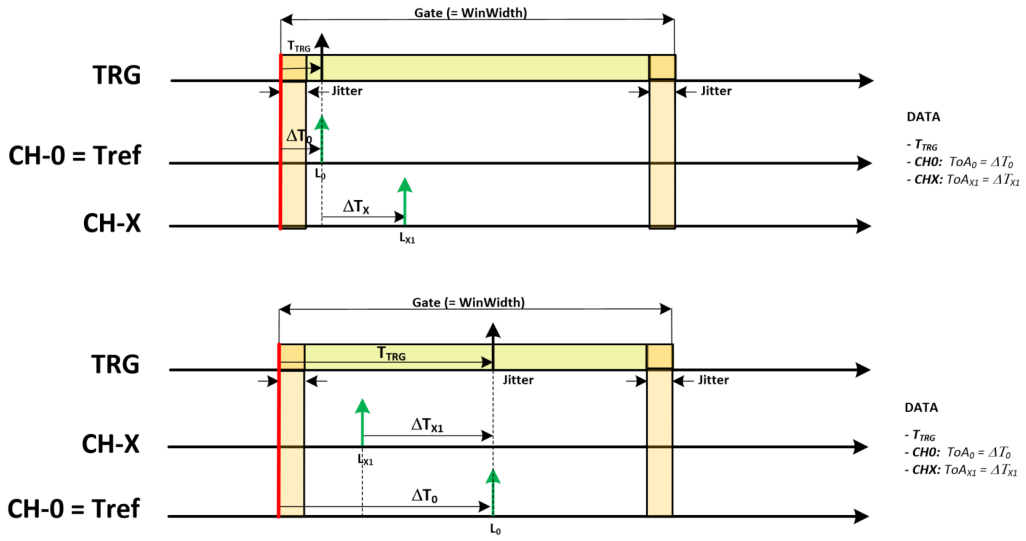


Fig. 9.12: Schematic diagram of Common Start (*top*) and Common Stop (*bottom*) acquisition modes.

9.5.2 Streaming

The Streaming acquisition mode implements a continuous hit recording, without any gate or trigger windowing. All hits received by the inputs are converted into a 64 bit time stamp (minimum LSB = 3.125 ps) and saved in the form of a sorted list. It is possible to save leading edge only, leading edge plus trailing edge (or leading edge plus ToT, **COMING SOON**). In order to make the data management easier, the list is split into time frames of fixed width, thus creating event data packets identified by an ID and a coarse time stamp.
With respect to the Common-Start/Common-Stop Acquisition Modes, the Streaming Acquisition Mode requires less data processing.

9.5.3 Trigger Matching

This acquisition mode is used to acquire multiple hits per channel that fall inside a defined trigger acquisition window (see the scheme of **Fig. 9.13**). The width and position of the trigger acquisition window can be defined by the software. There is no reference channel for the ΔT calculation. All time measurements are referred to the start of the acquisition window with coarse timing resolution (LSB = 25.6 ns). However, the relative timing between the channels keeps the maximum resolution of 3.125 ps.

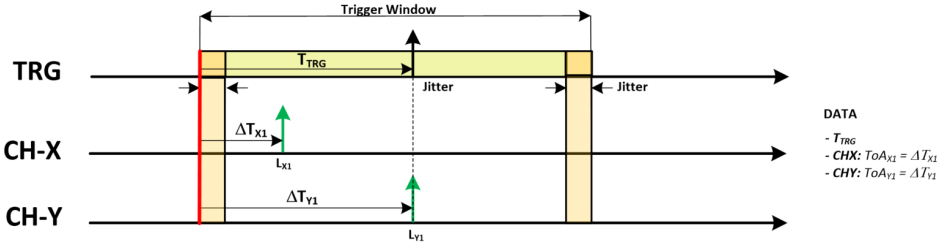


Fig. 9.13: Schematic diagram of Trigger Matching Acquisition Mode.

In Trigger Matching mode the event data are composed by the Trigger ID, the 56 bit coarse time stamp

(LSB = 12.8 ns) for the absolute time of the trigger, and the list of the hit time stamps of all channels (minimum LSB = 3.125 ps). It is possible to save the leading edge only, leading edge and trailing edge, or leading edge + ToT of the recorded hits.

9.5.4 Test Mode 1 & Test Mode 2

These test acquisition modes are used for readout tests and debug purposes: the picoTDC chip is disabled and fake data are produced by the FPGA to emulate the readout process. In Test Mode 1, 1 fake hit is created per channel per gate window, with hard-coded time values, using ch 0 as common start and the other channels from ch 1 to ch N (where N = 63 or 127) as common stops. Events are managed by the Janus 5203 software as if they were real data.
Test Mode 2 works in the same way as Test Mode 1, but producing 8 hits per channel, instead of 1. The 8 hits of one channel have the same time value.
Both test modes emulate the Common Start acquisition mode.

9.6 Measurement Modes

Depending on the data acquisition mode selected, a measurement mode can be chosen from the ones described below:

- **LEAD ONLY**: The picoTDC records only the leading edge of the hits, saving the timestamps over 24 bits (26 bits optional), thus with a maximum time range of 52.429 µs (209.715 µs). In case of the STREAMING acquisition mode, the timestamps dynamic is extended to 64 bits, thanks to a coarse time stamp added by the FPGA.

- **LEAD TOT8**: In addition to the leading edge timestamps, this measurement mode generates a list of ToT, that gives a rough estimation of the pulse amplitude (energy). The picoTDC acquires both leading and trailing edges, calculates the ToT and compacts the leading edge timestamp, and ToT over 8 bits, in a unique word (of 25/27 bits). At the maximum timing resolution, the dynamics is reduced with respect to the LEAD ONLY measurement mode, as the ToA is now written over 17/19 bits. Nevertheless, the ToA dynamics can be increased by diminishing the picoTDC resolution, down to 3.2 ns.

- **LEAD TOT11**: Similarly to the LEAD TOT8, the LEAD TOT11 provides the leading edge timestamp of the recorded hits and the ToT, this time over 11 bits. The ToA is then written over 14/16 bits.

- **LEAD TRAIL**: This measurement mode provides leading and trailing edges of the recorded hits, each in a single word. This permits to calculate the ToT at software level, and to have a wide dynamic range at the maximum time resolution of 3.125 ps. The LEAD TRAIL mode can be considered, then, as a LEAD TOT8 or LEAD TOT11, with an improved dynamics, but at the cost of a doubled data throughput.

Note: Not all the measurement modes can be chosen for each acquisition mode. Please, refer to previous section for more details.

Each detected, and not rejected, input signal hit is recorded as a 32 bit event. Events of 16 consecutive input channels, belonging to the same time acquisition window (gate or trigger window), are grouped together in one event packet. Information of the data acquisition, and of the board status are transferred, together with the event packet, in additional words. The latter can be an Header and a Trailer added, respectively, before and after the event packet (KEEPALL mode, i.e. +2 words per 16ch-event, meaning +8 words per 64ch-event packet, or +16 words per 128ch-event packet), or a one word Trailer added after the 64ch-event packet (ONEWORD mode, i.e. +1 word per 64ch-event packet, +2 words per 128ch-event packet).
Fig. 9.14, 9.16 and **9.18** are a schematic representation of the 32 bit events for the Lead Only, Lead ToT8 and Lead ToT11 measurement modes, in case the KEEPALL mode is selected.

Fig. 9.15, 9.17 and **9.19** are a schematic representation of the 32 bit events for the Lead Only, Lead ToT8 and Lead ToT11 measurement modes, in case the KEEPALL mode is selected.
The Lead Trail measurement mode is composed by two event words, one for the Lead Only and One for the Trail Only. The 32 bit content is thus the same of the Lead Only mode, both for the KEEPALL and ONEWORD modes.

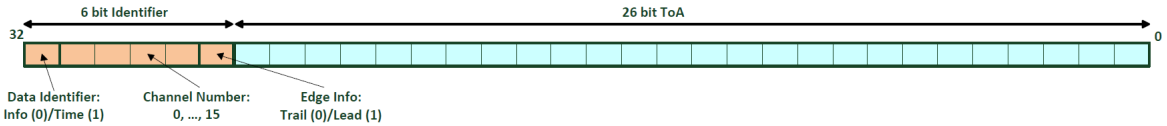


Fig. 9.14: 32-bit description of the Lead Only measurement mode, in case the Header and Trailer words are both acquired for each 8-channel event packet.

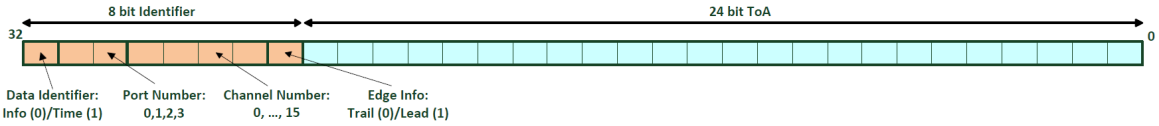


Fig. 9.15: 32-bit description of the Lead Only measurement mode, in case the Header and Trailer words are compressed in one word only for each 8-channel event packet.

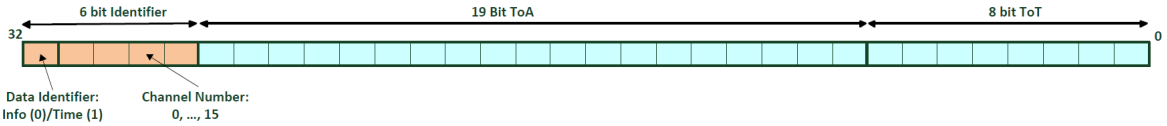


Fig. 9.16: 32-bit description of the Lead+ToT8 measurement mode, in case the Header and Trailer words are both acquired for each 8-channel event packet.

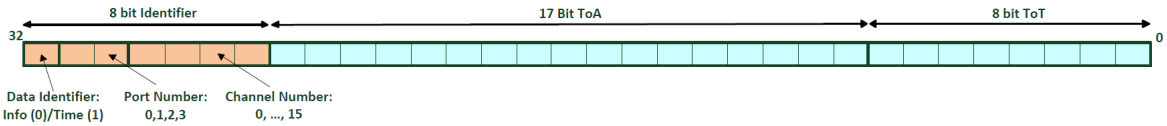


Fig. 9.17: 32-bit description of the Lead+ToT8 measurement mode, in case the Header and Trailer words are compressed in one word only for each 8-channel event packet.

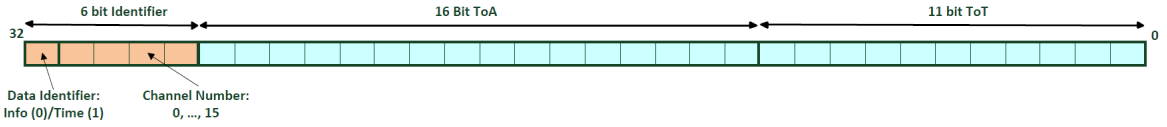


Fig. 9.18: 32-bit description of the Lead+ToT11 measurement mode, in case the Header and Trailer words are both acquired for each 8-channel event packet.

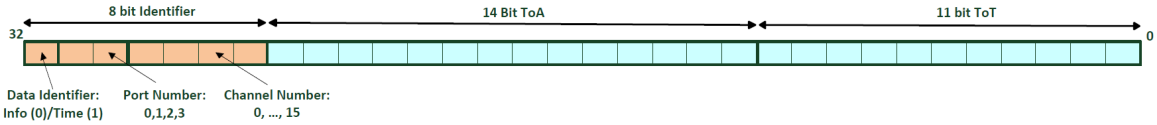


Fig. 9.19: 32-bit description of the Lead+ToT11 measurement mode, in case the Header and Trailer words are compressed in one word only for each 8-channel event packet.

9.7 Walk Correction

ToA measurements performed with the A5203(B)/DT5203 may suffer of amplitude walk issues. Avoiding the use of the bulky Constant Fraction Discriminator (CFD) electronics, commonly employed to reduce the walk effect, the walk correction through ToT is adopted and implemented in the Janus 5203 software **[RD3]**. The correction is performed by making use of the walk vs ToT calibration curve, obtained by measuring ToA and ToT values at different signal amplitudes.
With the walk correction, the time resolution improves of around a factor 10, passing from 200 ps RMS to 20 ps RMS.

10 TDlink Connection

In large readout systems, multiple FERS-5200 units can be connected together and managed by one DT5215 FERS Data Concentrator Module. Their control and read out is performed through the TDlink, a timing and data link able to distribute a reference clock, broadcast synchronization and acquisition commands (time reset, start run, stop run, bunch triggers), read/write registers for slow control, read event data packets. The physical layer of the TDlink is a 3.125 Gbit/s duplex link, running over optical fiber (LC connectors). The maximum readout bandwidth of the TDlink is 60 MB/s.

The TDlink guarantees that all the FERS-5200 units in the network run with a synchronized global time. Indeed, during the initialization, the DT5215 distributes a 156.25 MHz clock and sends a synchronization packet that allows the connected FERS-5200 units to reset their local time counter simultaneously. During the synchronization process, the TDlink master takes into account the propagation delay of each node along the daisy chain, with the granularity of one clock cycle (i.e. 6.4 ns). Once synchronized, any further broadcast command delivered by the DT5215 to the FERS units will be executed at the same local time in all the connected boards. This allows, for instance, to start the run simultaneously, thus having the same time stamp, in all the boards. Since the propagation delay can only be corrected with the precision of one clock cycle, a residual clock skew (phase shift) smaller than one clock period is still present between the boards after the synchronization. This skew does not affect the coarse time (trigger time stamping) but may produce an offset in the high resolution time measurements. This clock skew and the consequent offset in the time measurement is fixed within a group of 4 TDlinks, therefore it can be easily calibrated and corrected in the software. The clock skew is not deterministic between links belonging to two different groups and it may vary from run to run. Refer to **[RD4]** for more details.

10.1 picoTDCs Clock Connection

The FERS-5200 units TDlink connection to the DT5215 permits the synchronization of their FPGA's clock. The picoTDC clock is derived from this clock, but can be generated at a different phase for each unit. This fact results in a time variation of a couple of clock cycles (i.e. $\sim$7 ps), and, thus, in a worsening of the time resolution. As to avoid this, for high-resolution time measurements, in addition to the TDlink synchronization, picoTDC chips clocks need to be aligned together.
Two MCX clock connectors (CLK-IN, CLK-OUT) are present on the A5203(B)/DT5203 units. In a FERS-5200 network, it is possible to connect, in fan-in/fan-out, or daisy-chain the picoTDC clock lines via the apposite MCX connectors. An example of daisy-chain clock connection is shown in **Fig. 10.1**.
This clock propagation leads to an improvement of the time measurements, from around 20 ps resolution, to more or less 7 ps resolution.

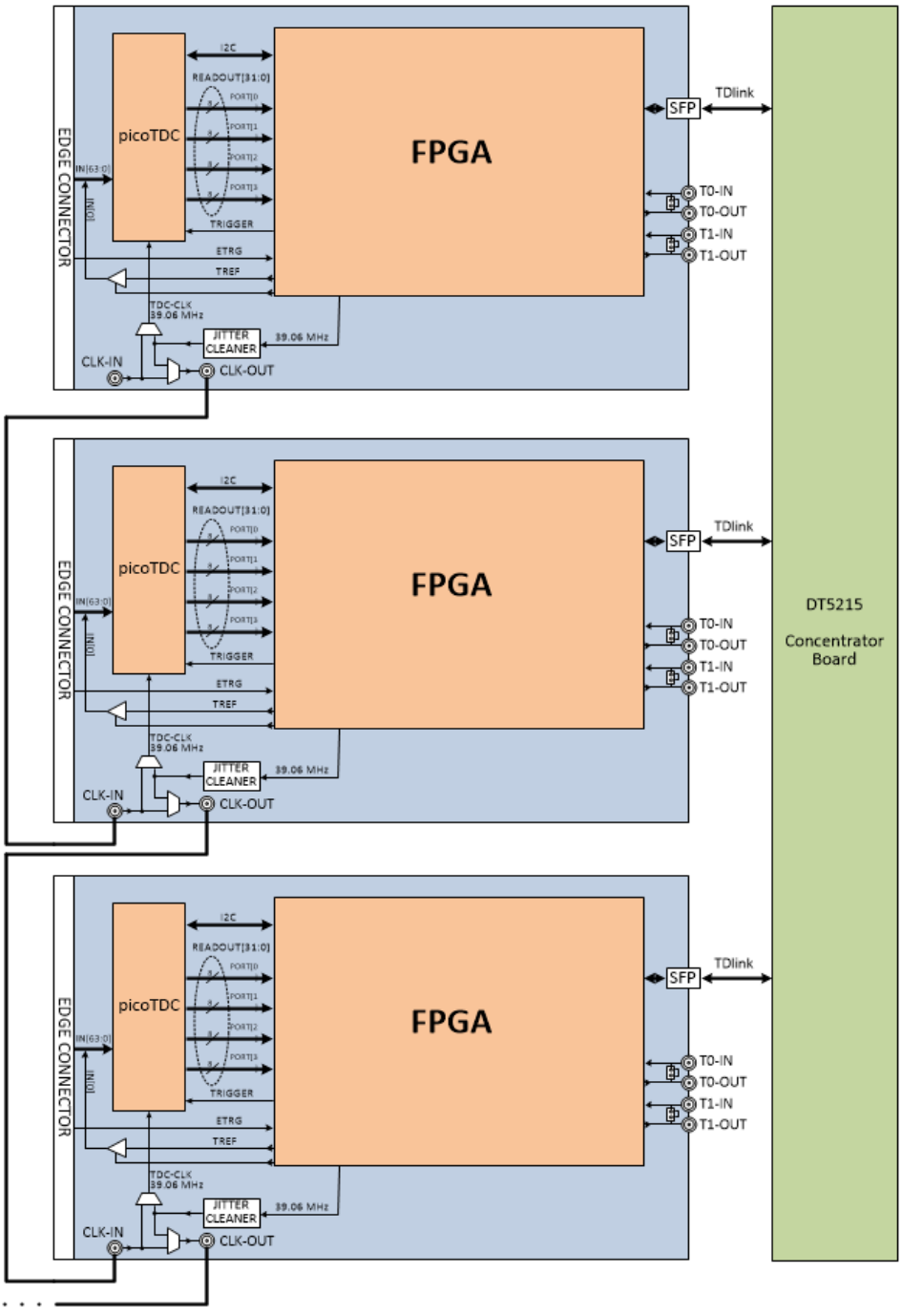


Fig. 10.1: Schematic diagram of a daisy chained picoTDC clock connection.

11 Getting Started

The aim of this chapter is to guide the user through the installation of the A5203(B)/DT5203 board and of the Janus 5203 software **[RD3]**. The basic instructions necessary to get familiar with the board and the software are also provided.

11.1 A5203(B)/DT5203 Installation and Power ON/OFF

To properly install and power ON/OFF the device the user is kindly suggested to follow the instructions below:

- Connect the AC/DC adapter to the DC power jack.
- Connect the power supply to the +12V connector of the A5203(B)/DT5203.

Note: In case of A5203(B), the DC connector polarities are [-.+] as marked in **Fig. 11.1**.

- The A5203(B) board immediately turns on, after few seconds the PWR green LED (see Sec. **8.1.1**) turns on and stays on as long as the board is connected to the power supply (see **Fig. 11.1**). To power on the DT5203, the user has to press the button on the module front panel (see Sec. **8.1.1**).

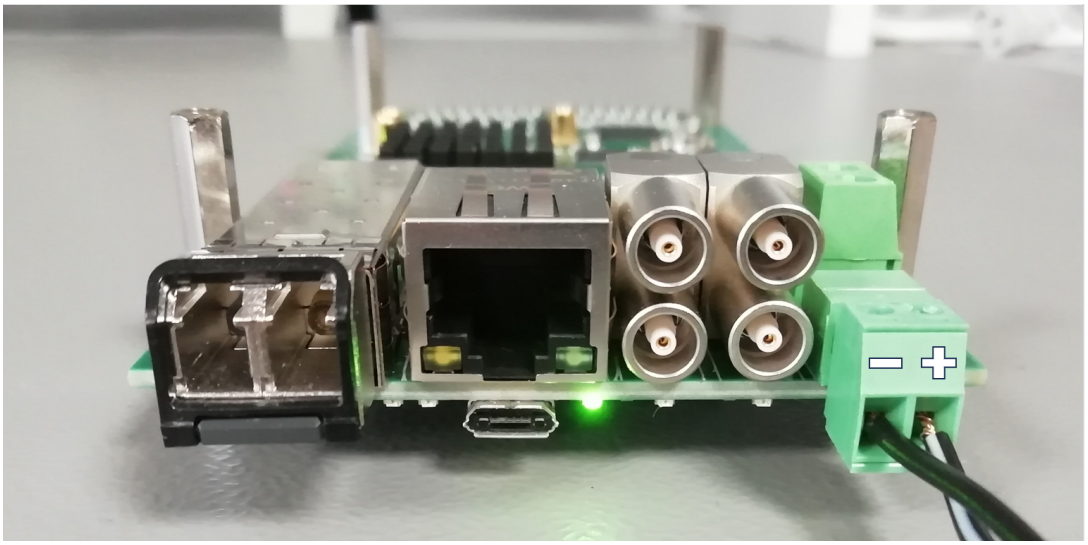


Fig. 11.1: A5203 status at power ON.

- To power off the A5203(B), disconnect the power supply from the board or extract the DC input switch (see **Fig. 8.4**). To power off the DT5203, the user has to press the button on the module front panel (refer to Sec. **8.1.1**).

FOR BENCH TESTS, IT IS HIGHLY RECOMMENDED TO NOT REMOVE THE METALLIC SPACERS MOUNTED ON THE NAKED BOARDS A5203(B)

11.2 How to Connect to the A5203(B)/DT5203

11.2.1 Ethernet Connection to the PC

The Ethernet connection of the A5203(B)/DT5203 can be done through a server, or it can be a point-to-point connection to the PC. In the latter case, the connection can be done using a crossed cable, a switch or a PC with a Gigabit Ethernet port. In order to properly configure the network, the user should follow the instructions below.

Note: The defaul IP Address of the A5203(B)/DT5203 is: **192.168.50.3**.

1. Connect the Ethernet cable from the A5203(B)/DT5203 to the PC.
2. Configure the Ethernet network of your PC.
   a. Open the path:
   `Control Panel - Network and Internet - Network and Sharing Center`
   as in **Fig. 11.2**.

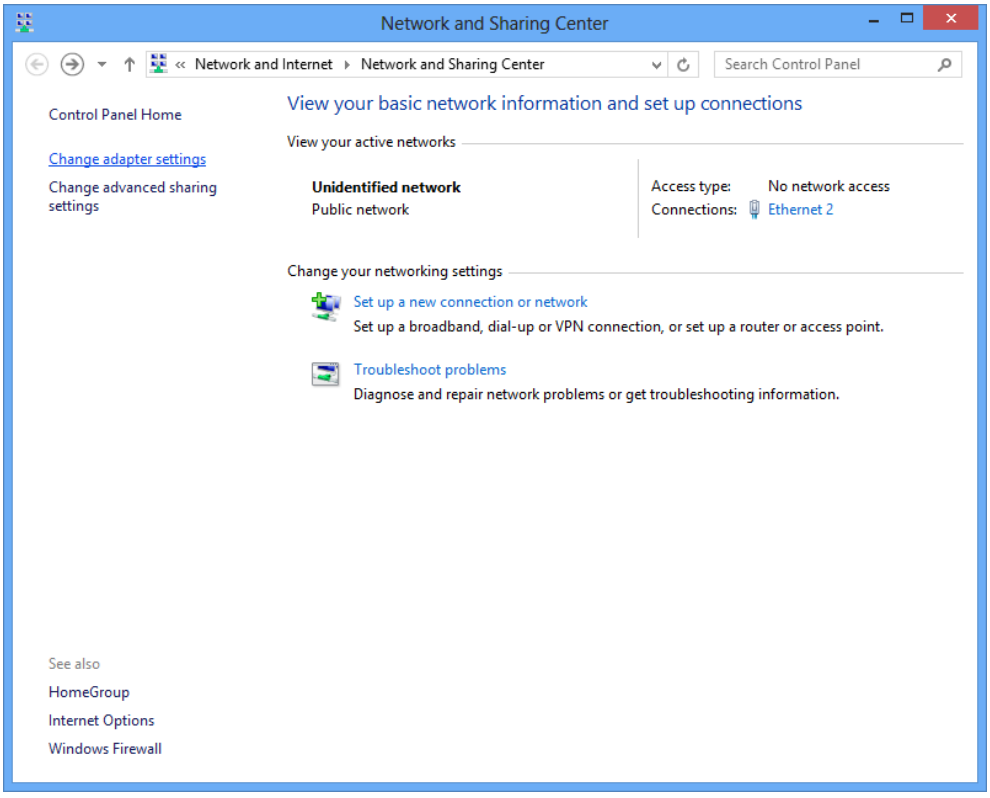


Fig. 11.2: The Network and Sharing Center window.

   b. Click on ”Change adapter settings”.

c. Right click on the Ethernet icon and select ”Properties”, as in **Fig. 11.3**.

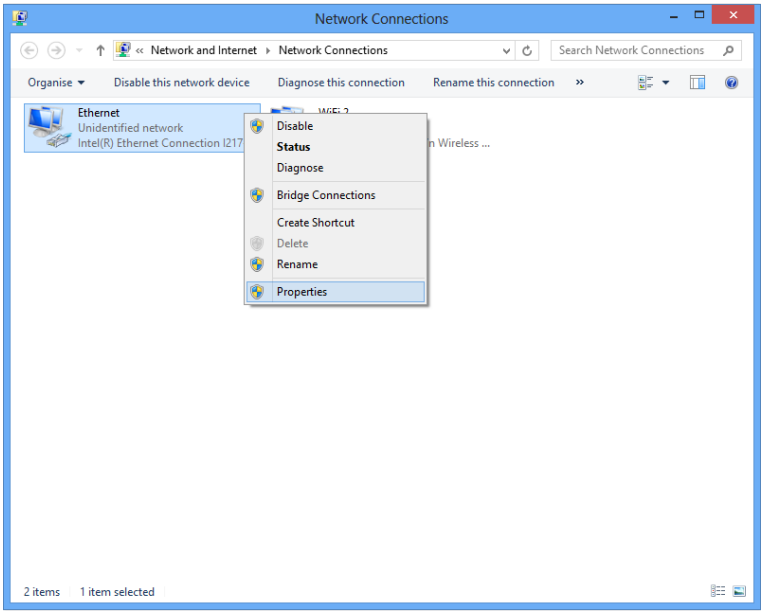


Fig. 11.3: Property window of the Ethernet network.

d. Click on ”Internet Protocol Version (TPC/IPv4)” and select ”Properties”, as in **Fig. 11.4**.

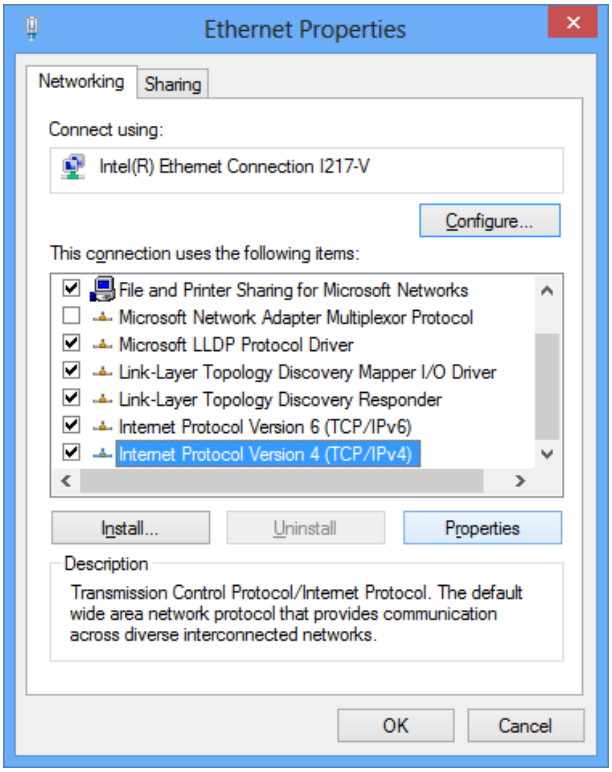


Fig. 11.4: Property window of the ”Internet Protocol Version (TPC/IPv4)”.

e. Copy the configuration in **Fig. 11.5** on the ”Internet Protocol Version (TPC/IPv4) Properties” window and press ”OK”.

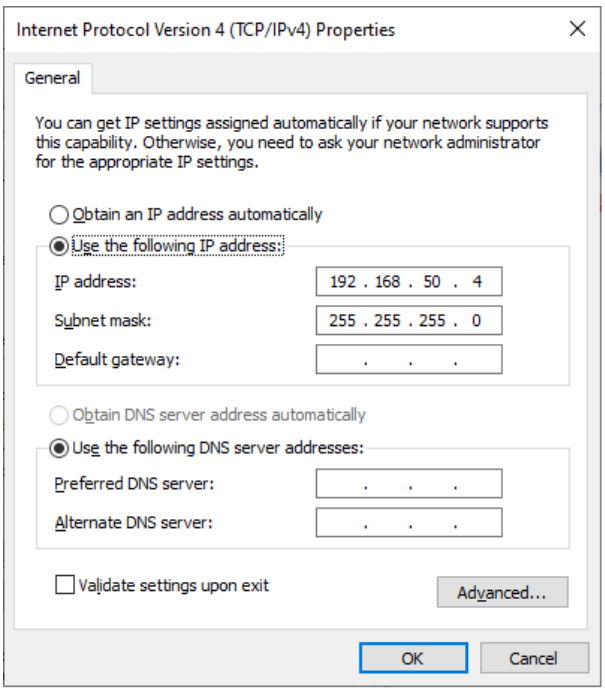


Fig. 11.5: ”Internet Protocol Version (TPC/IPv4) Properties” window.

3. The user can test if the communication between the PC and the A5203(B)/DT5203 is established by opening the ”Command Prompt” and typing the same command as in **Fig. 11.6**. If the communication is correctly established, the output message should be similar to that in **Fig. 11.6**.

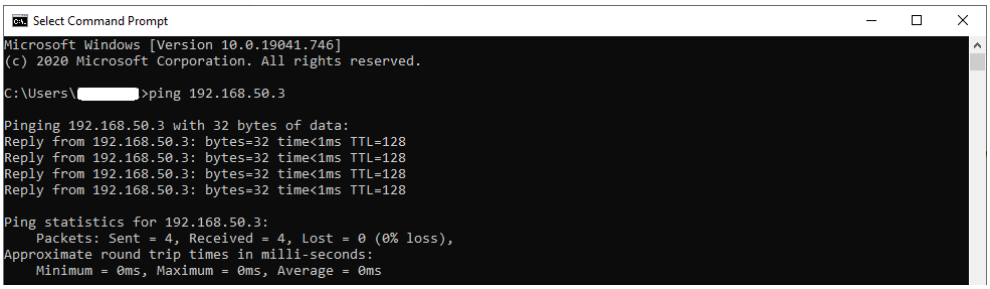


Fig. 11.6: Command prompt window with the command for testing the communication.

It is possible to monitor and define the Ethernet settings via the dedicated Web Interface. In order to access it, the user should:

1. Open a browser and enter the web address **192.168.50.3**. The homepage of the graphical web interface will open (see **Fig. 11.7**).
2. Open the Configuration tab (see **Fig. 11.8**). This window allows the user to read the device information, like the serial number, the hardware and firmware revision. Moreover, it is possible to set an IP address of the instrument different with respect to the default one. This last operation can be particularly useful in case the user wants to perform a multi-board Ethernet connection and therefore needs to associate each board with a different IP address (see Janus 5203 User Manual **[RD3]** for more details).

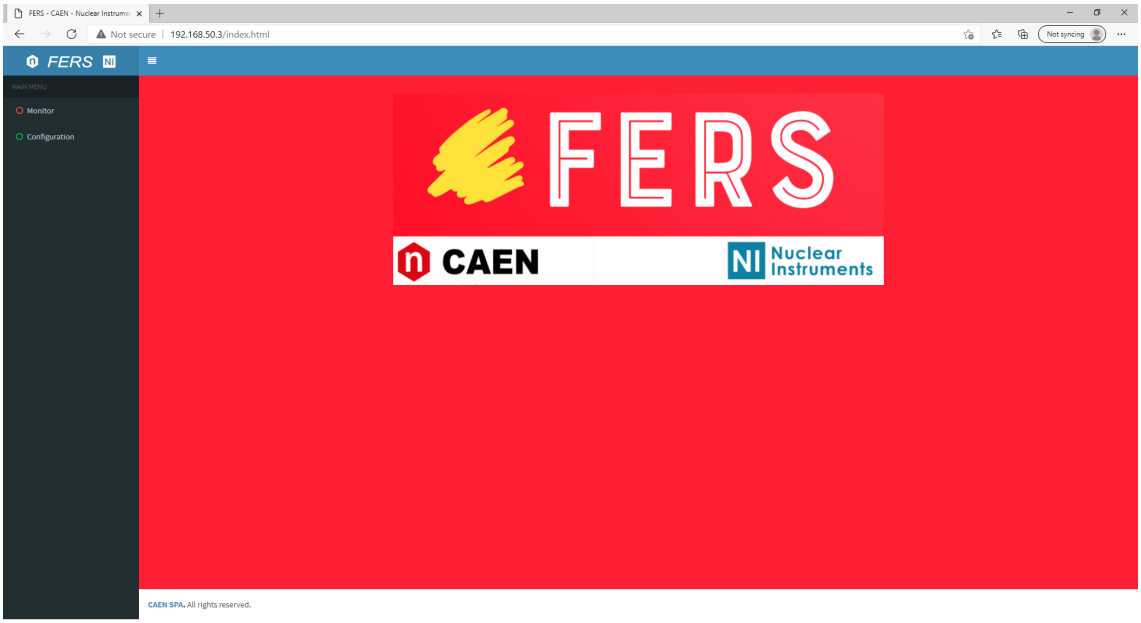


Fig. 11.7: Web Interface opening view.

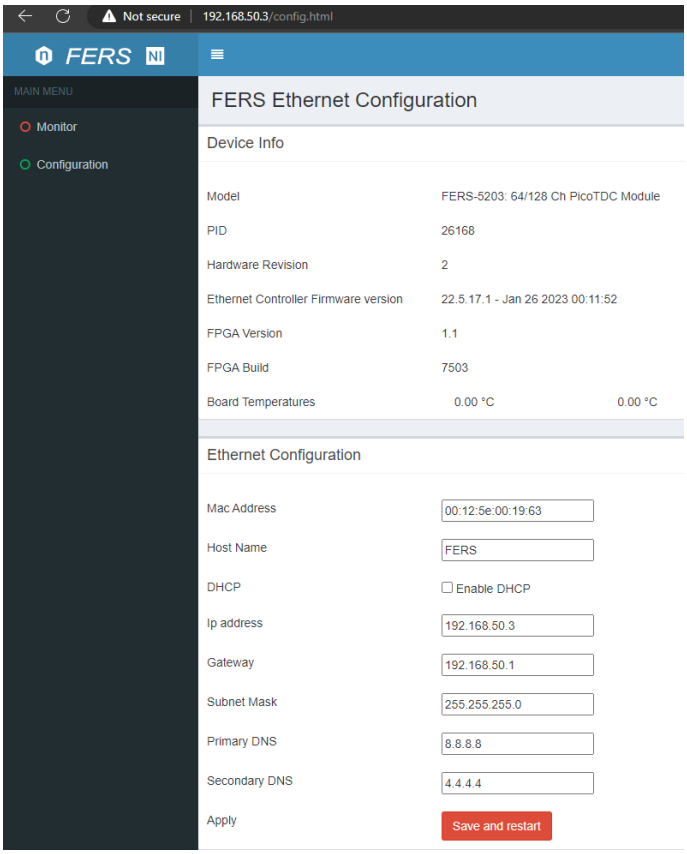


Fig. 11.8: Configuration Tab of the Web Interface for Ethernet settings.

11.2.2 USB Connection to the PC

In order to establish a USB connection between the board and the PC, the user should follow the instructions below (Windows only):

1. Download from the A5203(B)/DT5203 website the required USB driver folder according to the user PC platform and unzip it.
2. Connect the micro USB cable from the A5203(B)/DT5203 to the PC and power on the device. At this stage, the A5203(B)/DT5203 is not yet recognized by the OS.
3. From the ”Device Manager” window, right click on the ”Simple WinUSB Device Demo” item in the ”Other devices” list (see **Fig. 11.9**) and select the ”Upgrade Driver” option.

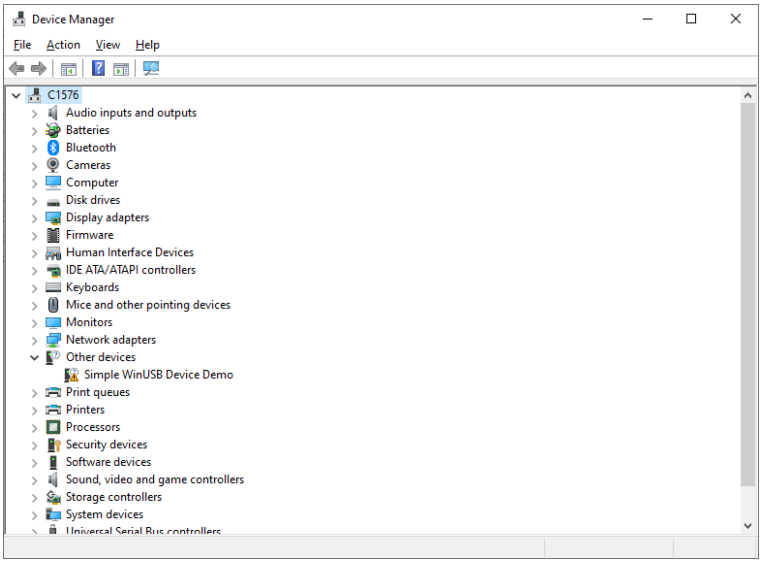


Fig. 11.9: Device Manager window with the USB driver not yet installed.

4. Select ”Browse my computer for drivers” (see Fig. **11.10**).

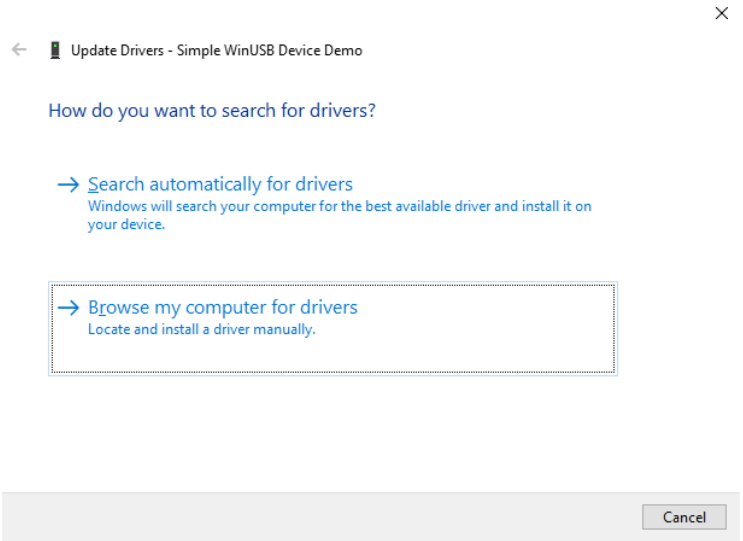


Fig. 11.10: ”Update Drivers” window.

5. Point the driver folder in the PC destination path through the ”Browse...” button and check ”Include subfolders” (see **Fig. 11.11**).

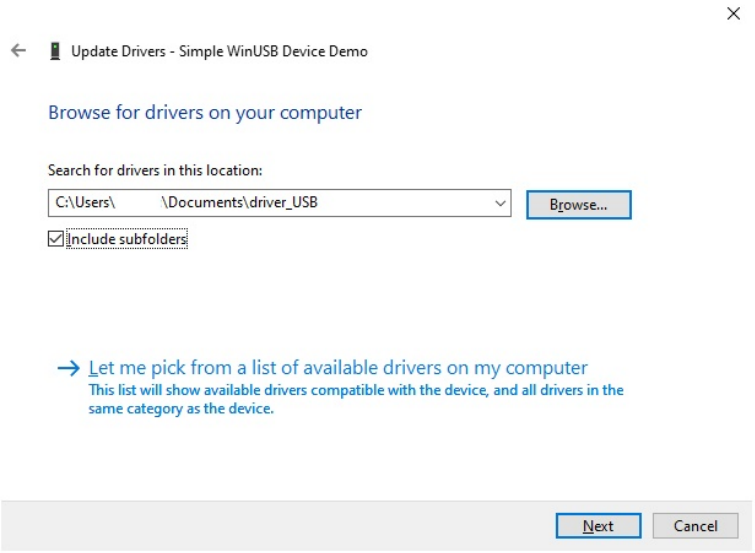


Fig. 11.11: ”Update Drivers” window including path to the USB driver.

6. Windows informs the driver software is successfully installed (see **Fig. 11.12**).

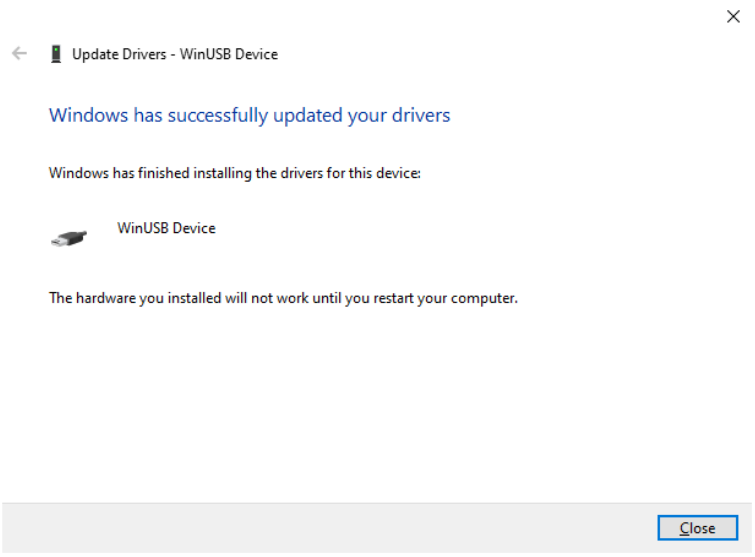


Fig. 11.12: USB driver installation completed.

7. The device is recognized by the operating system and listed in the ”Device Manager” window among ”Custom USB Devices” (see **Fig. 11.13**).

Note: The USB connection cannot be used to access the Web Interface. Please, use the Ethernet connection.

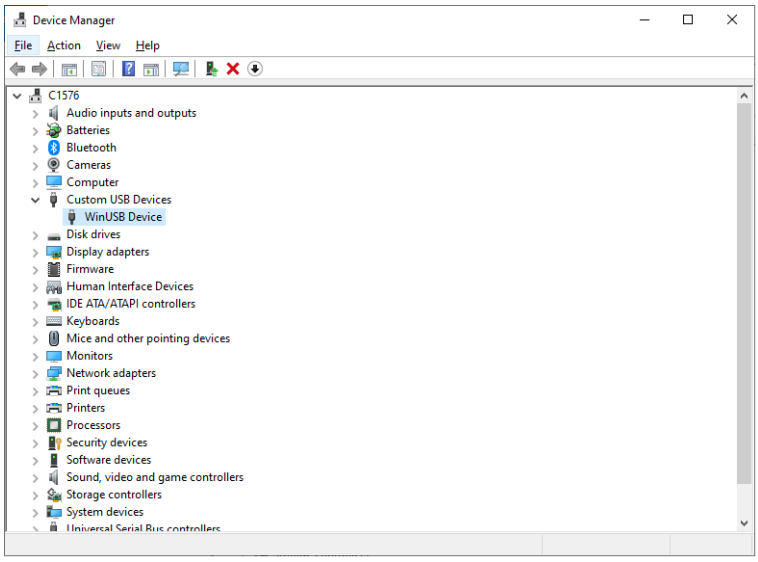


Fig. 11.13: USB device correctly recognized.

11.3 Software Installation

The A5203(B)/DT5203 is fully supported by the Janus 5203 software for Windows®and Linux®.

Janus 5203 requires the third-party software Python release 3.8.1 or later, downloadable from the python website. Before installing the software, please make sure that:

- The A5203(B)/DT5203 hardware is properly installed (refer to Sec. **11.1**).
- The A5203(B)/DT5203 connection is properly set. (see Sec. **11.2**).
- The required USB driver (Windows only) is correctly installed in case of a USB connection to the board (refer to Sec. **11.2.2**).

11.3.1 Windows Installation

Janus 5203 does not have an installer. It is provided by CAEN as a compressed ".zip" file to be unpacked in a directory on the PC that the user has write access to. A detailed description of the Janus 5203 software structure can be found in the Janus 5203 User Manual **[RD3]**. The user should follow the instructions below in order to properly run the software:

1. Download the Janus 5203 software from CAEN website for Windows OS (login required).
2. Extract the files and enter the "bin" folder (see **Fig. 11.14**) inside the Janus 5203 software folder.

Note: The Janus 5203 software can be used in two ways: "Console Mode" and "GUI Mode". In this chapter, the "GUI Mode" will be described. The user should refer to the Janus 5203 User Manual **[RD3]** for a more detailed description of the "Console Mode".

3. Double click on the **JanusPy.pyw** executable file. No installation steps will be required and a window similar to the one in **Fig. 11.15** will be opened. The connection between the software and the board is not yet established.

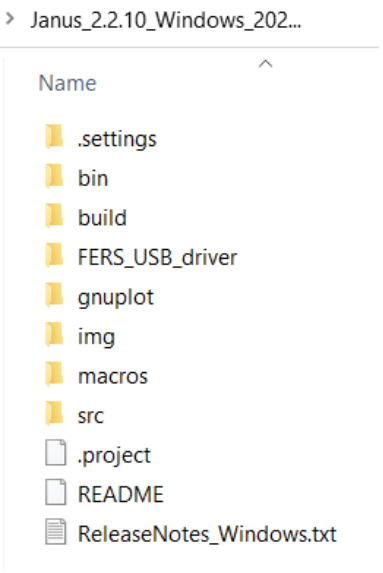


Fig. 11.14: View of the Janus 5203 software folder.

Note: The screenshots reported in this chapter may change between different versions of the software.

11.3.2 Linux Installation

Janus 5203 for Linux is provided by CAEN as a compressed ".tar.gz" file to be unpacked in a directory on the PC that the user has write access to. A detailed description of the Janus 5203 software structure can be found in the Janus 5203 User Manual **[RD3]**. The user should follow the instructions below in order to properly run the software:

1. Download the Janus 5203 software from CAEN website for Linux OS (login required).
2. Extract the files in folder with read/write permission and enter the "Janus" folder.
3. Run
   `sudo sh Janus_Install.sh`
4. The script will search for missing package. If any is found, please, install it and run again the Janus_Install.sh file.
5. Once completed, go into the folder "bin" and run
   `python3 JanusPy.pyw` for GUI mode or
   `./JanusC` for console mode

11.3.3 First Connection

1. Below the "PATH" field in the Connect tab the user has to write down the type of connection he/she is using to connect to the board. In case of a single board the available options are:
   - "usb:0" in case of an USB connection. It is also possible to use the syntax "usb:PID", being PID the unique board identification number that is located either on the bottom of the A5203(B) PCB or on the front panel of the DT5203.
   - "eth:192.168.50.3" (as it is shown in **Fig. 11.15**) or another Ethernet address in case this was changed (see Sec. **11.2.1**).
2. Press on the Apply button in order to make the changes effective.

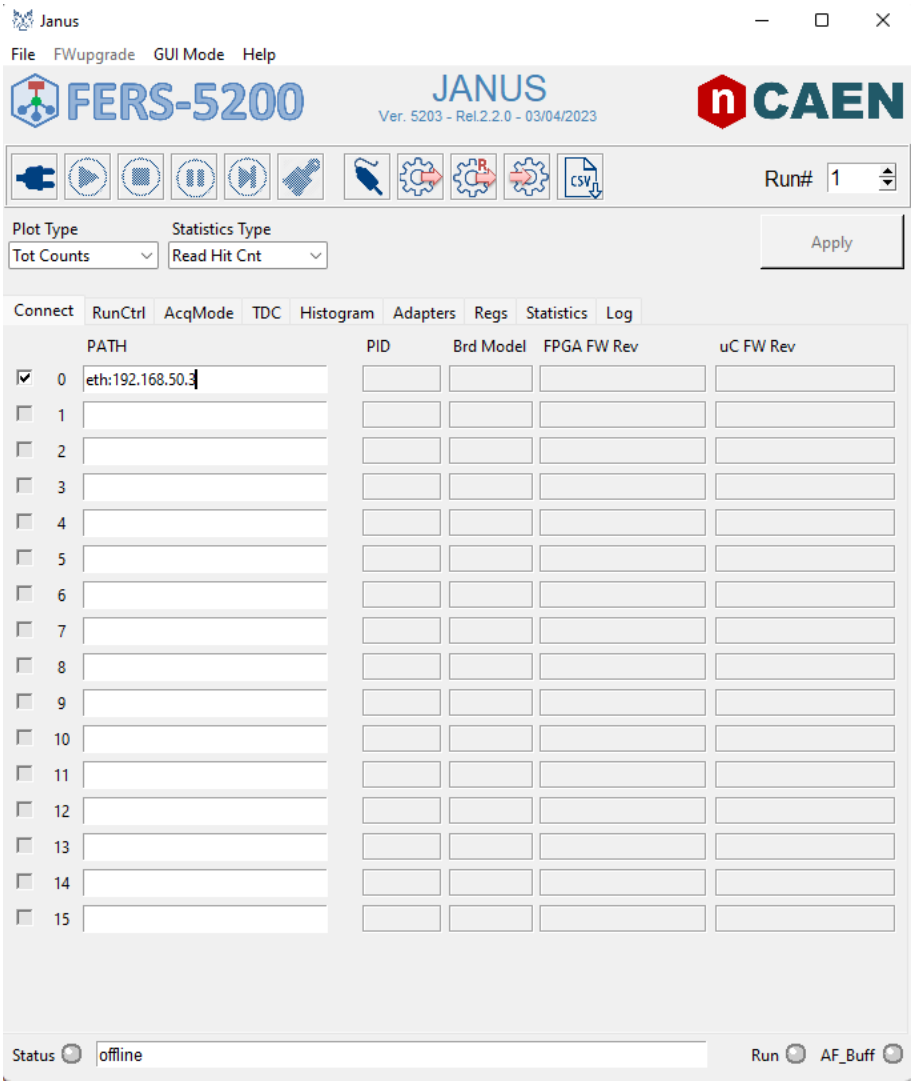


Fig. 11.15: Starting window of the Janus 5203 software GUI.

Note: For the instructions necessary to perform a multi-board connection via Ethernet or USB, the user should refer to the Janus 5203 User Manual **[RD3]**.

Note: Every time a change in the parameter settings is performed, the Apply button becomes red. The user has to press the button in order to make the changes effective.

3. Click on the Connect button on the top left part of the Janus 5203 window .
   The connection between the software and the board is established and the *gnuplot* graphic interface is opened as in **Fig. 11.16**.

Note: In case the connection is not established, an error message will be displayed in the status bar in the bottom part of the Janus 5203 GUI as in **Fig. 11.17**. In this case, the user is kindly suggested to re-check all the instructions in Sec. **11.2**.

Fig. 11.16: Janus 5203 GUI starting interface when the connection is correctly established.

Fig. 11.17: Message displayed in the Janus 5203 application in case of a not working USB connection.

11.3.4 GUI mode selection

The user has the possibility to select a simpler or advanced view of the Janus 5203 GUI by selecting the corresponding option from ”Gui Mode” menu. The ”Basic” view is recommended for beginner users to see just the fundamental settings.

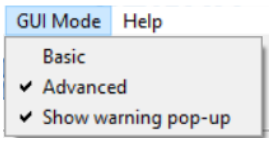


Fig. 11.18: GUI Mode menu to choose between Basic/Advanced GUI visualization mode.

12 Firmware & Upgrade

The A5203(B)/DT5203 board hosts one Artix XC7A75T-1FGG676C **[RD5]** FPGA with the corresponding firmware stored onto the on-board FLASH memory. At power-on, the microcontroller reads the FLASH memory page and programs the module automatically loading the FPGA firmware copy. It is possible to upgrade the FPGA firmware via USB or Ethernet, by writing the FLASH, taking advantage of the Janus 5203 software **[RD3]**.

In order to perform the FPGA firmware upgrade, the user should follow the instructions below:

1. Connect the board to the Janus 5203 software according to the instructions reported in Sec. **11.3** either via USB or Ethernet.
2. Click on the ”FWupgrade” drop-down menu that is present on the Janus 5203 Menu Bar (see **Fig. 12.1**). The ”Upgrade FPGA” option is visualized. By clicking on it, a window similar to that reported in **Fig. 12.2** is opened.

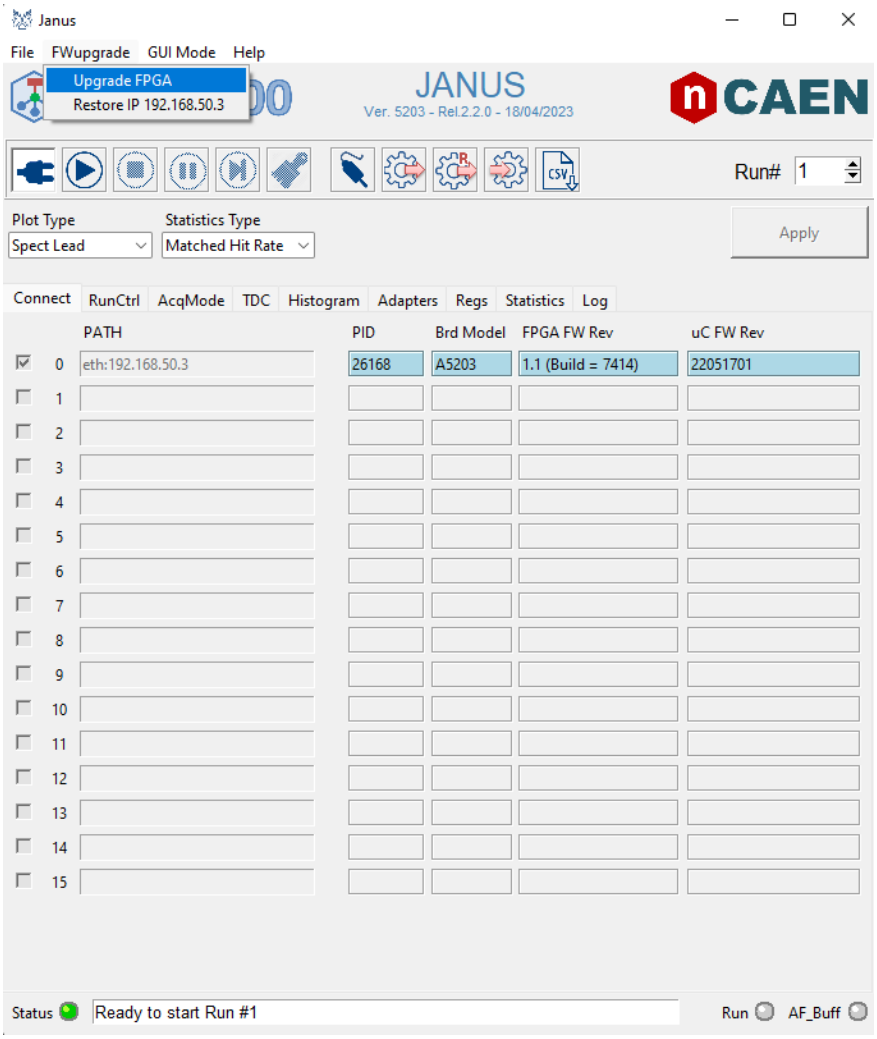


Fig. 12.1: A5203 board connected with the old version of FPGA firmware loaded.

3. Click on the ”Browse” button. A window allowing the user to select the new FPGA firmware file is

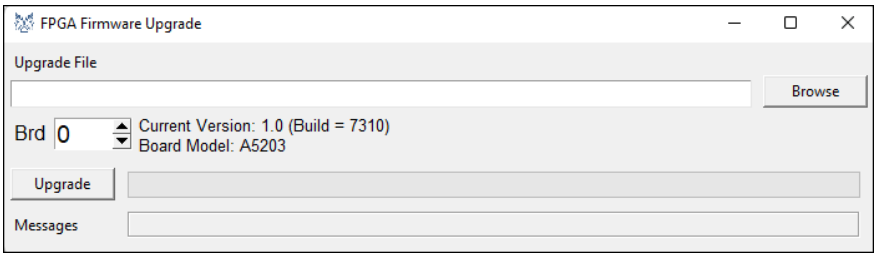


Fig. 12.2: FPGA Firmware Upgrade window.

opened. The latest version of FPGA firmware (.ffu file) can be downloaded from CAEN A5203(B)/DT5203 webpage (”Download” section).

4. Once the selection is finished, the file location is displayed on the ”Upgrade File” field, as in **Fig. 12.3**.

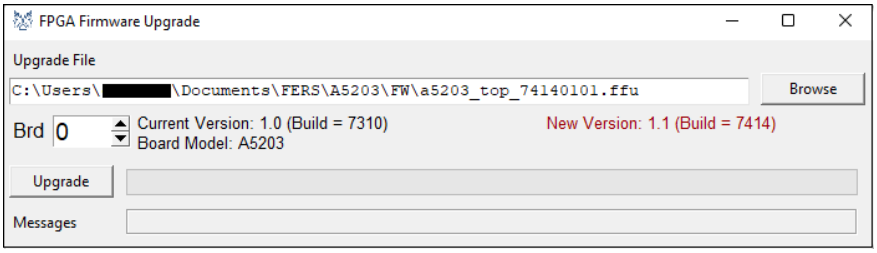


Fig. 12.3: FPGA Firmware Upgrade window with the new FPGA firmware file path visualized.

5. Press the ”Upgrade” button. First, the FPGA firmware file in the A5203(B)/DT5203 board is erased, then the new FPGA firmware selected by the user is written onto the on-board FLASH memory. The user can check the progress of this operation by looking at the green bar and at the ”Messages” field in the FPGA Firmware Upgrade window (see **Fig. 12.4**).

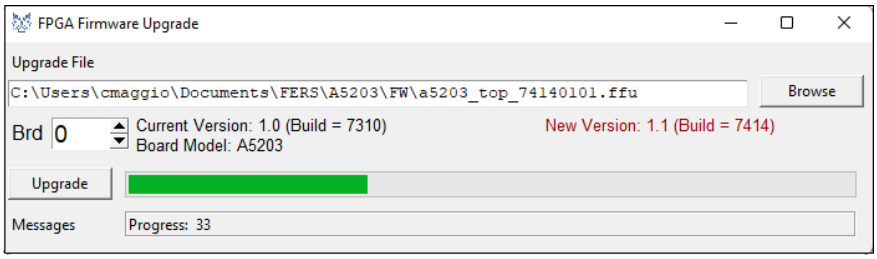


Fig. 12.4: FPGA Firmware Upgrade window while the firmware upgrade is in progress.

6. Once the operation is finished, the new FPGA firmware is loaded (the board connection with the Janus 5203 software is kept). The user can check that the new FPGA firmware version has been correctly loaded by looking at the FPGA FW Rev field in the Connect Tab of the Janus 5203 GUI.

13 Instructions for Cleaning

The equipment may be cleaned with isopropyl alcohol or deionized water and air dried. Clean the exterior of the product only.
Do not apply cleaner directly to the items or allow liquids to enter or spill on the product.

13.1 Cleaning the Air Vents

It is recommended to occasionally clean the air vents (if present) on all vented sides of the board. Lint, dust, and other foreign matter can block the vents and limit the airflow. Be sure to unplug the board before cleaning the air vents and follow the general cleaning safety precautions.

13.2 General Cleaning Safety Precautions

CAEN recommends cleaning the device using the following precautions:

- Never use solvents or flammable solutions to clean the board.
- Never immerse any parts in water or cleaning solutions; apply any liquids to a clean cloth and then use the cloth on the component.
- Always unplug the board when cleaning with liquids or damp cloths.
- Always unplug the board before cleaning the air vents.
- Wear safety glasses equipped with side shields when cleaning the board.

14 Device Decommissioning

After its intended service, it is recommended to perform the following actions:

- Detach all the signal/input/output cable
- Wrap the device in its protective packaging
- Insert the device in its packaging (if present)

THE DEVICE SHALL BE STORED ONLY AT THE ENVIRONMENT CONDITIONS SPECIFIED IN THE MANUAL, OTHERWISE PERFORMANCES AND SAFETY WILL NOT BE GUARANTEED

15 Disposal

The disposal of the equipment must be managed in accordance with Directive 2012/19 / EU on waste electrical and electronic equipment (WEEE).

The crossed bin symbol indicates that the device shall not be disposed with regular residual waste.

16 Technical Support

To contact CAEN specialists for requests on the software, hardware, and board return and repair, it is necessary a MyCAEN+ account on www.caen.it:

https://www.caen.it/support-services/getting-started-with-mycaen-portal/

All the instructions for use the Support platform are in the document:

A paper copy of the document is delivered with CAEN boards.
The document is downloadable for free in PDF digital format at:

https:/www.caen.it/safety-information-product-support

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