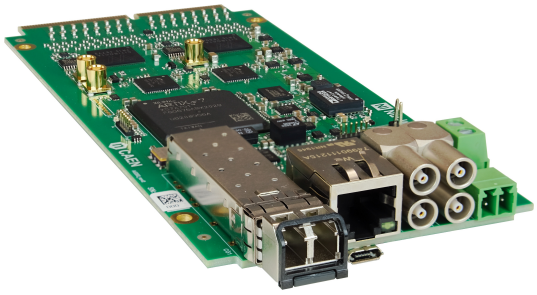
Rev. 4 - Jan 25th, 2023

A5202/DT5202

64-Channel Citiroc-1A Unit for FERS-5200



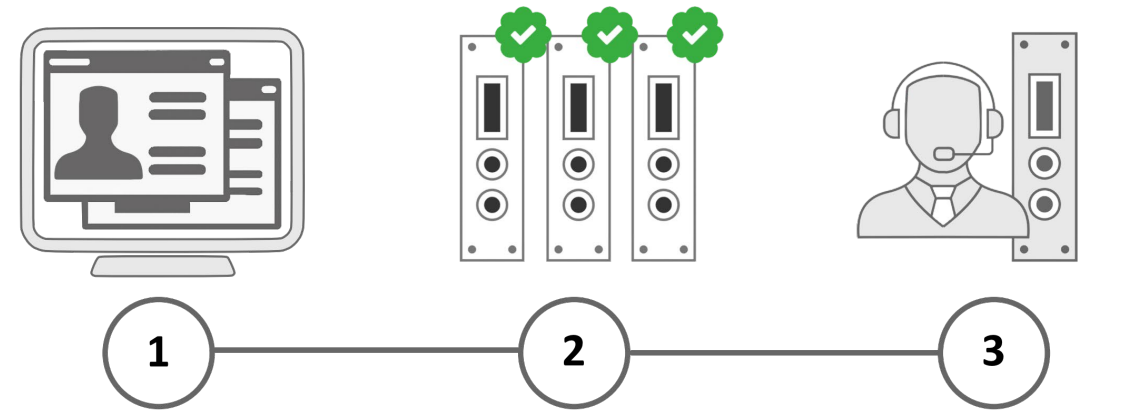
CAEN
Tools for Discovery

User Manual
UM7945

Register your device

Register your device to your **MyCAEN+** account and get access to our customer services, such as notification for new firmware or software upgrade, tracking service procedures or open a ticket for assistance. **MyCAEN+** accounts have a dedicated support service for their registered products. A set of basic information can be shared with the operator, speeding up the troubleshooting process and improving the efficiency of the support interactions.

MyCAEN+ dashboard is designed to offer you a direct access to all our after sales services. Registration is totally free, to create an account go to https://www.caen.it/become-mycaenplus-user and fill the registration form with your data.



https://www.caen.it/become-mycaenplus-user/

Purpose of this Manual

This document contains the hardware description of the A5202 and DT5202 FERS-5200 units, their principle of operation as well as all the instructions to start using them in a correct and easy way.

Change Document Record

Date	Revision	Changes
Mar 17th, 2021	00	Initial Release
May 21st, 2021	01	Inserted A5202 CE conformity warnings in Chap. **3**. Inserted A5202/DT5202 accessories table (Tab. **1.1**). Inserted pinout description in Sec. **7.5**. Updated Sec. **9.2.4**, Sec. **8.1.2** and Chap. **10** according to the Janus software release 1.1.5. Inserted Sec. **8.5.4** and Sec. **10.7.2**.
Sep 9th, 2021	02	Inserted DT5202 updated views in Chap. **7**. Updated list of accessories in Tab. **1.1**. Updated power consumption values in Tab. **2.1** according to FPGA firmware release 2.3. Inserted Chap. **6** regarding FPGA cooling management. Updated LED function description in Sec. **7.3**, updated Sec. **8.3** and Fig. **8.8** according to FPGA firmware release 2.3. Inserted Chap. **11** regarding FPGA firmware upgrade.
May 12th, 2022	03	Added Chap. **Safety Notices**. Modified Tab. **2.1**. Added Sec. **3.3**, Chap. **4**, Chap. **6**. Modified Sec. **8.4.2**. Added note to Sec. **8.5.2**. Added support to Janus for Linux. Modified Chap. **16**.
Jan 25th, 2023	04	Added Chap. **12**, **13**, **14**, **15**. Modified Chap. **Safety Notices**.

Symbols, Abbreviated Terms and Notation

ADC	Analog-to-Digital Converter
ASIC	Application Specific Integrated Circuit
DAQ	Data Acquisition
DCR	Dark Count Rate
FERS	Front-End Readout System
FERS-CB	FERS Collector Board
FPGA	Field Programmable Gate Array
FSR	Full Scale Range
GEM	Gas Electron Multiplier
GUI	Graphical User Interface
HG	High Gain
HV	High Voltage
INL	Integral Non-Linearity
LG	Low Gain
LSB	Least Significant Bit

LVTTL	Low Voltage TTL
MUX	Multiplexer
OS	Operating System
PC	Personal Computer
PCB	Printed Circuit Board
PHA	Pulse Height Analysis
QD	Charge Discriminator
RF	Radio-Frequency
RMS	Root-Mean-Square
SiPM	Silicon Photo-Multiplier
TDC	Time to Digital Converter
ToA	Time of Arrival
TCP	Transmission Control Protocol
TD	Time Discriminator
ToT	Time over Threshold
USB	Universal Serial Bus
ZS	Zero Suppression

Reference Documents

[RD1] Citiroc-1A Datasheet, https://www.weeroc.com/products/sipm-read-out/citiroc-1a

[RD2] UM6377 – A7585/DT5485 User Manual

[RD3] UM7946 – Janus User Manual

[RD4] DS8147 – A525x Adapters for FERS-5200 Board Inputs

[RD5] https://www.hamamatsu.com/jp/en/product/type/S13361-3050AE-08/index.html

[RD6] SP5601 – LED Driver

[RD7] https://www.digikey.it/product-detail/it/xilinx-inc/XC7A75T-1FGG676C/XC7A75T-1FGG676C-ND/5039539

All CAEN documents can be downloaded at:
`www.caen.it/support-services/documentation-area`

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Limitation of Responsibility

If the warnings contained in this manual are not followed, CAEN will not be responsible for damage caused by improper use of the device. The manufacturer declines all responsibility for damage resulting from failure to comply with the instructions for use of the product. The equipment must be used as described in the user manual, with particular regard to the intended use, using only accessories as specified by the manufacturer. No modification or repair can be performed.

Disclaimer

The information contained herein has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies. CAEN SpA reserves the right to modify its products specifications without giving any notice; for up to date information please visit www.caen.it.

Made in Italy

We remark that all our boards have been designed and assembled in Italy. In a challenging environment where a competitive edge is often obtained at the cost of lower wages and declining working conditions, we proudly acknowledge that all those who participated in the production and distribution process of our devices were reasonably paid and worked in a safe environment (while this is true for the boards marked ”MADE IN ITALY”, we cannot guarantee for third-party manufactures).

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Safety Notices

N.B. Read carefully the "Precautions for Handling, Storage and Installation document provided with the product before starting any operation.

The following HAZARD SYMBOLS may be reported on the unit:

	Caution, refer to product manual
	Caution, risk of electrical shock
	Protective conductor terminal
	Earth (Ground) Terminal
	Alternating Current
	Three-Phase Alternating Current

The following symbol may be reported in the present manual:

	General warning statement

The symbol could be accompanied by the following terms:

- **DANGER**: indicates a hazardous situation which, if not avoided, will result in serious injury or death.
- **WARNING**: indicates a hazardous situation which, if not avoided, could result in death or serious injury.
- **CAUTION**: indicates a situation or condition which, if not avoided, could cause physical injury or damage the product and / or the surrounding environment.

THIS DEVICE MUST NOT BE USED BY UNTRAINED PERSONNEL

CAUTION: Do Not Operate Without a Proper Shielding, and Without Covers (DT5202 only). See Chap. **12**.

THE A5202 BOARD COMES WITHOUT ENCLOSURE. THE FINAL USER MUST CONSIDER APPROPRIATE SHIELDING TO AVOID ANY ELECTRICAL SHOCK OR FIRE HAZARD.

TO AVOID ELECTRIC SHOCK OR FIRE HAZARD, DO NOT OPERATE THE DT5202 WITHOUT A PROPER SHIELDING

CAUTION: Do Not Operate in Wet/Damp Conditions

TO AVOID ELECTRIC SHOCK, DO NOT OPERATE THIS PRODUCT IN WET OR DAMP CONDITIONS

CAUTION: Do Not Operate in an Explosive Atmosphere

TO AVOID INJURY OR FIRE HAZARD, DO NOT OPERATE THIS PRODUCT IN AN EXPLOSIVE ATMOSPHERE

CAUTION: Avoid Potential Hazards

USE THE PRODUCT ONLY AS SPECIFIED.
SERVICE PROCEDURES CAN BE PERFORMED BY QUALIFIED PERSONNEL ONLY

Please, contact the Techincal Support in case Service Procedures are required.

DO NOT OPERATE WITH SUSPECTED FAILURES.
IF YOU SUSPECT THIS PRODUCT TO BE DAMAGED, PLEASE CONTACT THE TECHNICAL SUPPORT

See Chap. **16** for the Technical Support contacts.

IT IS UNDER THE RESPONSIBILITY OF THE CUSTOMER AN IMPROPER USE OF THE PRODUCT

1 Introduction

FERS-5200 is a front-end readout system designed for the readout of large detector arrays, such as SiPMs, multi-anode PMTs, Silicon Strip detectors, Wire Chambers, GEMs, Gas Tubes and others. FERS-5200 is a distributed and scalable system, where each unit is a small card that houses 64 or 128 channels with preamplifier, shaper, discriminator, ADC, trigger logic, synchronization, local memory and readout interface. In most cases, the front-end is based on ASIC chips that allow for high density, cost effective integration of multi-channel readout electronics into small size and low power consumption.

The first FERS-5200 unit being developed is the A5202 (DT5202 is the boxed version for desktop use) that uses the Citiroc-1A chip **[RD1]** produced by WeeROC for SiPM readout. More precisely, the A5202 is a small board ($\sim 7 \times 17$ cm^2) housing two Citiroc-1A chips for a total of 64 readout channels. Each readout channel is composed of a Preamplifier, a Slow Shaper with peak sensing detector, and a Fast Shaper followed by a discriminator. Peak sensing values from each Citiroc-1A are converted sequentially (multiplexed output) by an ADC. The 64 channel self-triggers (discriminator outputs) can be used for counting, time stamping, to determine the Time over Threshold (ToT) information, and also to generate the board bunch trigger that starts the A/D conversion. The A5202/DT5202 board is also provided with the A7585D power supply module for biasing the SiPMs **[RD2]** and the interfaces for readout, synchronization, and control.

The most relevant A5202/DT5202 acquisition modes are:

- **Spectroscopy Mode**: This mode (also indicated as Pulse Height Analysis, PHA) works with a global (bunch) trigger, either coming from an external source or generated by a combination of the channel self-triggers. As soon as a trigger is issued, all channels start simultaneously the A/D conversion of the pulse amplitude and create a data packet containing the common trigger time stamp followed by the individual energies. The packet is saved into the local memory buffer of the FERS-5200 unit, waiting for the readout, while a new cycle can start. In Spectroscopy Mode, the A/D conversion causes a systematic dead time and limits the maximum trigger rate. In particular, the dead time due to conversion with Citiroc-1A is about 10 µs.
- **Counting Mode**: In this mode, the self-triggers of each channel are individually counted. The counting intervals (the same for all channels) are defined by an internal periodic gate with programmable width or by an external signal. At the end of each counting interval, the counters are latched and saved in a data packet, while the counting continues in the next interval without any dead time. The maximum counting rate for the Citiroc-1A is 20 Mcps.
- **Timing Mode**: This mode generates a list of individual time stamps, optionally combined with the Time over Threshold (ToT) that gives a rough estimation of the pulse amplitude (energy). The channels run independently and are allowed to push an event (time stamp of the self-triggers and ToT) to a data packet. The timing resolution of both time stamp and ToT is 0.5 ns LSB ($\approx$ 250 ps RMS). When the data packet reaches the programmed size, it becomes available for the readout and the acquisition continues in a new packet. There is not any intrinsic dead time, even though a high input rate might produce huge amounts of data that saturates the readout bandwidth with consequent data loss.
- **Spectroscopy and Timing Mode**: both the PHA and timing information are available for each bunch trigger.

One A5202/DT5202 unit can be used stand alone, without any additional hardware, just connected to the PC via USB 2.0 or Ethernet 10/100T.

For large readout systems, a flexible and scalable network of units can be created by means of the high speed optical link called TDlink (**COMING SOON**) that allows up to 16 FERS-5200 units to be connected in daisy chain (ring) providing data readout, synchronization between the units and broadcasting of commands (e.g. triggers, time resets, etc.). The DT5215 (**COMING SOON**) is a data collector board (FERS-CB) housing 8 TDlink masters that will make it possible to manage up to 128 FERS-5200 units.

The A5202/DT5202 is fully supported by the CAEN Janus software on Windows®and Linux®**[RD3]**.

In Tab. **1.1**, the list of accessories and related products of the A5202/DT5202 boards are listed below.

Adapters	Description
A5250	2.54 mm pin header adapter for FERS-5200
A5251	MPPC header adapter for A5202/DT5202
A5253	3-pin header adapter for FERS-5200
Cables	**Description**
A5261	SiPM remotization cable for A5253 - 70 cm
A5260	Remotization cable for FERS-5200 boards - 50 cm
A5260B	Remotization cable for FERS-5200 boards - 100 cm
Kits	**Description**
A5253 Kit	A5253 adapter and 64 SiPM remotization cables

Tab. 1.1: CAEN accessories for A5202/DT5202 board.

2 Technical Specifications

INPUTS	64 channels (= 2 Citiroc-1A chips)
SIGNAL POLARITY	Positive
SENSITIVITY	Dual range: Low Gain (LG)/High Gain (HG). Channel-by-channel individual setting of the gain value through a CSP feedback capacitor, C_f, adjustable from 25 fF to 1575 fF (25 fF step): - LG = 1.5 pF/C_f (max gain = 60 v/v) - HG = 10 $\times$ LG = 15 pF/C_f (max gain = 600 v/v) Refer to Sec. **9.2.1** for more details.
DYNAMIC RANGE	The Citiroc-1A preamplifiers ensure a dynamic range from 160 fC to 400 pC (i.e. from 1 to 2500 photo-electrons with 10^6 SiPM gain) **[RD1]**. Refer to Sec. **9.2.1** for more details.
SHAPING TIME	**Slow Shaper** 7 options from 12.5 ns to 87.5 ns (12.5 ns step) **Fast Shaper** Fixed: 15 ns
SELF-TRIGGERS	- Programmable 10-bit DAC for common threshold - Minimum threshold: 1/3 photo-electron - Separate trigger line per channel - Programmable 4-bit DAC for channel-by-channel threshold fine adjustment - Logic combination (AND, OR, Majority) of triggers for start of A/D conversion and time reference. More details are reported in Sec. **8.3**.
EXTERNAL TRIGGER	From TDlink, T1-IN or T0-IN. T0/T1 lines can be daisy chained (IN-OUT) or wired-OR (bidirectional) to share a common global trigger between multiple units. More details in Sec. **8.4.5** and Sec. **8.4.6** respectively.
ACQUISITION MODES	**Spectroscopy Mode (PHA)** - Simultaneous acquisition of all channels - 13-bit A/D conversion - Systematic conversion time $\sim$ 10 µs $\rightarrow$ Max. trigger rate $\sim$ 100 kHz - Independent digital thresholds for channel-by-channel zero suppression (ZS) **Counting Mode** - Channel-by-channel independent counting - Common trigger to define counting window (Dwell time) - Maximum counting rate (per channel): $\sim$ 20 Mcps **Timing Mode** - Independent channels (merged list, time sorted) - 0.5 ns LSB resolution ($\sim$ 250 ps RMS) - Time stamp referred to a common time reference coming from T0-IN/T1-IN connectors or from the logic combination of channel self-triggers - Spectroscopy information (lower resolution) from Time over Threshold (ToT) information **Spectroscopy and Timing Mode** - Simultaneous acquisition of all channels - 13-bit A/D conversion - Systematic conversion time $\sim$ 10 µs $\rightarrow$ Max. trigger rate $\sim$ 100 kHz - Independent digital thresholds for channel-by-channel zero suppression (ZS) - 0.5 ns LSB resolution ($\sim$ 250 ps RMS) - Time stamp referred to a common time reference coming from T0-IN/T1-IN connectors or from the logic combination of channel self-triggers - Spectroscopy information (lower resolution) from Time over Threshold (ToT) information
TRIGGER TIME STAMP	- 56-bit counter, 8 ns step - Up to 128 boards can be synchronized with the DT5215 FERS-CB by sending a time stamp reset signal via TDlink (COMING SOON)

FRONT PANEL I/0s	4 general purpose programmable LEMO I/Os connectors available: - 2 (T0-IN and T1-IN) to be used as input (LVTTL and NIM) - 2 (T0-OUT and T1-OUT) to be used as output (LVTTL) The description of the available functions of each connector is reported in Sec. **8.4**. The T1-IN and T0-IN connectors are 50 Ω terminated with a jumper. The jumper can be moved to perform a bridged connection for daisy chain trigger distribution or wired-OR in a multi-board system (Sec. **8.4.4**).	
DIGITAL PROBE	LVTTL signal with different functions (see Sec. **8.4.3**) can be transmitted via the front panel output connectors.	
ANALOG PROBE	MCX connectors (A5202)/ SMA connectors (DT5202) allowing the user to acquire analog signals from a specific, software selectable stage of each Citiroc-1A signal shaping chain: - LG/HG Preamplifier output - LG/HG Slow Shaper output - Fast Shaper output	
HIGH VOLTAGE POWER SUPPLY	Single channel PCB mounted A7585D High Voltage Power Supply: - Common SiPM bias voltage: 20 ÷ 85 V - Settling precision: ± 20 mV - Individual channel adjustment: 8-bit (2.5V or 4.5V dynamic range) - Max. output bias current: 10 mA [1](software programmable limit) - Programmable temperature compensation	
COMMUNICATION INTERFACES	**USB** USB2.0 connector, type microUSB-B **TDlink** Optical link (4.25 Gbit/s) with synch distribution. Allows for multi-board synchronization, slow control and data readout (**COMING SOON**)	**Ethernet** Ethernet connector, type RJ-45. Supports 10/100 Mbit/s connection to a PC
FIRMWARE	Firmware can be upgraded via USB or Ethernet	
SOFTWARE	Fully controlled by the Janus software on Windows®and Linux®	
MECHANICAL	**Dimensions** 74.0 W × 22.0 H × 174.5 L mm^3 (A5202) 106.1 W × 56.1 H × 186.8 L mm^3 (DT5202 including A5250 pins)	**Weight** 132 g 503 g
ENVIRONMENTAL	**Environment**: Indoor use **Operating Temperature**: 0°C to +40°C [2] **Storage Temperature**: –10°C to +60°C **Operating Humidity**: 10% to 90% RH non condensing **Storage Humidity**: 5% to 90% RH non condensing **Altitude**: < 2000m **Pollution Degree**: 2 **Overvoltage Category**: II **EMC Environment**: Commercial and light industrial **IP Degree**: IPX0 Enclosure, not for wet location	
REGULATORY COMPLIANCE	**EMC** CE 2014/30/EU Electromagnetic compatibility Directive	**Safety** CE 2014/35/EU Low Voltage Directive
POWER REQUIREMENTS	Single power supply (+12 V). Regularly working in a range between +7 V and +15 V	
POWER CONSUMPTIONS	750 mA @ +12 V, i.e. ≈ 9 W (acquisition on, all channels enabled, HV on, 64 SiPMs mounted) 685 mA @ +12 V, i.e. ≈ 8.2 W (acquisition off, all channels enabled, HV off, no SiPMs mounted)	

Tab. 2.1: Specification table.

[1] Simoultaneously applying Voltage > 60 V and current > 2 mA could be dangerous for the user. Do not touch the A5202 board and take tare of the proper shielding.

[2] In case of A5202, for T ≥ +25°C, or in case the board is placed in an enclosed environment - like a box without air flow, the user must use an extenal fan unit to cool down the board temperature.

3 Packaging and Compliancy

3.1 A5202

The A5202 is avaiable as an electronic board without covers, with metal spacers that make possible to put multiple A5202 on top of each other (module dimensions: 74.0 W $\times$ 22.0 H $\times$ 174.5 L mm^3). The A5202 is mostly intended to be integraded into more complex systems.

The device is inspected by CAEN before the shipment, and it is guaranteed to leave the factory free of mechanical or electrical defects.

The content of the delivered package standardly consists of the part list shown in the table below **Tab. 3.1**.

	Part	Description	Qt
	A5202	64 Channel Citiroc unit for FERS-5200	x1
	Power supply connector	691361300002 WURTH Connector for DC Input	x1
	Ethernet cable	2MTCat6 S-FTP Ethernet Cable	x1
	USB cable	USB 2.0 cable type A to microUSB-B	x1
	Documentation	UM7945 - A5202/DT5202 User Manual	-

Tab. 3.1: Delivered kit content

WARNING: A5202 is an ESD sensitive item. Handling without ESD protective covering shall be performed only into approved ESD Protected Area (EPAs).

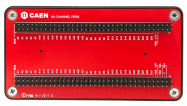
WARNING: A5202 complies with the EMC directive only if installed in a CE marked system.

3.2 DT5202

The DT5202 is avaiable as a Desktop module housed in an aluminum case and two external stand up rubber frames, one on the front and one on the rear panel (module dimensions: 106.1 W $\times$ 56.1 H $\times$ 186.8 L mm^3 including A5250 pins).

The device is inspected by CAEN before the shipment, and it is guaranteed to leave the factory free of mechanical or electrical defects.

The content of the delivered package standardly consists of the part list shown in the table below **Tab. 3.2**.

	Part	Description	Qt
	DT5202	64 Channel Citiroc unit for FERS-5200	x1
	A5250	A5250 FERS-5200 Header Adapter (already mounted)	x1
	DC Input Adapter	DC Input Adapter	x1
	AC-DC Adapter	45W 12V Single Output AC-DC Adapter	x1
	Power Supply Cable	Power Supply Cable	x1
	Ethernet cable	2MTCat6 S-FTP Ethernet Cable	x1
	USB cable	USB 2.0 cable type A to microUSB-B	x1

	Documentation	UM7945 - A5202/DT5202 User Manual	-

Tab. 3.2: Delivered kit content

3.3 Unpackaging Instructions

CAUTION: to manage the product, consult the operating instructions provided.

When receiving the unit, the user is strictly recommended to:

- Inspect containers for damage during shipment. Report any damage to the freight carrier for possible insurance claims.
- Check that all the components received match those listed on the enclosed packing list as in **Tab. 3.1** and **3.2**. (CAEN cannot accept responsibility for missing items unless any discrepancy is promptly notified.)
- Open shipping containers; be careful not to damage contents.
- Inspect contents and report any damage. The inspection should confirm that there is no exterior damage to the unit such as broken knobs or connectors and that the front panel is not scratched or cracked. Keep all packing material until the inspection has been completed.
- If damage is detected, file a claim with carrier immediately and notify CAEN service (see Chap. **16**).
- If equipment must be returned, carefully repack equipment in the original shipping container with original packing materials, if possible. Please contact CAEN service.
- If equipment is not installed when unpacked, place equipment in original shipping container and store in a safe place until ready to install.

DO NOT SUBJECT THE ITEM TO UNDUE SHOCK OF VIBRATIONS

DO NOT BUMP, DROP OR SLIDE SHIPPING CONTAINERS

DO NOT LEAVE ITEMS OR SHIPPING CONTAINERS UNSUPERVISED IN AREAS WHERE UNTRAINED PERSONNEL MAY MISHANDLE THE ITEMS

USE ONLY ACCESSORIES WHICH MEET THE MANUFACTURER SPECIFICATIONS

For a correct and safe use of the module, refer to Chap. **5** and **6**.

4 PID (Product Identifier)

PID is the CAEN product identifier, an incremental number greater than 10000 that is unique for each product[1]. The PID is on a label affixed to the product (Fig. **4.1**, **4.2**, and **4.3**).

Note: The serial number is still valid to identify older boards, where the PID label is not present.

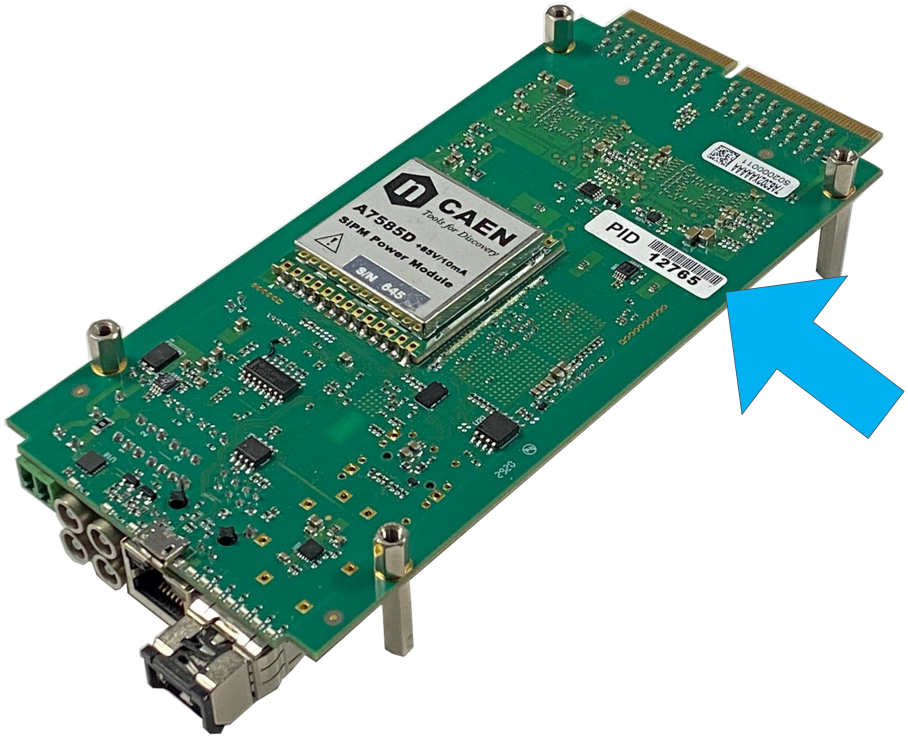


Fig. 4.1: PID location on A5202 (the number in the picture is purely indicative)

[1]The PID substitutes the serial number previously identifying the boards.

Fig. 4.2: PID location on DT5202 (the number in the picture is purely indicative)

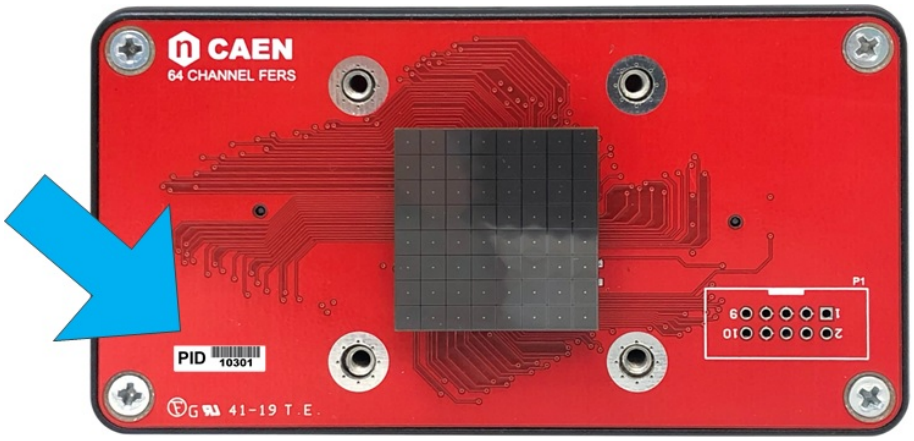


Fig. 4.3: PID location on DT5251 adapter (the number in the picture is purely indicative)

5 Power Requirements

The CAEN A5202 and DT5202 standalone modules are powered by an external 220 V-12 V AC/DC stabilized power supply. The AC/DC power supply is provided with the DT5202 board and included in the delivered kit, together with an adapter cable to easily connect the power supply jack to the DT5202 (see Fig. **5.1**). Only a DC connector is provided in the A5202 kit.

WARNING: Operating voltage ranges from 7 V to 15 V.

Fig. 5.1: AC/DC power supply adapter (left) and the jack cable provided with the DT5202 module (right).

In Fig. **5.2**, the datasheet of the AC/DC stabilized power supply included in the DT5202 kit is shown.

THE CORRECT FUNCTIONING AND SAFETY OF THE MODULE ARE NOT GUARANTEED IF POWER REQUIREMENTS SPECIFICATIONS ARE NOT FOLLOWED

Switchbox FRA030/045/050 Series

30-50W SINGLE OUTPUT AC/DC DESKTOP ADAPTOR

Features

- Universal input
- IEC320 receptacle 2P or 3P
- Optional output connector
- OVP, OCP, OPP, auto recovery
- CEC compliance

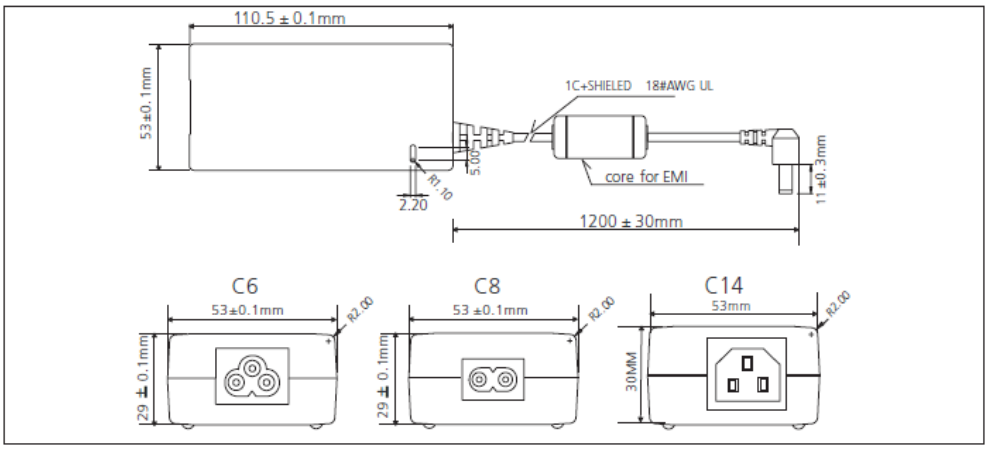
Specifications

INPUT	
Voltage range	100-240VAC.
Inrush current	40A at 115VAC / 80A at 230VAC max.
Dielectric withstand	Input/output 3,000VDC.
OUTPUT	
Output voltage	5-48V.
Ripple and noise	2% p-p max.
Load regulation	±5% max.
No load stand by power	<0.5W @ 230VAC.
Efficiency	>=85% for CEC requirement.
Hold up time	10mS at nominal line.
Protections	OCP, OVP, over power & short circuit.
GENERAL	
Std output connector	Dc barrel jack.
Std output cable/length	UL1185, #18AWG / 5 ft.
ENVIRONMENTAL	
Operating temperature	0°C to +40°C.
Storage temperature	–20°C to +85°C.
STANDARDS	
Safety standards	IEC/UL/EN60950-1, CE, CB.
EMC	EN55022 (CISPR 22) class B, FCC class B.

MODEL NUMBER	OUTPUT VOLTAGE	OUTPUT CURRENT	MAX WATTS	CEC*
FRA030-S05-X	5–7 V	6.00–4.30 A	30 W	
FRA045-S09-X	7–9 V	6.00–5.00 A	45 W	IV
FRA045-S12-X	12–15 V	3.75–3.00 A	45 W	IV
FRA045-S15-X	15–18 V	3.00–2.50 A	45 W	IV
FRA045-S24-X	18–24 V	2.50–1.88 A	45 W	IV
FRA050-S12-X	12–15 V	4.17–3.33 A	50 W	IV
FRA050-S15-X	15–18 V	3.33–2.87 A	50 W	IV
FRA050-S24-X	18–24 V	2.78–2.08 A	50 W	IV
FRA050-S36-X	30–36 V	1.67–1.38 A	50 W	IV
FRA050-S48-X	40–48 V	1.25–1.04 A	50 W	IV

*CEC compliance model provide under customer's request.
*CEC compliance model standby power (⊗ no load) <0.5W.

Note:
X = Inlet type code
X = 4, IEC320 C14 X = 6, IEC320 C6 X = 8, IEC320 C8



powerbox
www.powerbox.info
20081029

Fig. 5.2: AC/DC power supply provided with the DT5202 module.

6 Cooling Management

Starting from revision 2.3 of the FPGA firmware, the A5202 and DT5202 boards also manage the optical communication via the TDLink. This results in higher power consumption and higher FPGA temperature than previous firmware revisions. The user is thus suggested to monitor the FPGA temeperature (e.g. via the proper monitor in the Janus software **[RD3]**) and be sure that it does not exceed the 85 °C in order to prevent damages to the FPGA itself.

WARNING: The on-board FPGA operates correctly up to a temperature of 85 °C. The user must keep the temperature of the FPGA below this limit (e.g. by using a suitable ventilation system).

The User must take care to provide a proper cooling to the A5202 board with external fan if the board is used in an enclosure, or if the board is installed in a setup with poor air flow, or if the environmental temperature exceeds 25 °C.
Excessive temperature will, in first instance, reduce the performance and the quality of the measurements and can also damage the board.

If the board is stored in cold environment, please check for water condensation before power on.

The board has not been tested for radiation hardness. High energy particles can be source of errors and can damage the FPGA. If used in strong proton or neutron beams, arrange proper shielding, or remote the sensors with a custom cable.

EXTERNAL FANS MUST BE USED WITH THE A5202 BOARD WHEN ENVIRONMENTAL TEMPERATURE EXCEEDS 25 °C, OR WHEN THE BOARD IS PLACED IN AN ENCLOSED ENVIRONMENT - LIKE A BOX WITHOUT AIR FLOW. OVERHEATING MAY DAMAGE THE MODULE AND DEGRADE THE PERFORMANCES.

6.1 Cleaning Air Vents

CAEN recommends to occasionally clean the air vents on all vented sides of the board or crate, if present. Lint, dust, and other foreign matter can block the vents and limit the airflow. Be sure to power off the board and disconnect it from the power by physically detach the power chord before cleaning the air vents and follow the general cleaning safety precautions.

IT IS UNDER THE RESPONSIBILITY OF THE CUSTOMER A NON-COMPLIANT USE OF THE PRODUCT

7 Panels Description

7.1 A5202 Views

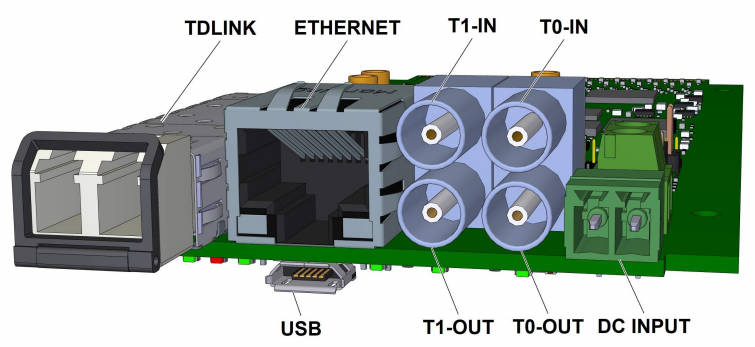


Fig. 7.1: A5202 front panel view.

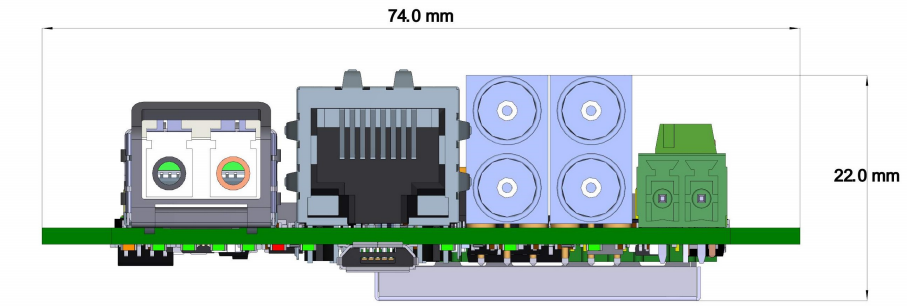


Fig. 7.2: A5202 front panel view with spatial dimensions.

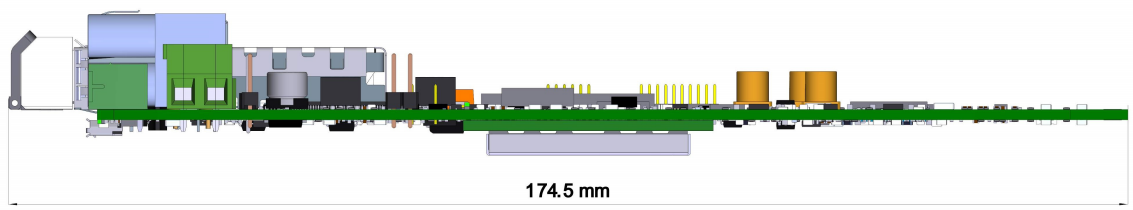


Fig. 7.3: A5202 lateral view with spatial dimensions.

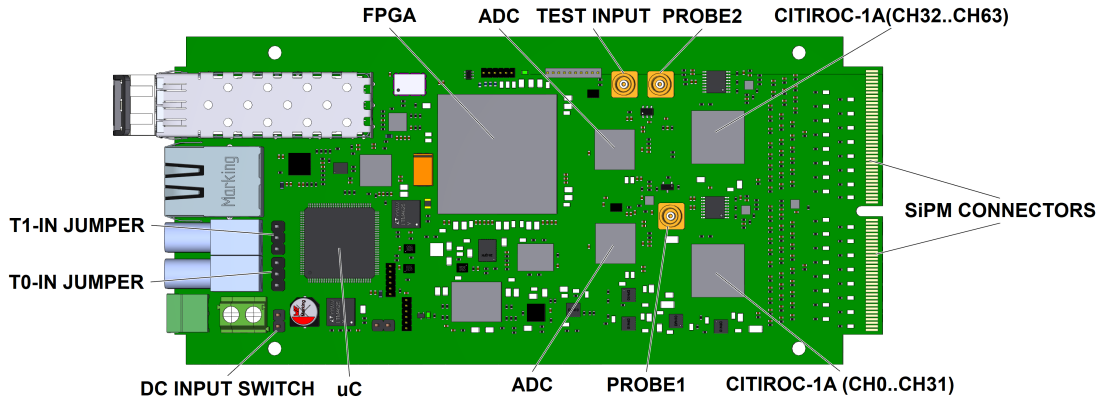


Fig. 7.4: A5202 top view.

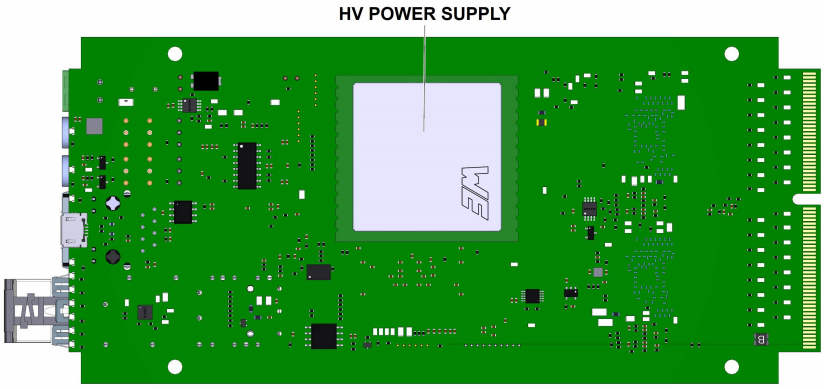


Fig. 7.5: A5202 bottom view.

7.2 DT5202 Views

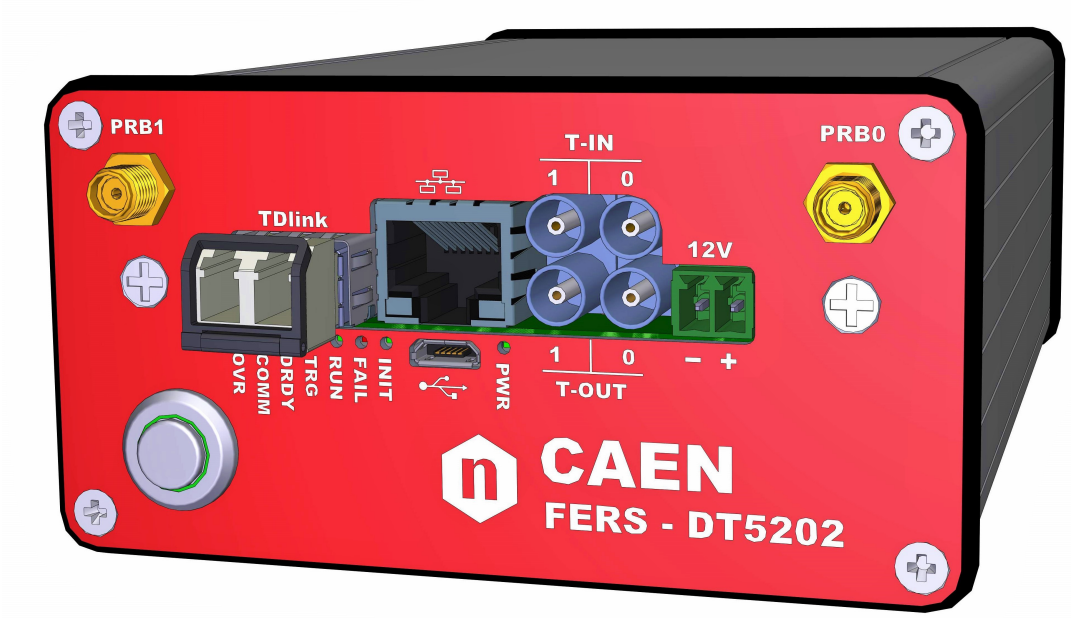


Fig. 7.6: DT5202 front panel view.

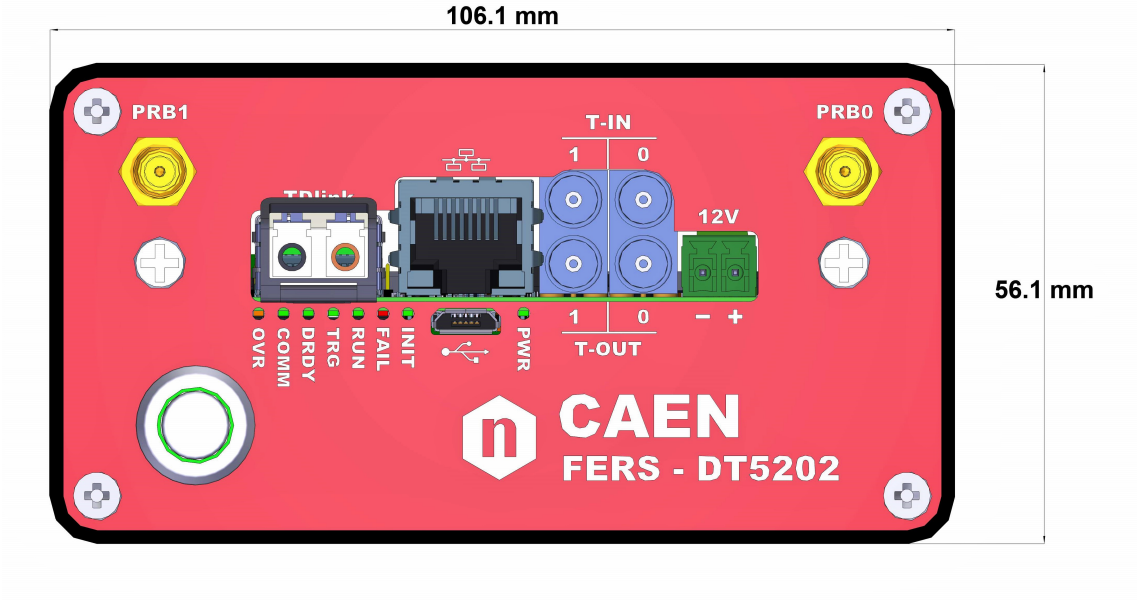


Fig. 7.7: DT5202 front panel view with spatial dimensions.

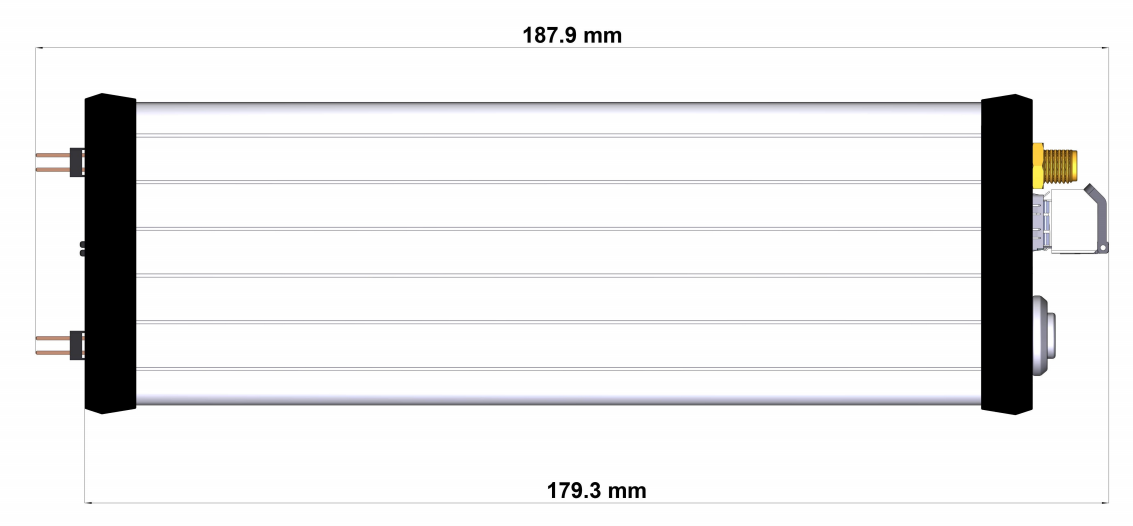


Fig. 7.8: DT5202 lateral view with spatial dimensions.

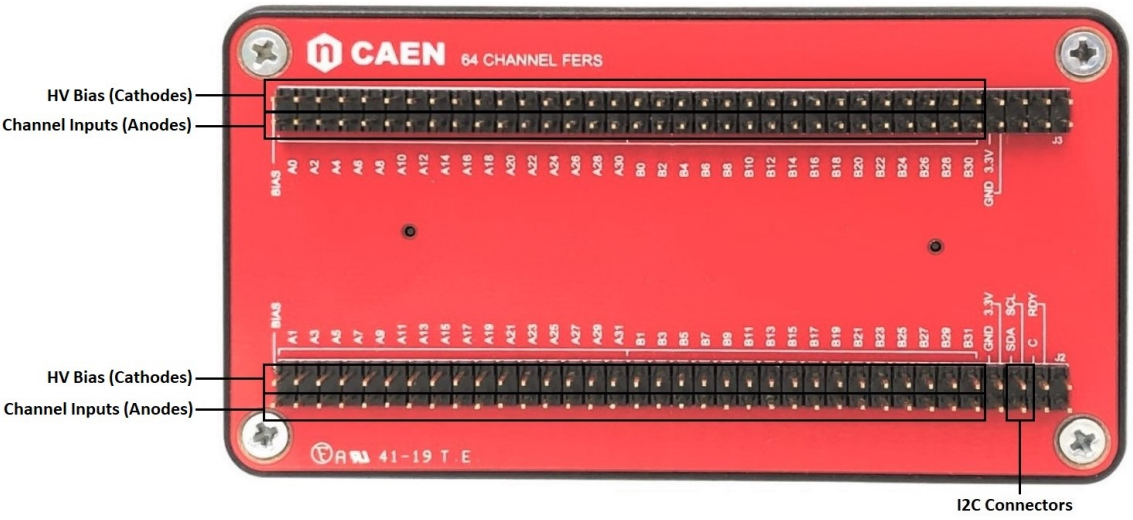
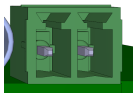
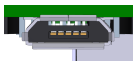
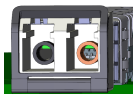


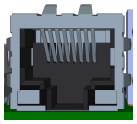
Fig. 7.9: DT5202 back panel view (A5250 adapter mounted).

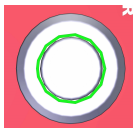
7.3 Panel Views

DC INPUT		
	**FUNCTION** Input connector for DC input mating to a 691361300002 WURTH ELEKTRONIK connector (already inserted in the DC input in the A5202 kit). **ELECTRICAL SPECS** Typ. Input voltage: +12 V DC.	**MECHANICAL SPECS** Manufacturer: WURTH ELEKTRONIK. Internal number: 691322310002.

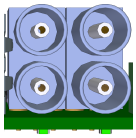
USB PORT		
	**FUNCTION** USB 2.0 connector for A5202 configuration and data readout. **ELECTRICAL SPECS** N.A.	**MECHANICAL SPECS** Series: USB connectors. Connector type: Micro USB, type B, reverse. Manufacturer: TE connectivity. Internal number: 1932788-1.

TDLINK		
	**FUNCTION** Optical link connector for data readout and flow control in multiboard configuration. Daisy chainable. Compliant with optical fibers 50/125 µm OM2 and OM3 (back-compliant with 62.5/125 µm OM1) cable featuring LC connectors on both sides. **ELECTRICAL SPECS** N.A.	**MECHANICAL SPECS** Series: SFF Transceivers. Type: FTLF8519F-2KNL (LC connectors). Manufacturer: FINISAR

ETHERNET PORT		
	**FUNCTION** Ethernet connector for A5202/DT5202 configuration and data readout. **ELECTRICAL SPECS** N.A.	**MECHANICAL SPECS** RJ45 female connector.

POWER ON BUTTON (DT5202)		
	**FUNCTION** Button allowing the user to power on/off the DT5202 board. **ELECTRICAL SPECS** N.A.	**MECHANICAL SPECS** N.A.

DIGITAL I/Os



FUNCTION
Digital software programmable input/output connectors. From left to right, from top to bottom (see Fig. **7.1**): T1-IN, T0-IN, T1-OUT, T0-OUT.

MECHANICAL SPECS
Series: 101 A 004 connectors.
Type: DLP 101 A 004-28.
Manufacturer: FISCHER.
Alternatively:
Type: EPL 00 250 NTN.
Manufacturer: LEMO.

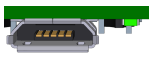
ELECTRICAL SPECS
Signal level: LVTTL/NIM (input), LVTTL (output).
The two outputs require 50 Ω termination.

DIAGNOSTIC LEDs

From left to right:

- **OVR (ORANGE)**: Indicates that a trigger arrived while the board was in a busy condition (Spectroscopy mode) and thus the A/D conversion could not be started. In Counting and Timing mode the LED indicates that the data could not be transmitted because of a full condition of the buffer.
- **COMM (GREEN)**: Indicates there is activity on the USB, TDLink or Ethernet channel.
- **DRDY (GREEN)**: Indicates the event/data is present in the Output Buffer.
- **TRG (GREEN)**: Indicates the trigger is accepted.
- **RUN (GREEN)**: Indicates the acquisition is running (data taking).
- **FAIL (RED)**: Indicates an FPGA over-temperature condition or that the FPGA firmware was not correctly loaded.
- **INIT (GREEN)**: Indicates that the connection between the board and the software is established when using an USB or an Ethernet connection.

POWER ON LED



PWR (GREEN): The led turns on as soon as the power supply is connected to the DC input connector.

7.4 Analog Probes and Test Inputs

ANALOG PROBEs (A5202)

FUNCTION
MCX connectors (top panel) to readout analog signals from Citiroc-1A amplification stages (Preamplifier, Slow Shaper, Fast Shaper).
Probe1: Channels from 0 to 31.
Probe2: Channels from 32 to 63.

MECHANICAL SPECS
Series: MCX connectors.
Type: SMT PCB jack (female), straight, 5.08.
Manufacturer: WURTH ELEKTRONIK.
Suggested plug/male: MCX-50-2-16.
Suggested cable: RG174 type.

ELECTRICAL SPECS
Input impedance (Z_{in}): 50 Ω.

ANALOG PROBEs (DT5202)		
	**FUNCTION** SMA connectors to readout analog signals from Citiroc-1A amplification stages (Preamplifier, Slow Shaper, Fast Shaper). **PRB0**: Channels from 0 to 31. **PRB1**: Channels from 32 to 63. **ELECTRICAL SPECS** Input impedance (Z_{in}): 50 Ω.	**MECHANICAL SPECS** Series: SMA connectors. Type: SMA PCB jack (female). Manufacturer: MOLEX. Suggested cable: RG174 type.

TEST INPUT (A5202)		
	**FUNCTION** MCX test input connector (top panel) for the Citiroc-1A Preamplifiers: charge injection capacitor = 3pF. See Sec. **8.1.4** for more details. **ELECTRICAL SPECS** Input impedance (Z_{in}): 50 Ω. Dynamic range: 2.5 V_{pp}.	**MECHANICAL SPECS** Series: MCX connectors. Type: SMT PCB jack (female), straight, 5.08. Manufacturer: WURTH ELEKTRONIK. Suggested plug/male: MCX-50-2-16. Suggested cable: RG174 type.

7.5 SiPM Connectors

The A5202/DT5202 has an input edge card connectors type HSEC8-170, mating to a Samtec HSEC8-170-01-S-DV. The A5202/DT5202 connector has 140 contacts (0.8 mm pitch) and brings 64 couples (SiPM anodes and cathodes), the temperature sensor and several grounds. The A5202/DT5202 edge connector pin out is presented in Fig. **7.10** and Fig. **7.11**.

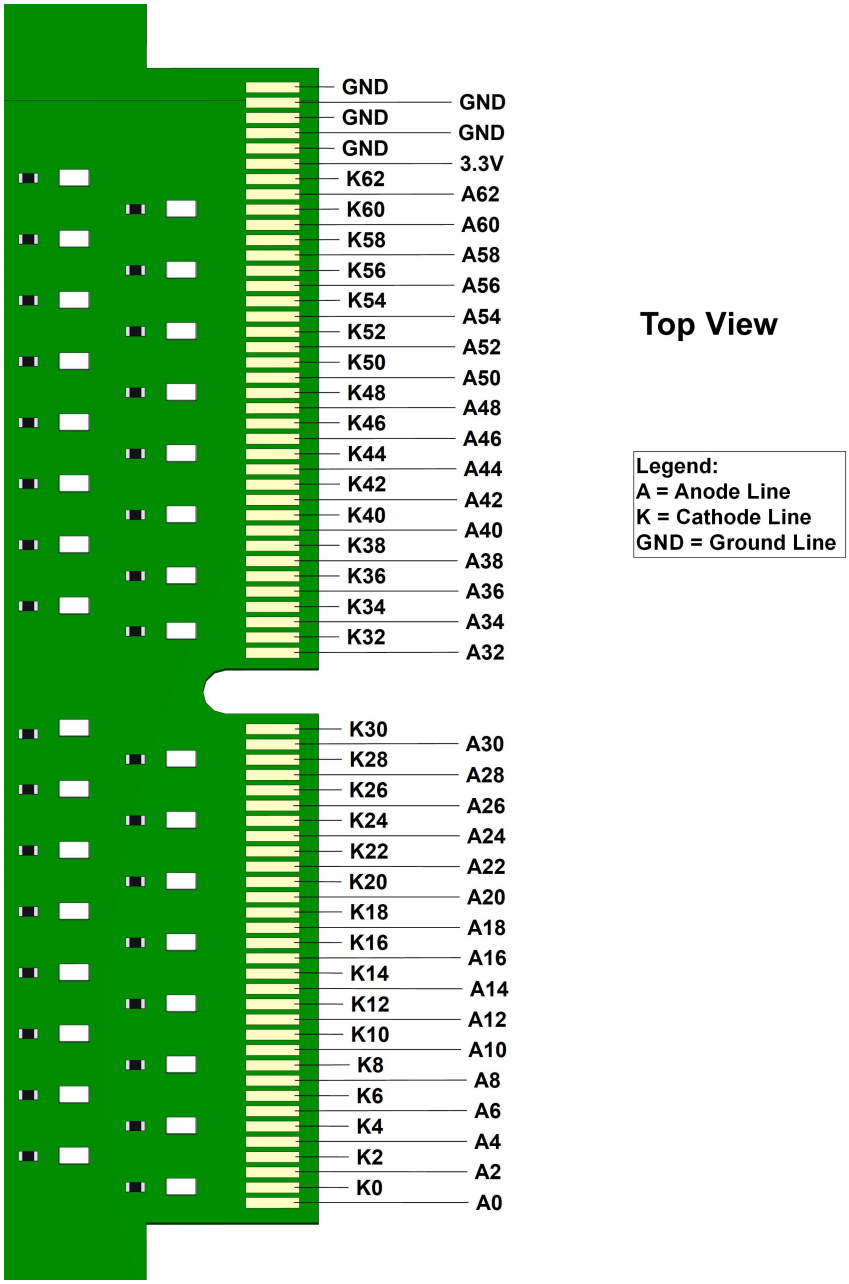


Fig. 7.10: Input edge connectors pin-out (A5202 top view).

Apart from the anode, cathode and ground lines:

- **I2C SCL** indicates the Serial Clock pin of the I^2C slave bus.
- **I2C SDA** indicates the Serial Data pin of the I^2C slave bus.

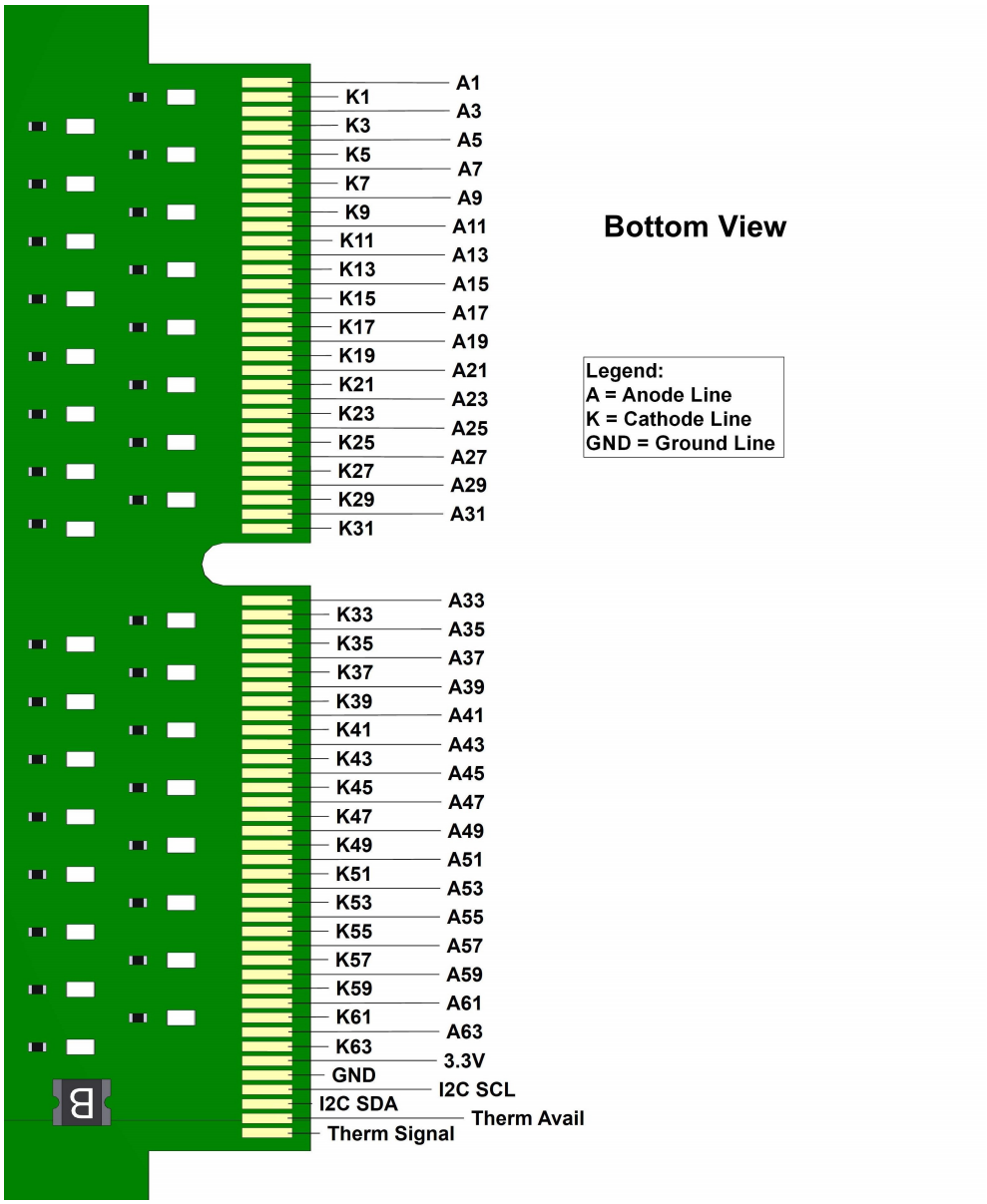


Fig. 7.11: Input edge connector pin-out (A5202 bottom view).

- **Therm Avail** indicates the pin that allows to signal the presence of a temperature sensor to the A7585D power supply module. When the pin is disconnected, the temperature measurement and compensation is enabled in the A7585D HV module.
- **Therm Signal** indicates the pin to transmit the signal proportional to the detector temperature (if a temperature sensor is connected) to the A7585D power supply module.

In Tab. **7.1**, the pin numbering scheme and correspondence with the various lines is presented.

Pin N.	Signal	Pin N.	Signal	Pin N.	Signal	Pin N.	Signal
1	A0	36	K17	71	K34	106	A53
2	A1	37	A18	72	K35	107	K52
3	K0	38	A19	73	A36	108	K53
4	K1	39	K18	74	A37	109	A54
5	A2	40	K19	75	K36	110	A55
6	A3	41	A20	76	K37	111	K54
7	K2	42	A21	77	A38	112	K55
8	K3	43	K20	78	A39	113	A56
9	A4	44	K21	79	K38	114	A57
10	A5	45	A22	80	K39	115	K56
11	K4	46	A23	81	A40	116	K57
12	K5	47	K22	82	A41	117	A58
13	A6	48	K23	83	K40	118	A59
14	A7	49	A24	84	K41	119	K58
15	K6	50	A25	85	A42	120	K59
16	K7	51	K24	86	A43	121	A60
17	A8	52	K25	87	K42	122	A61
18	A9	53	A26	88	K43	123	K60
19	K8	54	A27	89	A44	124	K61
20	K9	55	K26	90	A45	125	A62
21	A10	56	K27	91	K44	126	A63
22	A11	57	A28	92	K45	127	K62
23	K10	58	A29	93	A46	128	K63
24	K11	59	K28	94	A47	129	3.3 V
25	A12	60	K29	95	K46	130	3.3 V
26	A13	61	A30	96	K47	131	GND
27	K12	62	A31	97	A48	132	GND
28	K13	63	K30	98	A49	133	GND
29	A14	64	K31	99	K48	134	I2C SDL
30	A15	65	A32	100	K49	135	GND
31	K14	66	A33	101	A50	136	I2C SCA
32	K15	67	K32	102	A51	137	GND
33	A16	68	K33	103	K50	138	Therm Avail
34	A17	69	A34	104	K51	139	GND
35	K16	70	A35	105	A52	140	Therm Signal

Tab. 7.1: Pin number-electrical line correspondence table.

Note: The A5202/DT5202 is designed to provide positive bias voltage to the SiPMs. In this standard configuration, suitable for a wide range of SiPM matrices, the A7585D feeds the SiPMs with positive high voltage: the anodes of SiPMs have to be independently connected to the Citiroc-1A input lines (see Fig. **7.12**), while cathodes have to be connected to the bias voltage line.

Note: The Citiroc-1A chip only accepts positive input signals.

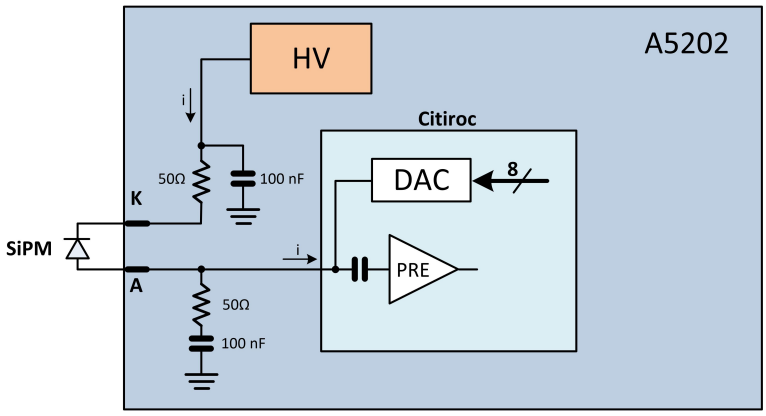


Fig. 7.12: SiPM connection scheme for the A5202/DT5202 board.

The edge connector makes it possible to build a backplane or a flange that houses the SiPMs on one side and the housing for the A5202 on the other side. A schematic representation of possible A5202 backplane connections is presented in Fig. **7.13**.

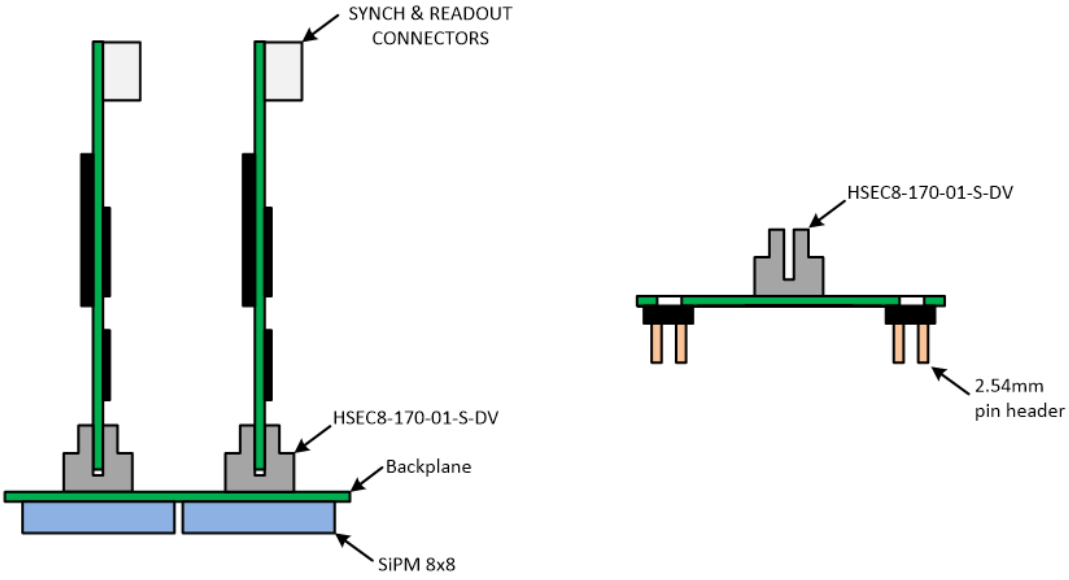


Fig. 7.13: Schematic representation of an example of detector backplane and pin adapter (A5250 header adapter on the right).

CAEN provides (only in the DT5202 kit) the A5250 header adapter to connect the HSEC8-170 edge connector to standard 2.54 mm pin headers (see Fig. **7.9**). The A5250 is already mounted on the back panel of the DT5202. The user can thus easily mount through-holes headers on the adapter PCB to connect anode/cathode lines.

The complete description of the A5202/DT5202 channel input adapters is provided in the FERS-5200 adapter data sheet **[RD4]**.

8 Functional Description

In the following chapter, operation principles and functional descriptions of the A5202/DT5202 module are treated in detail. The block diagram of the board is presented in Fig. **8.1**.

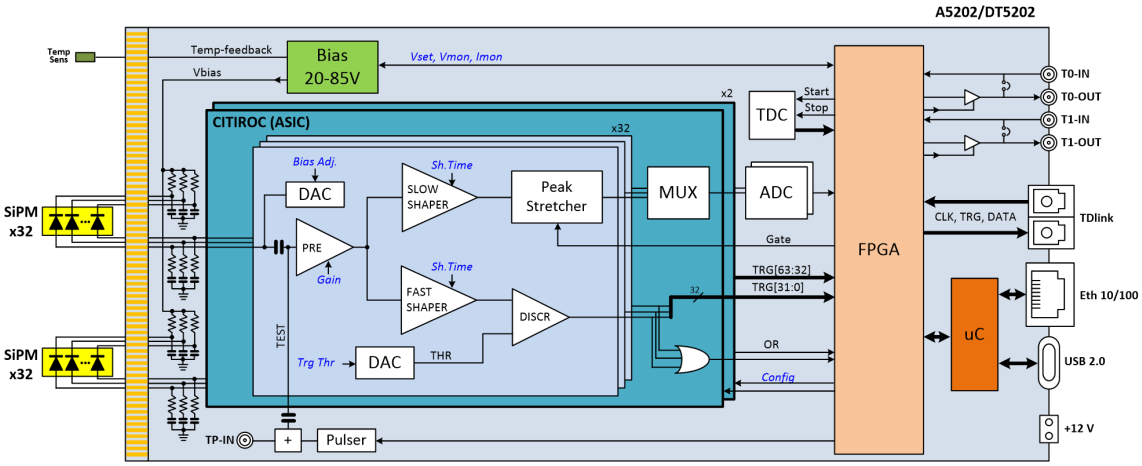


Fig. 8.1: Simplified block diagram of the A5202/DT5202 FERS-5200 unit.

The core of the A5202/DT5202 board are the 2 Citiroc-1A ASIC chips **[RD1]**. Citiroc-1A is a 32-channel front-end ASIC designed to readout SiPMs for scientific instrumentation application. The ASIC chip allows the user to trigger down to 1/3 photo-electron and provides the charge measurement with a good noise rejection and 1% linearity up to 2500 photo-electrons.
Citiroc-1A outputs the 32-channel triggers with a high timing resolution (better than 100 ps RMS), even though it does not have an internal TAC/TDC to acquire the timing measurement. However, the FPGA of the A5202 is programmed for this purpose and a low resolution TDC (0.5 ns) was implemented to calculate the time distance (ΔT) between a reference signal and the input pulses. For future applications, an additional TDC with 50 ps LSB is available to give a better timing information providing the ΔT measurement between a logic combination of the self-triggers and an asynchronous signal coming from T0-IN or T1-IN connector (typically a reference timing signal or the global acquisition trigger).

The A5202 embeds a programmable high voltage power supply (20 ÷ 85 V, 10 mA) for the bias of the SiPMs, featuring a feedback loop with the temperature sensor (internal or external) for the compensation of the gain drift. An individual adjustment of the high-voltage is possible using a DAC (internal to each channel) connected to the ASIC inputs, which gives the correction for the non-uniformity of SiPMs.

SIMOULTANEOUSLY APPLYING VOLTAGE > 60 V AND CURRENT > 2 mA COULD BE DANGEROUS FOR THE USER. DO NOT TOUCH THE A5202 BOARD AND TAKE CARE OF THE PROPER SHIELDING

8.1 Citiroc-1A

The A5202/DT5202 is based on the functions and readout chains of the Citiroc-1A ASIC. A scheme of the chip is shown in Fig. **8.2**

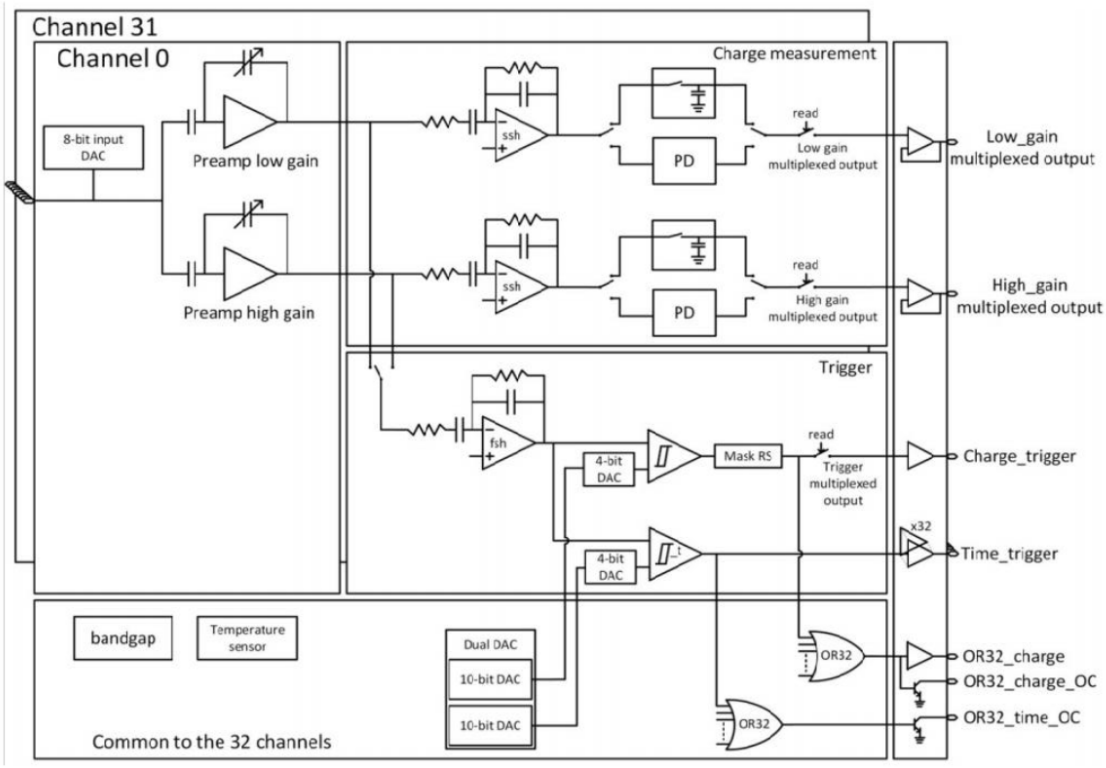


Fig. 8.2: Citiroc-1A block scheme.

Each of the 32 readout channels available in the chip integrates a classical readout chain made of Preamplifier (one for Low Gain and one for High Gain), Fast and Slow Shaper, a trigger line with a timing resolution better than 100 ps, a Peak Detector circuit and analog output MUX. Moreover, for each channel, a block for the SiPM bias regulation is available.

8.1.1 SiPM Gain Trimming

The A5202/DT5202 embeds a programmable high voltage power supply (A7585D) for the bias of the SiPMs. Moreover, each of the 32 Citiroc-1A inputs features a low power 4.5 V/2.5 V-range software programmable 8-bit DAC to finely adjust the SiPMs individual high voltage in order to correct for gain and noise non-uniformities of systems using several SiPMs.

Note: The value set for the voltage provided by the DAC (V_{DAC}) is subtracted to the common value of the HV:

$$V_{SiPM} = HV - V_{DAC}$$

WARNING: The Citiroc-1A DAC can only operate as a current sink. It is therefore not possible to measure the DAC voltage by placing a multimeter between the channel pin (anode connector) and ground. Indeed, this procedure could damage the chip. The user willing to perform such measurement has to follow the instructions reported in Sec. 9.1.1.

8.1.2 Charge Measurement

Each channel of Citiroc-1A embeds two channel-by-channel independent programmable variable-gain Preamplifiers ensuring a wide coverage of the dynamic range (see Fig. **8.3**). Both LG and HG Preamplifiers can be tuned according to the values of the feedback capacitance C_f, which can range from 25 fF to 1575 fF with a step of 25 fF (6 bits). Indeed, the voltage gain is given by the ratio C_{in}/C_f, with C_{in} = 15 pF for the HG amplification chain and 1.5 pF for the LG one.

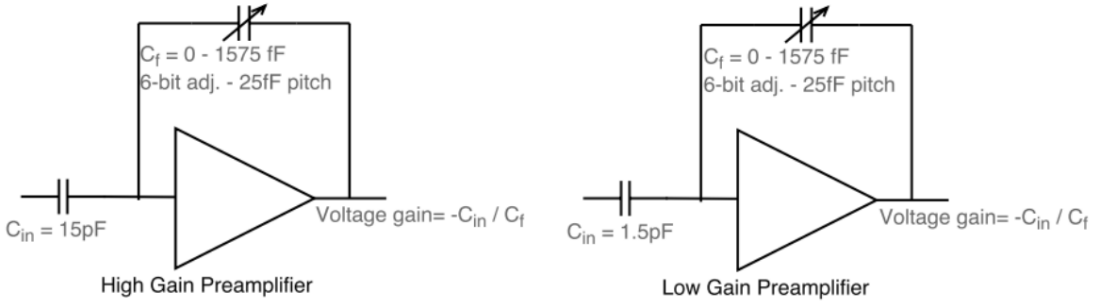


Fig. 8.3: High Gain and Low Gain voltage sensitive Preamplifiers.

The amplification chain is then composed of two CR-RC^2 Slow Shapers that are respectively connected on the two Preamplifier outputs for each channel (see Fig. **8.4**). The shaping time of each Slow Shaper can be tuned from 12.5 ns to 87.5 ns with a 12.5 ns pitch. The shaping time is common to all the 32 channels, even though it can be different between LG Slow Shaper and HG Slow Shaper.

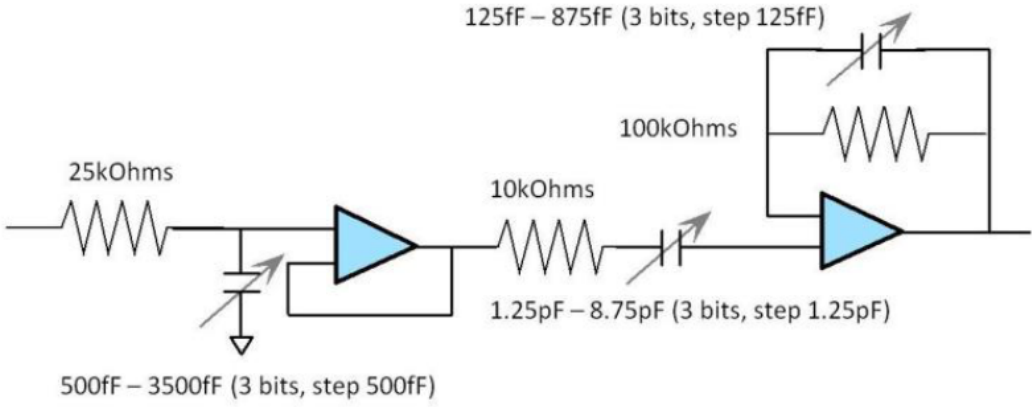


Fig. 8.4: Slow Shaper schematic.

The amplitude of the signal from the Slow Shaper output is measured with a peak sensing system, called

Peak Detector, that automatically stores the highest value of the Slow Shaper after being armed.
The Peak Detector allows the user to get the maximum of the peaks for each channel even if those peaks are not precisely defined in time, for example if incident photons come with a delay from channel to channel.

Note: The charge measurement of Citiroc-1A in the A5202/DT5202 works with a bunch (global) trigger, either external or generated by a combination of channel individual triggers (see Sec. **8.5.1**). As soon as a trigger is issued, all channels start the peak sampling.

The peak detector acquisition sequence works in 3 phases (see also Fig. **8.5**):

1. **OFF Phase**: before any trigger, the peak detector is turned off. Upon trigger, the peak detector switches to Peak Sensing Phase.
2. **Peak Sensing Phase**: in this mode, the peak detector memorizes the maximum of the input signal. That mode is kept until the internal logic provides a rising edge on the Hold signal, as it is shown in Fig. **8.5**, the Peak Detector switches to Hold Phase when that signal occurs.
   The time distance between the trigger and the Hold signal is defined by the Hold Delay (see Sec. **9.2.2**) parameter (programmable).
3. **Hold Phase**: The rising edge of the Hold signal causes the disconnection of the input of the Peak Detector from the Slow Shaper and ensures that no other input signal is memorized. That phase is used during the serial read-out of the ASIC. The falling edge of the Hold signal will cause the release of the Hold Phase and the Peak Detector will switch back to the OFF Phase for the next acquisition.

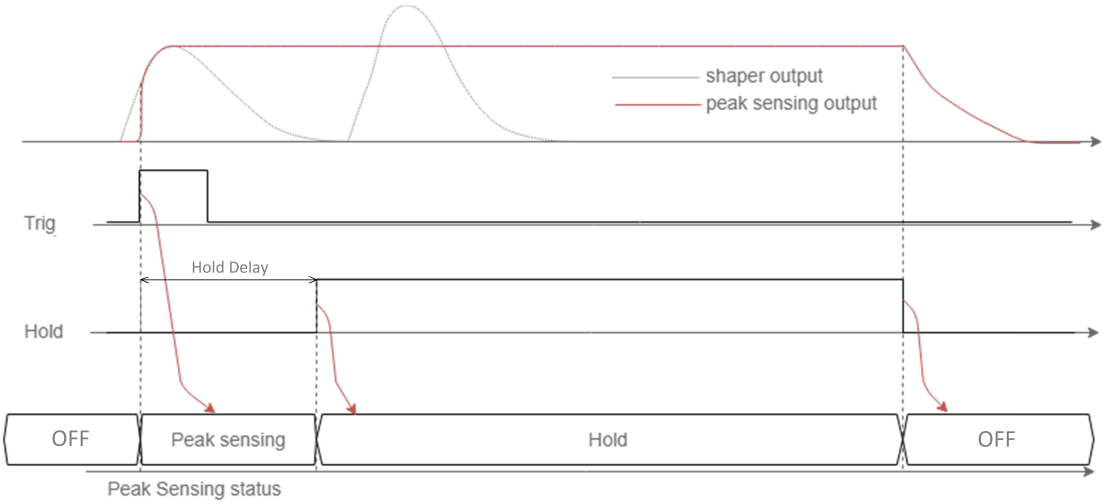


Fig. 8.5: Peak detector chronogram.

A proper setting of the **Hold Delay** parameter is *fundamental* in order to acquire a correct value for the peak amplitude of the pulse (see Sec. **9.2.2** for a detailed study on the argument). Indeed, if the trigger arrives too late (beyond the peaking time of the Slow Shaper), the Peak Sensing Detector stores a lower value of the signal. The peaking time of the Slow Shaper depends on the shaping time set but is typically less than 100 ns, so the trigger latency must be small. If, however, the trigger arrives significantly earlier, then it is important to set a Hold Delay value high enough so as not to risk stopping the Peak Sensing Phase when the signal has not yet reached the peak.
To understand how to properly set the Hold Delay parameter, two ways are viable:

- Look at the oscilloscope the Trigger, Hold (via the Digital Probe, see Sec. **8.4.3**) and Slow Shaper (via the Analog Probe) signals and measure the time distance between the Trigger signal and the Slow Shaper peak.
- Perform an Hold Delay Scan (see Sec. **10.7.2**).

ASICs like Citiroc-1A have not an integrated ADC, they just perform a peak detection operation on each channel. The two analog charge measurements (one from the LG amplification chain and one from the HG amplification chain) from each channel are sent out (via FPGA command) in parallel. The charge measurements from each channel (32 for each Citiroc-1A chip) are then sequentially multiplexed on a single analog output (see Sec. **8.5.1** and Sec. **9.2.4** and **[RD1]** for more details).

8.1.3 Discriminators

Citiroc-1A is an analog ASIC and there is no auto-trigger capability with it. The trigger going out of Citiroc-1A can eventually be sent to a DAQ system where a decision to convert the event in digital or not can be taken (otherwise a trigger external to the Citiroc-1A can be used). The Citiroc-1A trigger chain can be connected either to the LG or to the HG Preamplifier depending on the requested level of trigger (see Fig. **8.2**). The trigger chain is then composed of a 15 ns peaking-time Fast Shaper (see Fig. **8.6**) which directly receives the signal from one of the two Preamplifiers for each channel.

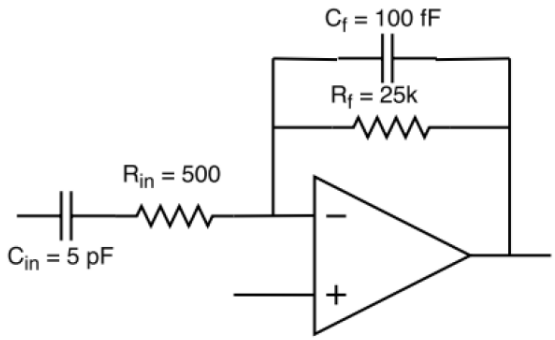


Fig. 8.6: Fast Shaper circuit scheme.

The output of the Fast Shaper is fed into two discriminators:

- The **Charge Discriminator** (QD) which provides an ASIC level trigger which is the logic OR of the enabled channels (Q-OR). The Q-OR signal toggles at the first QD trigger. Every time an A/D conversion sequence is started, the logic status (high or low) of the QD trigger of each channel is also transmitted and saved to the data packet, thus allowing the user to determine which channels triggered in the QD line.
- The **Time Discriminator** (TD), which provides accurate event time information on each channel. The 32 discriminator outputs are available on 32 digital outputs connected to the FPGA. The 64 lines (32 + 32) are then used for:
  1. Photon counting (see Sec. **8.5.2**).
  2. The acquisition of Time of Arrival (ToA) and Time over Threshold (ToT) information (see Sec. **8.5.3**).
  3. The generation of a bunch trigger signal from a logic combination (AND, OR, Majority) of the channel self-triggers (see Sec. **8.5.1** and the TLogic signal description in Sec. **8.3**).

Note: The channel self-trigger (either from the QD or the TD line) stays high as long as the Fast Shaper signal for that channel is over threshold. Indeed, the channel self-trigger duration (from the TD line) is used to determine the Time over Threshold (ToT) information when working in Timing Mode (see Sec. **8.5.3**).

More details on the trigger chain of the Citiroc-1A can be found on **[RD1]**.

The QD and TD thresholds are common for the 32 channels and are set by two 10-bit DACs. A 4-bit DAC on each discriminator allows adjusting each of the 2×32 thresholds individually to compensate for non-uniformities.

Note: When using the external trigger, the user is recommended to set a high value of the TD Threshold, to avoid noise from the TD lines, which remain active.

8.1.4 Test Pulser

A test input is included for each channel of Citiroc-1A chip and can be enabled for test purpose. A block diagram of the test input is presented in Fig. **8.7**.

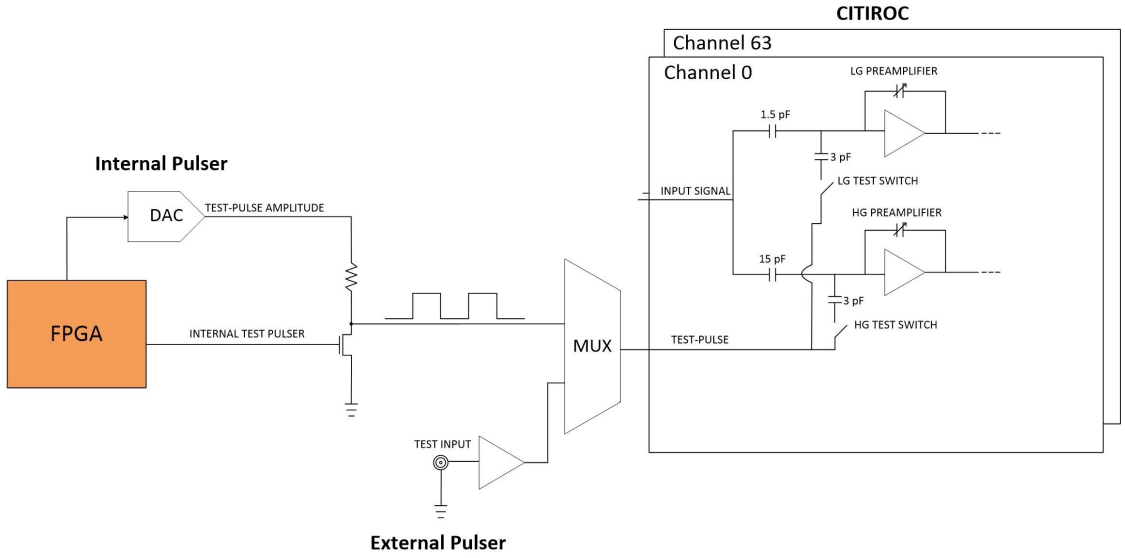


Fig. 8.7: Test Pulse signal block diagram.

The pulser can be:

- **Internal**. The A5202/DT5202 FPGA drives an internal test pulser whose amplitude is programmable via DAC. The internal test pulser can also be driven by an external signal fed into T0-IN, T1-IN connectors (see Sec. **8.4.1**).
- **External**. The Test Input MCX connector (see Fig. **7.4**) allows the user to propagate an external analog signal.

Note: A 1:5 attenuator is present between the Test Input MCX connector of the A5202 board and the Citiroc-1A test input.

The injection test capacitance value is 3 pF for both test pulsers (either internal or external). As it is shown in Fig. **8.7**, there is no difference between the LG and HG stage when using the test pulse, since the two input capacitors (1.5 pF and 15 pF respectively for LG and HG Preamplifier) are by-passed.
The user can select to which channels the test pulse should be transmitted at the same time. Moreover, the test pulse can be transmitted to the LG Preamplifier, to the HG Preamplifier or to both.

Note: WeeROC suggests to connect the test pulse to one channel at a time **[RD1]**.

Note: If using the internal pulser, the user has to keep the MCX bushing disconnected.

8.2 FPGA Block Diagram

After a description of the main functionalities of the Citiroc-1A chip, in Fig. **8.8** the FPGA schematic representation is presented.

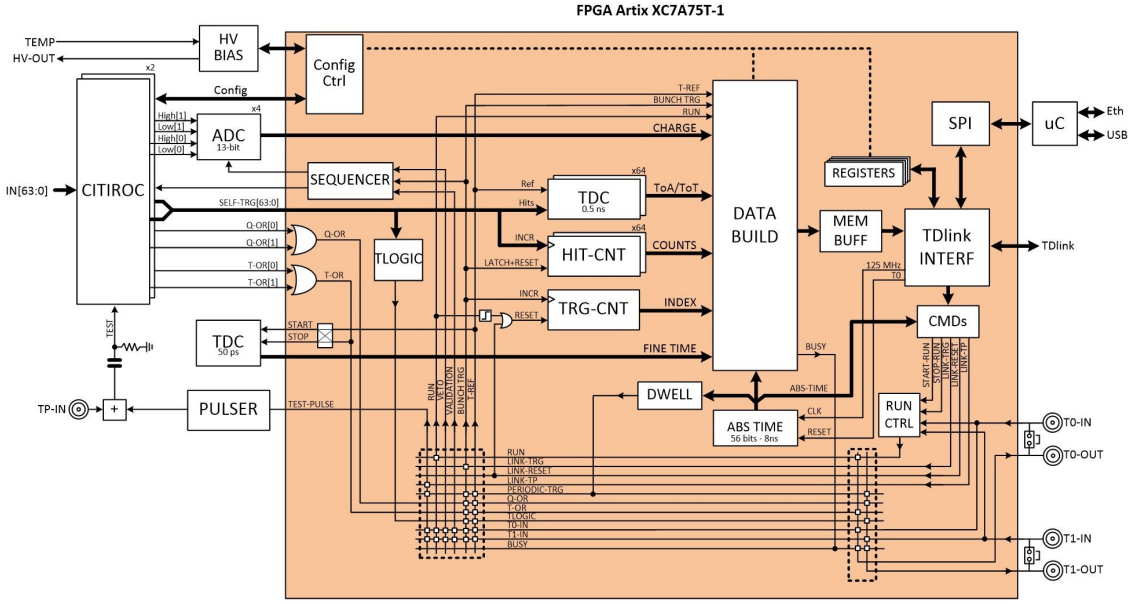


Fig. 8.8: FPGA block diagram.

8.3 Control Signals

In this section, a list of the main control signals available for the A5202/DT5202 board is presented, together with a brief explanation of their application:

- **Bunch Trigger**. A bunch (i.e. global) trigger signal directed to all channels (64) of the board. The Bunch Trigger is used for two purposes:
  1. To start the Peak Sensing Phase (see Sec. **8.1.2**) and the subsequent A/D conversion sequence when working in Spectroscopy Mode (see Sec. **8.5.1**).
  2. To define, when working in Counting Mode (see Sec. **8.5.2**) the time at which the channel counters are read (all 64 simultaneously), saved in memory and then reset to zero.
- **Time Reference**. In Timing Mode, the time reference (T_{ref}) signal opens/closes an acquisition window of programmable size and only the hits belonging to that time window are saved in the data packet. The Time of Arrival (ToA) information is then computed as the time difference between the T_{ref} signal and the individual hits. The Time over Threshold (ToT) of these individual hits, giving a rough estimation of their energy, is also saved.
- **Periodic Trigger**. The A5202/DT5202 board can generate a periodic trigger whose period is written as a 32-bit word. The available values for the period thus ranges from 16 ns, i.e. 2 clock cycles, to $\approx$ 34 s, i.e. (2^{32}-1) $\times$ 8 ns.
- **TLogic**. A logic signal generated by the combination of the channel self-triggers from the TD line. As explained in Sec. **8.1.3**, each channel can generate a TD self-trigger signal when the pulse from the Fast Shaper crosses a configurable threshold. The self-triggers of each channel are then processed at firmware level in order to create a TLogic trigger signal. The self-triggers coming from different channels can be masked, so that the user can define which channels participate to the logic definition. The logic functions associated to the TLogic signal (see Fig. **8.9**) are:

- *OR64*: The logic OR of the 64 channel TD outputs (i.e. self-triggers). With respect to the T-OR signal, which is directly sent out by the Citiroc-1A chip, the OR64 logic signal is created at firmware level. For this reason, the signal is much slower than the T-OR but, unlike this one, the OR64 can be masked.
- *AND2_OR32*: Triggers of consecutive channels are sent to a logic AND operator (e.g. CH0&CH1, CH2&CH3, etc.). The 32 outputs are then sent to an OR logic operator.
- *OR32_AND2*: Triggers of each Citiroc-1A (32 channels each) are sent to an OR logic operator. The 2 output signals (one for each Citiroc-1A) are then sent to a logic AND operator.
- *MAJ64*: The logic signal is the majority of the 64 channels, i.e. it goes to an high logic level when a minimum number of channels, determined by a "Majority Level" parameter (see Janus User Manual **[RD3]**), is associated to over threhsold signals.
- *MAJ32_AND2*: Two majority logic functions are performed separately on the TD triggers from the two Citiroc-1As. The two outputs are sent to a logic AND operator.

The TLogic signal can be used as a bunch trigger that starts the Peak Sensing Phase (see Sec. **8.1.2**) when working in Spectroscopy Mode (see Sec. **8.5.1**), or as a time reference that opens the acquisition window when working in Timing Mode (see Sec **8.5.3**).

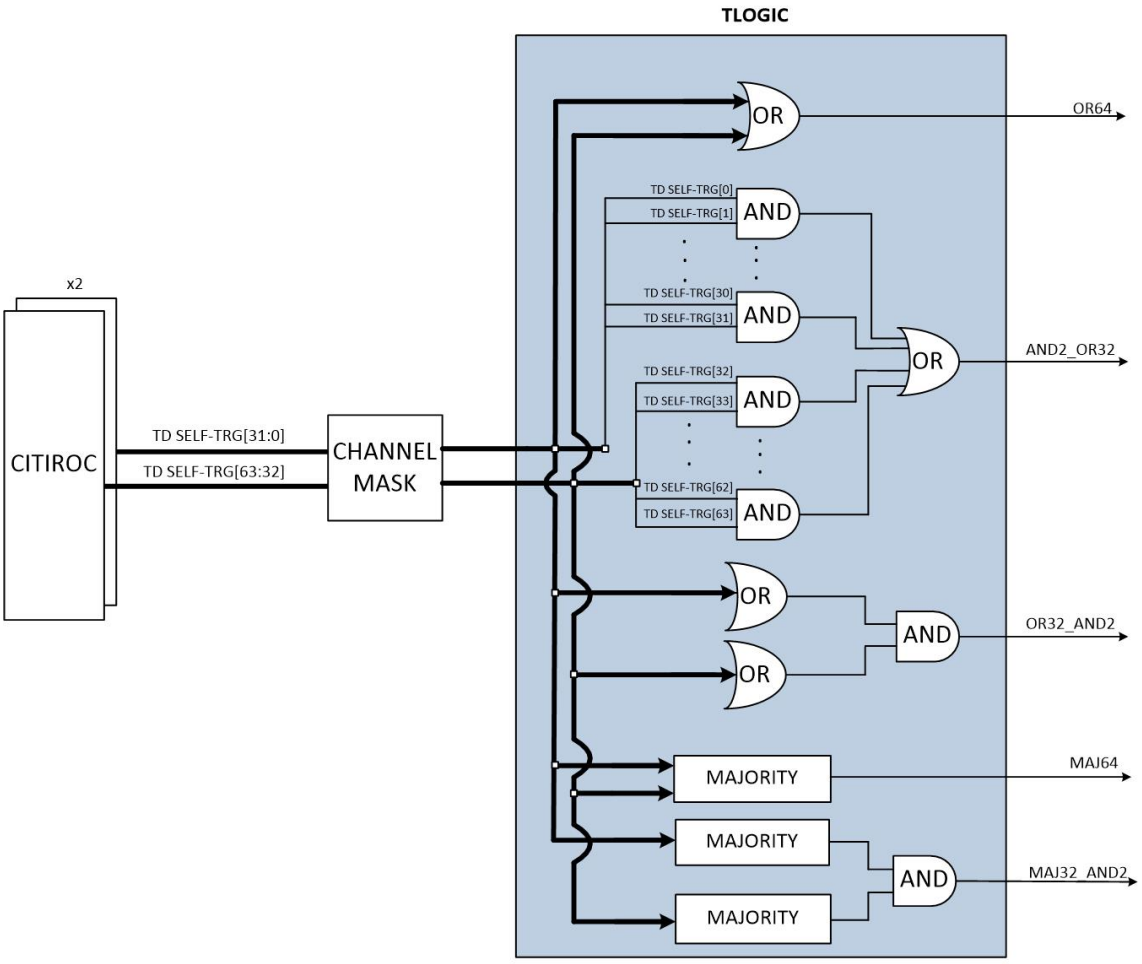


Fig. 8.9: TLOGIC signal block diagram.

- **Validation Signal**. When working in Spectroscopy Mode (see Sec. **8.5.1**), the Validation Signal allows to accept/reject a bunch trigger signal (defining the start of the A/D signal conversion). The validation signal, in order to be effective, must arrive in the time interval between the arrival of the bunch trigger and T_v, being T_v approximately the sum of 120 ns and the value set for the Hold Delay parameter (see

Sec. **8.1.2**). The user can precisely visualize the validation window at the oscilloscope by selecting the appropriate option for the Digital Probe (see Sec. **8.4.3**).
The user can decide at software level to use or not a validation signal when working in Spectroscopy Mode.

- **Veto Signal**. The Veto signal, as long as it is associated with a high logic level, inhibits all bunch trigger signals.
- **Test Pulse**. A test signal directed to the Preamplifier stage (see Sec. **8.1.4**) of a Citiroc-1A selectable channel (or to a programmable mask of channels).
- **Busy**. The busy signal can have a different behavior depending on the particular A5202/DT5202 board acquisition mode:
  - *Spectroscopy Mode*. The busy signal goes high as soon as the bunch trigger is asserted and remains high until the A/D conversion is finished. If a trigger occurs while the busy signal is high, the trigger ID is counted (and saved) but the energy information is lost (the A/D conversion sequence is not started). The logic signal goes high also when the memory buffer is filled.
  - *Counting Mode*. The trigger signal does not cause the busy signal to go to an high logic level (it only defines the time when the counters are latched and read). Instead, it goes high when the buffer memory is filled.
  - *Timing Mode*. Since each channel is independent in this operating mode, the busy signal goes high when the memory buffer of at least one channel is full.

8.4 Front Panel I/Os

The A5202/DT5202 board is provided with 4 general purpose programmable LEMO I/Os connectors (see Fig. **7.1** and **7.6**): two of them to be used as input and two of them to be used as output connectors. The description of the available functions of each connector is presented in this section.

8.4.1 Input Connectors

The two LEMO input connectors of the A5202/DT5202 board accept LVTTL/NIM signals whose function is programmable. The two connectors can be programmed independently in order to perform different functions:

- **T0-IN**:
  - *Bunch Trigger Source*. See Sec. **8.3**.
  - *External Time Reference*. See Sec. **8.3**.
  - *Test Input*. The input logic signal goes to the A5202/DT5202 internal pulser which in turn sends a programmable amplitude signal to the Citiroc-1A test input.
  - *Acquisition Start*. The input signal is used to start an acquisition (see "Start Run Mode" parameter inside Janus User Manual **[RD3]**).
  - *Validation Source*. When working in Spectroscopy Mode (PHA), the user can send a validation signal allowing to accept/reject a bunch trigger (see Sec. **8.3**).
  - *Veto Source*. When working in Spectroscopy Mode (PHA), the veto signal inhibits all bunch trigger signals as long as it is associated with an high logic level (see Sec. **8.3**).
- **T1-IN**:
  - *Bunch Trigger Source*. See T0-IN.
  - *External Time Reference*. See T0-IN.
  - *Test Input*. See T0-IN.
  - *Acquisition Start*. See T0-IN.
  - *Validation Source*. See T0-IN.
  - *Veto Source*. See T0-IN.

8.4.2 Output Connectors

The two LEMO output connectors of the A5202/DT5202 board allows the user to transmit programmable LVTTL signals. The two connectors can be programmed independently in order to perform different functions that are:

- **T0-OUT**:
  - *T0-IN*. The signal transmitted to the T0-IN connector is propagated, after having being processed by the FPGA, to the T0-OUT connector. This allows the user, when operating in multi-board configuration, to propagate the same signal to all boards, for instance.
  - *Bunch Trigger*. See Sec. **8.3**.
  - *T-OR*. The logic OR (generated inside the Citiroc-1A chip) of the channel self-triggers from the TD line of both Citiroc-1As (see Sec. **8.1.3**).
  - *TLogic*. See Sec. **8.3**.
  - *Run*. The signal goes to an high logic level as soon as a new run is started and goes down when the run ends.
  - *Periodic Trigger*. See Sec. **8.3**.
  - *Busy*. See Sec. **8.3**.
  - *Digital Probe*. Different programmable logic signals can be used as digital probes (see Sec. **8.4.3**).
  - *Square wave*. A periodic square wave having the same period of the internal periodic trigger of the board.
  - *TDL_SYNC*. Signal of synchronism from TDLink. The user can visualize the TDL_SYNC from multiple boards to check that they are all latched together.
  - *RUN_SYNC*. Signal of start run from TDLink. The user can visualize the RUN_SYNC from multiple boards to check that the starts run are all latched together.
  - *Zero*. A low logic level is transmitted (T0-OUT turned off). To be used when performing a daisy chained trigger distribution (see Sec. **8.4.5**).
- **T1-OUT**:
  - *T1-IN*. The signal transmitted to the T1-IN connector is propagated, after having being processed by the FPGA, to the T1-OUT connector. This allows the user, when operating in a multi-board configuration, to propagate the same signal to all boards for instance.
  - *Bunch Trigger*. See T0-OUT.
  - *Q-OR*. The logic OR (generated inside the Citiroc-1A chip) of the channel self-triggers from the QD line of both Citiroc-1As (see Sec. **8.1.3**).
  - *TLogic*. See T0-OUT.
  - *Run*. See T0-OUT.
  - *Periodic Trigger*. See T0-OUT.
  - *Busy*. See T0-OUT.
  - *Digital Probe*. See T0-OUT.
  - *Square wave*. See T0-OUT.
  - *TDL_SYNC*. See T0-OUT.
  - *RUN_SYNC*. See T0-OUT.
  - *Zero*. See T0-OUT.

8.4.3 Digital Probe

The digital probe, which can be transmitted via the A5202/DT5202 front panel output connectors (see Sec. **7.3**), is programmable by the user and can be one of the following LVTTL signals:

- *Peaking Time LG/HG*. The digital signal defining the peaking time of the LG/HG Slow Shaper amplifier (see Sec. **8.1.2**).

- *Hold Signal*. The Hold signal (see Sec. **8.1.2**).
- *Start of A/D Conversion*. The digital signal defining the start of the A/D conversion of the pulse height values (see Sec. **8.1.2**).
- *Data Commit*. The signal that commands a data packet to be sent to the readout interface.
- *Data Validation*.
- *Clock Signal*. The FPGA internal clock signal.
- *Validation Window*. It defines the validation window within which the validation signal (see Sec. **8.3**) must arrive in order to accept/reject a bunch trigger.

8.4.4 Bridged Connection

The T0-IN and T1-IN connectors are, by default, 50 Ω terminated via jumpers. A schematic overview of the default configuration of the TX-IN connectors (with X being 0 or 1) is presented in Fig. **8.10**.

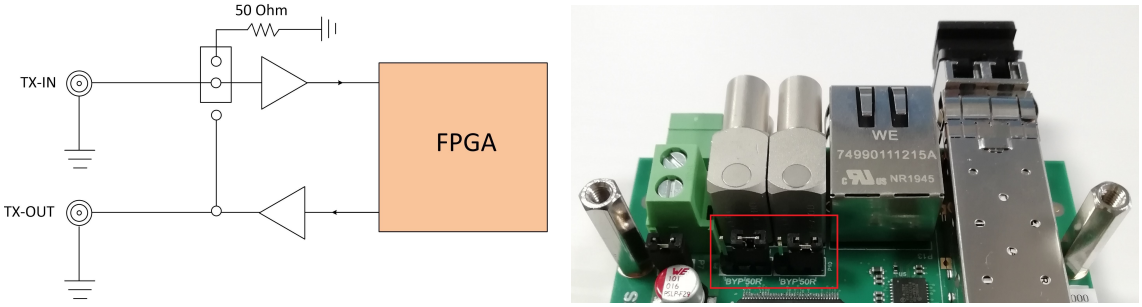


Fig. 8.10: Schematic diagram, on the left, of the TX-IN and TX-OUT connectors with the jumpers in the default position. On the right, an image of the jumpers in the A5202 board: both T1-IN and T0-IN jumpers are 50 Ω terminated.

In this configuration, the input signal on the TX-IN connector can be eventually propagated to the TX-OUT connector, but only after it has been transmitted to the FPGA, which introduces delays on the signal. The output signal from the TX-OUT connector has to be 50 Ω terminated. The TX-IN and TX-OUT connectors are independent in this configuration.

The user can perform a bridged connection by placing the jumper as it is shown in Fig. **8.11**.

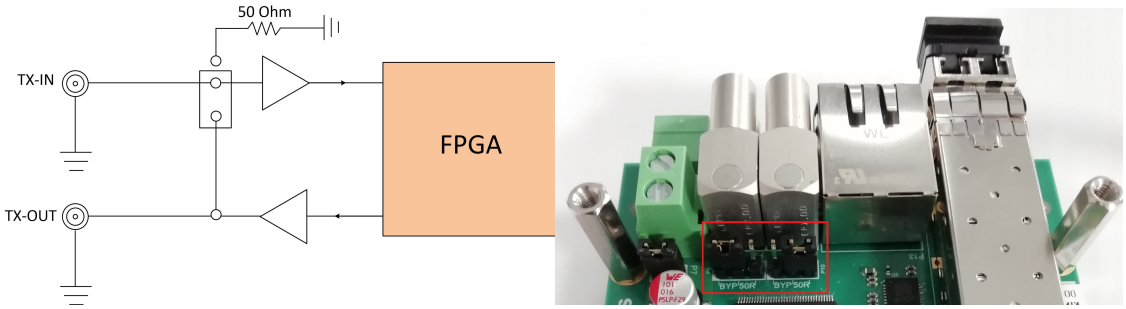


Fig. 8.11: Schematic diagram, on the left, of the TX-IN and TX-OUT connectors with the jumper positioned to form a bridged connection between TX-IN and TX-OUT. On the right, an image of the position of the jumper in the A5202 board: only the T0-IN jumper (on the left) is positioned to form a bridged connection.

In this configuration, a short circuit is created between the TX-IN and TX-OUT lines and the two connectors are no more independent. This second modality is particularly useful in order to perform a **Daisy Chained Trigger Distribution** (see Sec. **8.4.5**) or a **Wired-OR** (see Sec. **8.4.6**) when a system composed by several A5202 units is created.

8.4.5 Daisy Chained Trigger Distribution

This modality is particularly useful in case the user may want to propagate a common external trigger to all boards in the FERS-5200 system via the T1-IN/T1-OUT (or T0-IN/T0-OUT) connectors. However, by using a default configuration for the TX-IN jumpers, several delays would be introduced to the trigger signal when connecting in daisy chain TX-IN and TX-OUT connectors of all boards (due to FPGA processing of the signal). For this reason, a bridged connection for all TX-IN/TX-OUT connectors of all boards has to be created moving the jumpers as explained in Sec. **8.4.4**. In Fig. **8.12**, a schematic overview of a system composed of N A5202 units with a daisy-chained connection of the TX-IN/TX-OUT connectors is presented.

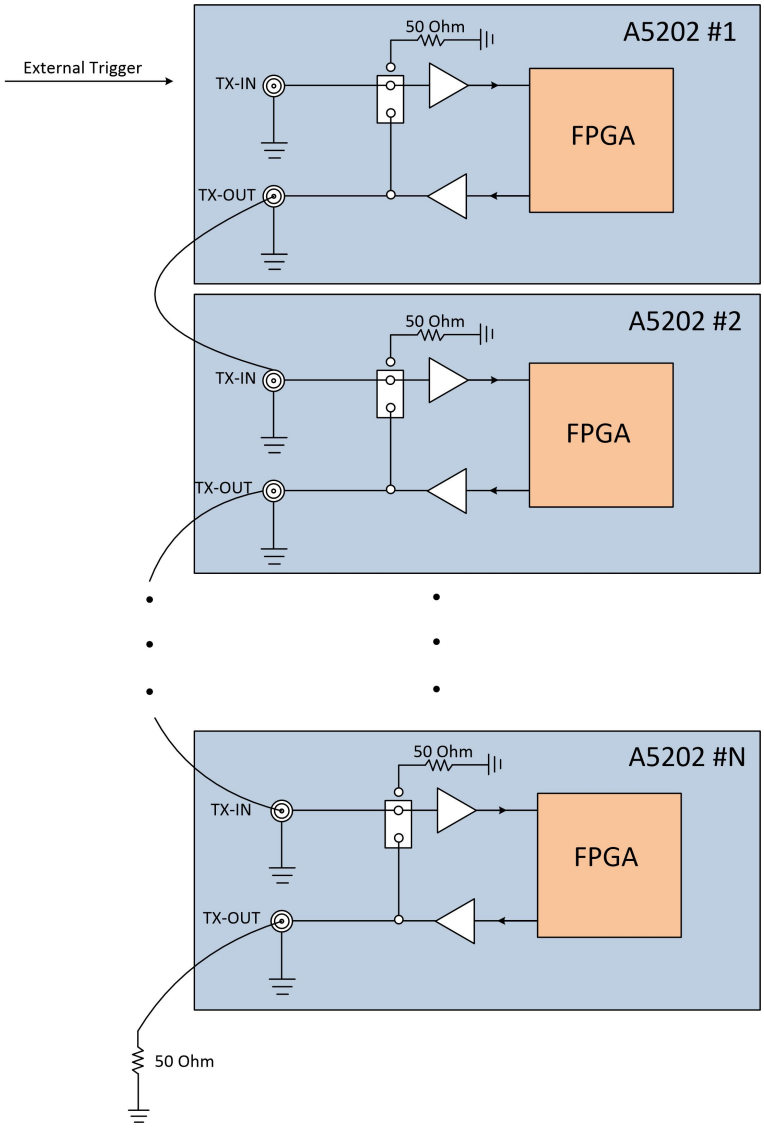


Fig. 8.12: Schematic diagram of a daisy chained trigger distribution.

In order to use an external trigger as a bunch trigger source directed to all boards, the user should then:

- Create a daisy chain as in Fig. **8.12** with an external trigger transmitted to the TX-IN connector of the first board.
- Select as bunch trigger source the signal from the TX-IN connector for all boards.
- Turn off the output from the TX-OUT connector of all boards by selecting the ZERO option (see Sec. **8.4.2**). In this way, no high logic level is transmitted by the FPGA to the TX-OUT connector and that

would interfere with the trigger signal transmitted in daisy chain.

As soon as a trigger is asserted, it is transmitted almost contemporary to all boards, with the only delay introduced by the cables connecting the TX-OUT connector of one board to the TX-IN connector of the next board.

8.4.6 Wired-OR

By performing slight changes to the system presented in Sec. **8.4.5**, the user can also create a wired-OR connection between all boards composing the FERS-5200 system. In Fig. **8.13**, a schematic overview of a system composed of N A5202 units with the connection necessary to perform a wired-OR of the TX-IN/TX-OUT connectors is presented.

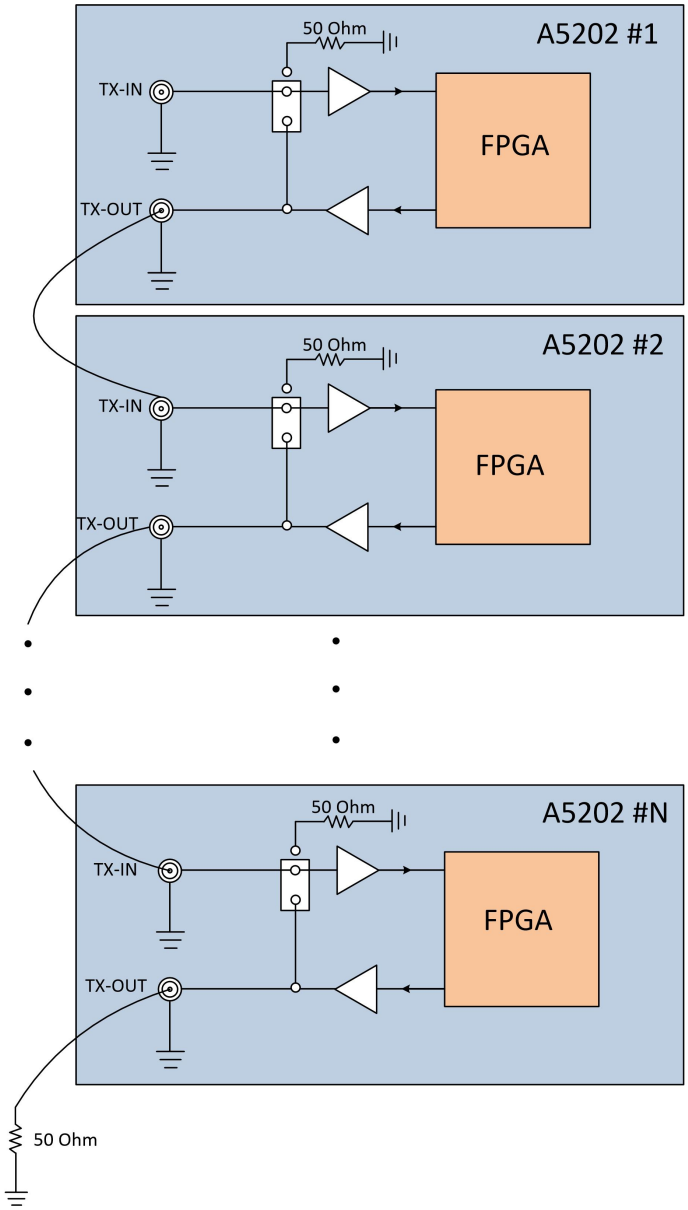


Fig. 8.13: Schematic diagram of a wired-OR connection.

In order to use the wired-OR connection as a bunch trigger source directed to all boards, the user should

then:

- Create a daisy chain connection as in Fig. **8.13**.
- Select as bunch trigger source the signal from the TX-IN connector of all boards.
- Select the T-OR (or TLOGIC or Q-OR) signal to be transmitted to the TX-OUT connector of all boards.

As soon as a T-OR trigger (or TLOGIC or Q-OR) is asserted by one of the boards, a trigger signal is transmitted almost contemporary to all boards, with the only delay introduced by the cables connecting the TX-OUT connector of one board to the TX-IN connector of the next board.

8.5 Acquisition Modes

8.5.1 Spectroscopy Mode (PHA)

This acquisition mode is always controlled by a bunch trigger signal and the acquisition is simultaneous on the 64 channels of the unit. The trigger can either be local to the unit, e.g. OR or a more complex logic combination of the 64 TD self-triggers (see TLogic description in Sec. **8.3**), or can come from an external trigger logic. In case the bunch trigger is internally generated starting from a logic combination of the channel TD self-triggers (TLogic signal), the time distance between the bunch trigger and the Slow Shaper peak is small and particular attention should be paid to the value set for the Hold Delay parameter (see Sec. **8.1.2** and **9.2.2**).

In Sec. **8.4.5** and Sec. **8.4.6**, two examples of trigger distribution for a system composed of several A5202 boards was presented. When available, the FERS-Collector Board (FERS-CB) will allow to receive the OR of the chain and combine it with other chains or with further external trigger sources. Eventually, the global trigger of the whole system could then be fed back into the T1-IN/T0-IN connectors of all FERS-5200 units. Alternatively, it would also be possible to propagate a global trigger from the FERS-CB to the FERS-5200 units through the TDlink, provided that the application can tolerate some jitter and/or delay on the arrival time of the trigger.

In Spectroscopy mode, when a trigger is asserted, the Sequencer implemented in the FPGA drives the Hold signal of the Citiroc-1A (see Sec. **8.1.2**) high to hold the peak values detected in the Slow Shaper amplifiers. The FPGA then controls the Multiplexer readout sequence using the serial output readout which provides in parallel the LG analog value, HG analog value and trigger status of each channel sequentially. The peak amplitudes are then converted by the on-board 13-bit ADCs.
This operation takes $\sim$ 10 µs and causes a systematic dead time for the acquisition (more details in Sec. **9.2.4**). During this time, the board is in a Busy condition (see Sec. **8.3**) and all other bunch triggers arriving in this time interval are counted (in order to determine the lost trigger statistics) but cannot give rise to another A/D conversion sequence, i.e. the energy information for that trigger is lost. The FPGA implements two counters for dead and real time determination. The value of these counters is periodically passed in the data flow together with other status registers (e.g. temperature, status flags, lost trigger counter, etc.).

A validation logic can also be enabled when working in Spectroscopy Mode in order to accept/reject only particular bunch trigger signals, with the validation signal that can be transmitted via the T0-IN/T1-IN front panel connectors (see Sec. **8.4.1**). A more detailed description of the validation signal functioning principle can be found in Sec. **8.3**. Inside the FPGA, the same counter implemented for the bunch trigger IDs can be alternatively used to count the number of validation signals arriving to the board **[RD3]**.

The T0-IN/T1-IN connectors can also be used to transmit a veto signal, allowing to reject particular bunch triggers arriving to the board.

The Zero Suppression (ZS) can also be enabled in order to discard those channels whose PHA values are lower than a certain programmable threshold. In particular, the advantage of using the ZS is that of reducing the amount of data transmitted from the board to the PC by transmitting only significant data. The ZS threshold can be set independently channel-by-channel and can be different for LG and HG amplification chains. More details are provided in the Janus User Manual **[RD3]**.

Besides the absolute time stamp of the trigger given with a granularity of 8 ns, a fine time measurement

coming from the high resolution TDC (50 ps) could be provided for future applications. This TDC will measure the time difference between the T-OR (i.e. OR of the self-triggers generated by the TD) and an external time reference (feeding T0-IN or T1-IN connectors).

The data readout in Spectroscopy Mode is designed to facilitate the event building. Indeed, when using the FERS-CB DT5215, data packets belonging to the same trigger and acquired by different FERS-5200 units are read out "horizontally", meaning that each block read initiated by the DAQ software involves the packets of a specific trigger index. The 1st FERS-5200 unit in the system transfers the data packet of the trigger N, then passes a token to the next unit in the chain that appends its data packet, going on up to the last unit in the chain. Multiple chains will be appended in the FERS-CB modules. If one FERS-5200 unit missed a trigger for any reason, it will skip the readout of that trigger (does not provide any data), so that the packets alignment is always guaranteed.

Note: The Spectroscopy Mode is typically used for trackers, veto systems, calorimeters and also for spectroscopy applications.

8.5.2 Counting Mode

The FPGA implements 64 counters (32-bit depth) connected to the individual self-triggers (output of each channel TDs, see Sec. **8.1.3**). The counters can be read on the fly (from the registers) or simultaneously latched and stored into the local memory buffer with the bunch trigger. In this mode, the counting intervals (or slots) are defined by the bunch trigger that, in most cases, is an internal periodic signal whose period is programmable in the range 16 ns to $\approx$ 34 s (Dwell time). However, it is also possible to use an external bunch trigger (from T0-IN/T1-IN connector as explained in Sec. **8.4.1**) or even an internal one (e.g. TLogic signal, see Sec. **8.3**). A data packet is produced for each interval: it contains a progressive index (slot ID), a 56-bit time stamp (absolute latching time of the counters) and 64 words with the value of the counters. The counters are reset after each interval. There is no dead time between two intervals as far as the throughput does not saturate the readout link.

Note: This mode is typically used for imaging, for instance with an 8x8 SiPM array. The trigger threshold for counting can be adjusted down to 1/3 of photo-electron, thus allowing for single photon counting. The Citiroc-1A internal comparator which generates the channel self trigger gives a maximum count up to 20 Mcps.

Note: The rate of counts should not be confused with the maximum bunch trigger rate allowed, which depends on the bandwidth. The counters continuously count the events and when the trigger arrives, the counters are reset to 0 and restarted. The trigger produces data which is written into memory and one event corresponds to about 300 byte (64 channels x 4 bytes of the counter). Supposing a bandwidth of about 2 MB/s, a possible value of bunch trigger frequency could be 1 kHz which gives a throughput of 300 kB/s and the possibility to get all data without losses.

8.5.3 Timing Mode

In Timing Mode, the channels acquire independently: for each channel self-trigger (output of the TD, see Sec. **8.1.3**), the FPGA saves the channel ID (0 to 63) and the time stamp of the hit into the local memory buffer. By default, also the Time over Threshold (ToT) information is also saved, i.e. the duration of the channel self-trigger signal, which gives a rough energy estimation of the hit.

Two timing modes are available:

- **Common Start Gating**, a Time Reference (T_{ref}) signal opens an acquisition window of programmable size and only the hits belonging to that time window are saved in the data packet.

- **Common Stop Gating**, the T_{ref} signal closes an acquisition window of programmable size and only the hits belonging to that time window are saved.

Note: If the user may need to save all hits sequentially to the list (with no acquisition window), the following approach can be pursued:

- Set the Common Start Gating as acquisition method with the internal periodic pulser used as T_{ref}.
- Set a certain value for the period (T) of the internal periodic pulser of the board.
- Set a time window (gate) width equal to T.

The T_{ref} signal can be propagated from the T1-IN/T0-IN connectors or it can be the OR signal of the channel self-triggers (either from channel QDs or from channel TDs) or even a logic combination of the channel self-triggers from the TD line (see TLogic signal in Sec. **8.3**).
The time stamp of the Tref signal is given as a 56-bit absolute time (the zero corresponds to the start of the run) and has a granularity of 0.5 ns. The time stamps of the hits (also at 0.5 ns of granularity) are given as ΔT values relative to T_{ref} (the previous one in Common Start, the following one in Common Stop mode). These ΔT are tipically indicated as **Time of Arrivals (ToA)**. They are expressed as a 25-bit number, therefore the dynamic range is $\sim$ 16,78 ms ($2^{25} \times$ 0.5 ns). When the ToT is enabled (selectable by software), the value is saved on 9 bits, thus reducing the dynamic range of the time stamp to 16 bits, i.e. a dynamic range of $\sim$ 32,77 µs ($2^{16} \times$ 0.5 ns). The ToT provides information about the pulse height (energy), thus making it possible to combine timing and spectroscopy analysis, even though the energy resolution is not as good as the one provided by the peak sensing A/D conversion (see Sec. **9.3.2**).

The time stamping mode is dead time free as far as the throughput does not saturate the readout link. When this happens, the acquisition is paused causing dead time (real and dead time counters are available, as explained in Sec. **8.5.1**).
Since there is not a bunch trigger and the data throughput of one FERS-5200 unit can be significantly different from another one, the data readout takes place "vertically" when several units are connected via the DT5215 FERS-CB: the software reads a block of data from each unit (containing a given number of time stamps belonging to the 64 channels of that unit), but there is not any correlation between the data coming from different units. The software gives priority to the units that are producing more data; silent units will be skipped until they have data to read.

8.5.4 Time Stamped Spectroscopy Mode

This mode is similar to the Spectroscopy Mode (see Sec. **8.5.1**), meaning that it performs the A/D conversion of the pulse heights, but individual time stamps and ToT information are added to the channels that have been fired. For each bunch trigger, the FPGA opens an acquisition window (Common Start Gating mode, see Sec. **8.5.3**) of programmable size and acquires the time stamps of the TD self-triggers occurring within the window together with the ToTs. If there are multiple self-triggers on the same channel, only the last one will be considered. The time stamp has a resolution of 0.5 ns and is referred to the bunch trigger (ToA). The channels that have not been fired (having no self-triggers falling in the acquisition window) are suppressed and will only give PHA data.

8.6 TDlink and Data Throughput

Note: The content of this section has to be considered preliminary and thus also the technical specifications are subject to change.

Multiple FERS units can be controlled and read out through the TDlink (**COMING SOON**), a timing and data link able to distribute a reference clock, broadcast synchronization and acquisition commands (start run, stop run, bunch triggers) and read/write data packets for both readout and slow control. The physical layer of the TDlink is a 4.25 Gbit/s duplex link, running over optical fiber (LC connectors). The readout bandwidth of the TDlink is $\sim$ 80 MB/s. When N units are connected in daisy chain (N from 1 to 16), the bandwidth is shared between the units; for instance, with 16 nodes, each unit has 5 MB/s on average.

The propagation delay of the data packets and commands circulating over the TDlink is not completely deterministic. In fact, the link performs occasional auto-synchronization procedures that require the transmission of low level data packets, not controlled by the user protocol. These packets have higher priority than the user payload and introduce an unpredictable delay. While this small uncertainty of the propagation delay is not an issue for the readout, it makes the link unsuitable for the distribution of timing signals and, sometimes, also for the distribution of the global trigger when low jitter and low propagation delay is mandatory. As already said, the physical signals from T0-IN and T1-IN connectors can be used for this purpose. Nevertheless, the TDlink is able to guarantee that all the FERS-5200 units in the network run with a synchronized global time. Indeed, after power on, the TDlink sends a series of synchronization packets that allow the link master to understand the number of connected slaves (FERS-5200 units) and the exact delay of each node. The synchronization procedure initializes the local time counter in each unit (set the same zero) and provides a low jitter clock signal (typically 200 MHz) that is used for the internal timing of the boards.

The required bandwidth for each FERS-5200 unit depends on the acquisition mode. In Spectroscopy Mode, the event data packet contains the header (16-bit), the channel mask (64-bit), the trigger time stamp (56-bit) and one charge value per channel (13-bit). Without zero suppression, the event data size is 120 bytes. Considering 10 µs conversion time, the maximum trigger rate is then 100 kHz and the maximum throughput is 12 MB/s. It is realistic to have data reduction of $\sim$ 80% after the zero suppression, thus reducing the throughput down to less than 3 MB/s/unit, which is below the available bandwidth also in the worst case of 16 units in daisy chain.

Besides the TDlink, the FERS-5200 unit provides USB 2.0 and Ethernet interface (TCP-IP @ 10 or 100 Mb/s) that allow a single unit to be controlled and read out by a PC without any additional hardware.

Note: The USB and Ethernet connections are very convenient for a quick and easy startup and evaluation of a small system, but they are not ideal for large systems and for scalability because there is no synchronization between multiple units.

9 Characterization Measures

In the following chapter, the technical characterization of the A5202/DT5202 board is presented.

9.1 HV and bias adjust

9.1.1 Linearity and Dynamics of the DAC bias adjustment

The internal DACs (see Sec. **8.1.1**) of the Citiroc-1A (8-bit, one DAC per channel) have a programmable dynamic range for the channel-by-channel HV adjustment: 2.5 V or 4.5 V. To measure the bias generated by the DAC and verify the linearity of the HV response, it is necessary to connect a multimeter between the channel pin and the HV pin (see Fig. **9.1**). The HV should be turned on (see Sec. **10.6**) to a known value, e.g. 20 V. The DAC tension can then be obtained as the difference between the value measured with the multimeter and the value set for the common HV.

Note: When the DAC is disabled the default value for the tension is measured to be 4.5 V.

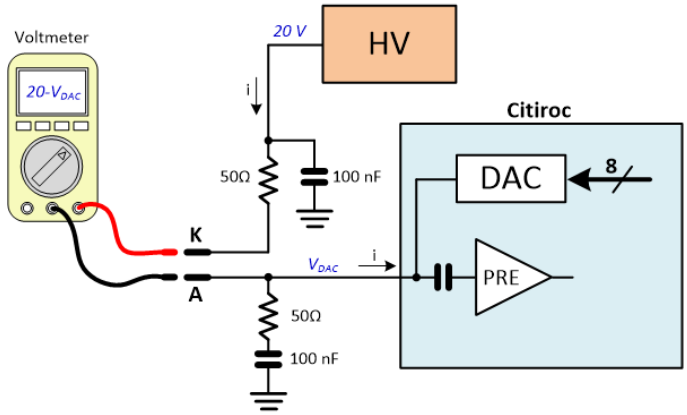


Fig. 9.1: How to measure the DAC voltage of the HV individual bias adjustment.

In Fig. **9.2**, the linearity of the DAC response to the set values and the DAC Integral Non-Linearity (INL) is presented. This parameter represents the deviation of the entire transfer function from the ideal function.

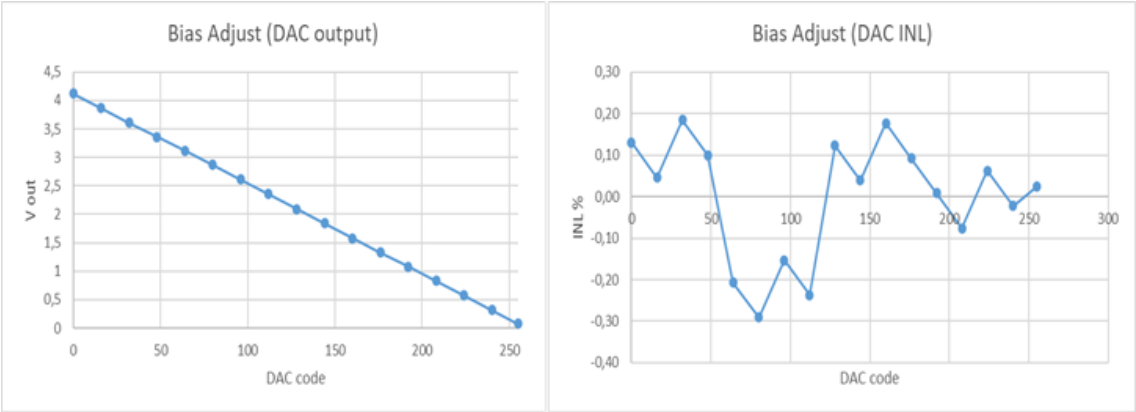


Fig. 9.2: Measurement of the DAC linearity (left plot) and of the DAC INL (right plot).

9.2 Test with External Pulser in Spectroscopy Mode

A series of tests were executed in CAEN with an external pulser injecting a certain amount of known charge into the acquisition channels of the A5202, with the aim of verifying the gain, dynamics, noise (i.e. the amplitude resolution), and other parameters of the board in the various acquisition modes. There are two ways to pulse the channels of the A5202: directly from the inputs, through a special charge injection circuit (see an example in Fig. **9.3**) connected to a specific channel, or through the test pulser, either internal or external (see Sec. **8.1.4**).

Note: There is a substantial difference between using the circuit in Fig. **9.3** (connected to the anode line in Fig. **9.1**) and using the test pulser. In the latter case, as explained in Sec. **8.1.4**, the test pulse is directly fed into the Preamplifier (other capacitors/resistances between the anode and the Preamplifier input are by-passed).

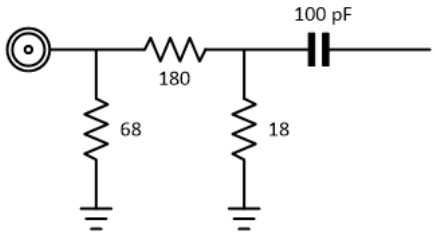


Fig. 9.3: Charge injector circuit used for testing purpose.

The signal feeds the inputs of both Citiroc-1As and can be connected or disconnected to/from the desired channels.

Note: Although it is possible to connect at the same time all channels to the test signal, WeeROC recommends pulsing one channel at a time.

Note: A 1:5 attenuator is present between the Test Input MCX connector of the A5202 board and the Citiroc-1A test input.

Note: If using the internal pulser, the user has to keep the MCX bushing disconnected.

9.2.1 Gain, dynamics and resolution as a function of the Citiroc-1A Gain Setting

The input signal used for this test is a square wave with 500 mV amplitude (5 ns for both leading and trailing edge) thus injecting in the Citiroc-1A channel $Q_{in} \sim 4.5$ pC (value obtained from the value of the capacitance in Fig. **9.3**). With such value of Q_{in} and a measured HG Slow Shaper output amplitude of ∼800 mV, the gain of the A5202 board (by setting the software "HG Gain" value of 50) is found to be ∼ 0.18 mV/fC.
The RMS resolution is measured to be ∼0.2% (0.44% FWHM).
By setting the maximum value for the gain value of the HG amplification chain, i.e. 63, a gain of ∼0.56 mV/fC is measured with an RMS resolution of approximately 1%.
By injecting a 0.9 pC charge the results presented in Fig. **9.4** and Fig. **9.5** were obtained.

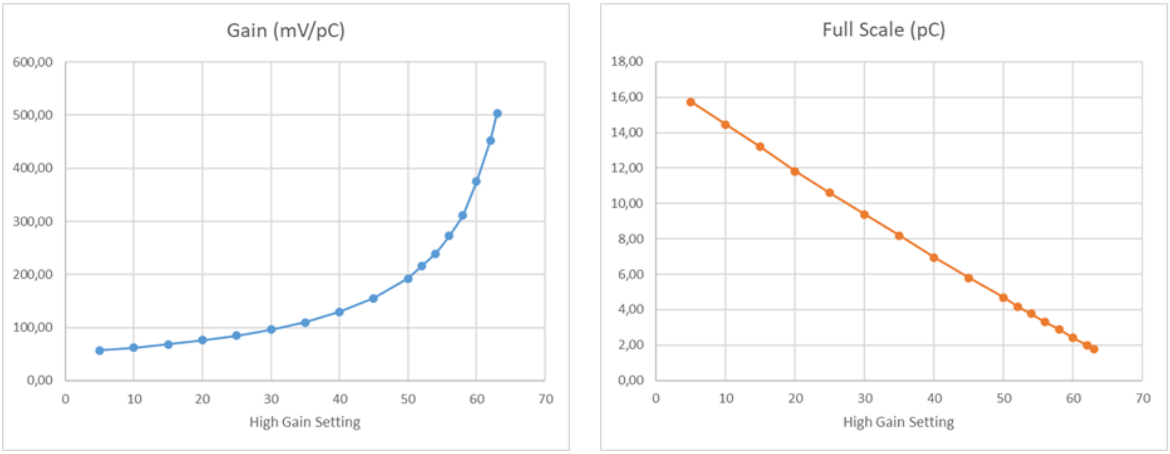


Fig. 9.4: Gain and Full scale range as a function of the HG Gain setting.

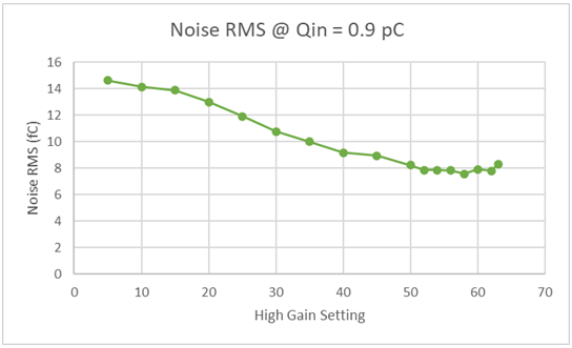


Fig. 9.5: RMS noise as a function of the HG Gain setting.

Note: The study was performed only for the HG amplification chain. For the LG one the same trends as those presented in Fig. **9.4** and Fig. **9.5** are expected.

9.2.2 Dependence of the ADC readout on the trigger-signal delay

The purpose of this test is the understanding of the maximum delay the trigger can have with respect to the signal in order not to compromise the measurement when acquiring pulse height data (see Sec. **8.1.2**). A square wave of 300 mV (5 ns rise time) is sent into the charge injection circuit in Fig. **9.3**, thus $Q_{in} \sim 2.7$ pC is injected (value obtained from the value of the capacitance in Fig. **9.3**). A LVTTL signal synchronous with the test wave, but with a certain delay, is propagated to the T1-IN connector of the A5202 and used as external trigger. The graph in Fig. **9.6** shows the variation of the value converted by the ADC as a function of the delay of the trigger relative to the pulse.

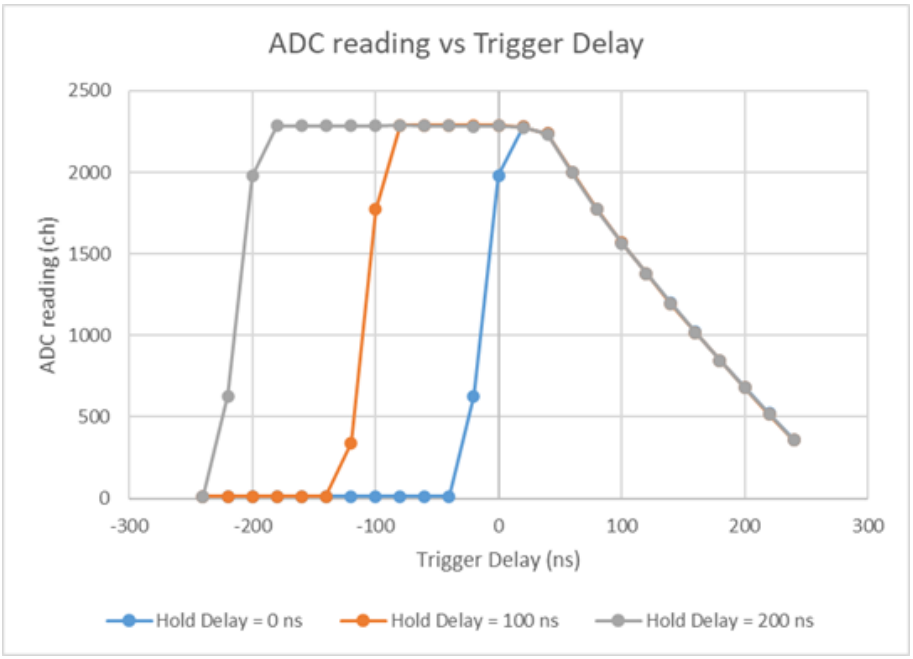


Fig. 9.6: ADC reading as a function of the trigger delay.

The three curves in Fig. **9.6** correspond to different values of the Hold Delay parameter (software programmable). This parameter determines the time distance between the global trigger signal, which puts the Citiroc-1A in Peak Sensing Phase (see Sec. **8.1.2**) and the Hold signal (see Fig. **8.5**).
Two opposite situations may occur depending on the delay between the trigger and the pulse (i.e. the output of the Slow Shaper):

- The trigger arrives before the peak of the pulse and the Hold Delay parameter is too small. In such case, the Peak Detector goes into Hold before the pulse has reached the peak, so the amplitude reading occurs along the rising edge of the pulse and the read value underestimates the peak amplitude. The amplitude reading can even occur when the pulse has not yet arrived and in that case the value read would be 0 on average.
- The trigger arrives after the peak of the pulse. Regardless of the Hold Delay value, the peak stretcher goes into Peak Sensing Phase too late, so it does not record the maximum of the pulse. The converted value will be the one relative to the point on the falling edge where the Peak Detector is activated.

Note: The peak reading reaches the best performances (in terms of resolution) only when the Peak Detector works correctly, i.e. when the trigger arrives before the peak and the Hold signal is activated after the peak. In other cases (Hold too early or trigger too late), since the sampling occurs in the rising edge, the reading is subjected to the error induced by the sampling jitter (1 clock cycle = 8 ns), so in addition to having an underestimation of the amplitude, also high RMS of the reading will be retrieved.

Note: The test considers as delay between trigger and pulse the one measured between an external trigger propagated through the T1-IN connector and the pulse at the analog input of the channel under test. The user should consider the presence of internal delays on both paths, i.e. preamplification and analog shaping for the pulse as well as trigger latency due to re-synchronization and signal processing in the FPGA.

In conclusion, in order to properly work in Spectroscopy Mode, the external trigger must arrive before the pulse (at most $\sim$ 20 ns later, see Fig. **9.6**). If it arrives with an advance equal to T, the Hold Delay parameter must be set with a value at least equal to T + $\sim$ 20 ns.

Note: The tests were done with a shaping time value of the HG Slow Shaper ("HG_ShapingTime" parameter)of 25 ns. By increasing the shaping time, the position of the peak would be delayed with respect to the beginning of the pulse, thus allowing to have a greater tolerance on the delay of the trigger with respect to the signal.

9.2.3 Resolution and Linearity

The aim of the test is the measurement of the linearity of the entire acquisition chain, from the input to the output of the ADC. For this purpose, the usual charge injection circuit (see Fig. **9.3**) connected to the input of the A5202 is used, sending a square wave with amplitude varying from 20 mV (Q_{in} $\sim$ 0.18 pC) to 500 mV (Q_{in} $\sim$ 4.5 pC). The measurement is performed with "HG Gain" = 50 and "HG Shaping Time" = 25 ns. Fig. **9.7** shows the results obtained for the resolution and linearity test.

Input			ADC						
Vin (mV)	Qin (pC)	p.e.	ADC	Fit	Resid	NLI (%)	RMS (ch)	RMS (fC)	RMS (%FSR)
20	0,18	1,1	155,6	185,7	-30,1	-0,74	7,59	8,78	0,19
40	0,36	2,3	318,3	333,3	-15,0	-0,37	7,72	8,73	0,19
60	0,54	3,4	476,7	480,9	-4,2	-0,10	7,61	8,62	0,19
80	0,72	4,5	631,7	628,5	3,2	0,08	7,47	8,51	0,18
100	0,90	5,6	784,5	776,1	8,4	0,21	7,40	8,49	0,18
150	1,35	8,4	1160,9	1145,0	15,9	0,39	7,19	8,36	0,18
200	1,80	11,3	1530,4	1514,0	16,4	0,40	7,12	8,37	0,17
250	2,25	14,1	1898,3	1883,0	15,3	0,37	7,20	8,53	0,18
300	2,70	16,9	2266,6	2251,9	14,7	0,36	7,15	8,52	0,17
350	3,15	19,7	2630,9	2620,9	10,0	0,24	7,21	8,63	0,18
400	3,60	22,5	2991,7	2989,9	1,8	0,04	7,35	8,84	0,18
450	4,05	25,3	3349,9	3358,9	-9,0	-0,22	7,22	8,73	0,18
500	4,50	28,1	3700,4	3727,8	-27,4	-0,67	7,50	9,12	0,18
		m_fit	819,94		RMS mean		7,36	8,63	0,18
		q_fit	38,12						

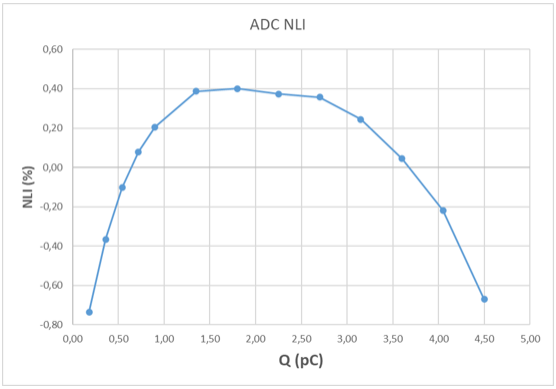


Fig. 9.7: Table with the result of the linearity test (left) and INL as a function of Q_{in} (right).

9.2.4 Resolution and Dead Time as a Function of the MUX Conversion Speed

Each Citiroc-1A **[RD1]**, after the signal peak sampling has occurred, waits for the FPGA to control the MUX readout sequence to output the channel peak amplitudes one after the other. The LG and HG amplitudes come out on two separate lines and are converted in parallel by the external ADC. Similarly, the conversion of the peak amplitudes from the two Citiroc-1A chips (64 channels total) is performed in parallel.
The minimum duration of the signal amplitude conversion of the MUX for one channel is 200 ns, which correspond to 6.4 µs for the 32 channel sequence. Moreover, a fixed time has also to be considered at the beginning and at the end of each sequence.
It is possible to program (via FPGA register or via the "MUX Clock Period" software command **[RD3]**) the

conversion clock period. Theoretically, by increasing the MUX conversion period, a better stabilization of the reading and therefore a lower level of noise in the conversion of the pulse height value may be reached. The ”MUX Clock Period” parameter has an impact on the conversion time and therefore on the dead time associated with each trigger.

Tab. **9.1** shows the RMS noise and dead time results as a function of the MUX conversion clock period. The test is performed sending a 300 mV test signal ($Q_{in} \sim 2.7$ pC). The value of the dead time can be measured by observing the Busy signal of the A5202 (e.g. sent out via the T1-OUT connector), or by sending a double trigger pulse separated by a time T, varying T until the board acquires a single trigger.

Mux Clk (ns)	Ns	Centroid (ch)	RMS (ch)	DeadTime (us)
600	1	2267,6	7,76	20,6
400	4	2268,2	7,66	13,9
400	1	2267,8	7,66	13,9
300	1	2269,1	7,60	10,4
200	1	2295,2	12,87	7.02

Tab. 9.1: RMS and Dead Time as a function of the MUX Readout Clock Period.

According to the test performed, it does not appear that averaging more than 1 ADC sample significantly improves the noise level and for this reason, inside the Janus software **[RD3]**, the value of the number of averaged ADC samples is set to 1 by default.

Moreover, a value of 200 ns for the ”MUX Clock Period” seems to be too short in order to have a good signal stability.

Note: CAEN suggests to set a **”MUX Clock Period” of $\sim$ 300 ns**. Indeed, higher values do not seem to bring benefit in terms of RMS noise reduction while increase the dead time.

9.3 Test with External Pulser in Timing Mode

In Timing Mode, the Slow Shaper, Peak Stretcher and ADC chain is not used. Only output signals from Citiroc-1A Time Discriminators (64 lines) are used. The TDs receive the signal produced by the Fast Shaper, whose shaping time is fixed (15 ns), and compares it with a programmable threshold which is set via two DACs, one common to all channels (10-bit) and one individual (4-bit) for the channel-by-channel threshold fine adjustment.
The output signal from the discriminator stays high as long as the signal remains over threshold. The rising edge of the signal determines the time stamp of the pulse, while the duration (ToT) is proportional to the pulse width, hence to the input charge.
Medium-resolution TDCs (1 LSB = 0.5 ns) are implemented in the A5202 FPGA to convert the 64 trigger signals from the two Citiroc-1As in order to determine time stamp and ToT values. The conversion of the TDCs is characterized by a very low dead-time, thus allowing to acquire pulses at a much higher rate than that sustainable in Spectroscopy Mode. Moreover, unlike the Spectroscopy Mode in which the trigger is common and the acquisition of amplitudes occurs simultaneously on the 64 channels, the Timing Mode makes the channels all independent, reducing to a minimum (a few tens of ns) the dead time of each channel.
In Timing Mode, a time reference (T_{ref}) signal acts as a gate for pulse acquisition. The T_{ref} can be both external (sent via T0-IN or T1-IN connector) or internal (T-OR of both Citiroc-1As, or periodically generated by the FPGA) and two possible acquisition modes are possible (see Sec. **8.5.3**).

9.3.1 Time resolution (ToA Spectrum)

For this test, a two-channel pulser is used. One channel produces the T_{ref} (LVTTL signal) propagated via the T1-IN connector, the other one the square wave (300 mV, i.e. $Q_{in} \sim 2.7$ pC) with programmable delay with respect to T_{ref} and propagated to the input of the charge injection circuit. The acquisition is performed in Common Start Mode and the measure of the mean and RMS of the ΔT between the channel TD self-trigger and the T_{ref} signal is retrieved. In this test, the spectrum is made on 4096 channels with each channel size corresponding to 0.5 ns (= 1 LSB of TDC). According to the results in Tab. **9.2**, the timing resolution is nearly constant within the dynamics (it does not vary as the measured delay varies) and is ∼250 ps RMS.

Delay (ns)	Mean (ch)	RMS (ch)	Mean (ns)	RMS (ns)
0	3,95	0,47	1,98	0,24
50	104,06	0,46	52,03	0,23
100	203,91	0,47	101,96	0,24
150	304,12	0,45	152,06	0,23
200	403,93	0,48	201,97	0,24
500	1003,99	0,48	502,00	0,24
1000	2004,00	0,49	1002,00	0,25

Tab. 9.2: Resolution values obtained from the ToA spectrum.

9.3.2 Resolution, dynamics and linearity of the ToT

The ToT measurement gives an amplitude (i.e. charge) information of the input pulse, even though with a non-linear relationship as can be seen in Fig. **9.8**. It is however possible to make a fit of the ToT curve as a function of the injected charge Q_{in}, for example logarithmic, in order to linearize the conversion, thus obtaining a sufficiently accurate charge measurement.

The table in Fig. **9.3** shows the result of the charge measurement performed via ToT (with a trigger threshold of 290).

As it can be noticed in Fig. **9.8**, the ToT curve as a function of injected charge Q_{in} is best approximated by a logarithmic curve. The fit output is the following function:

$$ToT = 31.514 \times \ln(Q_{in}) + 45.127$$

The residual INL after having applied the logarithmic fit is ∼ 6%. A better result (∼2%) is obtained by making a fit via 3rd degree polynomial (cubic):

$$ToT = 0.0409 \times Q_{in}^3 + 19.749 \times Q_{in}^2 - 1.4547 \times Q_{in} + 26.873$$

However, the logarithmic function (just for simplicity) is used for calculating the value of the charge from the ToT expressed in channels during this test. By applying it to the RMS value (expressed in channels), the RMS value in fC is obtained.
As it can be seen from the results in Tab. **9.3**, the RMS resolution (at Q_{in} = 4.5 pC) is more than three times (∼ 24 fC) higher with respect to that obtained in Spectroscopy Mode (∼ 9 fC, see Fig. **9.7**). It has to be remarked that, however, the greater dynamics obtained with the measurement of the ToT with respect to that achievable in Spectroscopy Mode: the ToT can measure up to Q_{in} = 13.5 pC, while the Spectroscopy Mode reached only Q_{in} = 4.5 pC. Indeed, even when the input signal saturates the Preamplifier (so the peak is clipped, preventing the acquisition in Spectroscopy Mode), the ToT follows a logarithmic curve. Conversely, for small signals, the ToT measurement shows strong non-linearity issues from 0.5 pC and below.

Note: The ToT, compared to the PHA, offers greater dynamics for higher amplitude signals, lower dead time, higher acquisition rate, possibility of independent acquisition on 64 channels, at the price of a lower resolution in charge (about 1/3), higher INL (about 6% with respect to 0.8%) and lower dynamics for the minimum detectable signal.

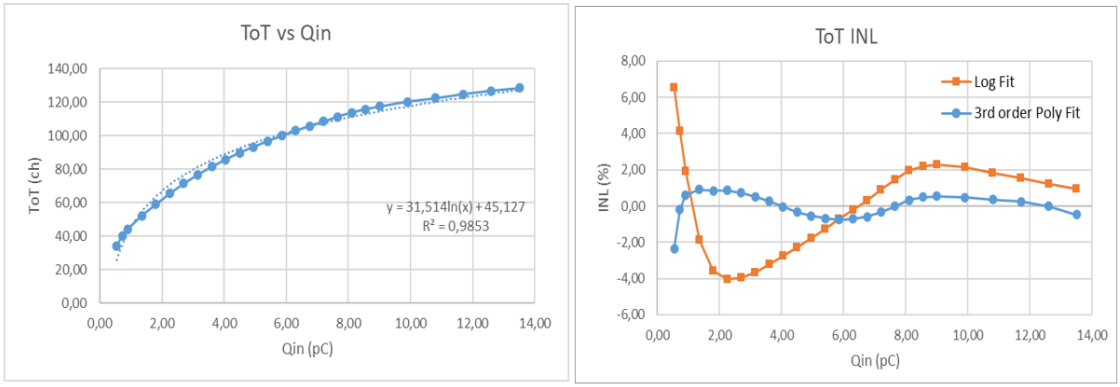


Fig. 9.8: ToT linearity. On the left, the ToT values as a function of the quantity of charge injected (Q_{in}). On the right, the INL values.

Test Pulse (mVpp)	Qin (pC)	ToT (ch)	RMS (ch)	RMS (%FSR)	RMS (fC)	Poly fit	INL (%)	Log fit	INL (%)
40	0,36	21,66	2,48	1,93	54,37	33,80	-9,45	12,93	6,80
60	0,54	34,10	0,87	0,68	17,98	37,12	-2,35	25,71	6,54
80	0,72	40,10	0,66	0,51	14,03	40,35	-0,20	34,77	4,15
100	0,90	44,28	0,66	0,51	14,51	43,50	0,61	41,81	1,93
150	1,35	52,16	0,61	0,48	14,62	50,98	0,92	54,58	-1,89
200	1,80	59,04	0,53	0,41	13,96	57,95	0,85	63,65	-3,59
250	2,25	65,51	0,56	0,44	16,32	64,41	0,86	70,68	-4,03
300	2,70	71,34	0,56	0,44	18,03	70,40	0,74	76,43	-3,96
350	3,15	76,60	0,57	0,44	20,20	75,93	0,52	81,29	-3,65
400	3,60	81,35	0,54	0,42	20,95	81,02	0,25	85,49	-3,23
450	4,05	85,66	0,52	0,41	21,97	85,71	-0,04	89,21	-2,76
500	4,50	89,59	0,53	0,41	24,25	90,01	-0,33	92,53	-2,29
550	4,95	93,24	0,51	0,40	25,18	93,95	-0,55	95,53	-1,78
600	5,40	96,66	0,52	0,41	27,60	97,54	-0,68	98,27	-1,26
650	5,85	99,85	0,49	0,38	27,86	100,81	-0,75	100,79	-0,74
700	6,30	102,87	0,45	0,35	27,33	103,78	-0,71	103,13	-0,20
750	6,75	105,71	0,48	0,37	31,05	106,48	-0,60	105,30	0,32
800	7,20	108,48	0,51	0,40	35,10	108,92	-0,34	107,34	0,89
850	7,65	111,11	0,42	0,33	30,68	111,13	-0,02	109,25	1,45
900	8,10	113,55	0,51	0,40	39,38	113,13	0,32	111,05	1,95
950	8,55	115,58	0,53	0,41	42,89	114,95	0,49	112,75	2,20
1000	9,00	117,29	0,52	0,41	43,77	116,60	0,54	114,37	2,27
1100	9,90	120,10	0,50	0,39	44,94	119,50	0,47	117,37	2,12
1200	10,80	122,47	0,58	0,45	55,11	122,01	0,36	120,12	1,83
1300	11,70	124,62	0,60	0,47	59,99	124,31	0,24	122,64	1,54
1400	12,60	126,55	0,58	0,45	60,71	126,58	-0,02	124,97	1,23
1500	13,50	128,38	0,56	0,44	61,24	128,99	-0,48	127,15	0,96

Tab. 9.3: ToT test results.

9.3.3 Maximum Acquisition Rate in Timing Mode

The purpose of the test is to measure the minimum separation between two input signals on the same channel so that they are seen (and counted) as two separate pulses. As in the previous test, a T_{ref} signal is sent on the T1-IN connector at a frequency of 100 Hz. With some delay with respect to it, a burst of 4 pulses is generated, separated by a time T. The value of T is then decreased until the acquisition lost one or more pulses of the burst.

Note: The output of the Fast Shaper typically has a duration of a few tens of ns, then the limitation to the double pulse resolution is mainly due to the time required to the Fast Shaper output to return below threshold. This time is a function of the input signal amplitude.

Fig. **9.9** shows the burst of 4 pulses spaced by 100 ns, which could be discriminated perfectly.

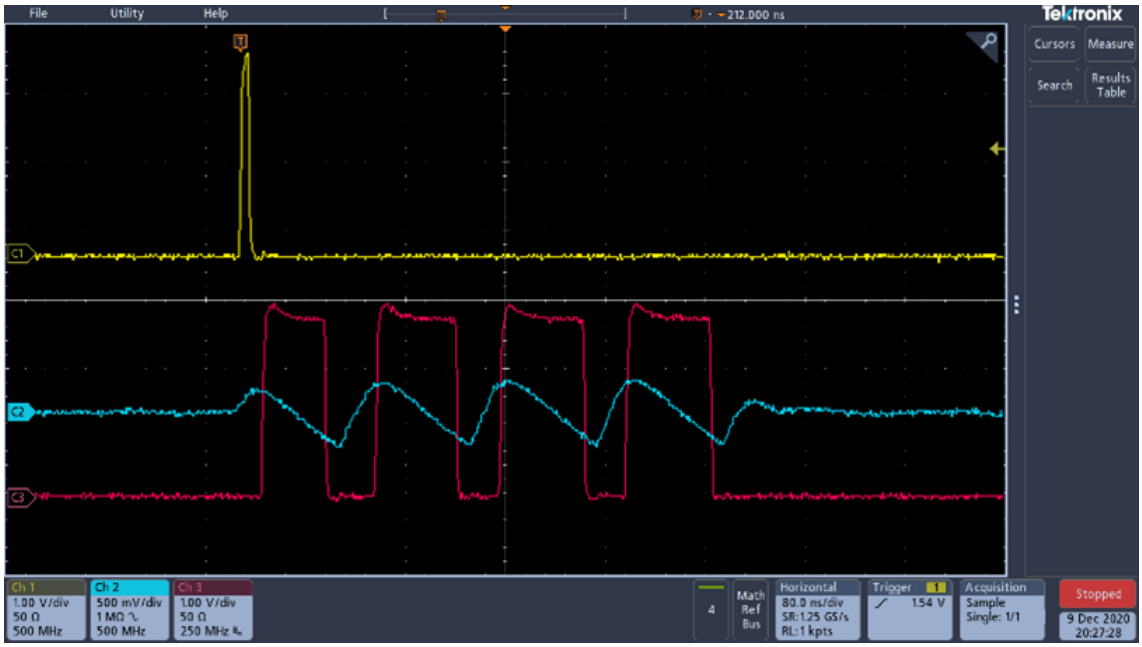


Fig. 9.9: Burst of 4 pulses spaced by 100 ns. In yellow the T_{ref} signal, in blue the output of the Fast Shaper and in red the T-OR signal.

For small signals (30 mV during the test), the timing mode allows the user to acquire pulses up to 10 MHz. During the test, the burst repetition is set to 100 Hz, to have no limitations due to the data throughput.

9.4 Test with External Pulser in Counting Mode

The test is similar to the one described in Sec. **9.3.3**, with the difference that instead of sending a burst, a periodic signal is sent. However, as already shown in Fig. **9.9**, the output of the Fast Shaper has a large undershoot so if pulsed by a periodic signal, peaks and valleys combine to form a signal whose maximum and minimum levels vary according to frequency and amplitude of the input signal. Under these conditions, in order to have an output logic signal from the discriminator having the same frequency of the input signal, it is necessary to adjust the trigger threshold in order to center it with respect to the level of the signals from the Fast Shaper.
The test is performed by setting the trigger for reading the counters on the internal periodic pulser (setting a value for its period of 1 ms, so that every ms the counters are read and reset).
The Counting Mode demonstrated to work without problems up to 15 Mcps. It is possible to reach 20 Mcps but it is necessary a fine tuning of the threshold that, in a real working condition with random signals instead of periodic ones, would be difficult.

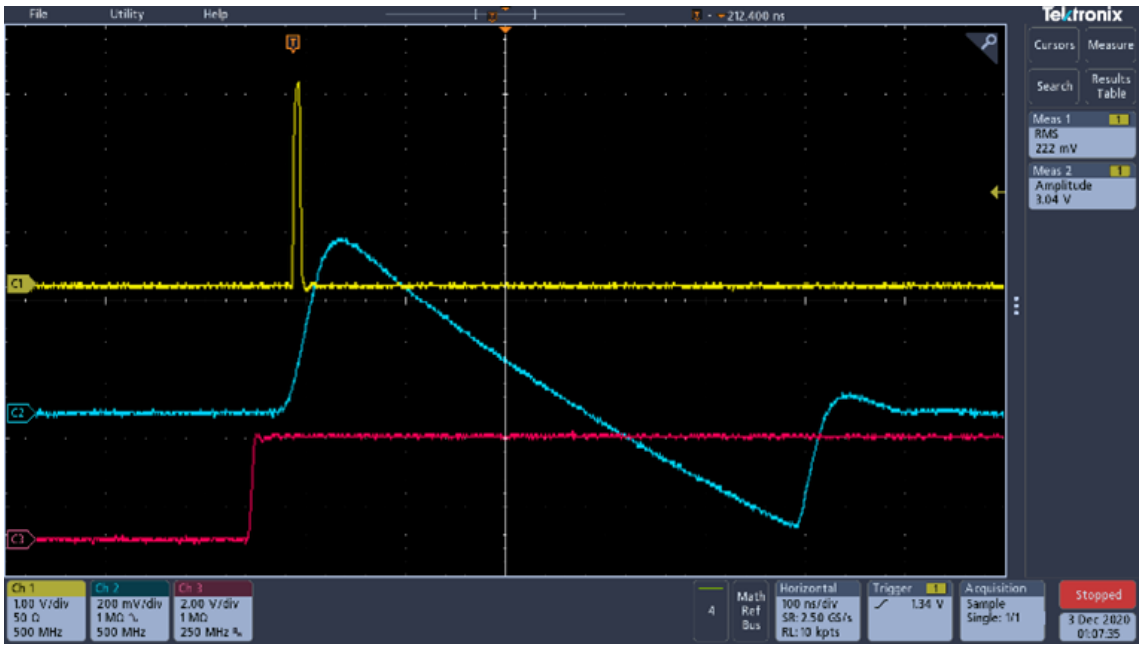


Fig. 9.10: Fast Shaper output (blue line).

Note: The limitation to the counting frequency is not in the counters implemented in the FPGA but in the analog part (Fast Shaper and Discriminator) of the Citiroc-1A.

10 Getting Started

The aim of this chapter is to guide the user through the installation of the A5202/DT5202 board and of the Janus software **[RD3]**. The basic instructions necessary to get familiar with the board and the software are also provided up to the instructions to acquire photoelectrons spectra with a SiPM matrix.

10.1 A5202/DT5202 Installation and Power ON/OFF

To properly install and power ON/OFF the device the user is kindly suggested to follow the instructions below:

- Connect the AC/DC adapter to the DC power jack.
- Connect the power supply to the +12V connector of the A5202/DT5202.
- The A5202 board immediately turns on, after few seconds the PWR green LED (see Sec. **7.3**) turns on and stays on as long as the board is connected to the power supply (see Fig. **10.1**). To power on the DT5202, the user has to press the button on the module front panel (see Sec. **7.3**).

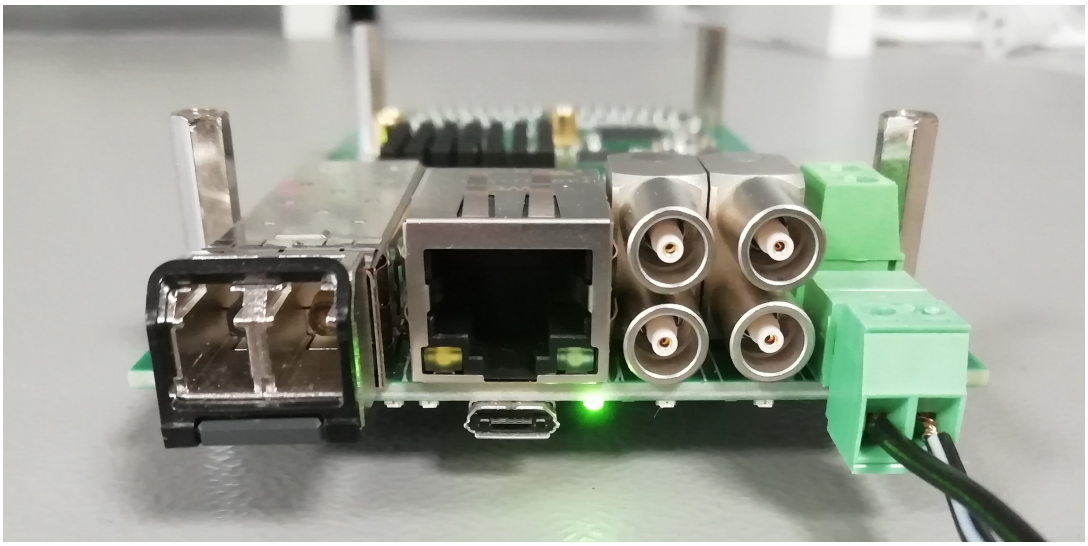


Fig. 10.1: A5202 status at power ON.

- To power off the A5202, disconnect the power supply from the board or extract the DC input switch (see Fig. **7.4**). To power off the DT5202, the user has to press the button on the module front panel (refer to Sec. **7.3**).

WARNING: TO PREVENT POSSIBLE DAMAGES TO THE ATTACHED DETECTOR AND ELECTRONICS, MAKE SURE TO TURN OFF THE HV CHANNELS BEFORE POWERING OFF THE BOARD!!!

10.2 How to Connect to the A5202/DT5202

10.2.1 Ethernet Connection to the PC

The Ethernet connection of the A5202/DT5202 can be done through a server, or it can be a point-to-point connection to the PC. In the latter case, the connection can be done using a crossed cable, a switch or a PC with a Gigabit Ethernet port. In order to properly configure the network, the user should follow the instructions below.

Note: The defaul IP Address of the A5202/DT5202 is: **192.168.50.3**.

1. Connect the Ethernet cable from the A5202/DT5202 to the PC.
2. Configure the Ethernet network of your PC.
   a. Open the path:
   `Control Panel - Network and Internet - Network and Sharing Center`
   as in Fig. **10.2**.

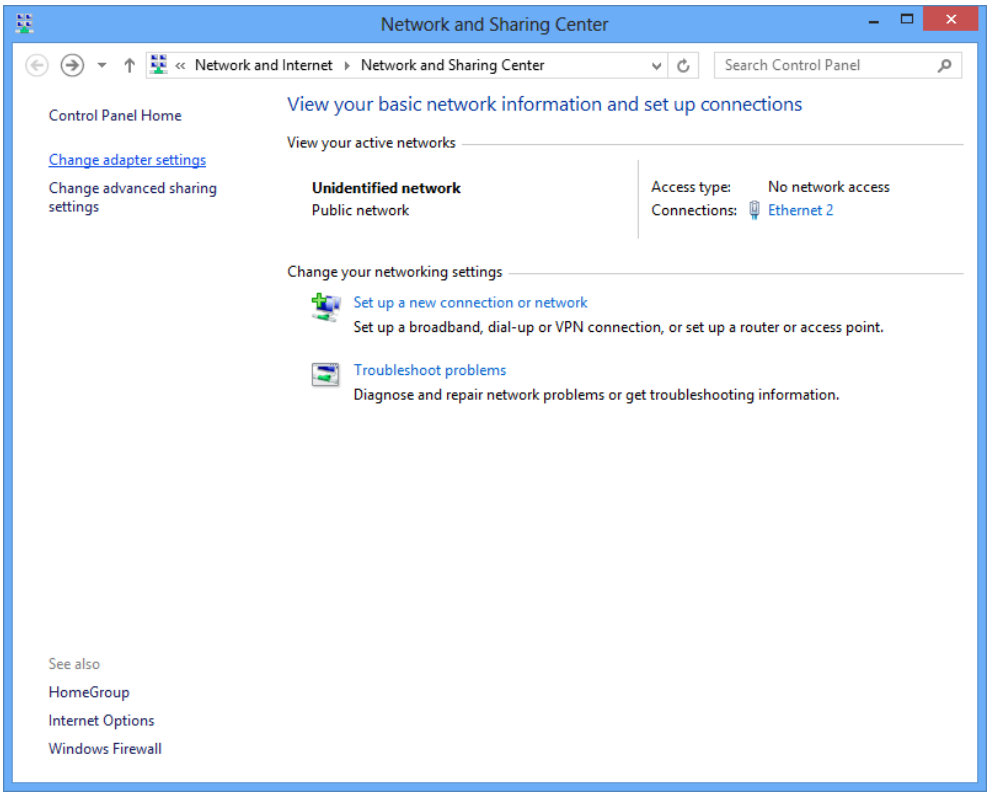


Fig. 10.2: The Network and Sharing Center window.

   b. Click on ”Change adapter settings”.

c. Right click on the Ethernet icon and select ”Properties”, as in Fig. **10.3**.

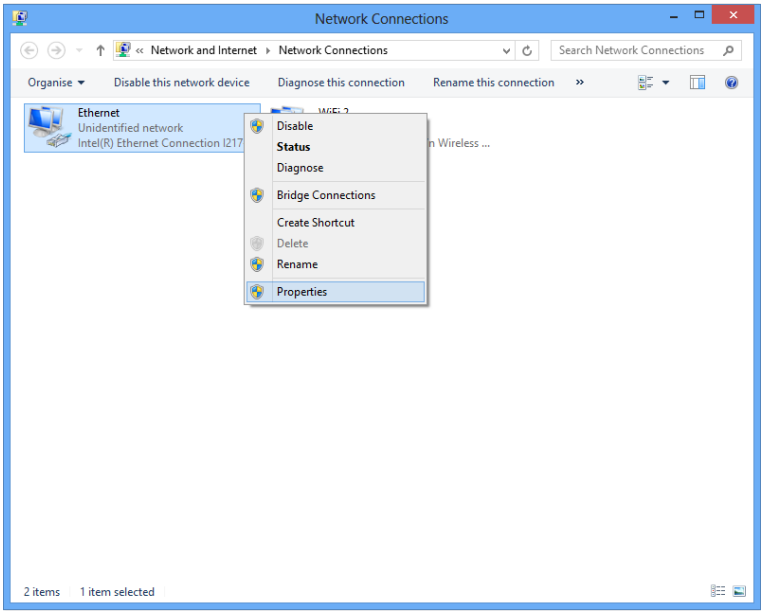


Fig. 10.3: Property window of the Ethernet network.

d. Click on ”Internet Protocol Version (TPC/IPv4)” and select ”Properties”, as in Fig. **10.4**.

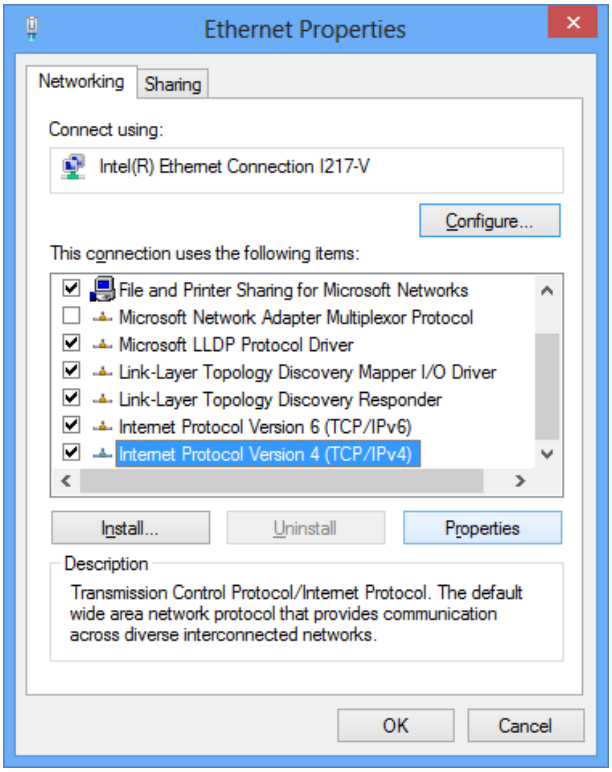


Fig. 10.4: Property window of the ”Internet Protocol Version (TPC/IPv4)”.

e. Copy the configuration in Fig. **10.5** on the ”Internet Protocol Version (TPC/IPv4) Properties” window and press ”OK”.

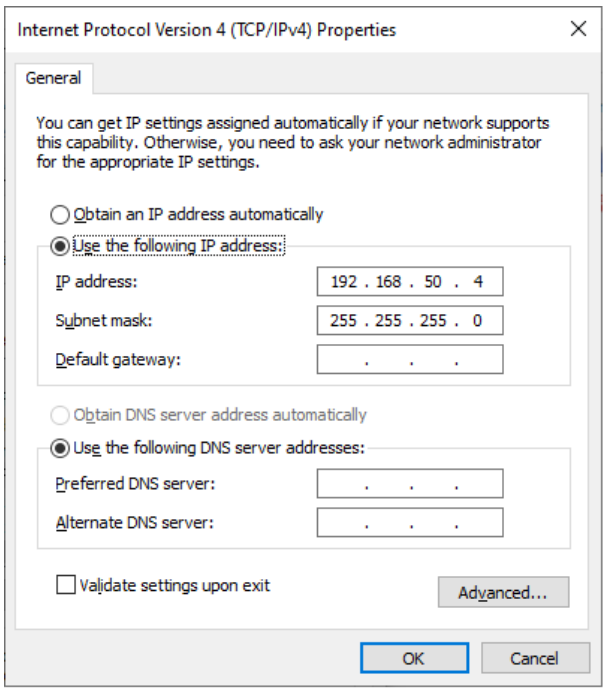


Fig. 10.5: ”Internet Protocol Version (TPC/IPv4) Properties” window.

3. The user can test if the communication between the PC and the A5202 is established by opening the ”Command Prompt” and typing the same command as in Fig. **10.6**. If the communication is correctly established, the output message should be similar to that in Fig. **10.6**.

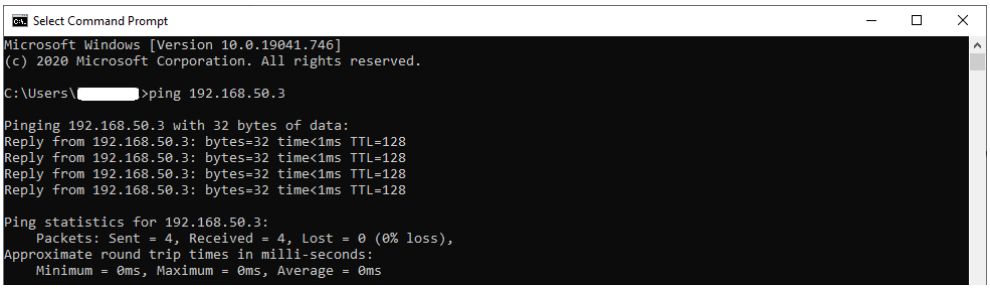


Fig. 10.6: Command prompt window with the command for testing the communication.

It is possible to monitor and define the Ethernet settings via the dedicated Web Interface. In order to access it, the user should:

1. Open a browser and enter the web address **192.168.50.3**. The homepage of the graphical web interface will open (see Fig. **10.7**).
2. Open the Configuration tab (see Fig. **10.8**). This window allows the user to read the device information, like the serial number, the hardware and firmware revision. Moreover, it is possible to set an IP address of the instrument different with respect to the default one. This last operation can be particularly useful in case the user wants to perform a multi-board Ethernet connection and therefore needs to associate each board with a different IP address (see Janus User Manual **[RD3]** for more details).

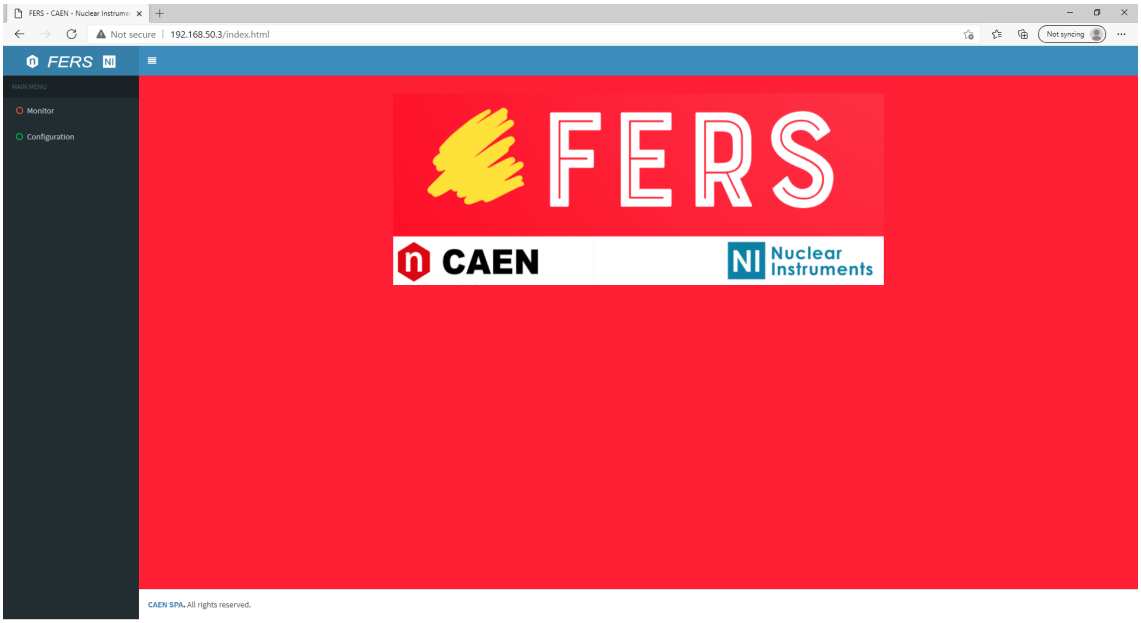


Fig. 10.7: Web Interface opening view.

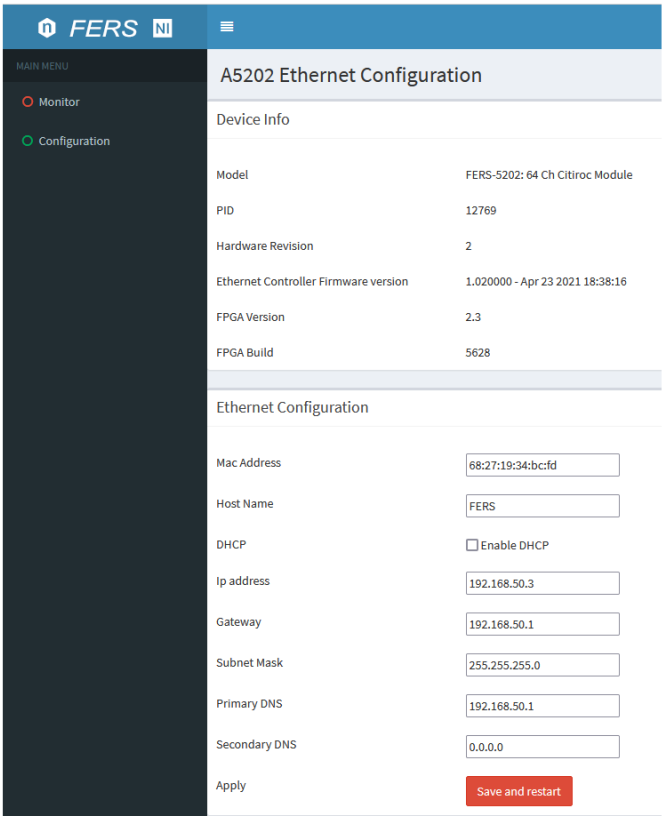


Fig. 10.8: Configuration Tab of the Web Interface for Ethernet settings.

10.2.2 Micro USB Connection to the PC

In order to establish a micro USB connection between the board and the PC, the user should follow the instructions below (Windows only):

1. Download from the A5202/DT5202 website the required USB driver folder according to the user PC platform and unzip it.
2. Connect the micro USB cable from the A5202/DT5202 to the PC and power on the device. At this stage, the A5202/DT5202 is not yet recognized by the OS.
3. From the ”Device Manager” window, right click on the ”Simple WinUSB Device Demo” item in the ”Other devices” list (see Fig. **10.9**) and select the ”Upgrade Driver” option.

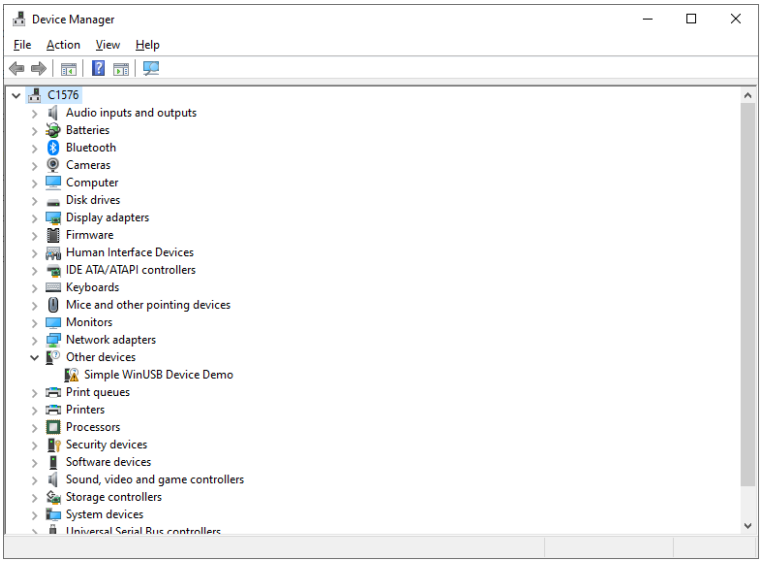


Fig. 10.9: Device Manager window with the USB driver not yet installed.

4. Select ”Browse my computer for drivers” (see Fig. **10.10**).

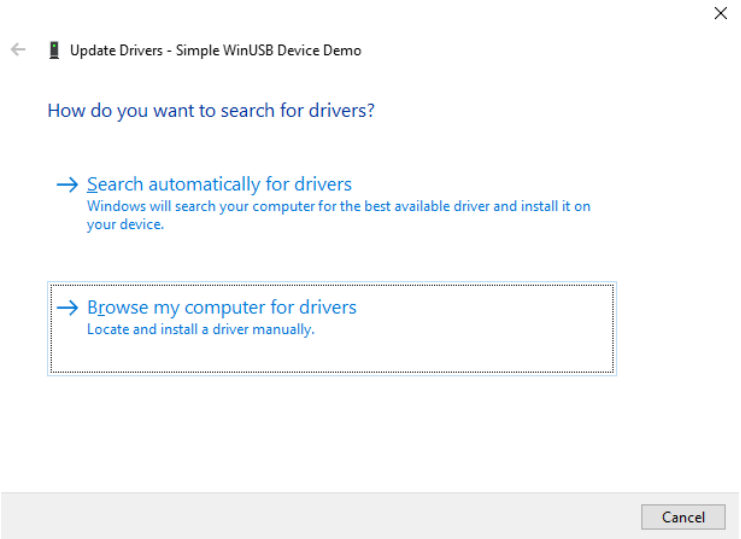


Fig. 10.10: ”Update Drivers” window.

5. Point the driver folder in the PC destination path through the ”Browse…” button and check ”Include subfolders” (see Fig. **10.11**).

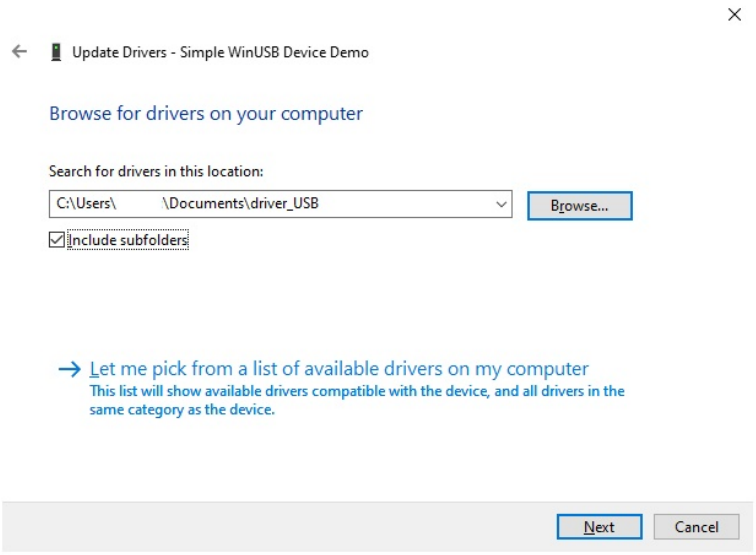


Fig. 10.11: ”Update Drivers” window including path to the USB driver.

6. Windows informs the driver software is successfully installed (see Fig. **10.12**).

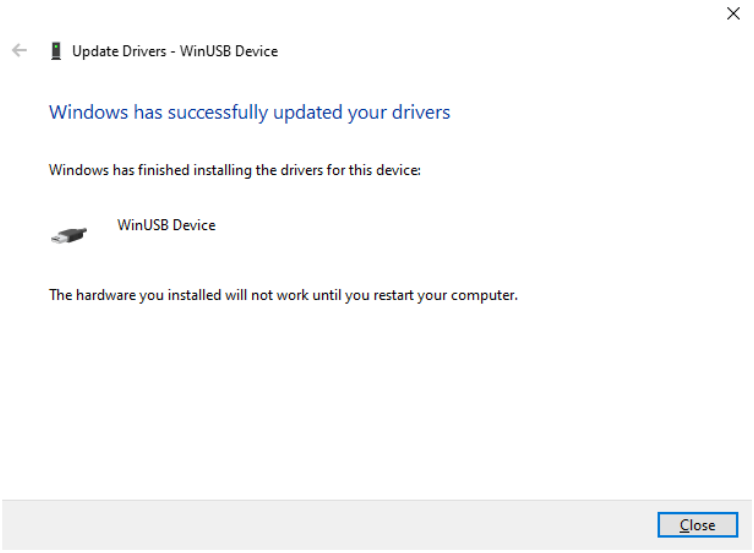


Fig. 10.12: USB driver installation completed.

7. The device is recognized by the operating system and listed in the ”Device Manager” window among ”Custom USB Devices” (see Fig. **10.13**).

Note: The micro USB connection cannot be used to access the Web Interface. Please, use the Ethernet connection.

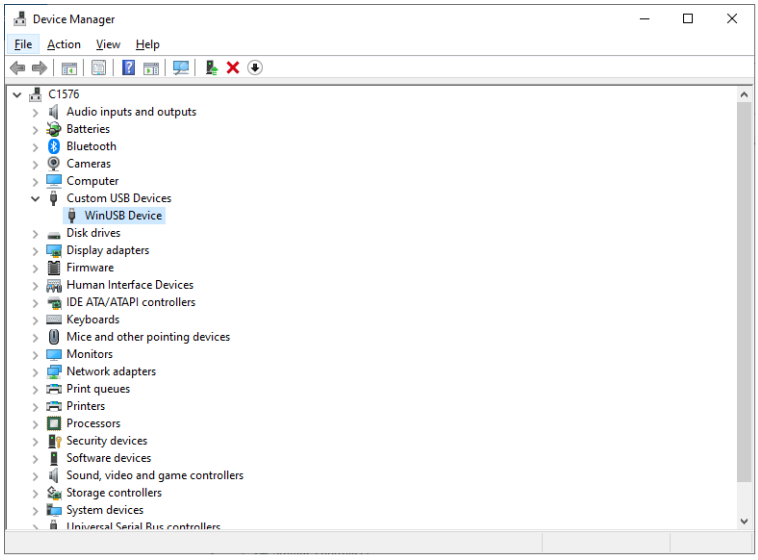


Fig. 10.13: USB device correctly recognized.

10.3 Software Installation

The A5202/DT5202 is fully supported by the Janus software for Windows®and Linux®.

Janus requires the third-party software Python release 3.8.1 or later, downloadable from the python website. Before installing the software, please make sure that:

- The A5202/DT5202 hardware is properly installed (refer to Sec. **10.1**).
- The A5202/DT5202 connection is properly set. (see Sec. **10.2**).
- The required USB driver (Windows only) is correctly installed in case of a USB connection to the board (refer to Sec. 10.2.2).

10.3.1 Windows Installation

Janus does not have an installer. It is provided by CAEN as a compressed ".zip" file to be unpacked in a directory on the PC that the user has write access to. A detailed description of the Janus software structure can be found in the Janus User Manual **[RD3]**. The user should follow the instructions below in order to properly run the software:

1. Download the Janus software from CAEN website for Windows OS (login required).
2. Extract the files and enter the "bin" folder (see Fig. **10.14**) inside the Janus software folder.

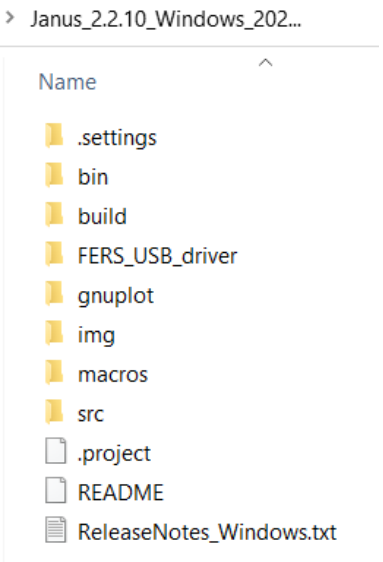


Fig. 10.14: View of the Janus software folder.

Note: The Janus software can be used in two ways: "Console Mode" and "GUI Mode". In this chapter, the "GUI Mode" will be described. The user should refer to the Janus User Manual **[RD3]** for a more detailed description of the "Console Mode".

3. Double click on the **JanusPy.pyw** executable file. No installation steps will be required and a window similar to the one in Fig. **10.15** will be opened. The connection between the software and the board is not yet established.

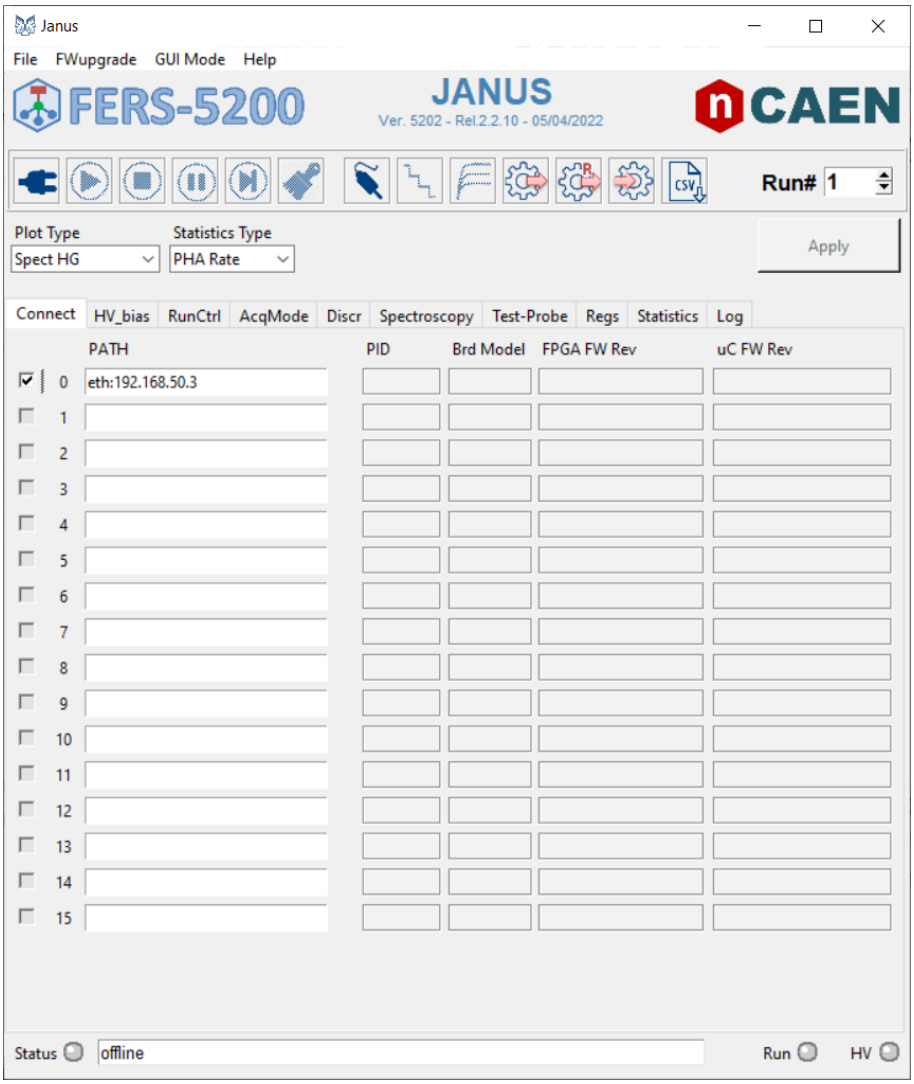


Fig. 10.15: Starting window of the Janus software GUI.

Note: The screenshots reported in this chapter may change between different versions of the software.

10.3.2 Linux Installation

Janus for Linux is provided by CAEN as a compressed ".tar.gz" file to be unpacked in a directory on the PC that the user has write access to. A detailed description of the Janus software structure can be found in the Janus User Manual **[RD3]**. The user should follow the instructions below in order to properly run the software:

1. Download the Janus software from CAEN website for Linux OS (login required).
2. Extract the files in folder with read/write permission and enter the "Janus" folder.
3. Run
   `sudo sh Janus_Install.sh`
4. The script will search for missing package. If any is found, please, install it and run again the Janus_Install.sh file.
5. Once completed, go into the folder "bin" and run

`python3 JanusPy.pyw` for GUI mode or
`./JanusC` for console mode

10.3.3 First Connection

1. Below the ”PATH” field in the Connect tab the user has to write down the type of connection he/she is using to connect to the board. In case of a single board the available options are:
   - ”usb:0” in case of an USB connection. It is also possible to use the syntax ”usb:PID”, being PID the unique board identification number that is located either on the bottom of the A5202 PCB or on the front panel of the DT5202.
   - ”eth:192.168.50.3” (as it is shown in Fig. **10.15**) or another Ethernet address in case this was changed (see Sec. **10.2.1**).

Note: For the instructions necessary to perform a multi-board connection via Ethernet or USB, the user should refer to the Janus User Manual **[RD3]**.

2. Press on the Apply button in order to make the changes effective.

Note: Every time a change in the parameter settings is performed, the Apply button becomes red. The user has to press the button in order to make the changes efffective.

3. Click on the Connect button on the top left part of the Janus window .
   The connection between the software and the board is established and the *gnuplot* graphic interface is opened as in Fig. **10.16**.

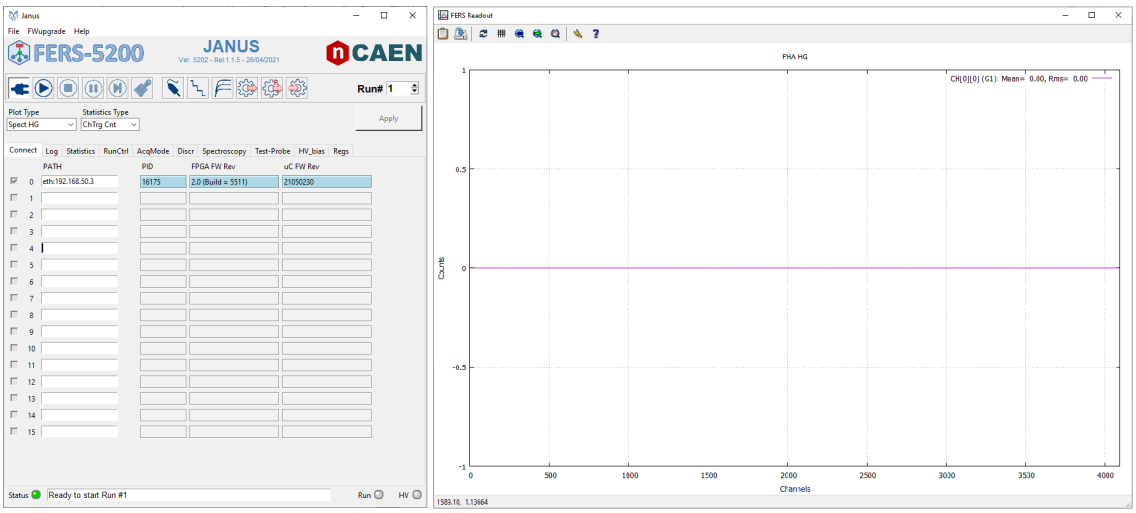


Fig. 10.16: Janus GUI starting interface when the connection is correctly established.

Note: In case the connection is not established, an error message will be displayed in the status bar in the bottom part of the Janus GUI as in Fig. **10.17**. In this case, the user is kindly suggested to re-check all the instructions in Sec. **10.2**.

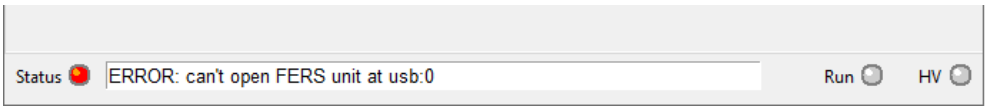


Fig. 10.17: Message displayed in the Janus application in case of a not working USB connection.

10.3.4 GUI mode selection

The user has the possibility to select a simpler or advanced view of the Janus GUI by selecting the corresponding option from "Gui Mode" menu. The "Basic" view is recommended for beginner users to see just the fundamental settings.

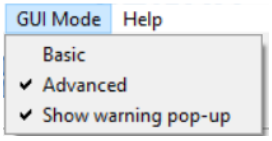


Fig. 10.18: GUI Mode menu to choose between Basic/Advanced GUI visualization mode.

10.4 Test with the Internal Pulser

In this section, the instructions necessary to start testing the A5202/DT5202 board with the internal pulser are reported (see Sec. **8.1.4**). This approach is particularly suggested to the user in order to start getting familiar with the board working principles.
The user should then:

1. Click on the Test-Probe tab of the Janus window.
2. Select the "PTRG" option under the "Test Pulse Source" field. This option allows the user to test the board channels with the internal periodic pulser of the board.
3. Select a value different from 0 for the "Test Pulse Amplitude" parameter. A value of 300 was selected for the presented example. Indeed, the source signal defined by the "Test Pulse Source" parameter only determines the time stamp of the test pulses.
4. Select for the "Test Pulse Ch Selection" the channels to which the pulse has to be transmitted.

Note: WeeROC **[RD1]** suggests to test one channel at a time in order to reduce the noise due to cross-talk effects between channels of the same Citiroc-1A chip.

5. Select which Citiroc-1A Preamplifiers (LG or HG) is used for the "Test Pulse Preamplifier" parameter. For the test described in this section the same settings as those in Fig. **10.19** are applied.
6. Click on the AcqMode tab of the Janus GUI (see Fig. **10.20**). The user can vary the period of the internal periodic pulse by writing down for the "Periodic Trigger Period" parameter a value between "16 ns" and "34 s". In this example a value of "1 ms" was chosen.
7. Connect the T0-OUT or T1-OUT LEMO connector to an oscilloscope.
8. Click on the AcqMode tab and select for the "T0-OUT" or "T1-OUT" parameter (depending on which one was previously connected to the oscilloscope) the "PTRG" option.
9. Press the Apply button. A LVTTL signal having the same frequency of the A5202/DT5202 internal periodic signal should be visualized at the oscilloscope (see Fig. **10.21**).

With the signal generated in this section the user can now start testing the various acquisition modes of the board.

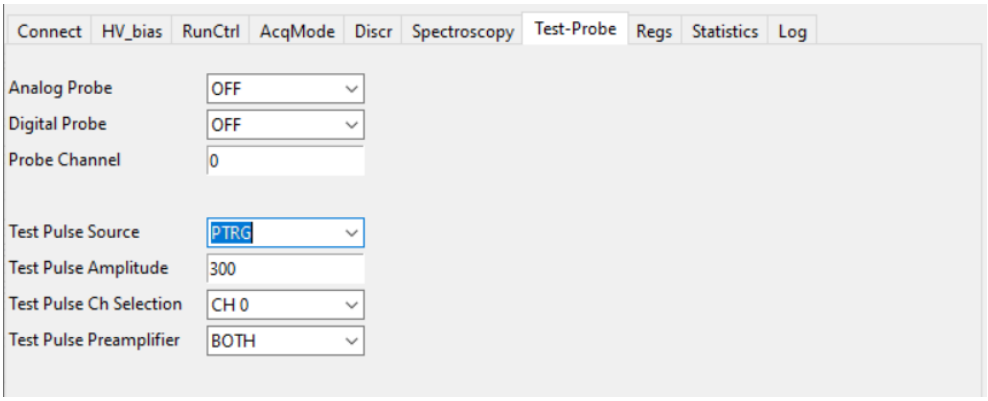


Fig. 10.19: Settings to test the board with the internal periodic pulser.

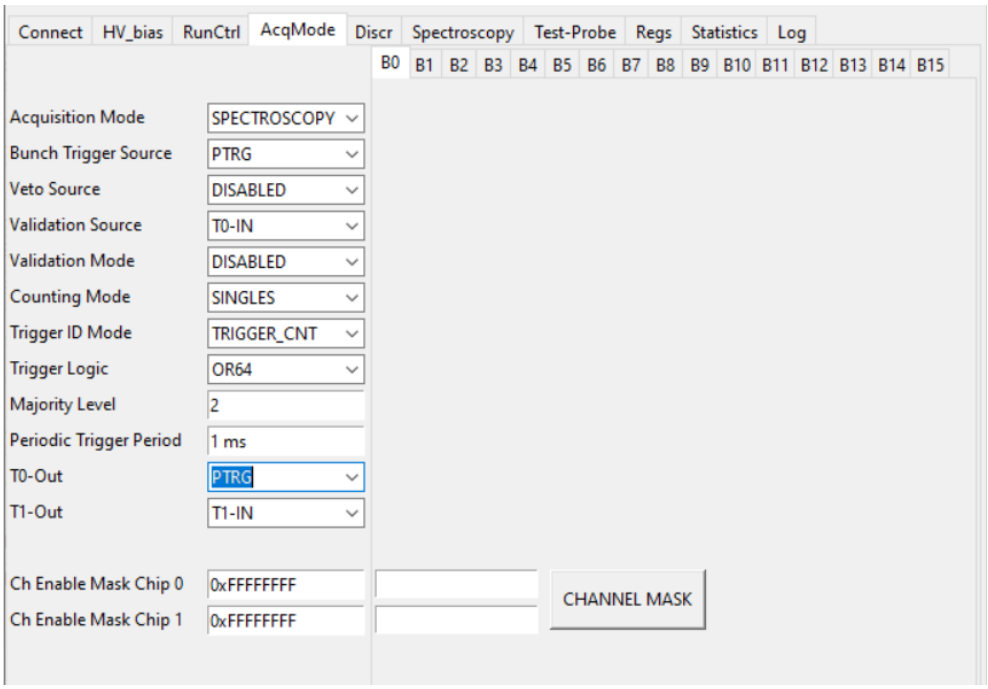


Fig. 10.20: AcqMode tab of the Janus GUI.

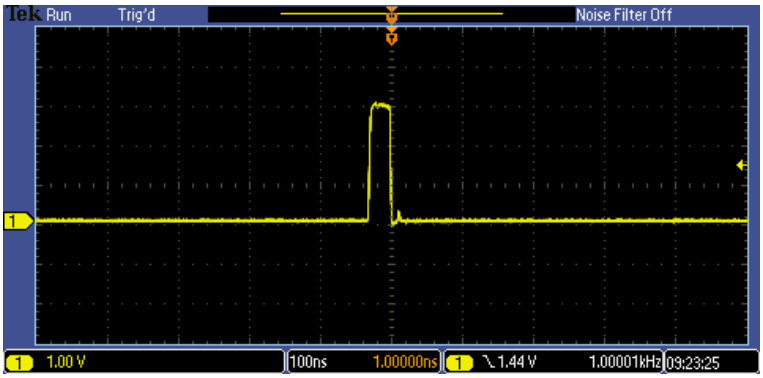


Fig. 10.21: A5202/DT5202 internal periodic signal at the oscilloscope.

10.4.1 Test in Spectroscopy Mode

In this operating mode, the A5202/DT5202 board works with a global (bunch) trigger, either internal, coming from an external source or generated by a combination of the channel self-triggers. As soon as a trigger is issued, all channels start simultaneously the A/D conversion of the pulse height amplitude and create a data packet containing the common trigger time stamp followed by the individual energies. To perform a spectroscopic acquisition with the internal pulser, the user should then:

1. Click on the AcqMode tab. Select the ”SPECTROSCOPY” option for the ”Acquisition Mode” parameter.
2. Select the ”PTRG” option for the ”Bunch Trigger Source” parameter. The internal periodic signal will then be used both to pulse the board channel and to force the triggers, i.e. the acquisition of the pulse height values. The user can refer to Fig. **10.20** in order to see the settings chosen for the test.
3. Click on the Spectroscopy tab (see Fig. **10.22**). The user can now choose from which Citiroc-1A amplification chain (LG or HG) the pulse height values have to be A/D converted and saved to the data packet by selecting the proper option of the ”Gain Selection” parameter. In particular, the available options are:
   - HIGH: The A/D converted pulse height values from the HG amplification chain are saved.
   - LOW: The A/D converted pulse height values from the LG amplification chain are saved.
   - AUTO: By default, the pulse height values saved are those from the HG amplification chain if they do not saturate the dynamic range. In that case, the pulse height values from the LG amplification chain are saved.
   - BOTH: The A/D converted values from both amplification chains are saved.

   In the described example, the ”BOTH” option was chosen.

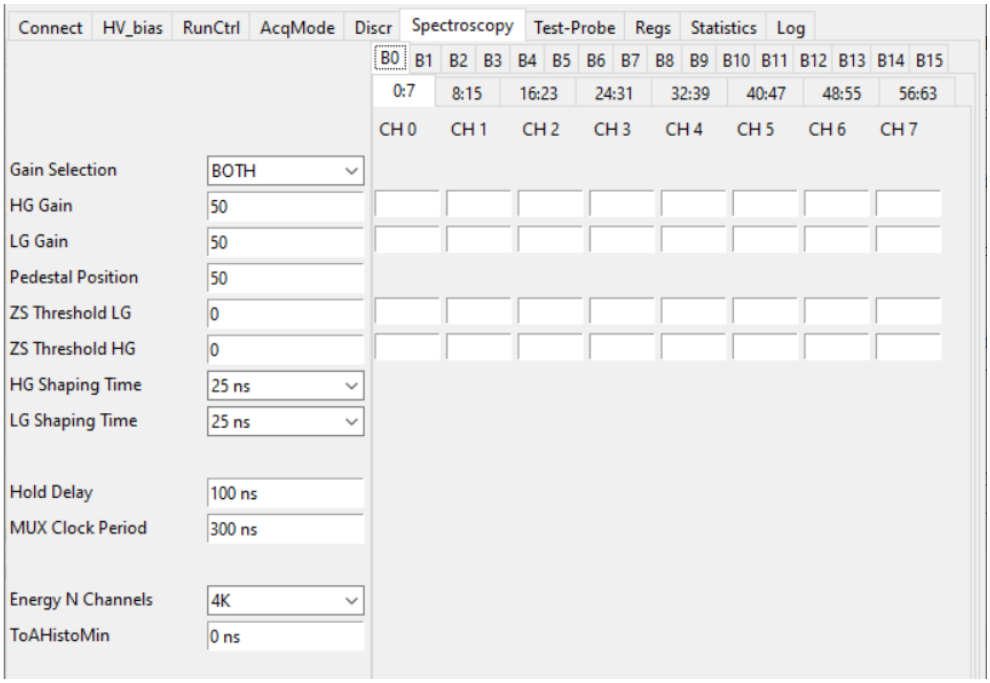


Fig. 10.22: Spectroscopy tab of the Janus GUI.

4. Select a value between 0 and 63 for the ”HG Gain” or the ”LG Gain” parameters depending on the value selected for the ”Gain Selection” parameter. A value of 50 was set for both parameters in the described example.
5. Select a value of at least 200 ns for the ”Hold Delay” parameter.
6. Press the Apply button.

7. Click on the ”Plot Type” parameter on the Command bar in the top part of the Janus GUI (see Fig. **10.23**) and select ”Spect HG” or ”Spect LG” in order to visualize the pulse height spectra from the HG or LG amplification chain in the *gnuplot* window.

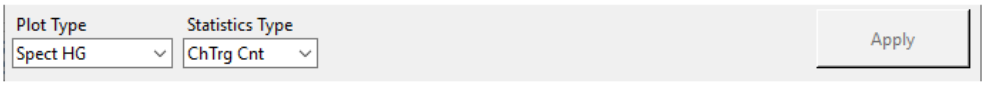


Fig. 10.23: The Command bar with the ”Spect HG” option selected for the ”PlotType” parameter.

8. Press the ”Plot Traces” button . A window similar to that in Fig. **10.24** is opened. The window allows the user to choose between the different traces that can be visualized in the same *gnuplot* window.

Fig. 10.24: Plot Traces window.

9. Press ”T1”. The command allows to select one channel (from 0 to 63) to be visualized as the 1st trace in the *gnuplot* window. Up to 8 traces from different channels can be visualized at the same time in the *gnuplot* window by pressing the T1, ..., T8 buttons and selecting the needed channels. More information about the *gnuplot* window settings can be found in the Janus User Manual **[RD3]**.
In this example, only the T1 trace was enabled and associated to the channel that was previously selected for the ”Test Pulse Ch Selection” parameter.
10. Press the Start button . A plot similar to that in Fig. **10.25** will be visualized for the HG pulse height spectrum.
11. The user can now vary the ”HG Gain” or the ”Test Pulse Amplitude” values in order to change the peak position.

Note: In case the option ”LOW” is set for the ”Gain Selection” parameter, the HG PHA spectrum will be empty (and vice-versa).

12. By selecting ”PHA Rate” for the ”Statistics Type” parameter of the Janus Command bar, the values of the frequency at which each channel pulse height values are sampled and converted can be visualized. The values are displayed in the ”Statistics” window of the Janus software together with other information regarding the ongoing acquisition run (see Fig. **10.26**). By selecting ”PHA Cnt”, the trigger counted since the start of the acquisition are displayed.

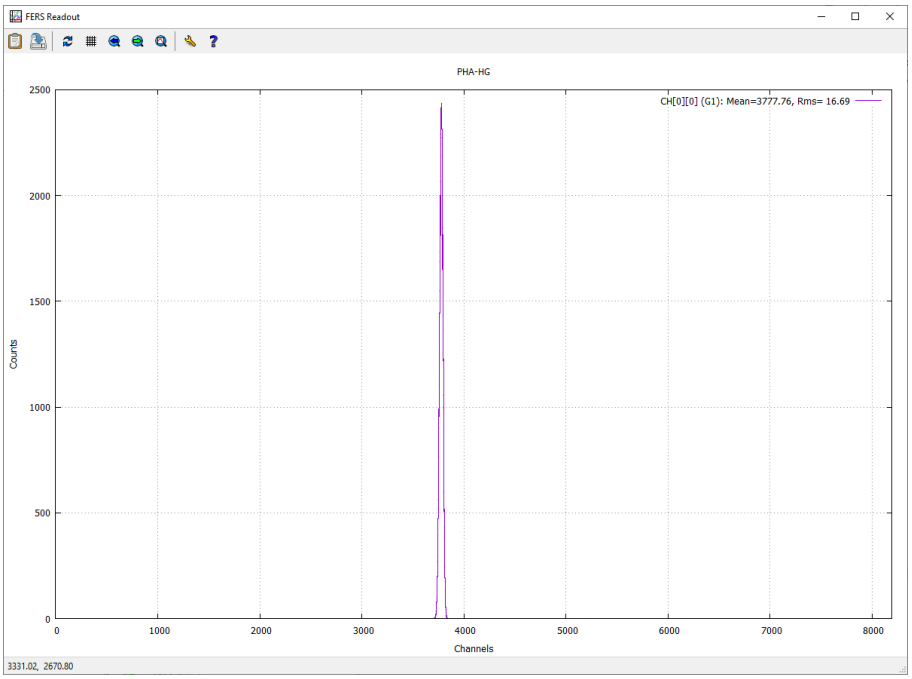


Fig. 10.25: Example of PHA spectrum obtained with the internal test pulser.

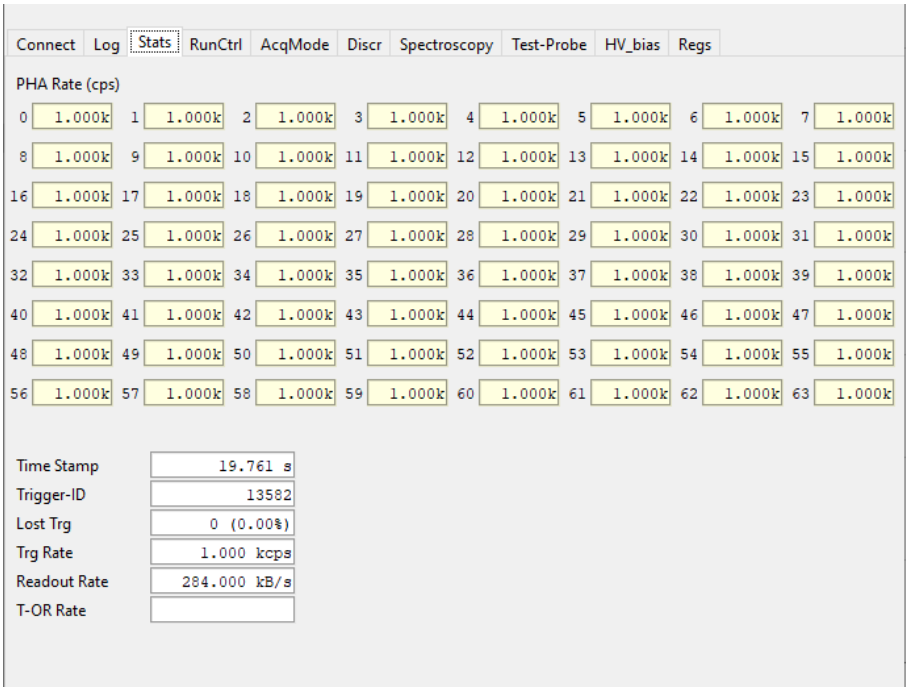


Fig. 10.26: The Stats tab of the Janus software GUI.

13. If the user may need to reset the values on the histograms, the Reset button has to be pressed .
14. Press the Pause button in order to freeze the plot update .
15. Press the Stop button in order to stop the acquisition .

10.4.2 Test in Timing Mode

When operating in Timing Mode, all channels acquire independently. For each TD self-trigger, the FPGA saves the channel ID (0 to 63) and the time stamp of the hit into the local memory buffer. The ToT information is also saved which gives a rough estimation of the pulse amplitude (energy).
Two timing modes are available:

- **Common Start Gating**: a time reference signal (T_{ref}) opens an acquisition window of programmable size and only the hits occurring during that acquisition window are saved in the data packet.
- **Common Stop Gating**: the concept is the same of the common start gating, but the time reference signal closes the acquisition window, i.e. the hits occurring before the arrival of the time reference signal are saved.

The instructions below allows the user to perform an acquisition in Timing Mode with the A5202/DT5202 board using the internal pulser:

1. Choose between ”TIMING_CSTART”, ”TIMING_CSTOP” for the ”Acquisition Mode” parameter in the AcqMode tab. The ”TIMING_CSTART” has to be chosen when using the internal test pulser.
2. Set via the ”Tref Source” parameter the proper time reference signal opening (or closing) the gating acquisition window. In this example, the ”PTRG” was chosen to define the time reference signal.
3. Set the value for the ”Tref Window” parameter in the AcqMode tab. This parameter defines the length of the gate whose start is defined by the T_{ref} signal (Common Start Gating) or whose stop is defined by the T_{ref} signal (Common Stop Gating). A value of 1 µs was chosen for this example (see Fig. **10.27**).

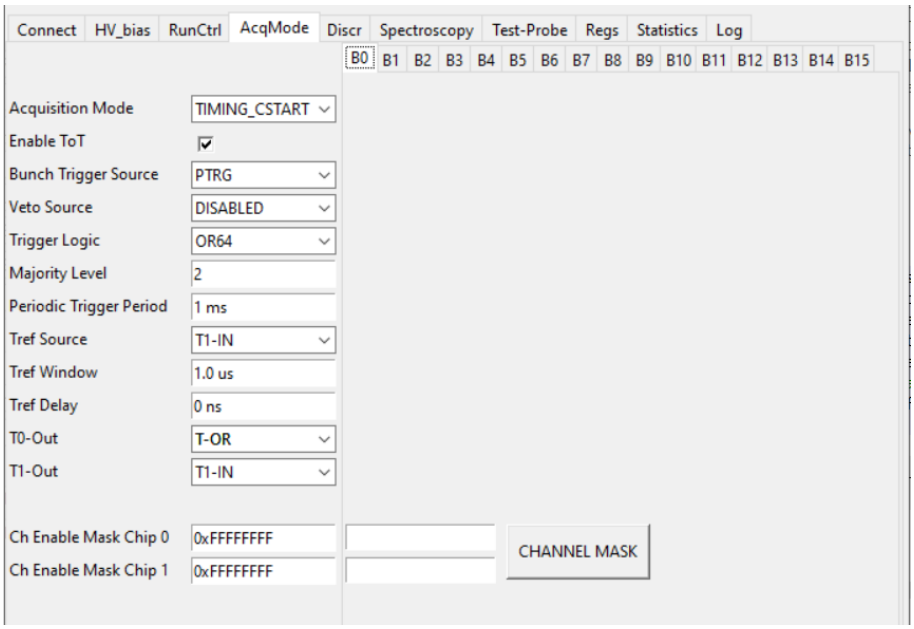


Fig. 10.27: The AcqMode tab with the settings chosen to test the board in Timing Mode.

4. Select the Discr tab (see Fig. **10.28**). This tab allows the user to set the values of the channel self-trigger thresholds. For each channel, a hit is saved if the output of the Fast Shaper exceeds a certain threshold in the TD chain. The user should then set for the ”TD Coarse Threshold” parameter a proper value for the channel self-trigger thresholds. In this example, a value of 300 was set for the ”TD Coarse Threshold” parameter.
5. Select for the ”Fast Shaper Input” parameter which Preamplifier signal (HG or LG) has to be fed into the Fast Shaper of each channel. In this example, the ”LG-PA” option was selected (see Fig. **10.28**).

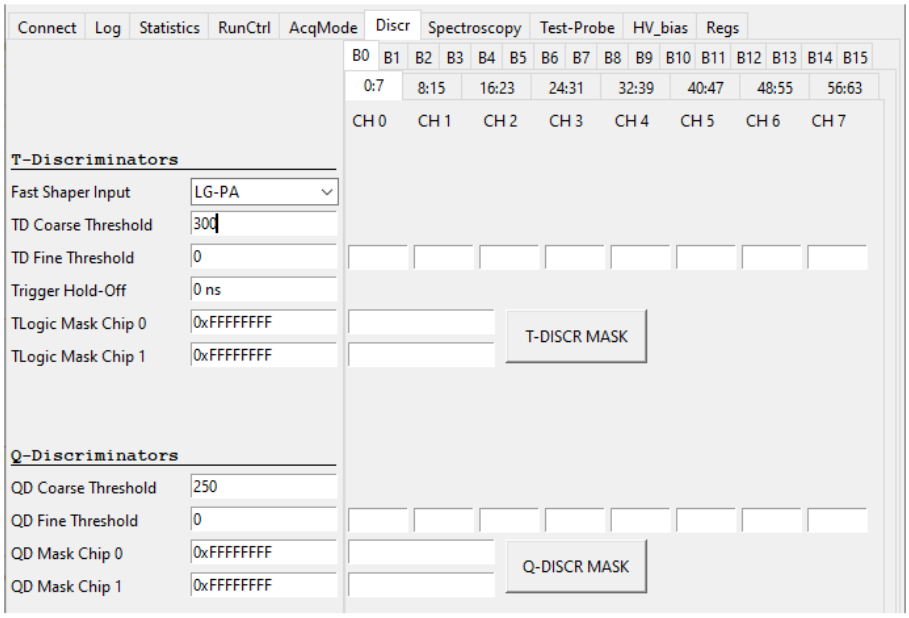


Fig. 10.28: The Discr tab of the Janus GUI.

6. Select ”Spec ToA” for the ”Plot Type” command in order to visualize the histogram of the ΔT values (the so called Time of Arrival) between the T_{ref} signal and the channel TD self-triggers.
7. Put a thick on the ”Calib X-axis” parameter of the Janus Plot Traces window (see Fig. **10.24**) in order to convert the X axis scale from Channels to ns.
8. Press the Start button. A spectrum similar to that in Fig. **10.29** will be displayed.

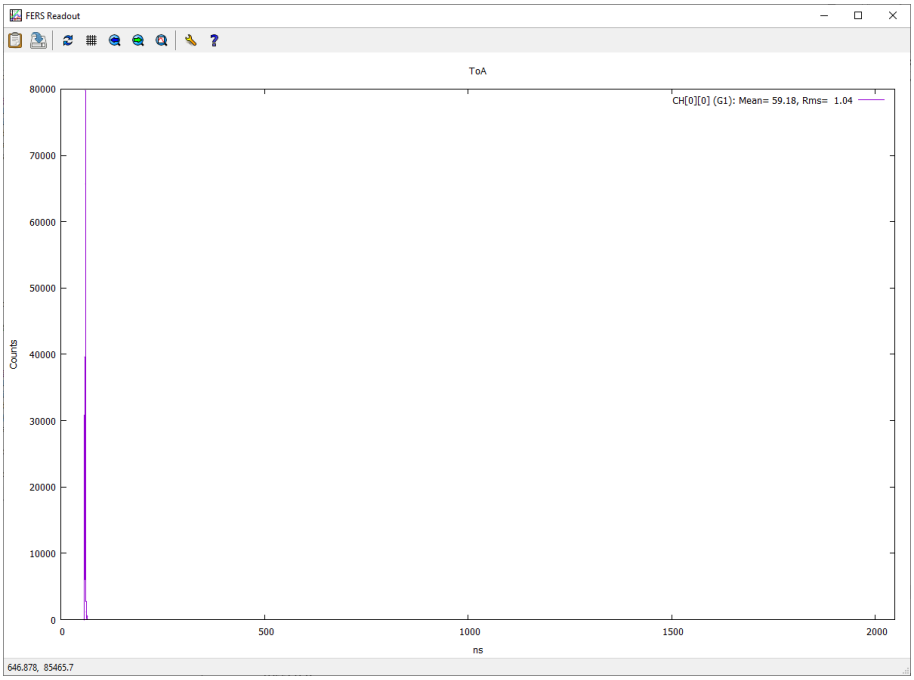


Fig. 10.29: Example of Time of Arrival (ToA) spectrum obtained with the internal pulser.

9. Select ”Tstamp Rate” for the ”StatsType” parameter in the Janus Command Bar. The time stamp rate of the channel TD self-triggers are visualized in the Stats tab (see Fig. **10.30**). By selecting ”Tstamp

Cnt" the number of time stamps counted since the start of the acquisition are instead visualized.

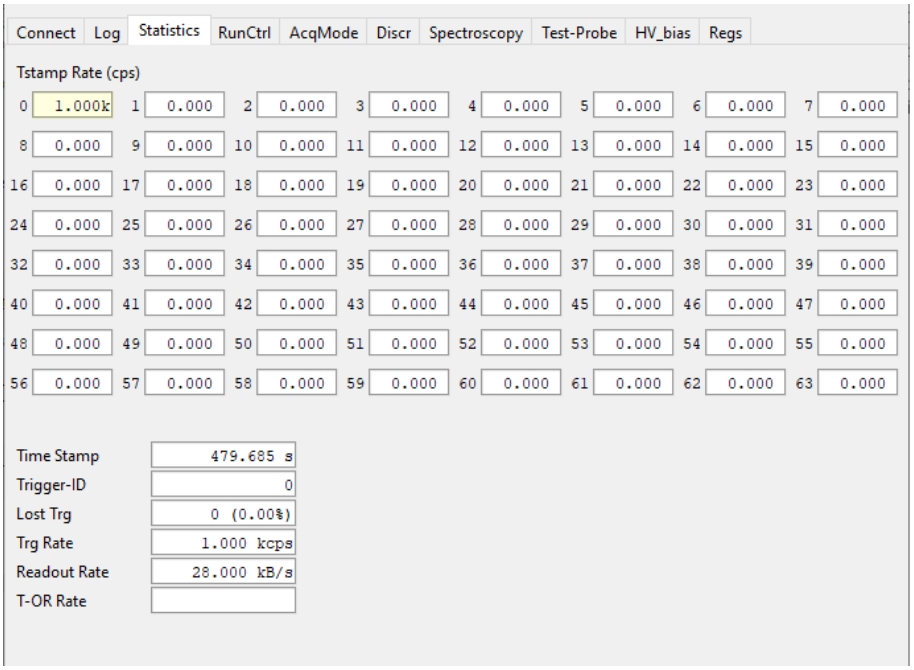


Fig. 10.30: The Stats tab of the Janus GUI with visualized the time stamp rate.

10. Select "Spec ToT" for the "Plot Type" parameter in order to visualize the histogram of the ToT values for the selected channel. An histogram similar to that in Fig. **10.31** will be displayed.

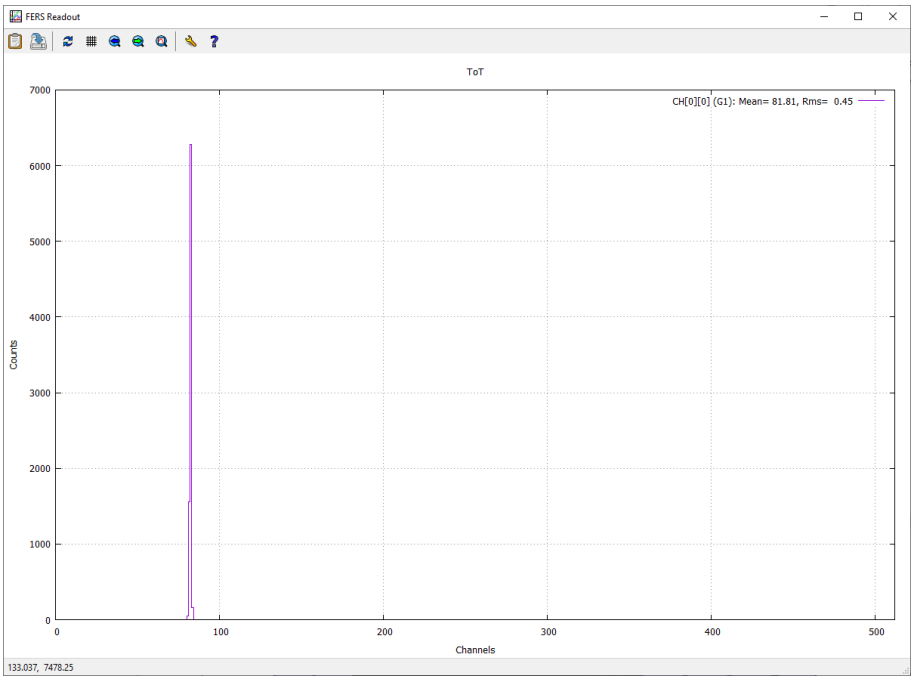


Fig. 10.31: Example of Time over Threshold (ToT) spectrum obtained with the internal pulser.

11. The user can vary the "Test Pulse Ch Selection" or the "TD Coarse Threshold" in order to change the peak position of the ToT spectrum.

10.4.3 Test in Counting Mode

In this operating mode, the self-triggers of each channel are individually counted. The counting intervals are defined by an internal periodic gate with programmable width or by an external signal. At the end of each counting interval, the counters are latched and saved in a data packet. The following instructions will guide the user to perform an acquisition in Counting Mode only using the A5202 board:

Note: The maximum rate of the counters for the Citiroc-1A is 20 Mcps.

1. Set ”COUNTING” for the ”Acquisition Mode” parameter in the AcqMode tab of the Janus GUI.
2. The counting intervals (or slots) are defined by the ”Bunch Trigger Source” parameter. In this example, the ”PTRG” option is chosen to define the counting intervals (with 1 ms period) as showed in Fig. **10.32**.

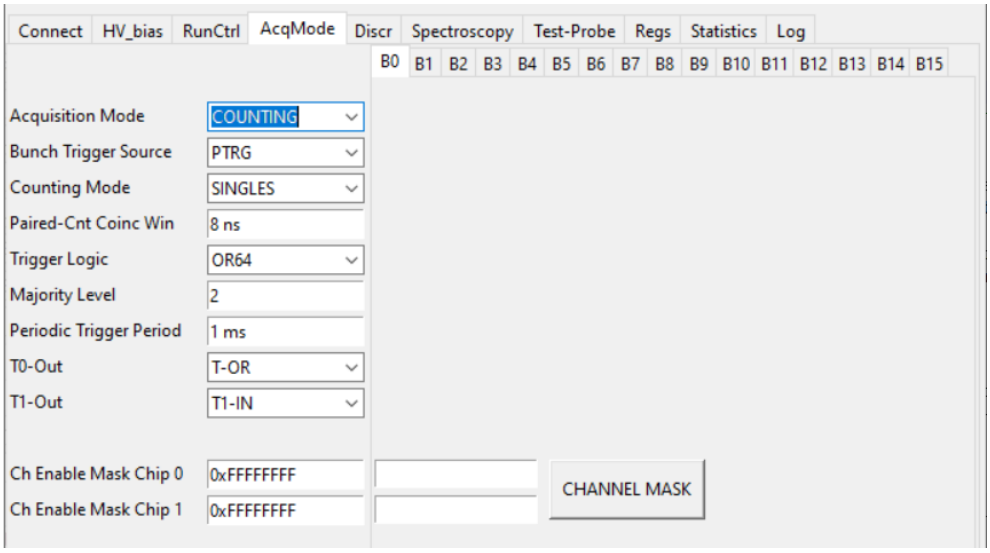


Fig. 10.32: The AcqMode tab with the settings used to perform a test in Counting Mode.

Note: The ”Bunch Trigger Source” parameter only defines the width of the counting intervals in this acquisition mode. The single channel countings are defined by the TD self-triggers.

3. Connect the Test Input (see Fig. **7.4**) to the T1-OUT connector.
4. Select the ”DPROBE” option for the ”T1-OUT” parameter in the AcqMode tab.
5. Select the Test-Probe tab. For the ”Digital Probe” parameter the user has to select the ”CLK_1024” option. The digital probe is now associated to an internal clock signal with a frequency of $\sim$ 61 kHz (the user can check at the oscilloscope).
6. Select the ”EXT” option for the ”Test Pulse Source” parameter.
7. Set the value of the channel TD self-trigger thresholds in the Discr tab. See Sec. **10.4.2** for more details regarding the settings chosen.
8. Select ”TrgRate-Ch” for the ”Plot Type” command in order to visualize the histogram of each channel self-trigger frequency (cps).
9. Press the Start button. A plot similar to that in Fig. **10.33** will be visualized.
10. Select the ”ChTrg Rate” option for the ”Stats Type” command. The channel self-trigger rates (from the TD lines) are visualized in the Stats tab.

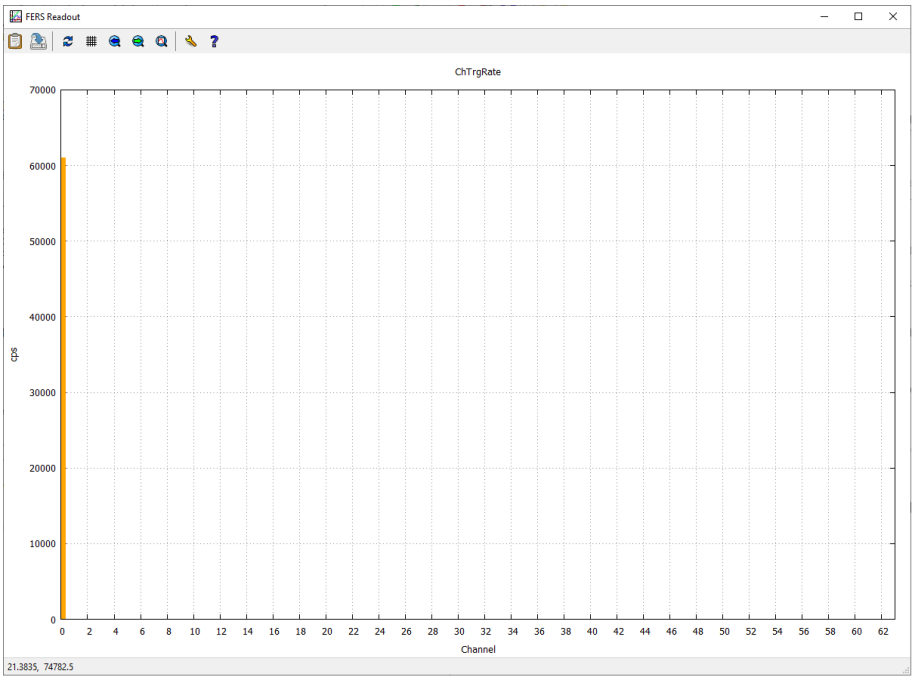


Fig. 10.33: Example of counting spectrum obtained with the internal clock.

10.5 Hardware Setup: Testing a SiPM Matrix

After having presented the working principle of the A5202/DT5202 board and of the Janus software, a more practical example of application of the board is presented in the following sections. More precisely, the example described in this guide is a typical application of the use of a single A5202 unit and of the Janus software for the characterization of SiPM detector response to light pulses. The high voltages for the SiPMs are provided by the A5202, which integrates in a single unit both the HV power supply (A7585D) and 64 readout channels.
The SiPM matrix used to perform this test is an 8×8 Hamamatsu S13361-3050AE-08 SiPM matrix **[RD5]**. The SiPM matrix was connected to the A5251 FERS-5200 header adapter **[RD4]** and then to an A5202 board. The CAEN SP5601 LED driver **[RD6]** was used to send a light signal to the SiPM matrix.
A schematic view of the hardware setup is shown on Fig. **10.34**.

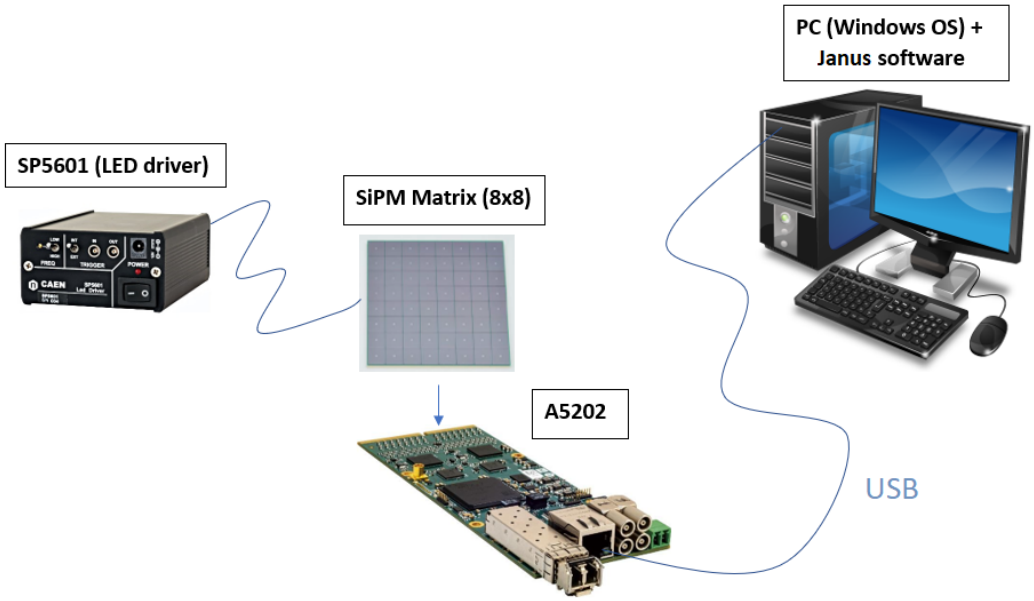


Fig. 10.34: Hardware setup for the characterization of an 8×8 SiPM matrix (Hamamatsu S13361-3050AE-08) response to LED pulses.

Note: In order to properly connect the SiPM matrix, the steps below were followed:

1. Connected the SiPM matrix to the A5251 header adapter.
2. Connected the A5251 header adapter to the A5202 board.
3. Connected the A5202/DT5202 board to the DC input.
4. Connected the A5202/DT5202 board to the PC.

We recommend the user to follow these passages in order to properly connect the detector to the readout board.

10.6 HV Management

In order to properly manage the HV, the user should follow the instructions below:

1. Once the connection between the board and the software is established (see Sec. **10.3**), the user has to select the ”HV_bias” tab of the Janus software. A graphic interface similar to that in Fig. **10.35** will be opened.

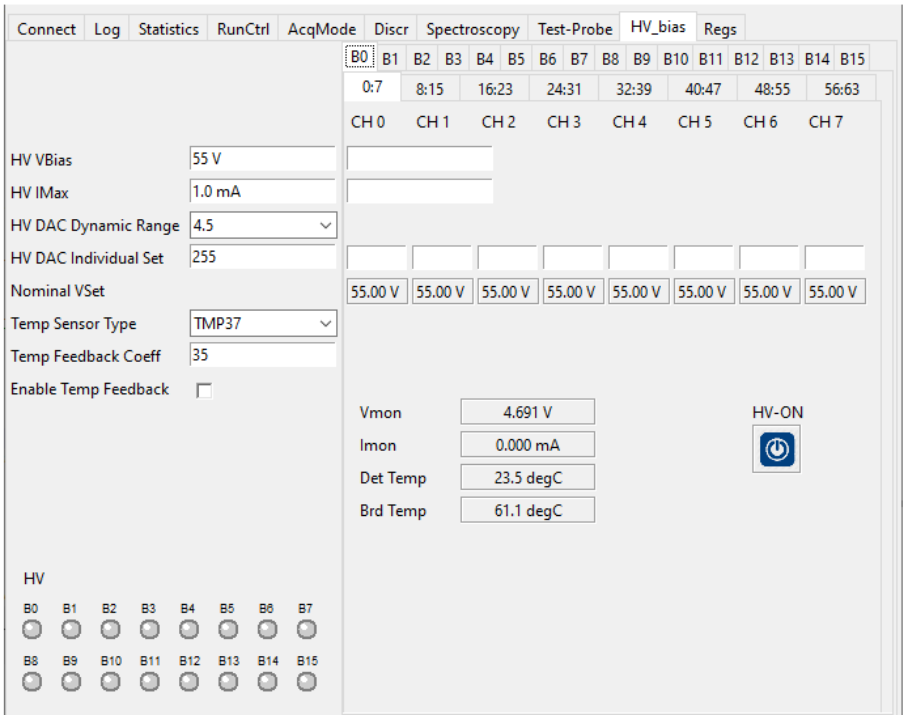


Fig. 10.35: The HV_bias tab of the Janus software.

2. Choose the value for:

   - ”HV Vbias”: set the bias voltage value provided by the A7585D to all channels.
   - ”HV IMax”: set the maximum output current from the HV power supply.
   - ”HV DAC Dynamic Range”: set the dynamic range value (options are ”2.5” V, ”4.5” V or DISABLED) for the channel-by-channel HV adjustment provided by the internal Citiroc-1A DACs.
   - ”HV DAC Individual Set”: set the value (expressed in LSB, from 0 to 255) for the channel-by-channel HV adjustment. The value 255 corresponds to the minimum value provided by the DAC, i.e. 0 V, while the 0 value corresponds to the maximum value. The maximum value can be 2.5 V or 4.2 V depending on the dynamic range set via the ”HV DAC Dynamic Range” parameter. Refer to Sec. **9.1.1** for more details.

3. The ”Vnom” parameter shows the total value (i.e. the combination of the common HV bias and of the individual one given by the internal DAC) of the HV provided to each channel.
4. Click on the Apply button. The HV settings are now defined.

Note: By pressing the Apply button the HV are not yet turned on.

5. Click on the ”HV-ON” button on the top left corner of the HV_bias tab . The HV will start the ramp up.

Note: **When the DAC is disabled (by acting on the ”HV DAC Dynamic Range”) the default value for the tension provided by the DAC is measured to be 4.5 V.**

6. Monitor the values of the voltage (”Vmon”) and current (”Imon”) provided by the A7585D power supply.

Note: The Vmon value is the value of the common HV provided by the A7585D module to all channels. The Vmon value does not take into account the value of the HV provided by each channel internal DACs.

Note: The HV remains ON even if the communication between the software and the board is interrupted (e.g. if the software is closed unexpectedly).

7. In order to turn off the HV the user has to click on the ”HV-ON” button again .

10.7 Before Starting

10.7.1 Checking the Citiroc-1A Outputs

Before starting the acquisition the user can check the output signals of the most relevant stages of the Citiroc-1A chip. Once the HV are turned on, the user can connect a LED pulser (the CAEN SP5601 in the presented example) or any light source to the SiPM and turn it on.

Note: The SiPMs are very sensitive to environmental light. We recommend the user to cover the SiPM matrix with a light absorbing material in order to protect the detector as much as possible from any light source different from the test one.

Then the user should:

1. Click on the Test-Probe tab of the Janus software GUI (see Fig. **10.19**).
2. Choose the Citiroc-1A channel to which the analog probe has to be connected by writing down a number (from 0 to 63) for the ”Probe Channel” parameter.
3. Power off any other test pulse directed to any channel by selecting the ”OFF” option for the ”Test Pulse Source” parameter.
4. Connect the A5202 MCX Probe 1 (in case the selected channel is between 0 and 31, Probe 2 otherwise) to an oscilloscope.
5. Connect the LED driver trigger to an oscilloscope and trigger on that signal.
6. Select the ”PREAMP_HG” option for the ”Analog Probe” parameter and press the Apply button. The output is the **negative** polarity signal from the Citiroc-1A HG Preamplifier of the selected channel and should be similar to the one shown in Fig. **10.36**.

Note: The activation of the Citiroc-1A analog probe may cause a small variation of the gain. The user is recommended to disable the analog probe (”OFF” option) during physics runs.

Note: Signals from the analog probe could have a significant DC offset. For this reason, the user is recommended to set an AC coupling in the oscilloscope.

Note: The output from the LG Preamplifier (selectable with the option ”PREAMP_LG”) is the same signal from the HG Preamplifier, with 1/10th of the gain.

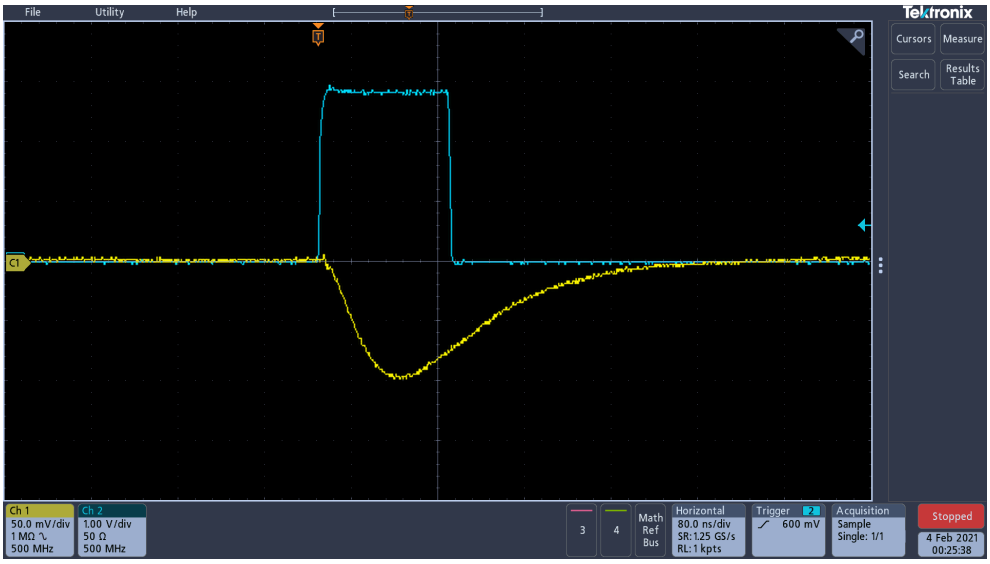


Fig. 10.36: Example of HG Preamplifier output (yellow line) together with the LED driver trigger (blue line).

7. Select the ”SLOW_HG” option for the ”Analog Probe” parameter. The output is the **bipolar** signal from the Citiroc-1A HG Slow Shaper of the selected channel, similar to that shown in Fig. **10.37**. The user is suggested to acquire the time difference between the rising edge of the trigger signal and the peak position of the Slow Shaper signal. The value of this ΔT will give a rough estimation of the minimum value to be set for the ”Hold Delay” parameter in the Spectroscopy tab and to be used during physics run (see Sec. **10.8**).

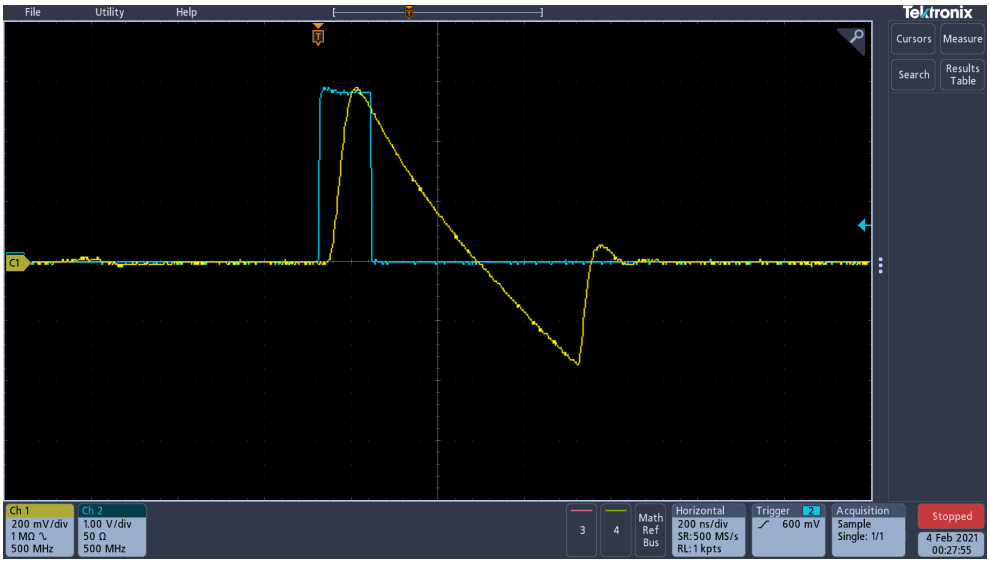


Fig. 10.37: Example of HG Slow Shaper output (yellow line) together with the LED driver trigger (blue line).

8. Select the ”FAST” option for the ”Analog Probe” parameter. The output is the **bipolar** signal from the Citiroc-1A Fast Shaper of the selected channel, similar to that shown in Fig. **10.38**.

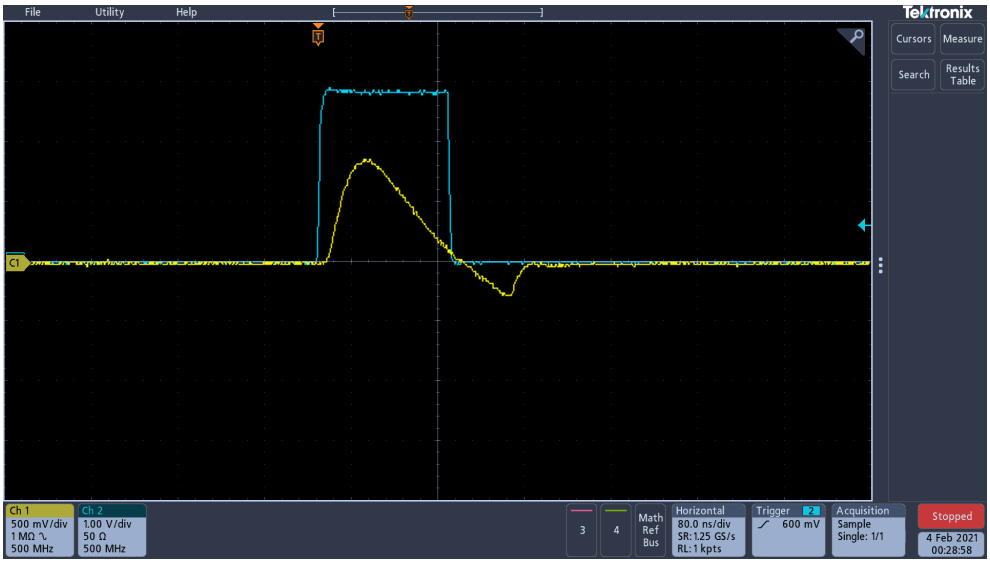


Fig. 10.38: Example of Fast Shaper output (yellow line) together with the trigger (blue line).

10.7.2 Hold Delay Scan

The Janus software allows the user to perform a scan of the ”Hold Delay” values as a function of the values converted by the ADC for each channel. The description of this parameter has been extensively treated in Sec. **8.1.2** and Sec. **9.2.2** and we invite the user to refer to those sections for further details. In order to perform an Hold Delay scan, the user should follow the instructions below:

1. In the AcqMode Tab, select for the ”Acquisition Mode” parameter the SPECTROSCOPY option.
2. For the ”Bunch Trigger Source” parameter, the user should select the trigger source that will be used also during physics acquisitions. For instance, if the user wants to perform a spectroscopic acquisition with an external bunch trigger (e.g. sent via the T1-IN connector as in the presented example), the same trigger source has to be used for the Hold Delay Scan.

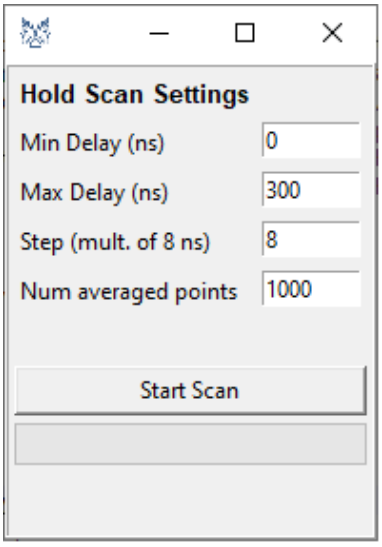


Fig. 10.39: ”Hold Delay Scan” window.

3. Click on the Hold Delay Scan button in the Janus Icon Bar . A window similar to that in Fig. **10.39** will appear and the values of the following parameters should be set by the user:
   - *Min Delay (ns)*: The minimum value for the Hold Delay parameter in the scan (suggested 0).
   - *Max Delay (ns)*: The maximum value for the Hold Delay parameter in the scan.
   - *Step (multipl. of 8) (ns)*: The time distance between two consecutive values of the Hold Delay parameter in the scan expressed in ns. The minimum value is 8, and the scan is sensitive only to values multiples of 8 ns (i.e. the clock period).
   - *Num averaged points*: The number of points, i.e. pulse height values, acquired for each value of the Hold Delay parameter.
4. Click on the Start Scan button and wait for the scan to finish without closing the window.

Note: The scan duration depends on the scan settings chosen and may last up to few minutes.

5. Select for the "Plot Type" command in the Janus Command Bar the "HoldDelay-Scan" option. The visualized plot is that corresponding to the first trace in the "Plot Traces" window.

In Fig. **10.40** an example of a 2D plot from an Hold Delay Scan obtained with the 8×8 Hamamatsu S13361-3050AE-08 SiPM matrix is presented. According to Fig. **10.40**, a value of 100 ns, for instance, for the "Hold Delay" parameter is large enough to guarantee a proper sampling of the pulse height amplitude. For "Hold Delay" parameter values lower than 50 ns, the pulse height value saved to data is lower than the effective peak amplitude.

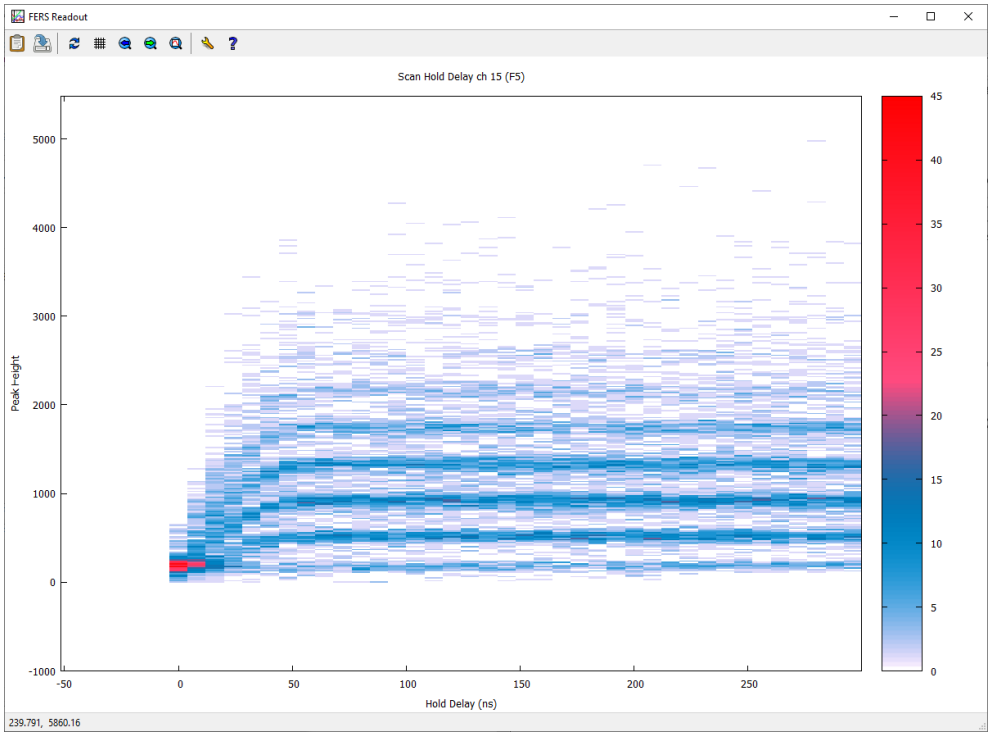


Fig. 10.40: Example of 2D plot from an Hold Delay scan. Each parallel line correspond to a different number of photo-electrons triggered.

10.7.3 Threshold Scan and SiPM Staircase

The Janus software features a tool which is particularly useful to set the proper values of the thresholds in case the channel TD self-trigger logic is used (i.e. in Counting Mode and Timing Mode) as well in case the T-OR, Q-OR or TLOGIC trigger logics are used for acquisitions in Spectroscopy Mode. More precisely, Janus allows the user to acquire the so called "Staircase", i.e. the rate of over threshold events (from the TD line) from each channel as a function of the threshold value ("TD Coarse Threshold" parameter in the Janus software). The instructions necessary to perform the threshold scan are reported below:

1. Power off the LED pulser or any other light test source connected to the SiPMs. Indeed, the SiPM staircase is tipically necessary to asses the Dark Count Rate (DCR) as a function of the threshold, in order to define a proper value of the threshold itself for physics runs.
2. Power on the HV (refer to Sec. **10.6**).
3. Press the "Staircase" button in the Icon bar of the Janus window . A window similar to that in Fig. **10.41** will be opened. The values of the following parameters should be set by the user:

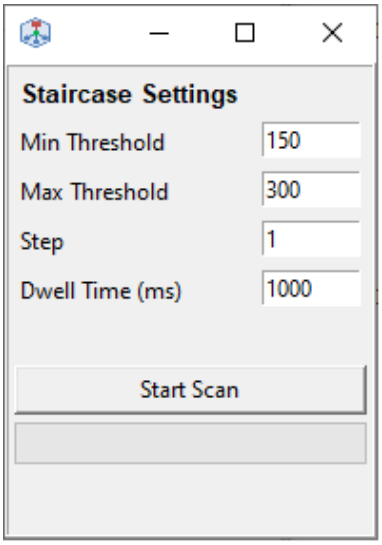


Fig. 10.41: "Staircase Settings" window.

- "Min Threshold": Set the minimum value of the "TD Coarse Threshold" in the scan.
- "Max Threshold": Set the maximum value of the "TD Coarse Threshold" in the scan.

Note: The typical values to be used for the threshold scan ranges from 150 to 500. Indeed, the 0 value of the threshold does not correspond to the baseline level of the signal.

- "Step": Set the step of the scan, i.e. the distance between two consecutive values of the threshold.
- "Dwell Time (ms)": Set the value of the time interval during which the TD self-triggers have to be counted. An example of the settings for a SiPM staircase acquisition are shown in Fig. **10.41**.

Note: The scan may last up to few minutes depending on the values set. However, the higher the value of the counting interval is, the higher the precision on the trigger frequency is achieved.

4. Press the "Start Scan" button without closing the "Staircase Settings" window. A green bar in the bottom of that window will appear, indicating the progress of the scan.
5. Open the Log tab of the software to check the value of the T-OR and Q-OR frequencies as the threshold values change.

6. Once the scan is finished, the ”ScanThr.txt” file is created. The file contains 67 columns. The first one contains the values of the threshold, the following 64 columns contain the cps for each channel TD self-trigger, while the last two columns contain the T-OR and Q-OR cps respectively.
7. The SiPM Staircase can be visualized by selecting the ”Staircase” option for the ”Plot Type” parameter in the Janus GUI window. An example of SiPM Staircase is presented in Fig. **10.42**.

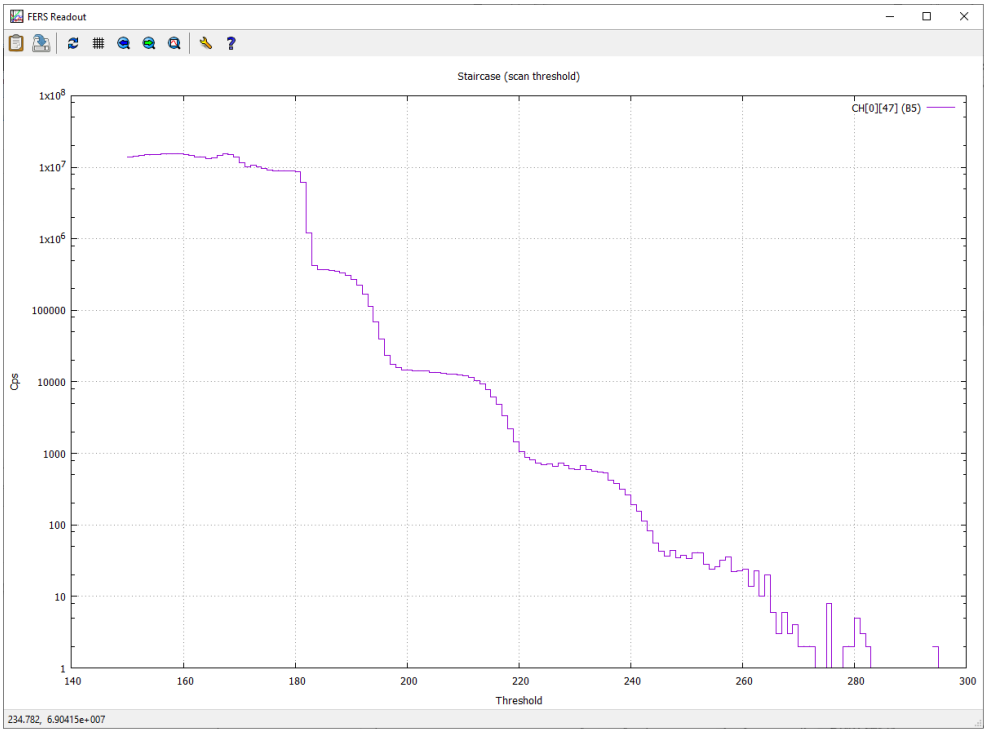


Fig. 10.42: Staircase obtained from the TD self-triggers of one channel. Each stair corresponds to a different number of photoelectrons triggered.

8. Select with the ”Plot Traces” button the Staircase of which channels have to be visualized in the *gnuplot* window.

A proper value for the ”TD Coarse Threshold” and ”TD Fine Threshold” can now be set, for instance, in order to reduce as much as possible the DCR during physics runs. If this is the case, Fig. **10.42** shows that a possible value for the ”TD Coarse Threshold” could be 300.

10.8 Single-Photon Spectrum

This section will guide the user throughout the settings necessary to acquire a single photon spectrum with the A5202/DT5202 FERS-5200 unit by working in Spectroscopy Mode. Once the LED pulser (SP5601 in the presented example) or any other appropriate light source is connected to the SiPMs, the HV can be turned on. The user should then:

1. Set ”SPECTROSCOPY” for the ”Acquisition Mode” parameter in the AcqMode tab.
2. Set the desired option for the ”Bunch Trigger Source” parameter and for the trigger thresholds.
3. Select the pulse height output from one of the two available amplification chains inside the Citiroc-1A through the ”Gain Selection” parameter. Fig. **10.43** shows the initial settings used for the acquisition of single photon spectra.
4. Select a proper value for the ”Hold Delay” parameter (see Sec. **10.7.2**).

Note: In order to reduce the DCR, the user is suggested to send an external trigger synchronized with the pulses using the ”T1-IN” (or ”T0-IN”) setting for the ”Bunch Trigger Source” parameter. In the reported example, the SP5601 LED pulser was used and its trigger signal was propagated to the A5202 board T1-IN connector.

Note: Even when using an external trigger fed into T0-IN or T1-IN, a value of the ”TD Coarse Threshold” sufficiently high is needed in order to reduce the irreducible noise induced by cross-talk between contiguous channels.

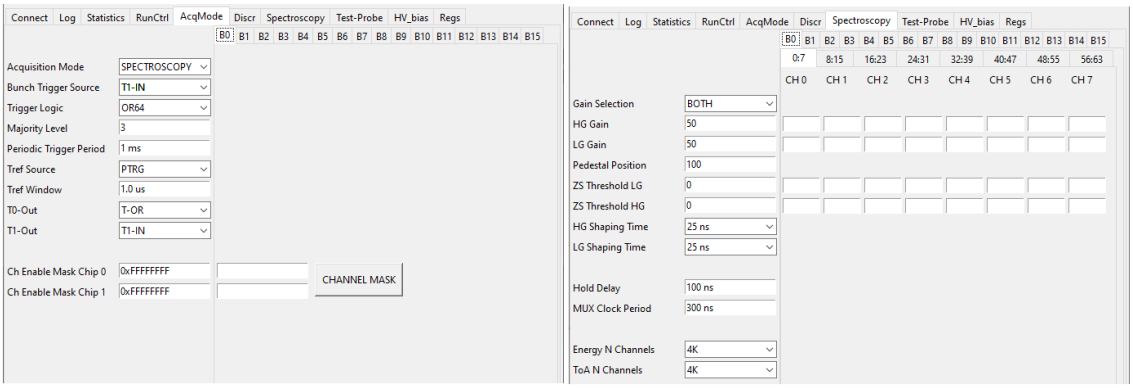


Fig. 10.43: The initial settings used for the acquisition of single photon spectra. On the left, the AcqMode tab, on the right the Spectroscopy tab.

Note: The ”Test Pulse Source” and ”Analog Probe” parameters must be set to ”OFF” when acquiring physics signals.

5. Press ”Apply” to save all changes and then the Start button .
6. Press the ”Plot Traces” button. Select ”Spect HG” or ”Spect LG” for the ”Plot Type” command in order to visualize the pulse height spectrum from one of the two amplification chains. In Fig. **10.44**, an example of the spectrum obtained for signals from the HG amplification chain is presented.

Note: A tuning of the light intensity and of the ”HG Gain” parameter was necessary to obtain the plot in Fig. **10.44**.

7. By selecting the ”2D-Charge HG” option for the ”Plot Type” parameter it is possible to visualize the 2D spectrum of the pulse height average values for each channel. An output similar to that presented in Fig. **10.45** should be obtained. The user can check the correspondence between the channel ID number and the position in the 2D-spectrum by looking at the values printed on each pixel of the 2D spectrum (e.g. channel 11 corresponds to the E6 position). This correspondence is loaded by the software from the ”pixel_map.txt” file in the ”bin” folder.
8. Press the HV-ON button in order to turn off the HV once the acquisition has been stopped .

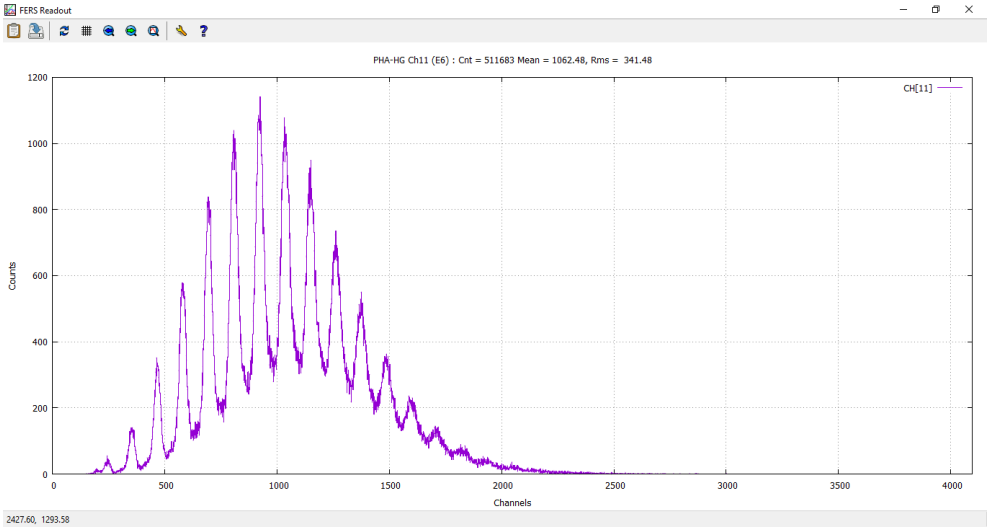


Fig. 10.44: Example of pulse height spectrum (from HG amplification chain) with the well visible photopeaks.

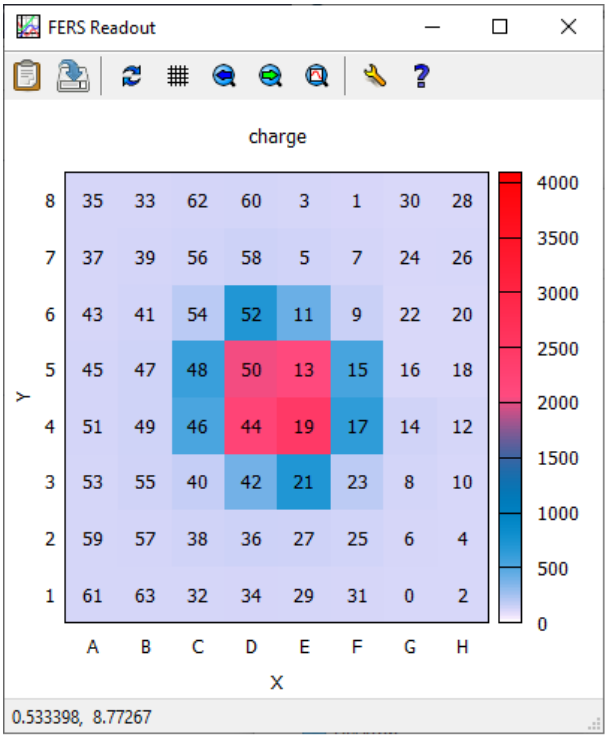


Fig. 10.45: Example of 2D pulse height spectrum.

10.8.1 Photopeaks Determination

The spectrum shown in Fig. **10.44** shows clearly the presence of photopeaks. The main issue could then be to determine how many triggered photoelectrons each peak corresponds to. The instructions reported below are quite general and may be useful to determine this information:

1. Set to the minimum value the intensity of the light sent to the SiPM while using the trigger from the LED pulser as a bunch trigger source. The pulse height spectrum obtained should be similar to that in Fig. **10.46**, with the first peak being the pedestal (0 photoelectrons triggered) and the second one being the peak associated to 1 photoelectron. The user can also define the position of the pedestal by acting on the "Pedestal Position" parameter **[RD3]** inside the Spectroscopy Tab.

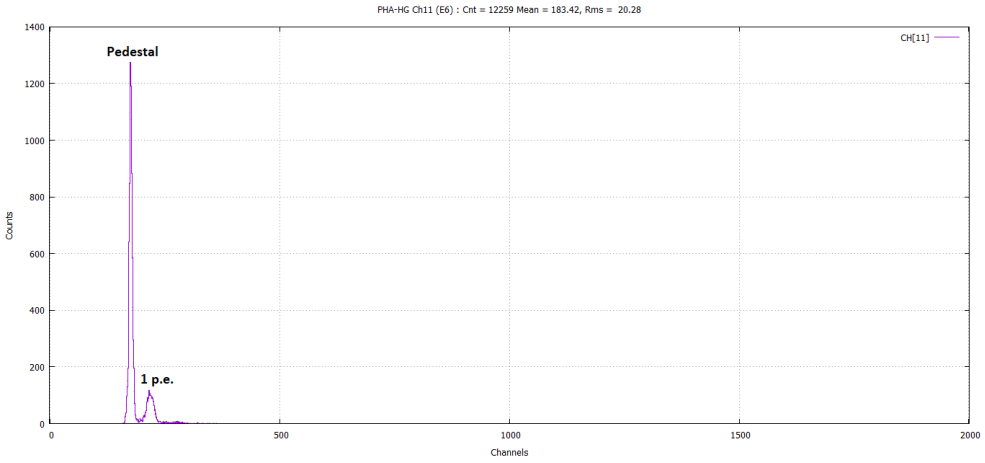


Fig. 10.46: Pulse height amplitude spectrum obtained with a trigger from the LED pulser (propagated to the T1-IN connector) when the minimum light intensity is set.

Note: Even though the external trigger is synchronized with the light pulses (thus only the pedestal is expected to appear when the lights is turned off) dark counts may occasionally occur at the same time of the trigger and give rise to the 1^{st} photopeak and 2^{nd} photopeak.

2. Increase the light intensity until other peaks at higher energies will start to appear in the spectrum (see Fig. **10.47**). The pedestal and the 1^{st} photopeak are still visible in the same position of the dynamic range.

Note: The distance between the pedestal peak position and that of the 1^{st} photopeak is always lower than those between two consecutive photopeaks.

3. Increase the light until a spectrum similar to that in Fig. **10.48** is obtained. The pedestal and the first three photopeaks disappeared; taking advantage of the previous step (see Fig. **10.48**), the association of each peak to the correspondent number of photoelectons triggered is possible.

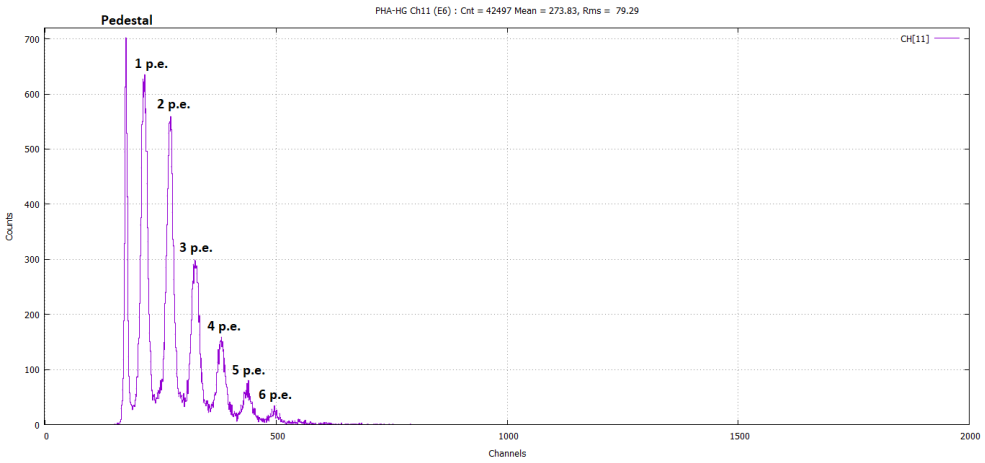


Fig. 10.47: Pulse height amplitude spectrum obtained with the pedestal and the first 6 photopeaks.

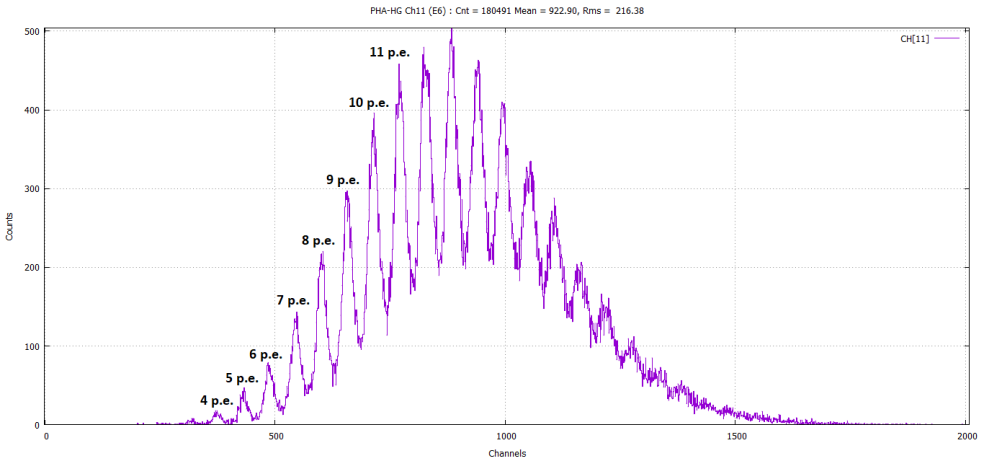


Fig. 10.48: Pulse height amplitude spectrum with the association of each peak to the correpondent number of photoelectrons triggered.

11 Firmware & Upgrade

The A5202/DT5202 board hosts one Artix XC7A75T-1FGG676C **[RD7]** FPGA with the corresponding firmware stored onto the on-board FLASH memory. At power-on, the microcontroller reads the FLASH memory page and programs the module automatically loading the FPGA firmware copy. It is possible to upgrade the FPGA firmware via USB or Ethernet, by writing the FLASH, taking advantage of the Janus software **[RD3]**.

In order to perform the FPGA firmware upgrade, the user should follow the instructions below:

1. Connect the board to the Janus software according to the instructions reported in Sec. **10.3** either via USB or Ethernet (see Fig. **11.1**).

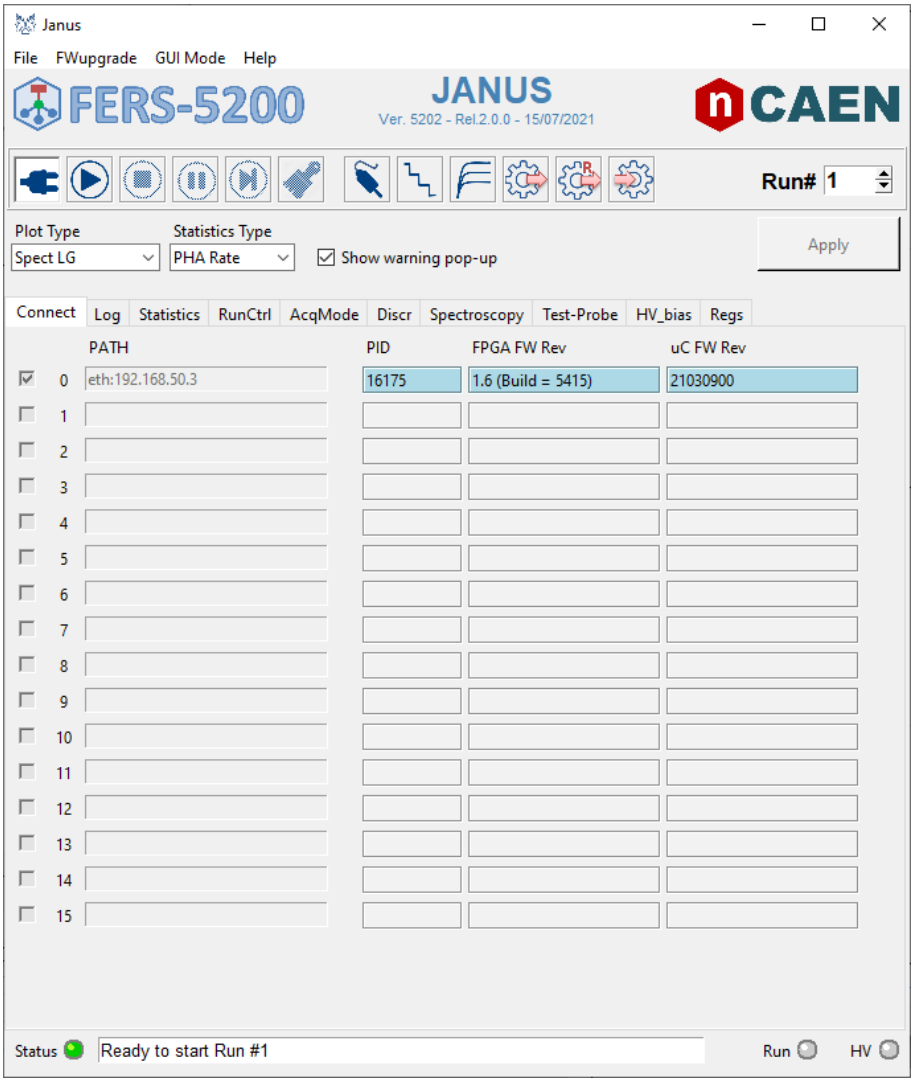


Fig. 11.1: A5202 board connected with the old version of FPGA firmware loaded.

2. Click on the ”FWupgrade” drop-down menu that is present on the Janus Menu Bar (see Fig. **11.1**). The ”Upgrade FPGA” option is visualized. By clicking on it, a window similar to that reported in Fig. **11.2** is opened.

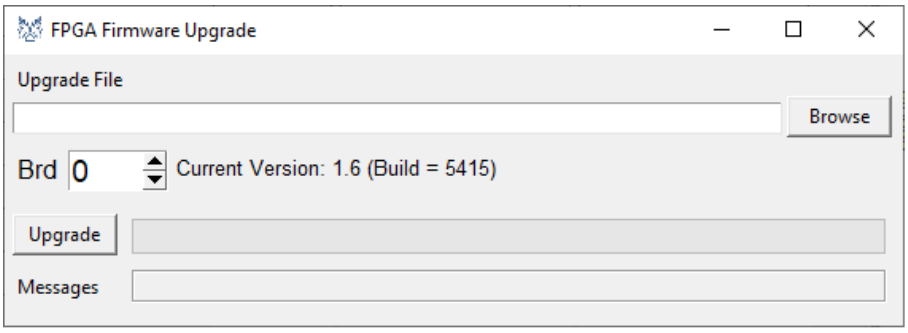


Fig. 11.2: FPGA Firmware Upgrade window.

3. Click on the ”Browse” button. A window allowing the user to select the new FPGA firmware file is opened. The latest version of FPGA firmware (.ffu file) can be downloaded from CAEN A5202/DT5202 webpage (”Download” section).
4. Once the selection is finished, the file location is displayed on the ”Upgrade File” field, as in Fig. **11.3**.

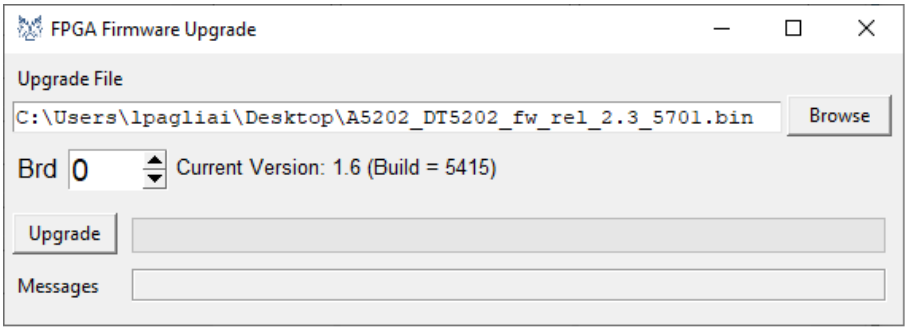


Fig. 11.3: FPGA Firmware Upgrade window with the new FPGA firmware file path visualized.

5. Press the ”Upgrade” button. First, the FPGA firmware file in the A5202/DT5202 board is erased, then the new FPGA firmware selected by the user is written onto the on-board FLASH memory. The user can check the progress of this operation by looking at the green bar and at the ”Messages” field in the FPGA Firmware Upgrade window (see Fig. **11.4**).

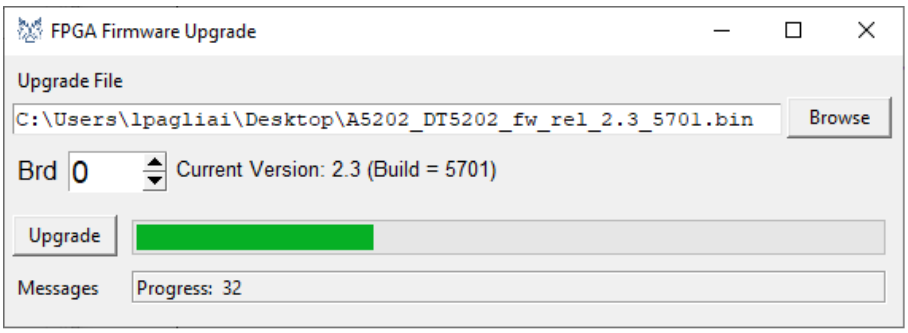


Fig. 11.4: FPGA Firmware Upgrade window while the firmware upgrade is in progress.

6. Once the operation is finished, the new FPGA firmware is loaded (the board connection with the Janus software is kept). The user can check that the new FPGA firmware version has been correctly loaded by looking at the PATH field in the Connect Tab of the Janus GUI (see Fig. **11.5**).

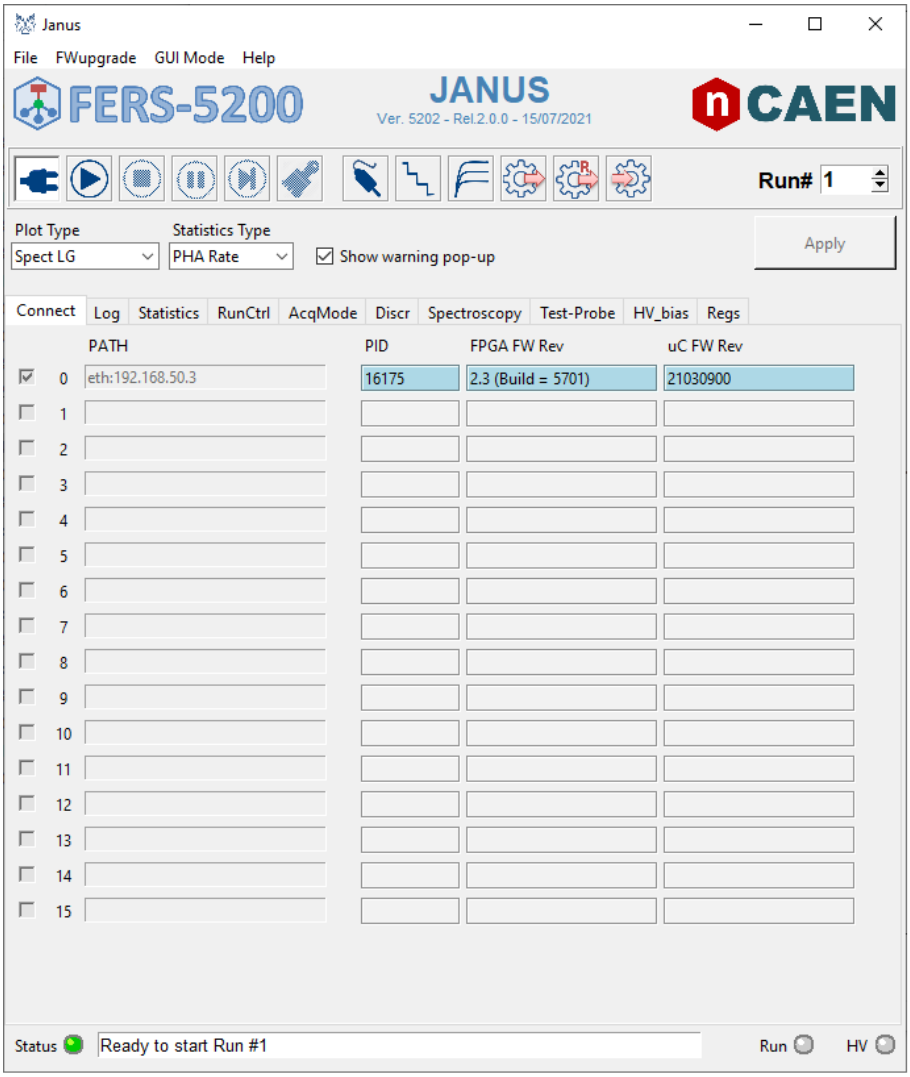


Fig. 11.5: A5202 board connected with the new version of FPGA firmware loaded.

12 Additional Instruction for a Safe Use

The device A5202 (bare board), and DT5202 has not or has a partial enclosure: this condition does not allow user to be protected properly against dangerous voltage parts. Moreover, the EMC compliance is not guaranteed if a proper enclosure/shielding is not provided. The construction of DT/A5202 allows final user to customize/use several boards according to experiment requirements. The final assembly system could be a combination of DT/A5202 and third parts devices. The final user has to build proper enclosure/shield or other precaution in order to make dangerous parts inaccessible and achieve EMC performance.

12.1 Electrical Safety Instructions

Several adapters can be used with the device: A5250, A5253, A5254 or SiPM connector without adapter. The following highlighted parts could become dangerous voltage, so the final users has to build proper enclosure or other means in the final installation to avoid unintentional contact.

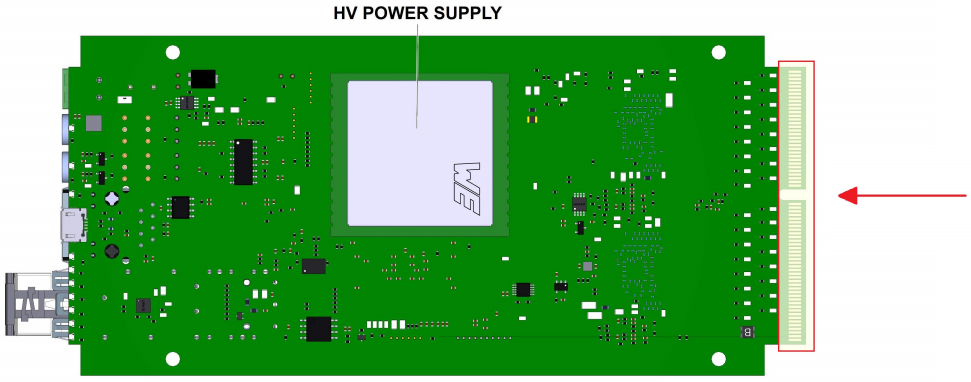


Fig. 12.1: HV connectors in the A5202

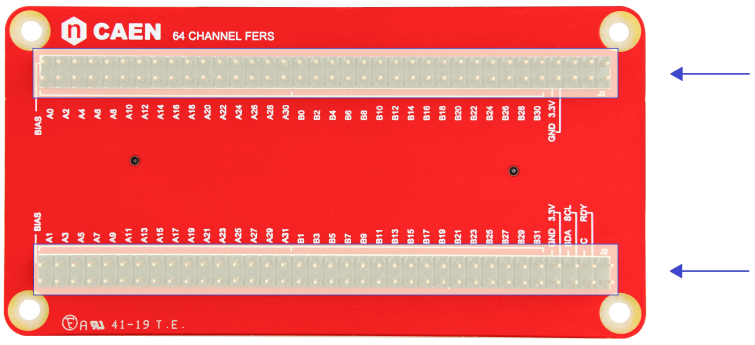


Fig. 12.2: HV connectors in the A5250 adapter

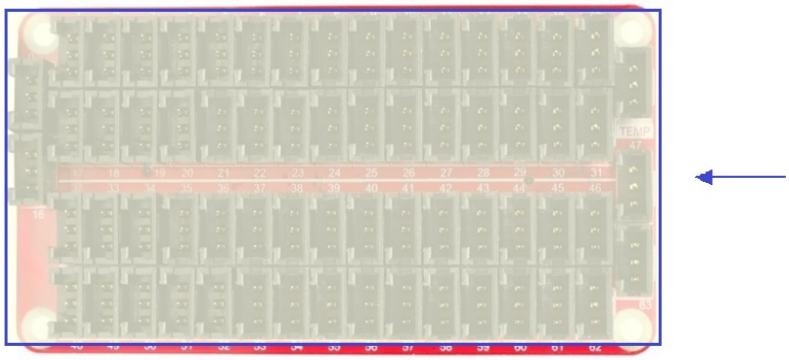


Fig. 12.3: HV connectors in the A5253 adapter

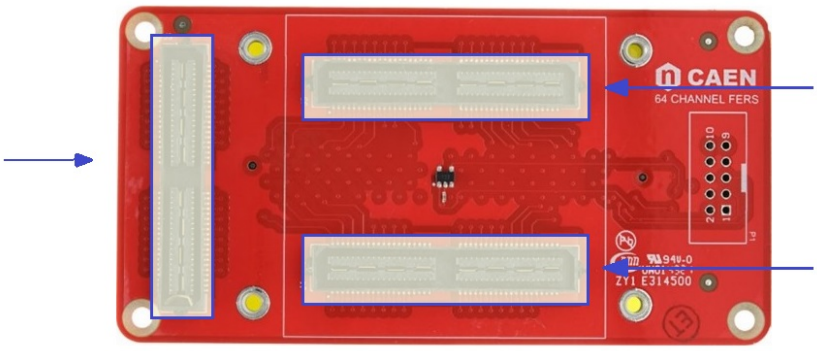


Fig. 12.4: HV connectors in the A5254 adapter

13 Instructions for Cleaning

The equipment may be cleaned with isopropyl alcohol or deionized water and air dried. Clean the exterior of the product only.
Do not apply cleaner directly to the items or allow liquids to enter or spill on the product.

13.1 Cleaning the Touchscreen

To clean the touchscreen (if present), wipe the screen with a towelette designed for cleaning monitors or with a clean cloth moistened with water.
Do not use sprays or aerosols directly on the screen; the liquid may seep into the housing and damage a component. Never use solvents or flammable liquids on the screen.

13.2 Cleaning the Air Vents

It is recommended to occasionally clean the air vents (if present) on all vented sides of the board. Lint, dust, and other foreign matter can block the vents and limit the airflow. Be sure to unplug the board before cleaning the air vents and follow the general cleaning safety precautions.

13.3 General Cleaning Safety Precautions

CAEN recommends cleaning the device using the following precautions:

- Never use solvents or flammable solutions to clean the board.
- Never immerse any parts in water or cleaning solutions; apply any liquids to a clean cloth and then use the cloth on the component.
- Always unplug the board when cleaning with liquids or damp cloths.
- Always unplug the board before cleaning the air vents.
- Wear safety glasses equipped with side shields when cleaning the board.

14 Device Decommissioning

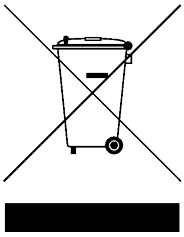
After its intended service, it is recommended to perform the following actions:

- Detach all the signal/input/output cable
- Wrap the device in its protective packaging
- Insert the device in its packaging (if present)

THE DEVICE SHALL BE STORED ONLY AT THE ENVIRONMENT CONDITIONS SPECIFIED IN THE MANUAL, OTHERWISE PERFORMANCES AND SAFETY WILL NOT BE GUARANTEED

15 Disposal

The disposal of the equipment must be managed in accordance with Directive 2012/19 / EU on waste electrical and electronic equipment (WEEE).



The crossed bin symbol indicates that the device shall not be disposed with regular residual waste.

16 Technical Support

To contact CAEN specialists for requests on the software, hardware, and board return and repair, it is necessary a MyCAEN+ account on www.caen.it:

https://www.caen.it/support-services/getting-started-with-mycaen-portal/

All the instructions for use the Support platform are in the document:

A paper copy of the document is delivered with CAEN boards.
The document is downloadable for free in PDF digital format at:

https://www.caen.it/wp-content/uploads/2022/11/Safety_information_Product_support_W.pdf

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