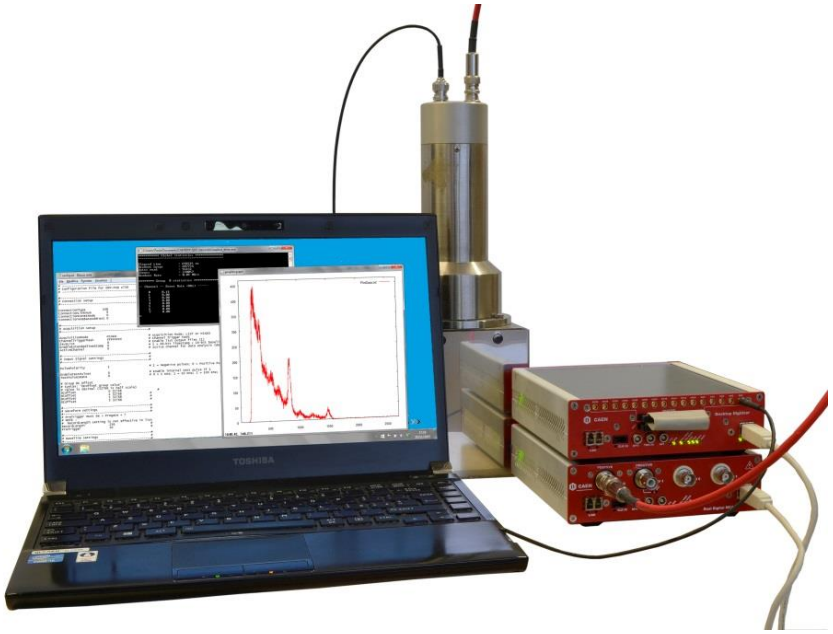
Rev. 5 - December, 23th 2022

DPP-QDC

Digital Pulse Processing for QDC



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User Manual
UM4495

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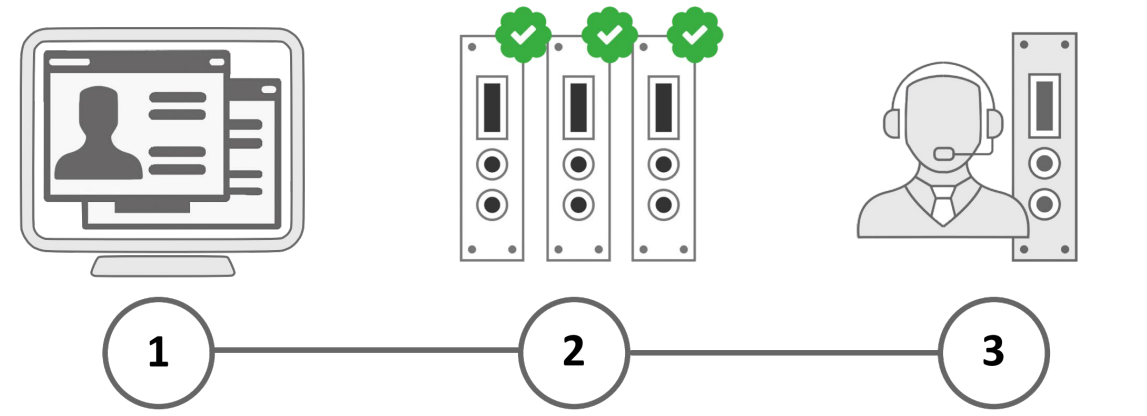

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Purpose of this Manual

This User Manual contains the full description of the Digital Pulse Processing for Charge to Digital Converter DPP-QDC implemented exclusively for the "D" model of 740 Digitizer series (740D). The description is compliant with DPP-QDC firmware release **4.25_135.17** and DPP-QDC demo release **2.2**. For future releases compatibility, check in the firmware and software revision history files.

Change Document Record

Date	Revision	Changes
November, 24th 2015	00	Initial release
December, 8th 2017	01	Revised and expanded Chap. **Software Interface**
October, 15th 2018	02	Revised Chap**. Software Interface** to add Linux support
June, 7th 2022	03	Updated Fig **4.1** and **4.2**
December, 13th 2022	04	Updated Chap. **Memory Organization.**
December, 23rd 2022	05	Updates Sec. **Drivers & Libraries**, **Installation** and **Configuration File Syntax, Technical support**

Symbols, abbreviated terms and notation

ADC	Analog-to-Digital Converter
DAQ	Data Acquisition
DPP	Digital Pulse Processing
DPP-QDC	DPP for Charge to Digital Converter
MCA	Multi-Channel Analyzer
OS	Operating System
PC	Personal Computer
PMT	Photo Multiplier Tube
QDC	Charge-to-Digital Converter
TDC	Time-to-Digital Converter
USB	Universal Serial Bus

Reference Documents

[RD1] WP2081 - Digital Pulse Processing in Nuclear Physics

[RD2] UM4868 DPP-QDC Registers Description

[RD3] UM1935 - CAENDigitizer User & Reference Manual

[RD4] GD2783 – First Installation Guide to Desktop Digitizers & MCA

[RD5] Technical Information Manual of V1718 and VX1718 VME – USB2.0 Bridge

[RD6] Technical Information Manual of A3818 PCI Express Optical Link Controller

[RD7] Technical Information Manual of A2818 PCI Optical Link Controller

[RD8] UM1935 - CAENComm User & Reference Manual

[RD9] AN2472 - CONET1 to CONET2 migration

[RD10] UM2784 – CAENDigitizer LabView User & Reference Manual

All documents can be downloaded from the CAEN website

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Limitation of Responsibility

If the warnings contained in this manual are not followed, CAEN will not be responsible for damage caused by improper use of the device. The manufacturer declines all responsibility for damage resulting from failure to comply with the instructions for use of the product. The equipment must be used as described in the user manual, with particular regard to the intended use, using only accessories as specified by the manufacturer. No modification or repair can be performed.

Disclaimer

The information contained herein has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies. CAEN spa reserves the right to modify its products specifications without giving any notice; for up to date information please visit www.caen.it.

Made in Italy

We remark that all our boards have been designed and assembled in Italy. In a challenging environment where a competitive edge is often obtained at the cost of lower wages and declining working conditions, we proudly acknowledge that all those who participated in the production and distribution process of our devices were reasonably paid and worked in a safe environment (this is true for the boards marked "MADE IN ITALY", while we cannot guarantee for third-party manufactures).

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1. Introduction

CAEN S.p.A. offers a wide range of digitizers to meet different needs of sampling frequency, resolution, form factor, etc. Besides the use of digitizers as waveform recorder (oscilloscope mode), the user can upload special versions of the FPGA firmware for the **Digital Pulse Processing** (DPP) algorithms. A digitizer running in DPP mode becomes a multipurpose instrument which replaces most of the traditional modules such as MCAs, QDCs, TDCs, Discriminators, etc. (for more details refer to the DPP overview **[RD1]**).

The purpose of the DPP is to perform online signal processing on detector signals directly digitized, and to transform the raw sequence of samples into a compressed data packet that preserves the information required, minimizing the event data size. DPP algorithms are implemented in the on-board FPGA and can be reprogrammed at any time. In one single module it is possible to have the complete information of the event and the capability to extract all the quantities of interest.

This user manual is intended to describe the **Digital Pulse Processing** for **Charge to Digital Converter** firmware (**DPP-QDC**) running exclusively on 740 digitizer series equipped with the Altera Cyclone III: x740D model). The complete list of digitizers running the DPP-QDC firmware is summarized on **Tab. 1.1**.

A x740D digitizer running the DPP-QDC firmware becomes a multichannel data acquisition system for nuclear physics and other applications requiring radiation detectors. The digitizer accepts signals directly from the detector and implements a digital replacement of *a Single Gate QDC, Discriminator and Gate Generator*. All these functionalities are performed inside the board FPGA without any use of external cables, nor additional boards or delay lines.

The acquisition is therefore performed by a single compact system which is able to self-trigger on 32/64 channels independently, according to the form factor (Desktop-NIM/VME-VX64). In addition the trigger filter can be programmed independently on each channel to get the best resolution from different detector systems. The integration gate width can be set for groups of eight consecutive channels. The DPP-QDC is particularly suitable in case of segmented detectors, and in any case where a large number of detectors has to be read simultaneously. Considering the 740D sampling rate, it is indicated in case of spectroscopy with slow scintillation detectors, such as NaI(Tl), $LaBr_3$(Ce), $CeBr_3$, etc.

Both the board configuration and the acquisition can be completely managed by the **CAEN DPP-QDC Demo Software**, a C console which allows the user to set the parameters for the acquisition, to configure the hardware, and to perform the data readout. The source codes are also available (Microsoft Visual Studio © project for Windows) for those who needs to customize the acquisition.

The main functionalities of a digitizer running DPP-QDC firmware are listed below:

- Auto selection of the events with a digital leading edge discrimination;
- Input signal baseline (pedestal) calculation and pedestal subtraction for energy calculation;
- Single gate integration for the energy spectra calculation.

Note: The description of the DPP-QDC system of this Manual is compliant with DPP-QDC firmware release **4.15_135.10** and CAEN DPP-QDC Demo Software release **2.0**. For future releases compatibility, check in the firmware and software revision history files.

Desktop Digitizers(*)	Description	Product Code
DT5740D	32 Ch. 12 bit 62.5 MS/s Digitizer: 192kSch, EP3C40, SE	WDT5740DXAAA
NIM Digitizers(*)	**Description**	**Product Code**
N6740D	32 Ch. 12 bit 62.5 MS/s Digitizer: 192kSch, EP3C40, SE	WN6740DXAAAA
VME Digitizers(*)	**Description**	**Product Code**
V1740D	64 Ch. 12 bit 62.5 MS/s Digitizer: 192kS/ch, EP3C40, SE	WV1740DXAAAA
VX1740D	64 Ch. 12 bit 62.5 MS/s Digitizer: 192kS/ch, EP3C40, SE	WVX1740DXAAA
DPP Firmware(*)	**Description**	**Product Code**
DPP-QDC	DPP-QDC- Digital Pulse Processing for Time Stamped Digital QDC (x740)	WFWDPPQDCAAA

Tab. 1.1: Supported CAEN digitizers for DPP-QDC firmware

(*) For accessories and customizations related to digitizers and for multiple DPP-QDC license packs, refer to the board User Manual or have a look at the board page on CAEN web site: www.caen.it

2. Principle of Operation

The figure below shows the functional block diagram of the DPP-QDC firmware:

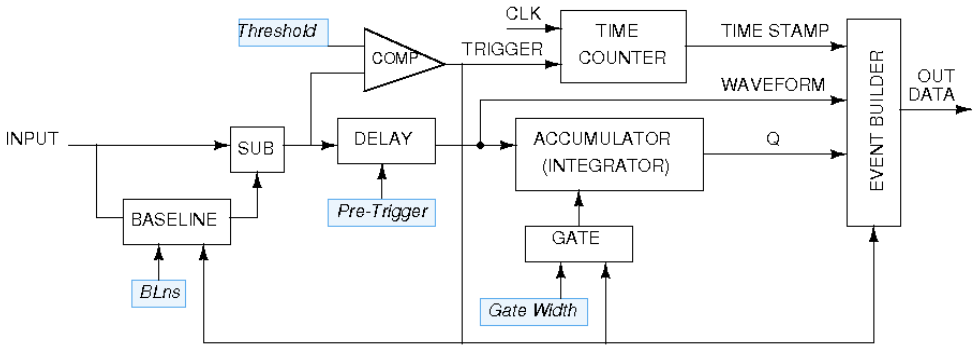

Fig. 2.1: Functional Block Diagram of the DPP-QDC

The aim of the DPP-QDC firmware is to evaluate the charge of the input signal in a multi-channel system. Each channel can be programmed and acquired independently from the other channels.

The main operations of the DPP-QDC firmware can be summarized as follows:

- receive an input signal directly from the detector and digitize it continuously. It is possible to adjust the dynamic range with a programmable DC offset to exploit the full dynamics of the digitizer;
- the algorithm continuously calculates the *baseline* of the input signal by averaging the samples belonging to a moving window of programmable size (see Sect. **Baseline**). The baseline is subtracted from the input signal, giving *input_sub= input – baseline* (Digital Baseline Restorer)*;*
- the *input_sub* value is compared with the value of the trigger threshold and the event is selected as soon as the *input_sub* signal crosses the threshold (see **Fig. 2.2**). *The threshold value can be set independently on each channel of the board.* Once the event is selected a local trigger is generated (refer to Sect. **DPP-QDC trigger management** for further details);
- at the trigger fire, the signal is delayed by a programmable number of samples (corresponding to the “Pre Trigger” value in ns) to be able to integrate the pulse before the trigger (“Gate Offset”). The gate for charge integration is then generated and it is therefore received by the charge accumulator before the signal. While the gate is active the baseline remains frozen to the last averaged value and its value is used as charge integration reference. *The gate width can be set independently for each group of eight channels.* **Fig. 2.2** summarizes all the DPP-QDC parameters;
- for the whole duration of a programmable “trigger hold-off” value, other trigger signals are inhibited. It is recommended to set a trigger hold-off value comparable with the signal width. The baseline remains frozen for the whole trigger hold-off duration;

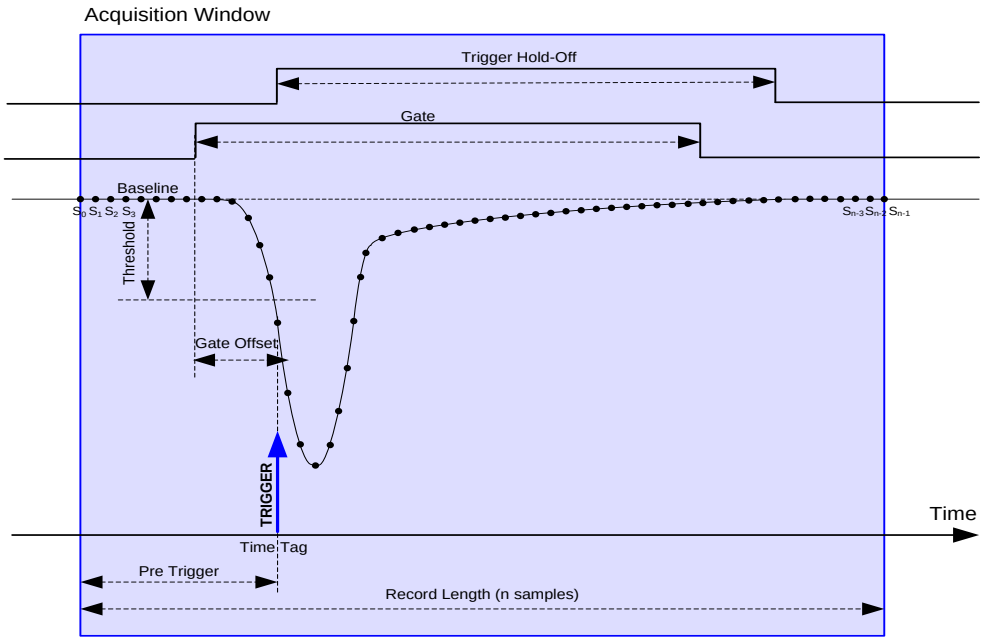

Fig. 2.2: Diagram summarizing the DPP-QDC parameters. The trigger fires as soon as the signal crosses the threshold value. Gate, Gate Offset, Pre-Trigger, Trigger Hold-Off, and Record Length are also shown for one acquisition window

- the trigger enables the event building, that includes the waveforms (i.e. the raw samples) of the input, the trigger time stamp, the baseline, and the charge integrated within the gate. After that the system gets ready for a new event;

Note: The DPP-QDC firmware is not designed to acquire continuous stream of waveforms. Only a statistical portion of the waveforms is saved, also in case of low rate. See also Sect. **Acquisition Modes**.

- the event data is saved into a memory buffer. The user can choose both the number of events inside the buffer, and the number of total buffers that the memory is divided in. If the buffer contains only one event, that buffer becomes immediately available for the readout and the acquisition continues into another buffer. If more events are written in one buffer, only when the buffer is complete those events become available for the readout;
- the software can then plot the signal waveforms for debugging and adjust the parameters, as well as plot the energy spectrum and timing distribution;
- finally output files (list and waveform) can be generated in different formats suitable for external spectroscopy analysis software tools. Energy and time spectra are not managed onboard but they can be generated and saved by the CAEN DPP-QDC Demo Software.

Baseline

The baseline calculation is an important feature of the DPP-QDC firmware, since its value is used as reference for the charge integration of the input pulses. Moreover, most of the DPP parameters are related to the baseline value. This paragraph describes in detail how the baseline calculation works.

The user can choose to set a fixed value for the baseline, or to let the DPP firmware calculate it. In the first case the user must set the *baseline value in LSB units*, where **1 LSB = 0.49 mV**.

The firmware can dynamically evaluate the baseline as the mean value of *N* points inside a moving time window. The user can choose the *N* value among `4, 16, and 64`. The baseline is then frozen from few clocks before the gates start up to the end of the maximum value between the long gate and the trigger hold-off. After that the baseline restarts again its calculation considering in the mean value also the points before the freeze. This allows to have almost no dead-time due to the baseline calculation.

Fig. 2.3 shows how the baseline calculation and freeze work. The trigger threshold dynamically follows the variation of the baseline.

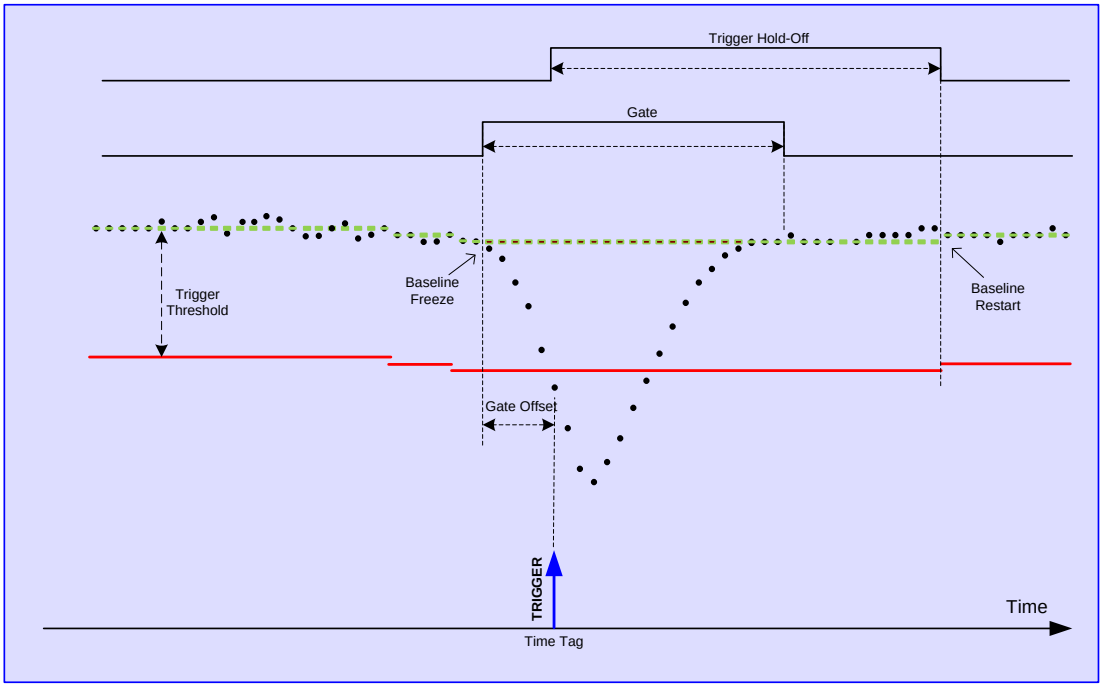

Fig. 2.3: Baseline calculation as managed by the DPP-QDC algorithm

DPP-QDC trigger management

The DPP-QDC firmware allows for several way of trigger generation:

1) Normal Mode: each channel can “self-trigger” on its own input signal when the input crosses a programmable threshold. The self-trigger works on each channel independently from the other channels;
2) Paired Mode: Each channel can both acquire on its own self-trigger and on the self-trigger of the paired channel. Pair “n” corresponds to channel n and channel n+2;
3) External Trigger Mode: the board can accept an external trigger on the TRG IN connector. The external trigger acquisition mode can be configured according to bits[21:20] of register 0x8000 (Board Configuration) (see also **[RD2]**). The following options are available:
    a. The acquisition is synchronized with the external trigger edge. All channels acquire simultaneously and their self-trigger is disabled;
    b. Veto: the acquisition is inhibited when the external trigger is active high;
    c. Anti-Veto: the acquisition is inhibited when the external trigger is active low.

Note: In case of external trigger mode it might be useful to disable the individual channel self-trigger. To disable the channel self-trigger the user must set bit[24] = 1 of register 0x8040 (DPP Algorithm Control) (see also **[RD2]**).

Trigger Hysteresis

When the input signal is no more over-threshold, the trigger could fire again in the tail of the pulse, especially in case the tail contains spikes or noise. The “Trigger Hysteresis” feature inhibits the trigger until the input pulse reaches half of the threshold value itself. See **Fig. 2.4** for a diagram of this feature. This option is enabled by default. To disable set bit[30] = 1 of register 0x8040 (DPP Algorithm Control) **[RD2]**, or disable the option in the configuration file of the CAEN DPP-QDC Demo Software (see Sect. **Trigger Settings**).

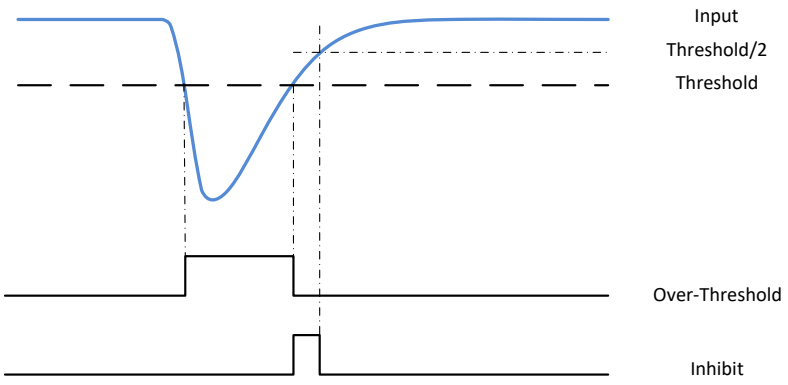

Fig. 2.4: Trigger Hysteresis in DPP-QDC firmware. The trigger is inhibited after the over-threshold until the input reaches the value of half the threshold.

Input Smoothing

The smoothing is a moving average filter, where the input samples are replaced by the mean value of the previous n samples. n is defined by bits[14:12] of register 0x8040 (DPP Algorithm Control) **[RD2]**, and the number of samples for the smoothing is defined as $n = 2^m$, where m = 0, …, 6. Option m = 0 disables the smoothing.

When enabled, the trigger is applied on the smoothed samples, thus reducing triggering on noise. The charge integration is either performed on the input samples or on the smoothed samples, according to the Analog Probe selection from bits[13:12] of register 0x8000 **[RD2]** or from the configuration file of the CAEN DPP-QDC Demo Software (see Sect. **On-line Commands**).

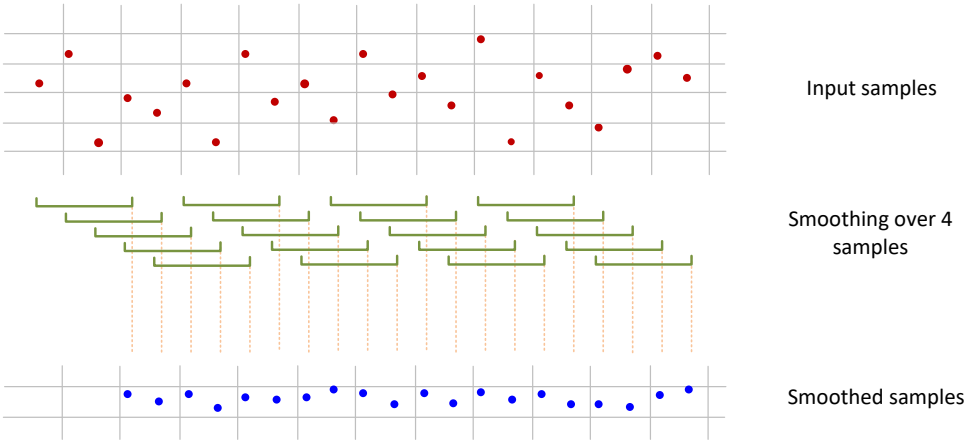

Fig. 2.5: Example of smoothing over four samples. The input samples are averaged over four samples and replaced in the smoothed samples by the mean value.

3. Acquisition Modes

As described on Sect. **DPP-QDC trigger management** each individual channel of the digitizer can trigger independently from the others. When the input signal fires the trigger the DPP-QDC firmware integrates the input samples within the programmed time window.

The main acquisition mode is called “List mode”, where the digitizer provides the time of arrival of the input (also called “Trigger Time Stamp”) and its charge. As soon as the list reaches a certain size, it is made available for readout and the acquisition continues in another buffer. Being the size of the event very small (typically few bytes), the throughput is extremely reduced. The firmware is not designed to make histogram onboard, anyway it can transfer the list information to the software for the histogram management.

The DPP-QDC firmware allows also to acquire waveform samples (i.e. a sequence of samples within a programmable acquisition window) together with the charge and time in the “Mixed” acquisition mode. The acquisition of the waveform is mainly intended to debug and to set the DPP parameters. Moreover, not all the waveforms are saved into memory, also in case of low input rate. Just a statistical portion of the total number of waveforms is saved into memory.

Running in Mixed mode, the user can view the input signal, the baseline, and other control signals (such as the trigger, the gate, the trigger hold-off, etc…) in the same plot, and easily adjust the parameters for the acquisition. Running in mixed mode may imply a very high data throughput, due to the amount of samples saved into the board memory and then read out by the DAQ software.

The CAEN DPP-QDC Demo Software can manage both the list and the mixed acquisition mode. In LIST mode the software can retrieve the list information from the digitizer to make the relevant histogram and save the output files. Working in MIXED mode the software can also plot the digital pulse for online monitoring and save the output file. Users who wants to further customize the acquisition can write their own software starting with the C codes of the demo software.

4. Memory Organization

The internal FPGAs of the board can access the SSRAM memory to save the events from two consecutive groups, as for example Group 0 (from channel 0 to channel 7), and Group 1 (from channel 8 to channel 15).

The memory is divided into a programmable number of buffers (also called "aggregates"), where each buffer contains a programmable number of events. The event format is programmable as well. The board registers **[RD2]** involved are the following:

- "Aggregate Organization" (*Nb*), address 0x800C: defines the total number of aggregates in which the memory is divided ($num.aggr = 2^{Nb}$).
- "Number of Events per Aggregate" (*Ne*), address 0x8020: defines the number of events contained in one aggregate.
- "Record Length" (*Ns*), address 0x8024: defines the number of samples of the waveform, if enabled.
- "Board Configuration", address 0x8000: defines the acquisition mode and the event data format.

Note: Those who need to write their own DAQ software, must take care to choose the *Ne* value according to the event and buffer size, as explained in the examples in the next section.

According to the programmed event format, an event can contain a certain number of samples of the waveform, one trigger time stamp, the charge *Q*, and the Baseline/Extras information.

For each possible value of Aggregate Organization the following maximum number of events per group is defined. In case of list mode, the parameter Record Length (rec_len) is equal to zero.

Number of Aggregates	Maximum number of Events per Aggregate
1024	$^{128}/_{(2+rec\_len)}$
512	$^{256}/_{(2+rec\_len)}$
256	$^{512}/_{(2+rec\_len)}$
128	$^{1024}/_{(2+\cdot rec\_len)}$
64	$^{2048}/_{(2+rec\_len)}$
32	$^{4096}/_{(2+rec\_len)}$
16	$^{8192}/_{(2+rec\_len)}$
8	$^{16384}/_{(2+rec\_len)}$
4	$^{32768}/_{(2+rec\_len)}$
2	$^{65536}/_{(2+rec\_len)}$
1	$^{131072}/_{(2+rec\_len)}$

Event Data Format

The Event Data Format decodes the structure of the event to be read in output. Events are grouped in aggregates and read group by group.

If groups are read consecutively, events of the second group are not time aligned with the events of the first group. Indeed it is required a further re-alignment of the events according to the time stamp. This alignment is performed in a specific function called *DecodeDPPAggregate* which is available in the CAENDigitizer library. The CAEN DPP-QDC Demo Software already performs the decode of the events to retrieve the relevant information for each event.

Group Aggregate Data Format for 740D series

The Channel Aggregate is composed by the set of *Ne* events, where *Ne* is the programmable number of events contained in one aggregate (see the previous section). The structure of the Channel Aggregate of two events (EVENT 0 and EVENT 1) for 740D series is shown in **Fig. 4.1**, where:

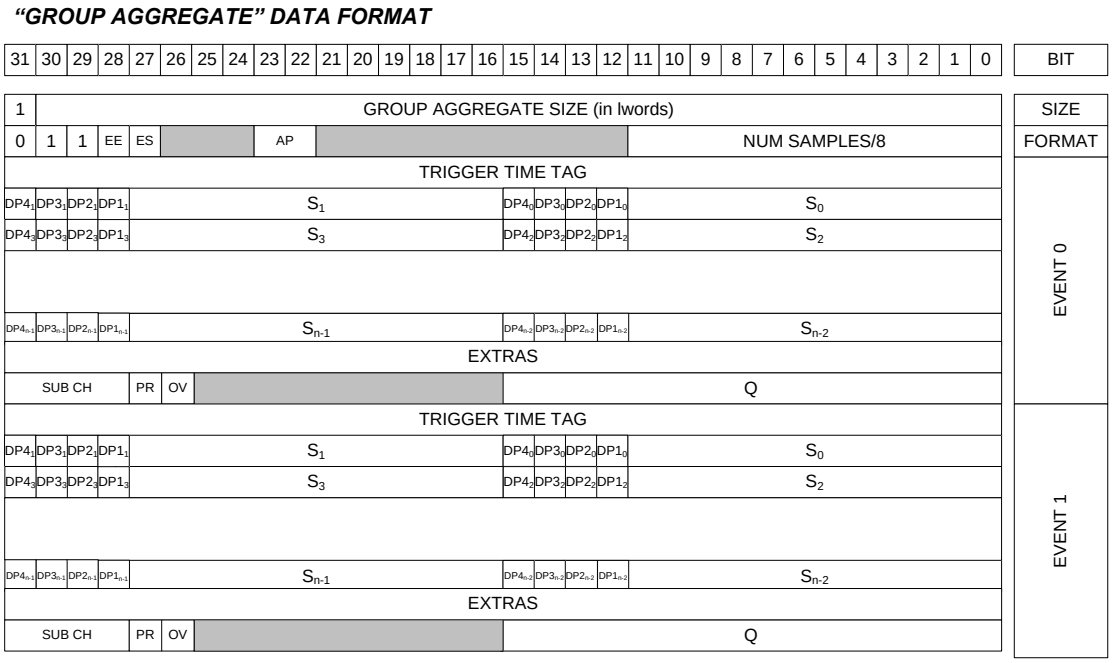

Fig. 4.1: Group Aggregate Data Format scheme for 740D series

EE: Extras enabled flag

ES: Waveform (samples) enabled flag. The number of recorded samples depends on the field "NUM SAMPLES/8"

AP: Analog Probe selection among:

00 = "Input";

01 = "Smoothed Input";

10 = "Baseline".

DPi_m (i=1, ...,4; m=0, 1, …,n-1): Digital Virtual Probe value i for sample m

DP1$_m$ is always the "Gate" probe value

DP2$_m$ is always the "Trigger" probe value

DP3$_m$ is always the "Trigger Hold-Off" probe value

DP4$_m$ is always the "Over-Threshold" probe value

S_m (m=0, 1, …,n-1): Samples of Analog Probe trace at time t=m

EXTRAS: the extras word corresponds to:

bits[31:16] = the baseline value multiplied by 16;

bits[15:0] = extended time stamp: those 16 bits can be added (left) to the Time Stamp representation, which becomes a 32+16=48 bit number.

Note: to enable the "EXTRAS" word set bit[17] of register 0x8000 (Board Configuration) **[RD2]**.

Q: integrated charge value in the gate width

SUB CH: sub channel identification number (SUB CH = 0, …, 7)

PR: Pile-up flag: not yet implemented

OV: Over-Range flag, identifies when the charge value is out of range

0x0 = the charge value is negative

0xFFFF = the charge has exceeded the upper limit

Board Aggregate Data Format

For each readout request (occurring when at least one group has data to be read) the "interface FPGA (ROC)" reads one aggregate from each enabled group memory. One aggregate per group is read each time, and the sum of Group Aggregates makes the Board Aggregate. If one group has no data, that group does not come into the Board Aggregate.

The data format when all 8 groups of a VME form factor have available data is shown in **Fig. 4.2**:

"BOARD AGGREGATE" DATA FORMAT

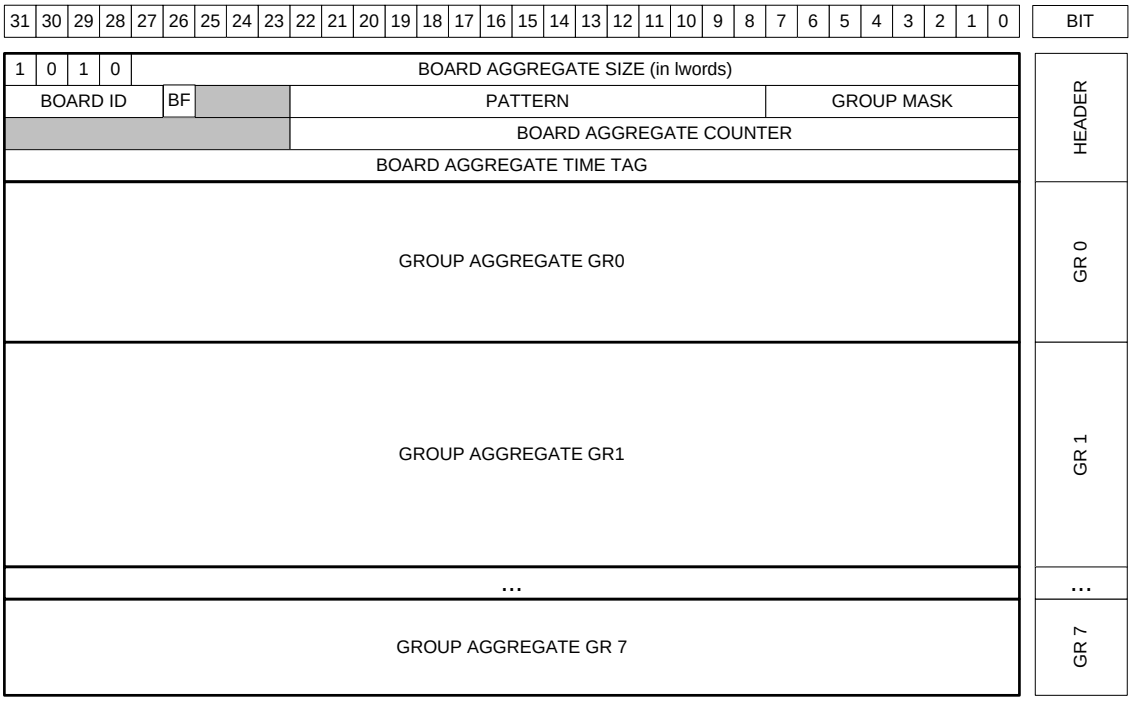

Fig. 4.2: Board Aggregate Data Format scheme for 740D series

BOARD AGGREGATE SIZE: total size of the aggregate

BOARD ID: corresponds to the GEO address of the board. In case of VX boards this number is automatically set for each board. In case of VME boards this value is by default = 0 for all boards. It is possible to set the Board ID through register 0xEF08 **[RD2]**. The GEO address is quite useful in case of concatenate BLT (CBLT) read.

BF: Board Fail flag. This bit is set to "1" as a consequence of a hardware problem, as for example the PLL unlock. The user can investigate the problem checking the *Board Failure Status* register 0x8178 **[RD2]**, or contacting CAEN support (refer to Chapter **Technical support)**.

PATTERN: is the value read from the LVDS I/O (VME only);

GROUP MASK: corresponds to those group participating to the Board Aggregate;

BOARD AGGREGATE COUNTER: counts the board aggregate. It increase with the increase of board aggregates;

BOARD AGGREGATE TIME TAG: is the time of creation of the aggregate (this does not corresponds to any physical quantity).

Data Block

The readout of the digitizer is done using the Block Transfer (BLT, refer to **[RD3]**); for each transfer, the board gives a certain number of Board Aggregates, consisting in the Data Block. The maximum number of aggregates that can be transferred in a BLT is defined by the READOUT_BTL_AGGREGATE_NUMBER. In the final readout each Board Aggregate comes successively. In case of n Board Aggregates, the Data Block is as in **Fig. 4.3**.

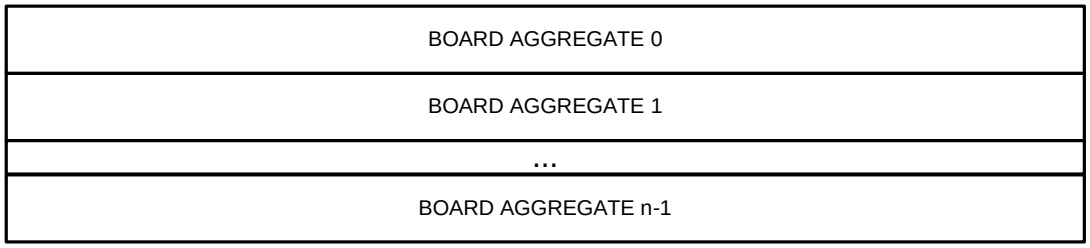

Fig. 4.3: Data Block scheme

5. Software Interface

Introduction

The CAEN DPP-QDC Demo Software is an application that manages the communication and the data acquisition from 740D digitizer series running the DPP-QDC firmware. The demo software allows the user to select the proper communication interface and DPP settings. Waveforms and histograms can also be plotted in real time for one channel at a time, and both waveforms and lists of time stamp and energy can be saved.

Block Diagram

The block diagram of the CAEN DPP-QDC Demo Software architecture is schematically reported in **Fig. 5.1**:

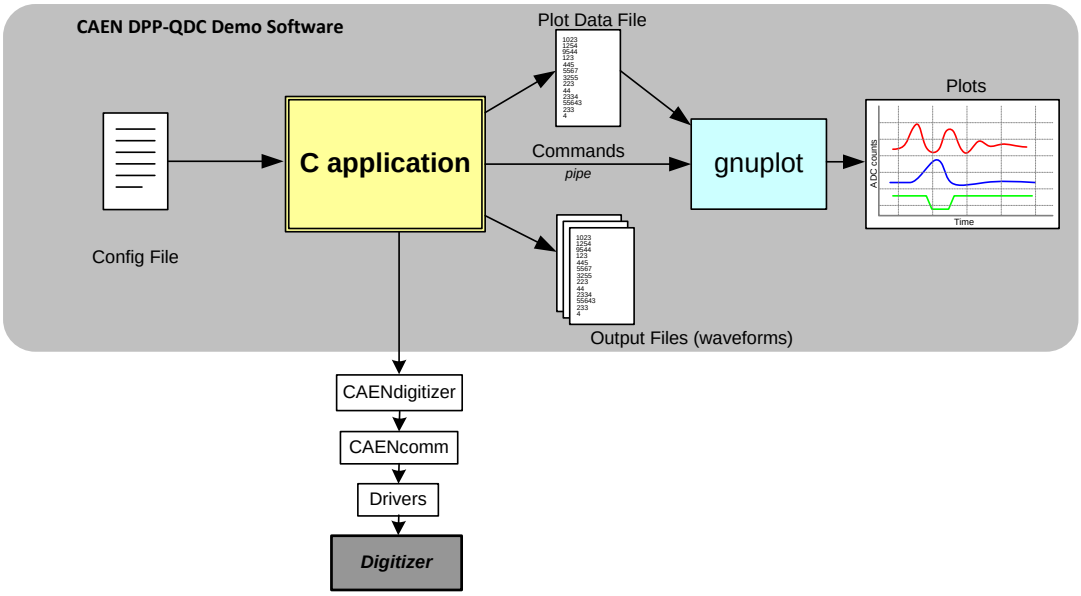

Fig. 5.1: The DPP-QDC Demo Software block diagram

The program core is a C application that programs the Digitizer according to a set of parameters written in the configuration text file. It then starts/stops the acquisition and manages the data readout. Data (waveforms and list of time stamps and energies) can be plotted using the external plotting tool *gnuplot*, or saved to output files and analyzed offline. The configuration file included in the program installation directory, called ***config.txt***, contains a list of possible parameters, which are explained in Sect. **Configuration File Syntax.**

Users who need to customize the application can use the source codes as starting point for their customization. The source codes are available in the CAEN DPP-QDC Demo Software folder, together with the Microsoft Visual Studio © project (Windows only).

Drivers & Libraries

Drivers

In order to deal with the hardware, CAEN provides the drivers for all the different types of physical communication interfaces featured by the specific digitizer and compliant with Windows and Linux OS:

- **USB 2.0 Drivers for NIM/Desktop** boards are downloadable on CAEN website (www.caen.it) in the digitizer web page (**login required**).

Note: Windows OS USB driver installation for Desktop/NIM digitizers is detailed in **[RD4]**.

- **USB 2.0 Drivers for V1718** CAEN Bridge, required for VME boards interface, is downloadable on the CAEN website.

Note: For the installation of the V1718 USB driver, refer to the User Manual of the Bridge (**[RD5]**).

- **Optical Link Drivers** are managed by the A2818 PCI card or the A3818 PCIe card. The driver installation package is available on CAEN website in the "Software/Firmware" area at the A2818 or A3818 page (**login required**)

Note: For the installation of the Optical Link driver, refer to the User Manual of the specific Controller (**[RD6]**, **[RD7]**).

Libraries

CAEN libraries are a set of middleware software required by CAEN software tools for a correct functioning. These libraries, including also demo and example programs, represent a powerful base for users who want to develop customized applications for the digitizer control (communication, configuration, readout, etc.):

- **CAENDigitizer** is a library of functions designed specifically for the Digitizer family and it supports also the boards running the DPP firmware. The CAENDigitizer library is based on the CAENComm library. For this reason, **the CAENComm libraries must be already installed on the host PC before installing the CAENDigitizer**.

  The CAENDigitizer installation package is available on the CAEN website. Reference document: **[RD3]**.

- **CAENComm** library manages the communication at low level (read and write access). The purpose of the CAENComm is to implement a common interface to the higher software layers, masking the details of the physical channel and its protocol, thus making the libraries and applications that rely on the CAENComm independent from the physical layer. Moreover, the CAENComm requires the CAENVMELib library (access to the VME bus) even in the cases where the VME is not used. This is the reason why **CAENVMELib has to be already installed on your PC before installing the CAENComm**.

  The CAENComm installation package, and the link to the required CAENVMELib, is available on the CAEN website. Reference document: **[RD8]**.

Note: For Windows only, all libraries are automatically installed through the standalone DPP-QDC Demo Software Setup tool. Linux users have to install them separately.

Currently, the CAENComm (and so the CAENDigitizer) supports the following communication interfaces:

- PC → USB 2.0 → Digitizers (either Desktop or NIM models)
- PC → USB 2.0 → V1718/V3718 → VME → Digitizers (VME models only)
- PC → USB 3.0 → V4718 → VME → Digitizers (VME models only)
- PC → ETH → V4718 → VME → Digitizers (VME models only)
- PC → USB 3.0 → A4818 → CONET → Digitizers (all models)
- PC → PCI (A2818) → CONET → Digitizers (all models)
- PC → PCI (A2818) → CONET → V2718/V3718/V4718 → VME → Digitizers (VME models only)

- PC → PCIe (A3818) → CONET → Digitizer (all models)
- PC → PCIe (A3818) → CONET → V2718/V3718/V4718 → VME → Digitizers (VME models only)
- PC → USB → A4818 → CONET → V2718/V3718/V4718 → VME → Digitizers (VME models only)

CONET (Chainable Optical NETwork) indicates the CAEN proprietary protocol for communication on Optical Link. Refer to **[RD9]** for more information.

Note: CAENDigitizer library for LabVIEW (only for Windows OS) is also available. CAENDigitizer LabVIEW needs the *labview* subfolder of CAENComm to be installed. Please, refer to **[RD10]** for detailed information.

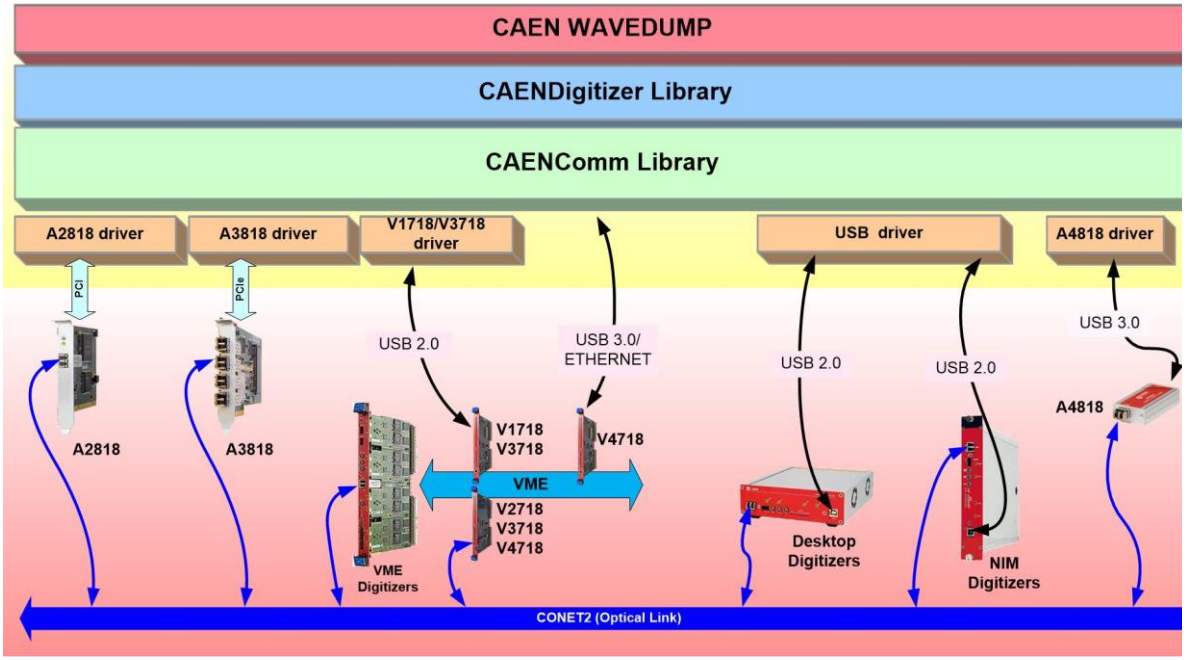

Fig. 5.2: Libraries and drivers required for the DPP-QDC system

Firmware and Licensing

The firmware upgrade is an advanced feature that can be performed only in case the user wants to upgrade the current firmware to a new version, or to upload a different firmware on the board. The .cfa file format checks for the board model to ensure that firmware upgrade is made on the correct board.

✓ **How to load the firmware on the board**

Download the **DPP-QDC Firmware** (.cfa) for 740D series on CAEN website

Download the **CAENUpgrader** software to upload the firmware on your board. The program full installation package for Windows OS is available on the CAEN website.

Unpack the **installation package, launch** the **setup file** and **complete** the **Installation wizard.**

Power on the board.

Run the **CAENUpgrader GUI** by one of the following options:

- The **desktop icon** for the program
- The **Quick Launch icon** for the program
- The **.jar file** in the *bin* folder from the installation path on your host

Select '**Upgrade Firmware**' in the '**Available actions**' scroll box menu of the '**Board Upgrade**' tab.

Select the **model** of your board in the '**Board Model**' scroll box menu.

Enter the **.cfa file** in the '**Firmware binary file**' text box by the '**Browse**' button.

Set the '**Connection Type**' and, eventually, the '**VME Base Address**'

Check '**Standard Page**' in the '**Config Options**'.

Press the '**Upgrade**' button to perform the upload; after few seconds, a pop up message will inform you about the successful upgrade.

Power cycle the **board**.

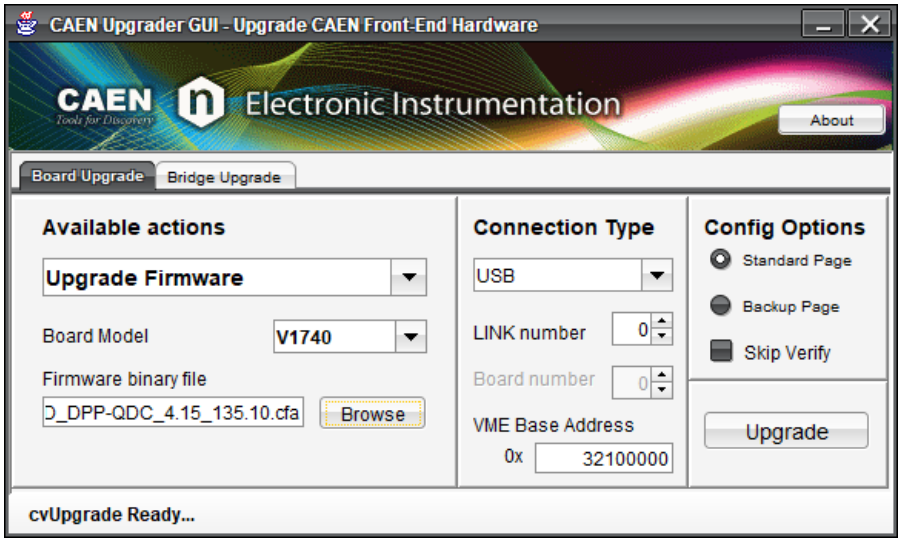

Fig. 5.3: CAENUpgrader settings for DPP-QDC firmware upgrade

Installation

The DPP-QDC Demo Software is compliant with both Windows and Linux OS, 32 and 64 bits.

Before installing the software, perform the following steps:

- **Make sure** that your **hardware** (Digitizer and/or Bridge, or Controller) is **properly installed** (refer to the related User Manual for hardware installation instructions) and **connected** to the PC.
- **Make sure** that the **appropriate firmware** is **running on the board**. You can use the CAENUpgrader tool to read the digitizer firmware revision.
- **Make sure** you **have installed the driver** for your OS and the physical communication layer to be used. Driver installation packages are downloadable on CAEN website (**login required**) as reported in the **Drivers & Libraries** paragraph.

For Windows users:

CAEN provides the full installation package for the CAEN DPP-QDC Demo Software in a **standalone version** for **Windows OS**. This version installs all the binary files required to directly use the software (i.e. no need to install the required CAEN libraries in advance).

- **Download the CAEN DPP-QDC Demo Software installation package** compliant with your Windows from CAEN website
- **Extract** the **files** to your host PC.
- **Complete** the **installation wizard**.

CAEN DPP-QDC Demo Software is then installed under the folder:

C:\Program Files\CAEN\Digitizers\CAENDPP-QDC-Demo

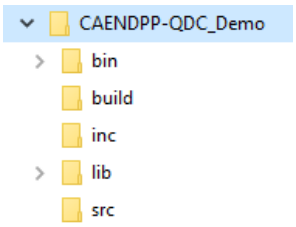

Fig. 5.4: Subfolders structure of CAEN DPP-QDC Demo Software main directory

The subfolders are:

- "*bin*" which contains the executable file (**readout_demo.exe**). Double click in the readout_demo.exe file to start the program.

Note: the **default configuration file** is "C:\Users\<*username*>\CAENDPP-QDC_Demo\config.txt". A custom configuration file can be used if the demo is launched within "bin" folder with the following shell command

CAENQDC_Demo [-d acquisition_time] [-n numer_of_events] [-id run_id] <config_file_path>

If not specified, default acquisition_runtime is 0 = infinite run

- *"build"* which contains the Microsoft Visual Studio project,
- "*inc*" contains the relevant header files.
- "*lib*" contains the 32 and 64-bit version libraries
- *"src"* contains all the relevant source codes for the CAEN DPP-QDC Demo Software.

For Linux users:

CAEN provides the full installation package for the CAEN DPP-QDC Demo Software for **Linux OS**. To use this version the CAEN libraries must be downloaded from the CAEN website and installed on your host PC.

- Be sure **GNUplot** is installed on your PC
- Download and install the **CAENVME**, **CAENComm** and **CAENDigitizer (rel. 2.12.0 or higher)** libraries.
- **Download the CAEN DPP-QDC Demo Software installation package** for Linux from CAEN website
- **Extract** the **archive** to your host PC.
- **Run the following shell command** from the DPP-QDC Demo extracted folder

  ./configure

  make

  sudo make install

- The DPP-QDC Demo is installed in the extracted folder

The CAEN DPP-QDC Demo can be launched running the following shell command:

CAENQDC_Demo [-d acquisition_time] [-n numer_of_events] [-id run_id] <config_file_path>

If not specified, default acquisition runtime is 0 = infinite run

The **default configuration file** is "/etc/CAENQDC_Demo/config.txt", which is loaded if no configuration file is specified.

The subfolders in the CAENDPPQDC_Demo folder are:

- *"src"* contains all the relevant source codes for the CAEN DPP-QDC Demo Software.
- *"Setup"* contains a local configuration file for easier management.
- "*include*" contains the relevant header files.

On-line Commands

Once started, the CAEN DPP-QDC Demo Software executes the settings written in the configuration file; if a formal error occurs, it is displayed on the shell.

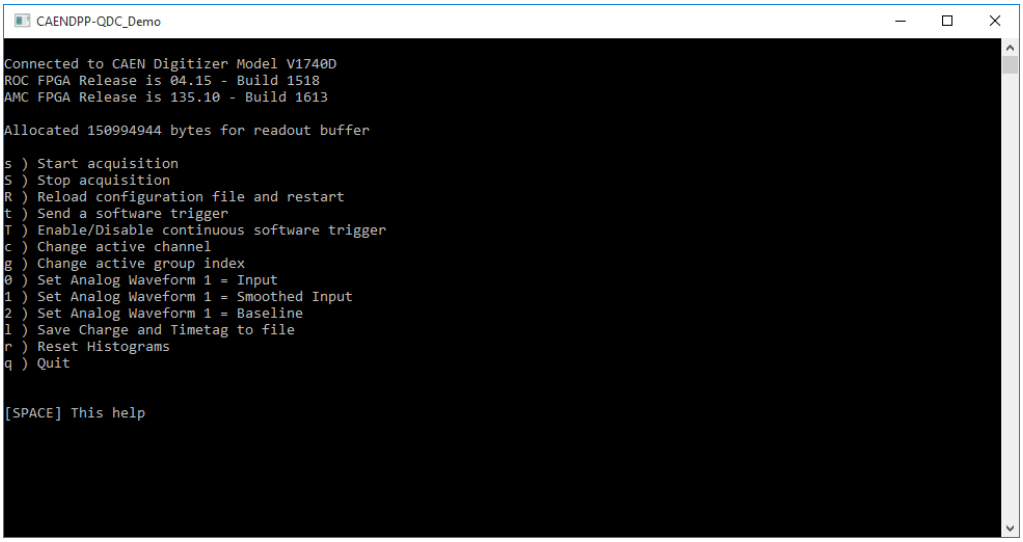

Fig. 5.5: the CAEN DPP-QDC Demo at first run.

The software connects to the board using the connection settings written in the configuration file (see **Connection Settings**). At first connection, the Demo reads the connected board model and its firmware release and reports these information in the shell.

The software accepts some on-line commands associated with particular keys that are described in **Tab. 5.1** below. The available commands are listed at the first run of the software and whenever the user press the [SPACE] command. Those commands have to be written in the shell itself.

Key	Function
s	Start the acquisition
S	Stop the acquisition
R	Reloads the configuration file and restart
t	Sends a software trigger (single shot): this command forces the acquisition of one event. In analogy with an oscilloscope, this command corresponds to the “Force trigger” button
T	Enables / disables the continuous generation of software trigger: inside the acquisition loop, the program sends a trigger, reads the corresponding event and executes the algorithm analysis. This command corresponds to the "Auto trigger” in an oscilloscope.
c	Selects the channel to be shown; after “c” type the desired number of channel. The DPP-QDC Demo Software manages the plot of one channel at a time.
g	Selects the group to be shown in the statistics area; after “g” type the desired group number.
0, …, 7	After the *“c” or ”g”* command, selects the channel or group *n* to be plotted. If the channel is not enabled for acquisition from the configuration file, a message will appear on shell.
0	Set the Analog Waveform 1 displayed in the plot to be the input signal. “Enter” must be pressed to confirm this command.

1	Set the Analog Waveform 1 displayed in the plot to be the smoothed input signal. "Enter" must be pressed to confirm this command.
2	Set the Analog Waveform 1 displayed in the plot to be the baseline signal. "Enter" must be pressed to confirm this command.
l	Enables the list file dump for each enabled channel. The charge and the timetag information are saved in the file. Data are saved in - "C:\Users\<*username*>\CAENDPP-QDC_Demo" (*Windows*) - "/home/<*username*>/CAENDPPQDC_Demo" (*Linux*)
r	Reset the histogram and the number of events
q	Quits the DPP-QDC Demo Software
[SPACE]	Shows the help menu

Tab. 5.1: CAEN DPP-QDC Demo Software on-line commands

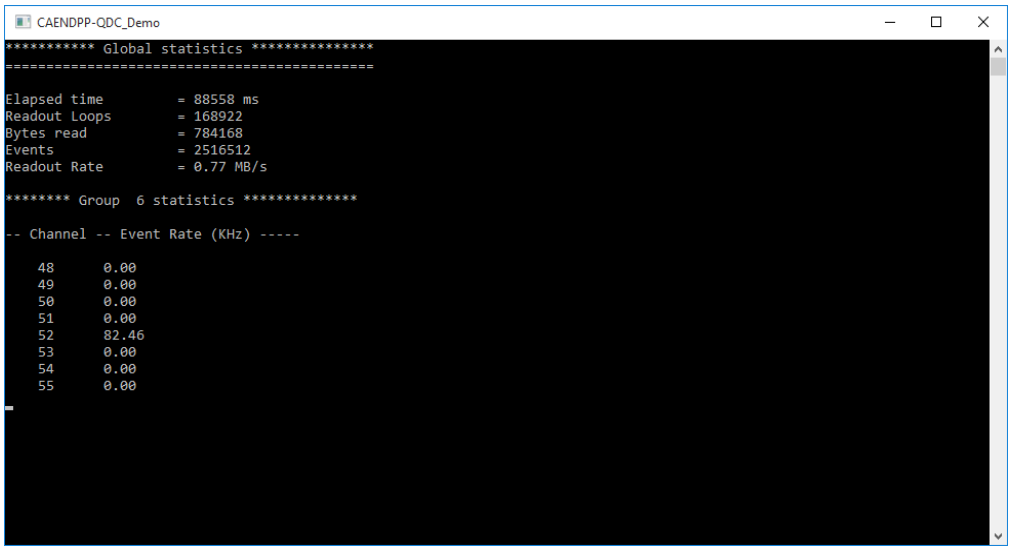

Fig. 5.6: the CAEN DPP-QDC Demo during acquisition (after "s" command has been sent). The "Global statistics" are always visible, while it is possible to change the "Group statistics" via the "g" command. In this example, the group 6 has been selected and, from the statistics we see that only Ch 52 is triggering at the reported rate.

Configuration File Syntax

The default configuration file is located in

- C:\Users\<*username*>\CAENDPP-QDC_Demo\config.txt (*Windows users*)
- /etc/CAENQDC_Demo/config.txt (*Linux users*)

Connection Settings

```
ConnectionType             <value>   # Connection link : USB / OPT
ConnectionLinkNum          <value>   # Connection Link number
ConnectionConetNode        <value>   # Connection Node :
                                     # Node Id in CONET daisy chain (0-7)
ConnectionVmeBaseAddress   <value>   # VME Base Address: needed only for
                                     # VME access via USB/Optical Bridge
```

- `ConnectionType`: Identifies the type of communication channel, choosing between **`USB`** and **`OPT`**. USB corresponds to both the direct connection from PC to digitizer (Desktop models or NIM), and the connection through V1718 and VME bus (VME models). OPT corresponds to both the direct connection from PC A2818 (PCI controller) or A3818 (PCIe controller) to the digitizer through optical fibre (all models), and connection through V2718 and VME bus (VME models).
- `ConnectionLinkNum`: The number of the connection. Typically is **0** (only one digitizer connection to the PC). In case of more digitizers connected it is necessary to specify which has to be accessed. Remember that the CAEN DPP-QDC Demo Software can handle only one digitizer at a time. The Link Number identifies which USB or A2818/A3818 is in use. Be aware that it is not known in advance which LinkNumber corresponds to which USB port or PCI slot.
- `ConnectionConetNode`: This parameter must be specified only when connected via optical link (PCI) and indicates the node in the daisy chain. Typically is **0** (only one digitizer in the optical chain), it may be different if more than one digitizer (or V2718) is connected in a daisy chain.
- `ConnectionVmeBaseAddress`: Indicates the Base Address (32-bit hexadecimal number) to access the digitizer via the VME bus. This number should be 0 for the direct connections from PC to digitizer.

Acquisition Setup

```
AcquisitionMode           <value>        # Acquisition Mode: LIST or MIXED
ChannelTriggerMask        <value>        # Channel Trigger Mask
SaveList                  <value>        # Enable list output files (1)
EnableCSV                 <value>        #  Enable the list output file in CSV
                                         #  format (1)
EnableExtendedTimeStamp   <value>        # 1 = 48-bit Timestamp + 16-bit baseline
ActiveChannel             <value>        # Active channel for data analysis
                                         # (default=0 if unset)
```

- `AcquisitionMode`: Select the acquisition mode, choosing between LIST and MIXED. In case of List mode the board retrieves the energy and time of each pulse. Then the software makes the relative histograms. In case of Mixed mode also waveform samples are acquired and plotted.
- `ChannelTriggerMask`: This is the bit mask of the enabled channels for the acquisition. For example to enable even channels of a VME board write: 5555555555555555 (in case of DT/NIM form factors: 55555555). To enable all channels of a VME board write FFFFFFFFFFFFFFFF.
- `SaveList`: Enables the dump of the List file with the information of time stamp and energy for each event. One file is saved for each enabled channel. The list file is a two column file, where the first column is the trigger time stamp, and the second is the charge in ADC channels. Every 32 bits the time stamp rolls over, and starts again from 0. The software takes into account the roll- over and automatically extend it to 64 bit.
- `EnableCSV`: Enables the dump of the List file in CSV format with the information of event ID, time stamp and energy for each event. One file is saved for each enabled channel. The list file is a three column file, where the first column is event ID, the second is the trigger time stamp, and the third is the charge in ADC channels.
- `EnableExtendedTimeStamp`: It is possible to extend the time stamp representation from 32 bits to 48 bits on-board. The additional 16 bits are written in the EXTRAS word, together with 16 bits of baseline (refer to Sect. **Group Aggregate Data Format for 740D series** for additional details). The extended time stamp is not reported in the list file.
- `ActiveChannel`: Selects the active channel for the plot visualization. While the acquisition is running, it is possible to modify the active channel via software, by pressing “c” and the channel number on the shell interface. To change the group number press “g” and the desired group number.

Input Signal Settings

```
PulsePolarity      <value>     # 1 = Negative pulses; 0 = Positive Pulses

EnableTestPulses   <value>     # Enable internal test pulse if 1
TestPulsesRate     <value>     # 0 = 1 KHz; 1 = 10 KHz; 2 = 100 KHz; 3 = 1 MHz

DCoffset           <group> <value> # NOTE : DC Offset range is 0-65535 (16 bit);
                                   # 0 = above upper limit (4095);
                                   # 64K = below lower limit (0)
                                   # Parameter value is decimal
                                   # (32768 is half scale)
```

- `PulsePolarity`: Set this parameter according to the input pulse polarity
- `EnableTestPulses`: For debug purposes data from the ADC can be replaced by an internal test pulser.
- `TestPulsesRate`: Corresponds to the rate of the internal test pulses.
- `DCOffset`: Adjusts the DC offset level to exploit the full dynamics of the digitizer. The user can set this value for each group of the board. Options are the *group number* and the DC Offset *value*. Since the internal DAC is represented with 16 bits, and the ADC is rather 12 bits, the desired DC offset value has to be multiplied by 16. For example, `32768` is the mid-scale value, 2048.

Waveform Settings

```
RecordLength          <value>     # RecordLength setting is not effective in list
PreTrigger            <value>     # PreTrigger must be > |Pregate| + 112 ns
```

- `RecordLength`: Sets the number of samples for the waveform acquisition. Each sample corresponds to 16 ns.
- `PreTrigger`: The Pre Trigger corresponds to the time the samples are delayed before the triggers, to ensure that the waveform is completely acquired. Note that the Pre-Trigger value must be greater than the Gate Offset (`PreGate`) by at least 112 ns.

Baseline Settings

```
BaselineMode          <value>    # 0 = fixed, 1 = 4 samples, 2 = 16 samples,
                                 # 3 = 64 samples, 4 = 256 samples
FixedBaseline         <value>    # baseline value when BaselineMode = 0
```

- `BaselineMode`: Selects how the baseline is calculated. Use 0 to select the “Fixed Baseline” option. Options 1, …, 4 enables the automatic baseline calculation on a moving window of 4, 16, 64, and 256 samples respectively.
- `FixedBaseline`: In case of BaselineMode = 0 the user can write the corresponding value of the fixed baseline in LSB unit.

Gate Settings

```
GateWidth             <group> <value>
Pregate               <value>    # gate position with respect to the trigger
                                 # (in steps of 16 ns)
```

```
EnableChargePedestal <value>    # 0 = disabled; 1 = enabled
                                # (add 1024 to the charge)
ChargeSensitivity    <value>    # 0=0.16pC, 1=0.32pC, 2=0.64pC, 3=1.28pC,
                                # 4=2.56pC, 5=5.12pC, 6=10.24pC, 7=20.48pC
```

- `GateWidth`: Set the duration of the integration gate in steps of 16 ns.
- `PreGate`: Corresponds to the shift in time of the integration gate position with respect to the trigger. It is expressed in steps of 16 ns.
- `EnableChargePedestal`: Through this command it is possible to add a fix quantity of 1024 to the charge value. This is particularly useful in case of charges close to zero.
- `ChargeSensitivity`: Defines how many pC of charge correspond to one channel of the energy spectrum. Options are: 0 = 0.16 pC, 1 = 0.32 pC, 2 = 0.64 pC, 3 = 1.28 pC, 4 = 2.56 pC, 5 = 5.12 pC, 6 = 10.24 pC, 7 = 20.48 pC.

Trigger Settings

```
TrgMode                          <value>    # 0 = Normal; 1 = Paired; 2= External
trigger
TrgSmoothing                     <value>    # 0 = no smoothing, otherwise mean over
                                            # 2^n samples, with n <= 6
TrgHoldOff                       <value>    # Trigger hold off (in steps of 16ns)
DisableTriggerHisteresys         <value>    #
DisableSelfTrigger               <value>    # 0 = enabled; 1 = disabled
TriggerThreshold     <channel> <value>     # individual trigger thresholds
                                            # expressed in ADC LSB (1 LSB = 0.5mV)
```

- `TrgMode`: Selects between the two internal trigger modes and the external trigger mode . In “Normal” mode each channel triggers on its own self-trigger, while in the “Paired” mode each channel of a couple ’n’ acquire the event in logic OR between its self-trigger and the self-trigger of the other channel of the couple. Couple n corresponds to channel n and channel n+2. In “External Trigger” mode the *self-trigger is disabled* and the acquisition is synchronized with the external trigger edge, with all channels acquiring simultaneously.
- `TrgSmoothing`: In case of noisy signal it is possible to apply a smoothing filter on the input samples, where each sample is replaced with the mean value of n previous samples. When enabled, the trigger is evaluated on the smoothed samples, while the charge integration will be performed on the samples corresponding to the ”Analog Probe” selection (see online commands 1, …, 3 from Sect. **On-line Commands)**. Options are: 0 = no smoothing; n =1, …, 6 the smoothing is performed over 2^n samples. See Sect. **Input Smoothing** for additional details.
- `TrgHoldOff`: Logic signal of programmable width generated by a channel in correspondence with its local self- trigger. Other triggers are inhibited for the overall Trigger Hold- Off duration. The Trigger Hold Off width is expressed in steps of 16 ns.
- `DisableTriggerHysteresis`: The firmware allows to inhibit further triggers during the trailing edge of a pulse, to avoid re-triggering on the same pulse. See Sect. **Trigger Hysteresis** for additional details. Select 0 to enable this option (default), or 1 to disable it.
- `DisableSelfTrigger`: Disable the self-trigger of all channels. Select 0 to enable the self-trigger, 1 to disable it.
- `TriggerThreshold`: Sets the Trigger Threshold in LSB units (1 LSB = 0.49 mV) for each channel independently. Write the channel number and the threshold value in the corresponding fields.

Avdanced Settings

```
NevAggr                  <value>    # Number of event per aggregate (0= automatic)
```

- `NevAggr:` Sets the number of events per aggregate. See Sect. **Event Data Format** for additional details. Select 0 for the automatic evaluation of the NevAggr.

Practical use

As an example of the software use, we report the result of an acquisition made with a **V1740D** board equipped with the DPP-QDC firmware and a CAEN A746B 64ch adapter for LEMO connector.

We used the CAEN Digital Detector Emulator **DT5800D** to emulate exponential signals from a ^{60}Co radioactive source. We set negative polarity input signals with Poissonian rate of 20 kHz, a rise time of 0.1 µs and a decay time of 2 µs.

A CAEN V1718 USB bridge was used to establish a connection between the software and the board.

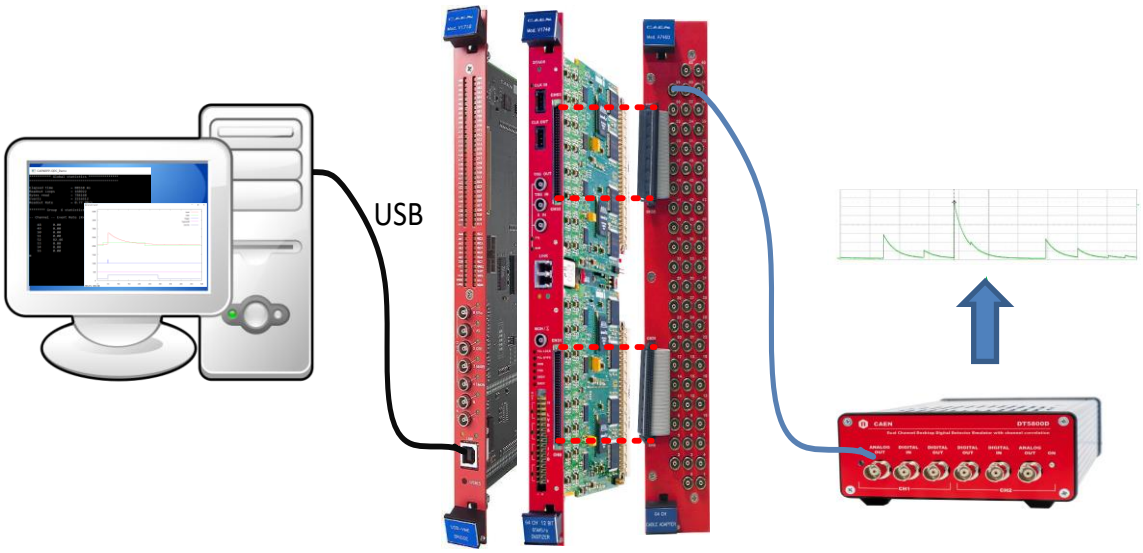

Fig. 5.7: setup for measurements with the V1740D equipped with the DPP-QDC firmware

We set the main acquisition parameters in the '*config.txt*' file as reported below:

```
ConnectionType              USB
ConnectionLinkNum           0
ConnectionConetNode         0
ConnectionVmeBaseAddress    32100000

AcquisitionMode             MIXED
ChannelTriggerMask          800000000000000     #only channel 59 enabled

PulsePolarity               1

DCoffset                    7 32768

RecordLength                600
PreTrigger                  50

PreGate                     20
EnableChargePedestal        0
ChargeSensitivity           5
GateWidth                   7 250

TrgHoldOff                  80
TriggerThreshold            59 20
```

We performed the acquisition on a single channel (ch59) of the board, in MIXED mode, so that we could visualize the **waveform** and the **spectrum**.

The waveform plot (see **Fig. 5.8)** shows the input signal, the integration gate, the trigger signal, the trigger hold off (if set) and the over-threshold (high for the amount of time the signal is above the threshold).

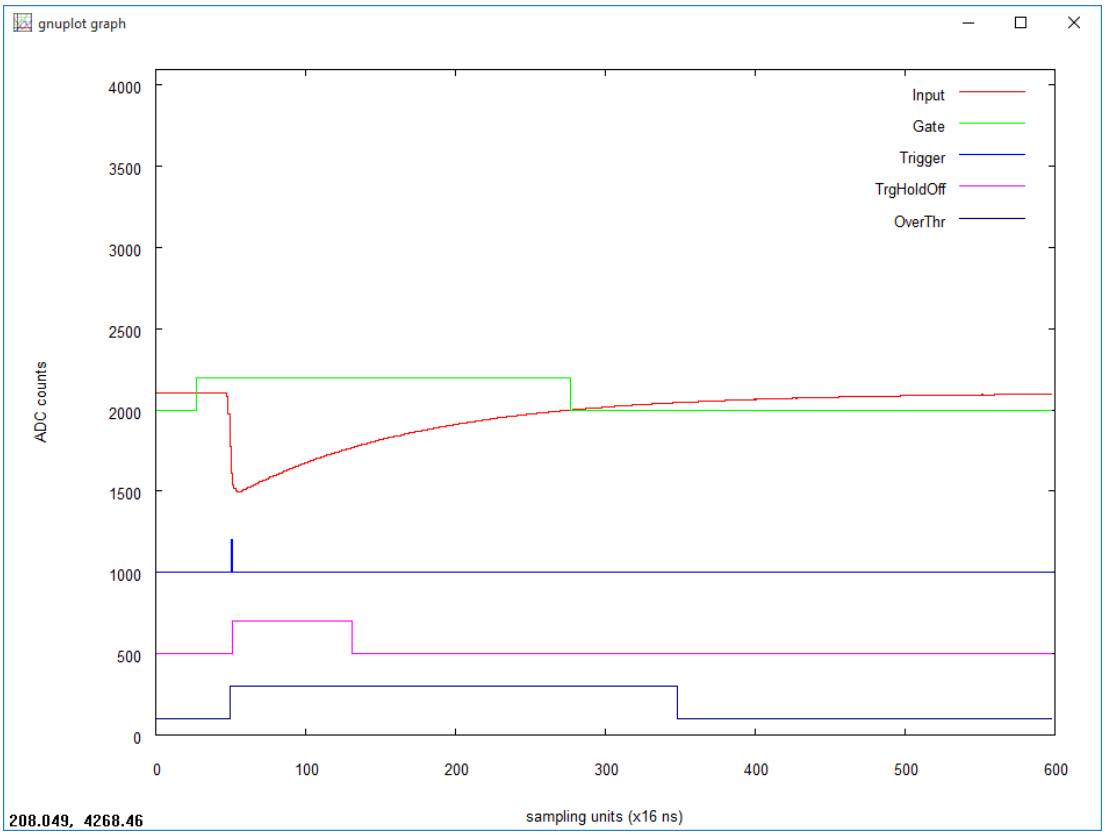

Fig. 5.8: the waveform plot of the DPP-QDC Demo software. The main signals processed by the DPP-QDC firmware are shown.

The spectrum is shown in **Fig. 5.9**. In this example, the spectrum of ^{60}Co emulated by the CAEN DT5800D is reproduced.

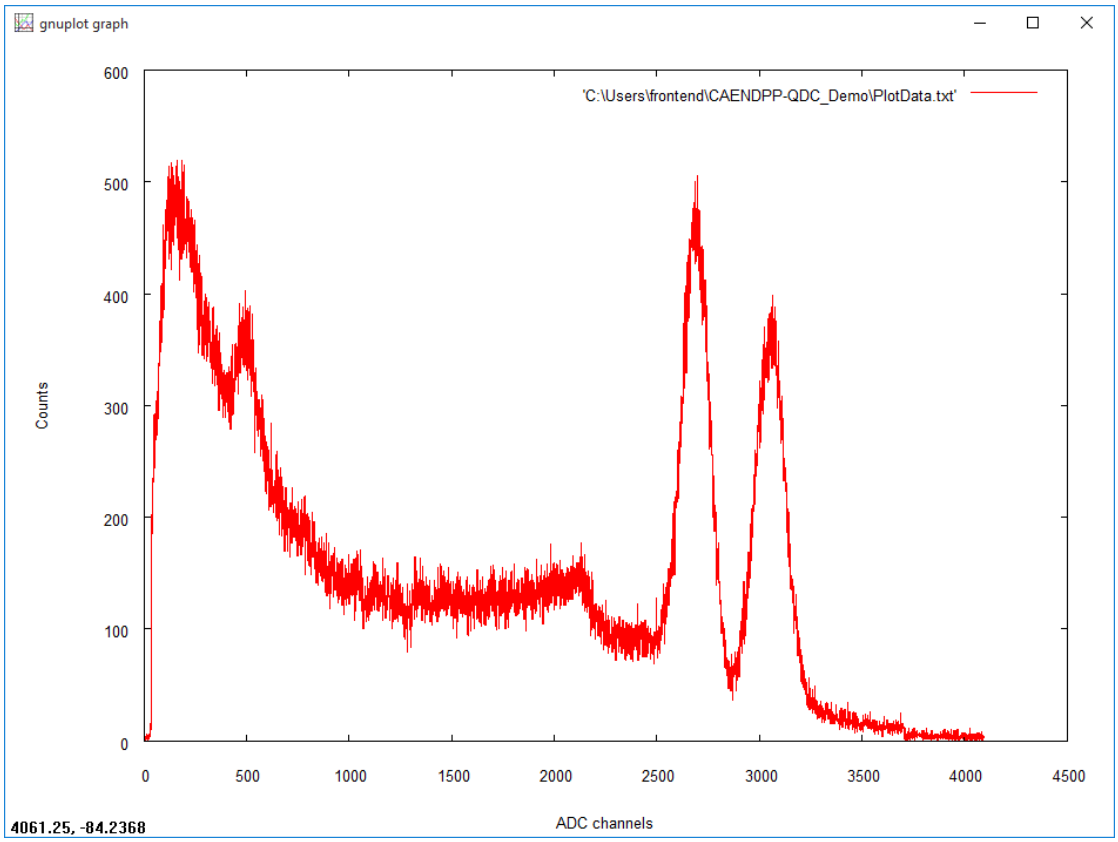

Fig. 5.9: the spectrum of ^{60}Co acquired using the DPP-QDC Demo software. The two typical photopeaks are clearly visible. The charge sensitivity was set in the configuration file to be 5.12 pC.

6. Technical support

To contact CAEN specialists for requests on the software, hardware, and board return and repair, it is necessary a MyCAEN+ account on www.caen.it:

https://www.caen.it/support-services/getting-started-with-mycaen-portal/

All the instructions for use the Support platform are in the document:

A paper copy of the document is delivered with CAEN boards.

The document is downloadable for free in PDF digital format at:

https://www.caen.it/wp-content/uploads/2022/11/Safety_information_Product_support_W.pdf

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