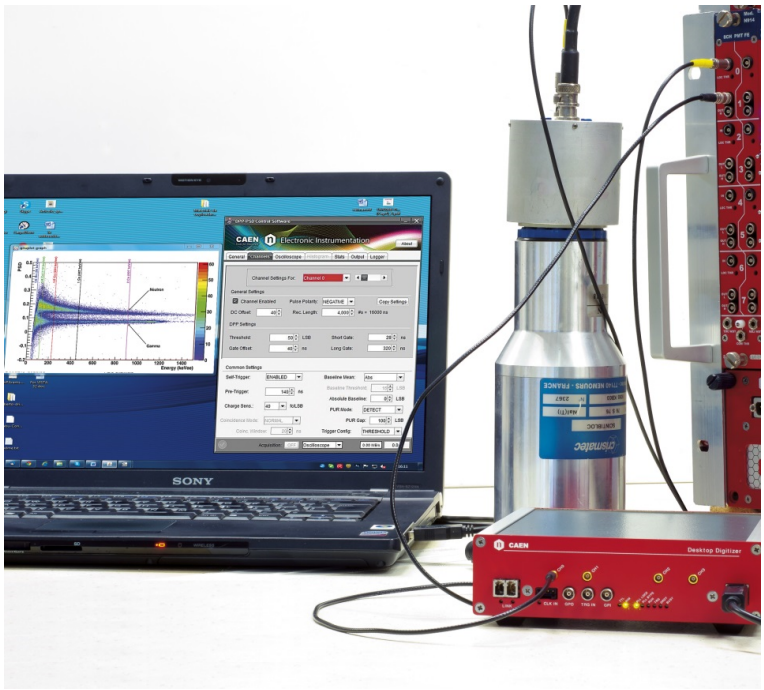
Rev. 7 - April 3rd, 2023

725 and 730 DPP-PSD

Register Description and Data Format



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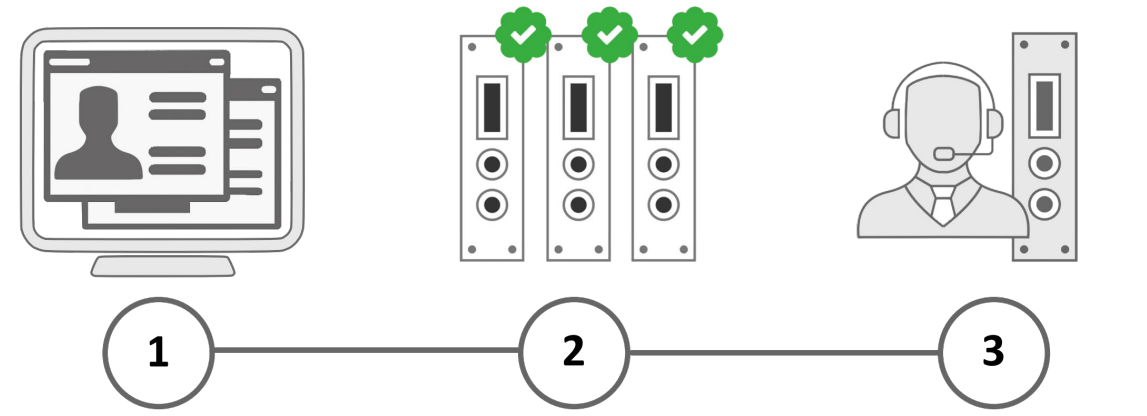

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Purpose of this Manual

The User Manual contains the full description of the DPP-PSD firmware registers and data format for 725(S) and 730(S) family series. The description is compliant with the DPP-PSD firmware revision **4.25_136.20** for 725 and 730 series and with **4.25_136.137** for 725S and 730S series. For future release compatibility check the firmware history files.

Change Document Record

Date	Revision	Changes
September 1st, 2015	00	Initial Release
October 2nd, 2015	01	Added support to 725 series
September 16th, 2016	02	Added registers: Charge Zero Suppression Threshold, PUR-GAP Threshold, Early Baseline Freeze. Added bits[11:10] to register CFD settings. Added option 101 to bits[2:0] of register DPP Algorithm Control. Added bit[25], bit[26], and bit[31] to register DPP Algorithm Control. Register 0x1n84 has been renamed from Local Trigger Management to DPP Algorithm Control 2. Modified bits[5:4] and bits[10:8] of register DPP Algorithm Control 2. Bit[7] of DPP Algorithm Control 2 register has been discontinued (use bit[19:18]=”10” for the same functionality). Added bits[17:16], bits[19:18], and bit[24] of register DPP Algorithm Control 2. Modified access to DPP Algorithm Control 2 register: bits [7:0] are common to the couple (writing to even channel writes also odd and vice-versa); all other bits are individual (different settings on odd and even are allowed). Modified bit[11] and bits[13:12] of register Board Configuration. Added bit[31] to register Board Configuration.
November 25th, 2016	03	Added step for 725 series in registers: Shaped Trigger Width, Trigger Hold-Off Width, Veto Width, and Early Baseline Freeze. Modified description of Number of Events per Aggregate to make it more clear.
February 26th, 2018	04	Modified register Veto Width, and digital traces in register Board Configuration. Modified register Run/Start/Stop Delay. Added bit[15] at DPP Algorithm Control. Modified bit[5:4] and added bits[26:25] of register DPP Algorithm Control 2. Added register Extended Veto Delay. Added bit[12] of register Acquisition Control.
August 28th, 2018	05	Added bit[27] and [28] of register DPP Algorithm Control 2.
April 24th, 2020	06	Added register Trigger Latency. Added Chap. DPP-PSD Memory Organization.
April 3rd, 2023	07	Added bit [23:20] of the register DPP Algorithm Control 2.

Symbols, abbreviated terms and notation

ADC	Analog-to-Digital Converter
AMC	ADC & Memory Controller
DAQ	Data Acquisition
DAC	Digital-to-Analog Converter
DC	Direct Current
DPP	Digital Pulse Processing
DPP-QDC	DPP for Charge to Digital Converter
DPP-PHA	DPP for Pulse Height Analysis
DPP-PSD	DPP for Pulse Shape Discrimination
LVDS	Low-Voltage Differential Signal
ROC	ReadOut Controller
USB	Universal Serial Bus

Reference Documents

[RD1] UM1935 - CAENDigitizer User & Reference Manual.

[RD2] UM5960 - CoMPASS User Manual.

[RD3] GD2827 - How to make coincidences with CAEN digitizers.

All CAEN documents can be downloaded at:
`www.caen.it/support-services/documentation-area`

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Limitation of Responsibility

If the warnings contained in this manual are not followed, CAEN will not be responsible for damage caused by improper use of the device. The manufacturer declines all responsibility for damage resulting from failure to comply with the instructions for use of the product. The equipment must be used as described in the user manual, with particular regard to the intended use, using only accessories as specified by the manufacturer. No modification or repair can be performed.

Disclaimer

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1 Registers and Data Format

All registers described in the User Manual are 32-bit wide. In case of VME access, **A24** and **A32** addressing mode can be used.

Register Address Map

The table below reports the complete list of registers that can be accessed by the user. The register names in the first column can be clicked to be redirected to the relevant register description. The register address is reported on the second column as a hex value. The third column indicates the allowed register access mode, where:

R	**Read only**. The register can be accessed in read only mode.
W	**Write only**. The register can be accessed in write only mode.
R/W	**Read and write**. The register can be accessed both in read and write mode.

According to the attribute reported in the fourth column, the following choices are available:

I **Individual register**. This kind of register has N instances, where N is the total number of channels in the board. Individual registers can be written either in single mode (individual setting) or broadcast (simultaneous write access to all channels). Read command must be individual.
Single access can be performed at address 0x1nXY, where n is the channel number, while broadcast write can be performed at the address 0x80XY. For example:

- access to address 0x1570 to read/write register 0x1n70 for channel 5 of the board;
- to write the same value for all channels in the board, access to 0x8070 (broadcast write). To read the corresponding value, access to the individual address 0x1n70.

G **Group register**. This kind of register is similar to the individual register since it has N instances, where N is the total number of channels in the board. Anyway, group registers are bind in couples, where couple m corresponds to channel 2m and channel 2m+1, and two channels of the same couple must have the same setting. Group registers can be written either in single group mode on the even channel of the couple (the same value is automatically written in the odd channel) or broadcast (simultaneous write access to all couples). Read command must be individual.
Single group access can be performed at address 0x1nXY, where n is the channel number, while broadcast write can be performed at the address 0x80XY.

Note: Some group registers might have bits that are common for the couple and some bits that are individual. Specific cases are reported in the register description itself.

Example:

- to read/write register 0x1n70 for couple 3 of the board (i.e. channel 6 and channel 7), access to address 0x1670. The same value is applied also to channel 7.
- to write the same value for all couples in the board, access to 0x8070 (broadcast write). To read the corresponding value, access to the individual address 0x1n70.

C **Common register**. Register with this attribute has a single instance, therefore read and write access can be performed at address 0x80XY only.

Register Name	Address	Mode	Attribute
Record Length	0x1n20, 0x8020	R/W	G
Input Dynamic Range	0x1n28, 0x8028	R/W	I
Number of Events per Aggregate	0x1n34, 0x8034	R/W	G
Pre Trigger	0x1n38, 0x8038	R/W	I
CFD settings	0x1n3C, 0x803C	R/W	I
Forced Data Flush	0x1n40, 0x8040	W	I
Charge Zero Suppression Threshold	0x1n44, 0x8044	R/W	I
Short Gate Width	0x1n54, 0x8054	R/W	I
Long Gate Width	0x1n58, 0x8058	R/W	I
Gate Offset	0x1n5C, 0x805C	R/W	I
Trigger Threshold	0x1n60, 0x8060	R/W	I
Fixed Baseline	0x1n64, 0x8064	R/W	I
Trigger Latency	0x1n6C, 0x8n6C	R/W	I
Shaped Trigger Width	0x1n70, 0x8070	R/W	I
Trigger Hold-Off Width	0x1n74, 0x8074	R/W	I
Threshold for the PSD cut	0x1n78, 0x8078	R/W	I
PUR-GAP Threshold	0x1n7C, 0x807C	R/W	I
DPP Algorithm Control	0x1n80, 0x8080	R/W	I
DPP Algorithm Control 2	0x1n84, 0x8084	R/W	G
Channel n Status	0x1n88	R	I
AMC Firmware Revision	0x1n8C	R	I
DC Offset	0x1n98, 0x8098	R/W	I
Channel n ADC Temperature	0x1nA8	R	I
Individual Software Trigger	0x1nC0, 0x80C0	W	I
Veto Width	0x1nD4, 0x8084	R/W	I
Early Baseline Freeze	0x1nD8, 0x80D8	R/W	I
Board Configuration	0x8000, 0x8004 (BitSet), 0x8008 (BitClear)	R/W	C
Aggregate Organization	0x800C	R/W	C
Channel ADC Calibration	0x809C	W	C
Channels Shutdown	0x80BC	W	C
Acquisition Control	0x8100	R/W	C
Acquisition Status	0x8104	R	C
Software Trigger	0x8108	W	C
Global Trigger Mask	0x810C	R/W	C
Front Panel TRG-OUT (GPO) Enable Mask	0x8110	R/W	C
LVDS I/O Data	0x8118	R/W	C
Front Panel I/O Control	0x811C	R/W	C
Channel Enable Mask	0x8120	R/W	C
ROC FPGA Firmware Revision	0x8124	R	C
Voltage Level Mode Configuration	0x8138	R/W	C
Software Clock Sync	0x813C	W	C
Board Info	0x8140	R	C
Analog Monitor Mode	0x8144	R/W	C
Event Size	0x814C	R	C
Time Bomb Downcounter	0x8158	R	C
Fan Speed Control	0x8168	R/W	C
Run/Start/Stop Delay	0x8170	R/W	C
Board Failure Status	0x8178	R	C
Disable External Trigger	0x817C	R/W	C
Trigger Validation Mask	0x8180+(4n), n=couple index	R/W	G
Front Panel LVDS I/O New Features	0x81A0	R/W	C
Buffer Occupancy Gain	0x81B4	R/W	C
Extended Veto Delay	0x81C4	R/W	C
Readout Control	0xEF00	R/W	C

Readout Status	0xEF04	R	C
Board ID	0xEF08	R/W	C
MCST Base Address and Control	0xEF0C	R/W	C
Relocation Address	0xEF10	R/W	C
Interrupt Status/ID	0xEF14	R/W	C
Interrupt Event Number	0xEF18	R/W	C
Aggregate Number per BLT	0xEF1C	R/W	C
Scratch	0xEF20	R/W	C
Software Reset	0xEF24	W	C
Software Clear	0xEF28	W	C
Configuration Reload	0xEF34	W	C
Configuration ROM Checksum	0xF000	R	C
Configuration ROM Checksum Length BYTE 2	0xF004	R	C
Configuration ROM Checksum Length BYTE 1	0xF008	R	C
Configuration ROM Checksum Length BYTE 0	0xF00C	R	C
Configuration ROM Constant BYTE 2	0xF010	R	C
Configuration ROM Constant BYTE 1	0xF014	R	C
Configuration ROM Constant BYTE 0	0xF018	R	C
Configuration ROM C Code	0xF01C	R	C
Configuration ROM R Code	0xF020	R	C
Configuration ROM IEEE OUI BYTE 2	0xF024	R	C
Configuration ROM IEEE OUI BYTE 1	0xF028	R	C
Configuration ROM IEEE OUI BYTE 0	0xF02C	R	C
Configuration ROM Board Version	0xF030	R	C
Configuration ROM Board Form Factor	0xF034	R	C
Configuration ROM Board ID BYTE 1	0xF038	R	C
Configuration ROM Board ID BYTE 0	0xF03C	R	C
Configuration ROM PCB Revision BYTE 3	0xF040	R	C
Configuration ROM PCB Revision BYTE 2	0xF044	R	C
Configuration ROM PCB Revision BYTE 1	0xF048	R	C
Configuration ROM PCB Revision BYTE 0	0xF04C	R	C
Configuration ROM FLASH Type	0xF050	R	C
Configuration ROM Board Serial Number BYTE 1	0xF080	R	C
Configuration ROM Board Serial Number BYTE 0	0xF084	R	C
Configuration ROM VCXO Type	0xF088	R	C

Record Length

Sets the record length for the waveform acquisition. The DPP-PSD algorithm is meant to acquire small size events, typically time stamps and charges, and possibly small portions of the waveform for post- processing. In case of record length less than 1792 samples, each channel of the couple has enough memory in its local buffer to acquire events independently from the other channel. For record length greater than 1792 samples, the couple must use an external SRAM memory, and a memory arbiter decides in ”fair mode” which event of the two channels is saved. Refer to the CoMPASS User Manual for additional details.
NOTE: in case of List mode, the Record Length is ignored.

Address	0x1n20, 0x8020
Mode	R/W
Attribute	G

Bit	Description
[13:0]	Number of samples in the waveform according to the formula Ns = N * 8, where Ns is the record length and N is the register value. For example, write N = 3 to acquire 24 samples. Each sample corresponds to 4 ns for 725 series and 2 ns for 730 series.
[31:14]	Reserved

Input Dynamic Range

This register sets the input dynamic range of each channel individually.

Address	0x1n28, 0x8028
Mode	R/W
Attribute	I

Bit	Description
[0]	Input Dynamic Range. Options are: 0 = 2 Vpp (default); 1 = 0.5 Vpp.
[31:1]	Reserved.

Number of Events per Aggregate

Each couple of channels has a fixed amount of RAM memory to save the events. The memory is divided into a programmable number of buffers, called ”aggregates”, whose number of events can be programmed by this register. The maximum number of events per aggregate depends on the aggregate size (which is defined by the number of aggregates per memory, 0x800C), and the event size (which is defined by the record length, 0x1n20, the acquisition mode and the event format, 0x8000).
Note: it is usually recommended to keep this value high to optimize the readout, except in case of small input rate, where it is recommended to use a smaller value (even 1). Since the memory cannot be read until the aggregate is full, setting a a small number of events per aggregate makes the events ready to be read in a shorter time scale. Users can also force the readout through the flush register.

Address	0x1n34, 0x8034
Mode	R/W
Attribute	G

Bit	Description
[9:0]	Number of events per aggregate.
[31:10]	Reserved

Pre Trigger

The Pre Trigger defines the number of samples before the trigger in the waveform saved into memory.

Address	0x1n38, 0x8038
Mode	R/W
Attribute	I

Bit	Description
[8:0]	Number of pre trigger samples according to the formula Ns = N * 4, where Ns is the pre trigger and N is the register value. For example, write N = 5 to set 20 samples of pre trigger. Each sample corresponds to 4 ns for 725 series and 2 ns for 730 series. NOTE: the Pre Trigger value must be greater than the Gate Offset value by a fixed value which depends on the waveform lenght. Too short values of Pre Trigger are automatically adjusted to the minimum correct value by the firmware itself.
[31:9]	Reserved.

CFD settings

Sets the Constant Fraction Discrimination (CFD) delay and fraction parameters

Address	0x1n3C, 0x803C
Mode	R/W
Attribute	I

Bit	Description
[7:0]	Set the CFD delay in time sample unit (4 ns for 725 series and 2 ns for 730 series).
[9:8]	Set the CFD fraction. Options are: 00 : fraction = 25%; 01 : fraction = 50%; 10 : fraction = 75%; 11 : fraction = 100%.
[11:10]	Sets the Interpolation Points, corresponding to the n-th sample before and after the zero crossing that are used for the linear interpolation. These bits can be used both in case of CFD and LED (Leading Edge Discrimination). Options are: 00: the sample before and after the zero crossing; 01: second sample before and after the zero crossing; 10: third sample before and after the zero crossing; 11: fourth sample before and after the zero crossing.
[31:12]	Reserved

Forced Data Flush

Data events are grouped into aggregates of N events each, where N can be programmed through register 0x1n34. As soon as an aggregate reaches N events then it is ready to be read. An aggregate containing a number of events smaller than N cannot be read and must be forced to flush its current data. This is for example the case of low input rate, where the board might appear empty (no data) even if a small amount of events is already stored in the buffer, or at the end of the run where the last aggregate might be incomplete. A write access to this register forces the read of the current incomplete aggregate.

Address	0x1n40, 0x8040
Mode	W
Attribute	I

Bit	Description
[31:0]	A write access to this register causes the flush of the current aggregate.

Charge Zero Suppression Threshold

Input signals of small amplitude can be selected by setting a small threshold level. Unfortunately, this might result in an increase of the noise level. The noise can be distinguished by real signals in the energy spectrum, since it usually appears as a peak close to the 0 energy. This register allows the user to set a threshold in the spectrum (Qthr) to cut events with charge Qlong < Qthr.

Address	0x1n44, 0x8044
Mode	R/W
Attribute	I

Bit	Description
[15:0]	Threshold value, where 1 LSB corresponds to a specific value of charge which depends on the Charge Sensitivity value.
[31:16]	Reserved

Short Gate Width

Sets the Short Gate width for the charge integration of the fast component in the Pulse Shape Discrimination

Address	0x1n54, 0x8054
Mode	R/W
Attribute	I

Bit	Description
[11:0]	Number of samples for the Short Gate width. Each sample corresponds to 4 ns for 725 series and 2 ns for 730 series.
[31:12]	Reserved

Long Gate Width

Sets the Long Gate width for the charge integration of the slow component in the Pulse Shape Discrimination. The Long integration Gate is also used for the energy spectra calculation

Address	0x1n58, 0x8058
Mode	R/W
Attribute	I

Bit	Description
[15:0]	Number of samples for the Long Gate width. Each sample corresponds to 4 ns for 725 series and 2 ns for 730 series.
[31:16]	Reserved

Gate Offset

To correctly integrate the input pulse, the integration Gate starts before the trigger position. The Gate Offset defines how many samples the Gate starts before the trigger.

Address	0x1n5C, 0x805C
Mode	R/W
Attribute	I

Bit	Description
[7:0]	Number of samples of the Gate Offset. Each sample corresponds to 4 ns for 725 series and 2 ns for 730 series.
[31:8]	Reserved

Trigger Threshold

Sets the Trigger Threshold value for the Leading Edge discrimination

Address	0x1n60, 0x8060
Mode	R/W
Attribute	I

Bit	Description
[13:0]	Set the number of LSB counts for the Trigger Threshold, where 1 LSB = 0.12 mV for 725 and 730 series with 2 Vpp input range, and 1 LSB = 0.03 mV for 725 and 730 series with 0.5 Vpp input range. The threshold is referred to the baseline level and can be used to trigger on Leading Edge Discrimination or to arm the digital Constant Fraction Discrimination.
[31:14]	Reserved.

Fixed Baseline

The baseline calculation can be performed either dynamically or statically. In the first case the user can set the samples of the moving average window through register 0x1n80. In the latter case the user must disable the automatic baseline calculation through bits[22:20] of register 0x1n80 and set the desired value of fixed baseline through this register. The baseline value then remains constant for the whole acquisition.
Note: This register is ignored in case of dynamic calculation.

Address	0x1n64, 0x8064
Mode	R/W
Attribute	I

Bit	Description
[13:0]	Value of Fixed Baseline in LSB counts
[31:14]	Reserved

Trigger Latency

This register allows the user to set a time window (latency) to be added to the Shaped Trigger Width (i.e. the lenght of the correlation window) required to take into account the latency in the trigger propagation from the piggyback to the motherboard when setting coincidence/anticoincidence between the digitizer channels.
Mandatory values are:
- 0x9 for the x720 (DT5790) and x751 series
- 0x2 for the x725 and x730 series when setting coincidence/anticoincidence within the same channel couple
- 0x9 for the x725 and x730 series when setting coincidence/anticoincidence between channels belonging to different couples.

Address	0x1n6C, 0x8n6C
Mode	R/W
Attribute	I

Bit	Description
[9:0]	Value of the latency in trigger clock cycles: 8 ns for x730 and 16 ns for x725 family.
[31:10]	Reserved

Shaped Trigger Width

The Shaped Trigger is a logic signal of programmable width generated by a channel in correspondence to its local self-trigger (that is the output of the leading edge discriminator). It is used to propagate the trigger to the other channels of the board and to other external boards, as well as to feed the coincidence trigger logic.

Address	0x1n70, 0x8070
Mode	R/W
Attribute	I

Bit	Description
[9:0]	Shaped Trigger width in steps of 16 ns for 725 series and 8 ns for 730 series.
[31:10]	Reserved

Trigger Hold-Off Width

The Trigger Hold-Off is a logic signal of programmable width generated by a channel in correspondence with its local self- trigger (that is the output of the leading edge discriminator). Other triggers are inhibited for the overall Trigger Hold-Off duration

Address	0x1n74, 0x8074
Mode	R/W
Attribute	I

Bit	Description
[15:0]	Trigger Hold-Off width expressed in steps of 16 ns for 725 series and 8 ns for 730 series.
[31:16]	Reserved

Threshold for the PSD cut

Sets the PSD threshold to online select events according to their PSD value. PSD ranges from 0 to 1.

Address	0x1n78, 0x8078
Mode	R/W
Attribute	I

Bit	Description
[9:0]	Set the PSD threshold value. The desired value has to be multiplied by 1024. For example for a PSD threshold of 0.12, write 122 (= 0.12 * 1024). Set bits[28:27] of register 0x1n80 to enable the cut on gamma or neutron respectively.
[31:10]	Reserved

PUR-GAP Threshold

A pile-up event is detected when there is a situation of ”peak-valley-peak” inside the same gate. The gap between the valley and the peak can be programmed through this register. Refer to the CoMPASS User Manual for additional details.

Address	0x1n7C, 0x807C
Mode	R/W
Attribute	I

Bit	Description
[11:0]	PUR-GAP value in LSB unit, where 1 LSB = 0.12 mV for 725 and 730 series with 2 Vpp input range, and 1 LSB = 0.03 mV for 725 and 730 series with 0.5 Vpp input range.
[31:12]	Reserved

DPP Algorithm Control

Management of the DPP algorithm features

Address	0x1n80, 0x8080
Mode	R/W
Attribute	I

Bit	Description
[2:0]	Charge Sensitivity: defines how many fC of charge correspond to one channel of the energy spectrum. Options for Input Range = 2 Vpp are: 000: 5 fC; 001: 20 fC; 010: 80 fC; 011: 320 fC; 100: 1.28 pC. 101: 5.12 pC. Options for Input Range = 0.5 Vpp are: 000: 1.25 fC; 001: 5 fC; 010: 20 fC; 011: 80 fC; 100: 320 fC. 101: 1.28 pC.
[3]	Reserved
[4]	Charge Pedestal: when enabled a fixed value of 1024 is added to the charge. This feature is useful in case of energies close to zero.
[5]	Trigger Counting. Options are: 0 (default value): the shaped trigger used for TRG-OUT and coincidences reflects only the accepted self-triggers, i.e. the real events saved into memory; 1: the shaped trigger used for TRG-OUT and coincidences reflects all the self-triggers, even those of rejected events (for example consecutive events on the same gate, or events occurring during the board busy condition).
[6]	Discrimination mode for the event selection. Options are: 0 (default value): leading edge discrimination (LED); 1: digital constant fraction discrimination (CFD).
[7]	Pile-up within the gate (where a pile-up is defined by a peak-valley-peak condition) is counted as a trigger. In this mode, pile-up pulses contribute to the ICR tick and to the TRG-OUT generation. Options are: 0 = disabled; 1 = enabled.
[8]	Internal Test Pulse. It is possible to enable an internal test pulse for debugging purposes. The ADC counts are replaced with the built-in pulse emulator. Options are: 0: disabled. 1: enabled.
[10:9]	Test Pulse Rate. Set the rate of the built-in test pulse emulator. Options are: 00: 1 kHz for 730 series, 500 Hz for 725 series; 01: 10 kHz for 730 series, 5 kHz for 725 series; 10: 100 kHz for 730 series, 50 kHz for 725 series; 11: 1 MHz for 730 series, 500 kHz for 725 series.
[14:11]	Reserved.
[15]	When enabled, this bit forces the baseline calculation to restart at the end of the long gate, regardless the signal over/under threshold. This option is useful in case of fast and short pulses (no tails) sitting over a fluctuating baseline. Options are: 0 = disabled (default); 1 = enabled.

[16]	Pulse Polarity. Options are: 0: positive pulse; 1: negative pulse.
[17]	Reserved
[19:18]	Trigger Mode. Options are: 00: Normal mode. Each channel can self- trigger independently from the other channels. 01: Coincidence mode. Each channel saves the event only when a validation signal occurs inside the shaped trigger coincidence window. 10: Reserved. 11: Anti-coincidence mode. Each channel saves the event only when no validation signal occurs inside the shaped trigger coincidence window.
[22:20]	Baseline Mean. Sets the number of samples for the baseline mean calculation. Options are: 000: Fixed: the baseline value is fixed to the value set in register 0x1n64; 001: 16 samples; 010: 64 samples; 011: 256 samples; 100: 1024 samples.
[23]	Reserved.
[24]	Disable Self Trigger. When disabled, the self-trigger is still propagated to the mother board for coincidence logic and TRG-OUT front panel connector, though it is not used by the channel to acquire the event. Options are: 0: self-trigger used to acquire and propagated to the trigger logic; 1: self-trigger only propagated to the trigger logic.
[25]	Discard events with Qlong < Qthr, where Qthr is defined through bits[15:0] of register 0x1n44. Options are: 0: Disabled; 1: Enabled.
[26]	Pile-Up Rejection. Options are: 0: Disabled 1: Enabled
[27]	Enable PSD cut below threshold (to cut on gammas)
[28]	Enable PSD cut above threshold (to cut on neutrons).
[29]	Over-range Rejection. Reject the event when the ADC sample value is over/under the dynamic range during the long gate integration. Options are: 0: disabled; 1: enabled.
[30]	Trigger Hysteresis. The trigger can be inhibited during the trailing edge of a pulse, to avoid re-triggering on the pulse itself. Options are: 0 (default value): enabled; 1: disabled.
[31]	Detection of signals of opposite polarity to inhibit the zero crossing on CFD. Options are: 0: Enabled; 1: Disabled.

DPP Algorithm Control 2

This register controls the DPP features such as the local shaped trigger and validation, the readout data format, etc. NOTE: the access to this register has been modified from firmware revision greater than 136.9. Bits[7:0] are common to the couple (writing to the even channel writes also the odd and viceversa), while all other bits are individual (different settings on odd and even channels are allowed).

Address	0x1n84, 0x8084
Mode	R/W
Attribute	G

Bit	Description
[1:0]	Local Shaped Trigger mode. Sets how to combine the self-triggers of the channels inside each couple to generate a trigger request to the mother board. Enable Local Shaped Trigger mode by setting bit[2] of this register. Options are: 00: AND of the channels 01: even channel of the couple only 10: odd channel of the couple only 11: OR of the channels
[2]	Enable Local Shaped Trigger. Options are: 0: disabled; 1: enabled
[3]	Reserved
[5:4]	Local Trigger Validation mode. Sets how the trigger validation signal (val) is generated for the two channels inside a couple with respect to the local trigger (trg) or to the validation from mother-board. Enable the Local Trigger Validation mode by setting bit[6] of this register. Options are: 00: reserved; 01: val0 = val1 = signal from mother-board mask; 10: AND (val0 = val1 = trg0 AND trg1); 11: OR (val0 = val1 = trg0 OR trg1). This option must be used with bits[19:18] of register 0x1n80 equal to 00.
[6]	Enable Local Trigger Validation. Options are: 0: disabled; 1: enabled.
[7]	Reserved from firmware revision 136.9. Refer to bits[19:18]=10 to set a veto from individual trigger logic.
[10:8]	Extras Word options. The channel aggregate data format has a 32 bit word, called EXTRAS word which can be configured to have the following information (firmware release greater than 136.2): 000: bits[31:16] = Extended Time Stamp, bits[15:0] = Baseline * 4; 001: bits[31:16] = Extended Time Stamp, bits[15:0] = Flags; 010: bits[31:16] = Extended Time Stamp, bits[15:10] = Flags, bits[9:0] = Fine Time Stamp; 011: Reserved; 100: bits[31:16] = Lost Trigger Counter, bits[15:0] = Total Trigger Counter; 101: bits[31:16] = Positive Zero Crossing, bits[15:0] = Negative Zero Crossing; 110: Reserved; 111: Fixed value = 0x12345678 (debug use only). ”Flags” correspond to: bit[15]: Trigger Lost (the first event after a trigger lost has this flag set); bit[14]: Over-range (identifies an event saturating inside the gate - clipping); bit[13]: 1024 trigger counted (every 1024 counted events this flag is high); bit[12]: N lost trigger counted (every N counted lost events this flag is high, where N is set from bits[17:16] of register 0x1n84).
[11]	Use smoothed signal (see bits[15:12]) for charge integration. Options are: 0: disabled; 1: enabled.

[15:12]	Input smoothing factor. Sets the number of averaged samples for smoothing the input pulse. The smoothed input can be used both for CFD and LED triggering. Options are: 0000: disabled; 0001: 2 samples; 0010: 4 samples; 0011: 8 samples; 0100: 16 samples.
[17:16]	Select the step for the trigger counter rate flag (see bits[10:8]). Options are: 00 = 1024 (default); 01 = 128; 10 = 8192.
[19:18]	Defines the source of the veto: 00 = disabled; 01 = the veto signal is common among all channels. It can be set through register 0x810C, and it can be generated by an external trigger or by a combination of the trigger requests from couples; 10 = the veto signal is individually set for the couple of channels (each couple can have a different veto). It can be set through register 0x8180 (+4n), where n is the couple index, and it can be generated by an external trigger or by a combination of the trigger requests from couples; 11 = the veto signal comes from events saturating inside the gate (clipping) or from events with opposite polarity. Refer to the CoMPASS User Manual for additional details. NOTE: from revision 136.9 the former bit[7] option has been discontinued. Use option ”10” for the same functionality.
[19]	Reserved
[23:20]	These bits allows to select which signal is passed from the piggyback to the motherboard. The motherboard can then use it for its own processing or redirect it on the TRG-OUT front panel connector when bit [17:16] of the 0x811C register are set to 10. Options are: - 0001: Ovethrehsold - 0010: Channel self-trigger (default option) - 0011: Pile up - 0100: PIle up or self-trigger - 0101: Veto - 0110: Coincidence - 0111: Trigger validation - 1000: Trigger valid acquisition window - 1001: Neutron pulse (signal is sent as soon as neutron is identified and lasts 1 clock step) - 1010: Gamma pulse (signal is sent as soon as gamma is identified and lasts 1 clock step) - 1011: Neutron pulse (signal is sent as soon as neutron is identified and lasts until the end of the gate) - 1100: Neutron pulse (signal is sent at the end of the gate and lasts 1 clock step)
[24]	Mark saturated pulses (clipped) in the gate by setting bit[15] = 1 of the CHARGE word (Qlong-Qshort) in the aggregate data format. Refer to the CoMPASS User Manual for additional details. Options are: 0: Disabled 1: Enabled
[26:25]	Additional Local Trigger Validation options: 00 = options from bits[5:4]; 01 = validation from paired channel AND mother board; 10 = validation from paired channel OR mother board; 11 = reserved. Note: bit[6] of this register must be enabled. Note: bit[5:4] of this register must be set to 00. Note: when using option 01 and 10 there are about 30 ns of transition window between coincidence and not coincidence level. This should be taken into account in the offline data processing by the user.
[27]	Veto signal operating mode: 0: the Veto is used after the charge integration to discard the event data (before saving to the memory buffer). In this mode, the Veto can arrive also during the integration gate. 1: the Veto is used to inhibit the self-triggers. In this mode, the charge integration does not start when the Veto is active and there is no dead-time for vetoed triggers

[28]	When enabled, this bit allows the user to reset the time stamp when the external veto (coming from TRG-IN) is active. The aim of this option is to create data spills synchronized to an external signal. Each spill is separated in the data flow by the restarting of the time stamp.
[31:29]	Reserved

Channel n Status

This register contains the status information of channel n.

Address	0x1n88
Mode	R
Attribute	I

Bit	Description
[1:0]	Reserved.
[2]	If 1, the SPI bus is busy.
[3]	If 1, the ADC calibration has been done.
[7:4]	Reserved.
[8]	ADC Power Down. When set to 1, it means that the ADC of channel n has been shut down due to an over-temperature condition.
[31:9]	Reserved.

AMC Firmware Revision

Returns the DPP firmware revision (mezzanine level).
To control the mother board firmware revision see register 0x8124.
For example: if the register value is 0xC3218303:
- Firmware Code and Firmware Revision are 131.3;
- Build Day is 21;
- Build Month is March;
- Build Year is 2012.

NOTE: since 2016 the build year started again from 0.

Address	0x1n8C
Mode	R
Attribute	I

Bit	Description
[7:0]	Firmware revision number.
[15:8]	Firmware DPP code. Each DPP firmware has a unique code.
[19:16]	Build Day (lower digit).
[23:20]	Build Day (upper digit).
[27:24]	Build Month. For example: 3 means March, 12 is December.
[31:28]	Build Year. For example: 0 means 2000, 12 means 2012. NOTE: since 2016 the build year started again from 0.

DC Offset

This register allows to adjust the baseline position (i.e. the 0 Volt) of the input signal on the ADC scale. The ADC scale ranges from 0 to 2^NBit - 1, where NBit is the number of bits of the on-board ADC. The DAC controlling the DC Offset has 16 bits, i.e. it goes from 0 to 65535 independently from the NBit value and the board type.
Typically a DC Offset value of 32K (DAC mid-scale) corresponds to about the ADC mid-scale. Increasing values of DC Offset make the baseline decrease. The range of the DAC is about 5% (typ.) larger than the ADC range, hence DAC settings close to 0 and 64K correspond to ADC respectively over and under range.
WARNING: before writing this register, it is necessary to check that bit[2] = 0 at 0x1n88, otherwise the writing process will not run properly! After writing, the user is recommended to wait for few seconds before a new RUN to let the DAC output (i.e. the new programmed DC offset) get stabilized.

Address	0x1n98, 0x8098
Mode	R/W
Attribute	I

Bit	Description
[15:0]	DC Offset value in DAC LSB unit
[31:16]	Reserved

Channel n ADC Temperature

This register monitors the temperature of the ADC chips.
NOTE: if the temperature varies significantly during the digitizer operation, the user is recommended to perform a new channel calibration procedure (see register 0x809C) to restore the board performance. This is not true in case of 725S and 730S as these models do not require any calibration.

Address	0x1nA8
Mode	R
Attribute	I

Bit	Description
[7:0]	ADC Chip Temperature (expressed in °C). Values are signed, ranging from - 64°C to 127°C.
[31:8]	Reserved.

Individual Software Trigger

Sends the Software Trigger to the individual channel n. This is not affected by the Trigger Validation, i.e. the Individual Software Trigger can be issued also when coincidences are enabled without being affected.

Address	0x1nC0, 0x80C0
Mode	W
Attribute	I

Bit	Description
[31:0]	A write access to this register enables a software trigger for channel n.

Veto Width

When a veto is enabled through register 0x1n84, this register sets the veto duration.
Note: A Veto Width equal to 0 means that the veto lasts for the duration of the signal that generated it. A Veto Width different from 0 sets the veto duration by the amount of time written in the register.

Address	0x1nD4, 0x8084
Mode	R/W
Attribute	I

Bit	Description
[15:0]	Value of the veto width.
[17:16]	Steps of the veto width. Options are: 00: 16 ns for 725, 8 ns for 730; 01: 4 us for 725, 2 us for 730; 10: 1048 us for 725, 524 us for 730; 11: 264 ms for 725, 134 ms for 730.
[31:18]	Reserved

Early Baseline Freeze

When the baseline is dynamically evaluated by the firmware, its calculation stops before the gate by a programmable amount of time, that can be set by this register. The baseline value is then frozen n samples before the trigger. Modifying this register can be useful in case of slow signals, like the gaussian output of a shaping amplifier. The user can program a gate of short duration centered in the peak position and freeze the baseline many samples before the gate, thus avoiding that the baseline follows the input and produces a wrong result.

Address	0x1nD8, 0x80D8
Mode	R/W
Attribute	I

Bit	Description
[9:0]	Baseline freeze time expressed in steps of 16 ns for 725 and 8 ns for 730. Default value is 2, which is useful for signals from PMTs.
[31:10]	Reserved.

Board Configuration

This register contains general settings for the board configuration.

Address	0x8000, 0x8004 (BitSet), 0x8008 (BitClear)
Mode	R/W
Attribute	C

Bit	Description
[0]	Enable Automatic Data Flush: in case of very slow rate, this command forces the automatic data readout in a time window of 16-32 ms, even if the buffer is not completed. This is valid from AMC firmware revision greater than 136.2. Options are: 0: disabled (default value); 1: enabled.
[1]	Reserved: must be 0
[2]	Trigger Propagation: enables the propagation of the individual trigger from mother board individual trigger logic to the mezzanine. This is required in case of coincidence trigger mode
[3]	Reserved: must be 0
[4]	Reserved: must be 1.
[7:5]	Reserved: must be 0
[8]	Individual trigger: must be 1
[10:9]	Reserved: must be 0
[11]	Dual Trace: in oscilloscope or mixed mode, it is possible to plot two different waveforms. When the dual trace is enabled, the samples of the two signals are interleaved, thus each waveform is recorded at half of the ADC frequency. According to the Analog Probe selection (see bits[13:12]) the following selections are available. Dual Trace = 0, Analog Probe = 0 => Trace 1 = Input, Trace 2 = N/A; Dual Trace = 0, Analog Probe = 1 => Trace 1 = CFD, Trace 2 = N/A; Dual Trace = 1, Analog Probe = 0 => Trace 1 = Input, Trace 2 = Baseline; Dual Trace = 1, Analog Probe = 1 => Trace 1 = CFD, Trace 2 = Baseline; Dual Trace = 1, Analog Probe = 2 => Trace 1 = Input, Trace 2 = CFD. Note: The CFD trace is available only if bit[6] of register 0x1n80 is equal to 1. If bit[6] = 0, the CFD trace becomes the Smoothed Input (refer to bits[15:12] of register 0x1n84).
[13:12]	Analog Probe selection: selects which signal is associated to the analog probes. According to the Dual Trace value (see bit[11]) the following selections are available. Dual Trace = 0, Analog Probe = 0 => Trace 1 = Input, Trace 2 = N/A; Dual Trace = 0, Analog Probe = 1 => Trace 1 = CFD, Trace 2 = N/A; Dual Trace = 1, Analog Probe = 0 => Trace 1 = Input, Trace 2 = Baseline; Dual Trace = 1, Analog Probe = 1 => Trace 1 = CFD, Trace 2 = Baseline; Dual Trace = 1, Analog Probe = 2 => Trace 1 = Input, Trace 2 = CFD. Note: The CFD trace is available only if bit[6] of register 0x1n80 is equal to 1. If bit[6] = 0, the CFD trace becomes the Smoothed Input (refer to bits[15:12] of register 0x1n84).
[15:14]	Reserved: must be 0
[16]	Waveform Recording: enables the data recording of the waveform. The user must define the number of samples to be saved in the Record Length (register 0x1n20). According to the Analog Probe option one or two waveforms are saved. Options are: 0: disabled; 1: enabled.
[17]	Extras Recording: when enabled the EXTRAS word is saved into the event data. Refer to the ”Channel Aggregate Data Format” chapter below for more details about the EXTRAS word. Options are: 0: disabled; 1: enabled.
[18]	Time Stamp Recording: must be 1
[19]	Charge Recording: must be 1
[22:20]	Reserved: must be 0

[25:23]	Digital Virtual Probe 1: when the mixed mode is enabled, the following digital virtual probes can be selected: 000 = ”Long Gate”; 001 = ”Over Threshold”, digital signal that is 1 when the input signal is over the requested threshold; 010 = ”Shaped TRG”, logic signal of programmable width generated by a channel in correspondence with its local self- trigger. It is used to propagate the trigger to the other channels of the board and to other external boards, as well as to feed the coincidence trigger logic; 011 = ”TRG Val. Acceptance Win.”, logic signal corresponding to the time window where the coincidence validation is accepted. The validation enables the event dump into the memory; 100 = ”Pile Up”, logic pulse set to 1 when a pile up event occurred. This trace remains high for the whole long gate duration; 101 = ”Coincidence”, logic pulse set to 1 when a coincidence occurred; 110 = Reserved; 111 = ”Trigger”
[28:26]	Digital Virtual Probe 2: when the mixed mode is enabled, the following digital virtual probes can be selected: 000 = ”Short Gate”; 001 = ”Over Threshold”, digital signal that is 1 when the input signal is over the requested threshold; 010 = ”TRG Validation”, digital signal that is 1 when a coincidence validation signal comes from the mother board FPGA; 011 = ”TRG HoldOff”, logic signal of programmable width generated by a channel in correspondence with its local self- trigger. Other triggers are inhibited for the overall Trigger Hold-Off duration; 100 = ”Pile Up Trigger”, digital signal that is 1 whenever a pile-up occurred; 101 = ”PSD cut high”, logic pulse that is 1 when the event has a PSD value greater than the set PSD threshold (see register 0x1n78); 110 = ”Baseline Freeze”, logic pulse that is 1 when the baseline calculation is frozen for the gate integration or during the trigger hold-off; 111 = ”Trigger”.
[30:29]	Reserved: must be 0
[31]	Enable/Disable the digital traces in the waveform data. Options are: 0: Enabled 1: Disabled

Aggregate Organization

The internal memory of the digitizer can be divided into a programmable number of aggregates, where each aggregate contains a specific number of events. This register defines how many aggregates can be contained in the memory. Note: this register must not be modified while the acquisition is running.

Address	0x800C
Mode	R/W
Attribute	C

Bit	Description
[3:0]	Aggregate Organization Nb: the number of aggregates is equal to N_aggr = 2^Nb. The corresponding values of Nb and N_aggr are: Nb: N_aggr 0x0 - 0x1: Not used 0x2 : 4 0x3 : 8 0x4 : 16 0x5 : 32 0x6 : 64 0x7 : 128 0x8 : 256 0x9 : 512 0xA : 1024
[31:4]	Reserved: must be 0

Channel ADC Calibration

This register is meaningless for x725S and x730S digitizers as they do not require channel calibration; writing to this register does not generate any error (BERR) but simply has no effect.

Other x725 and x730 digitizers require a channel calibration to achieve the best performances. A calibration of the ADCs is automatically performed by the firmware at the power-on, but the user is recommended to manually execute the calibration after the ADCs have stabilized their operating temperature (see register 0x1nA8). The calibration will not need to be repeated at each acquisition run, unless the operating temperature varies significantly, or clock settings are modified (e.g. switching from internal to external clock).
WARNING: before writing this register, it is necessary to check that bit[2] = 0 of register 0x1n88, otherwise the writing process cannot run properly.
WARNING: It is normally not required to calibrate after a board reset but, if a Reset command is intentionally issued to the digitizer (write access at 0xEF24) to be directly followed by a calibration procedure, it is recommended to wait for the board to reach stable conditions (indicatively 100 ms) before to start the calibration.
WARNING: at power-on, a Sync command is issued by the firmware to the ADCs to synchronize all of them to the board's clock. In the standard operating, this command is not required to be repeated by the user. If a Sync command is intentionally issued (see register 0x813C), the user must consider that a new calibration procedure is needed for a correct board operating.

Address	0x809C
Mode	W
Attribute	C

Bit	Description
[31:0]	Write any value to start the automatic simultaneous calibration of the ADC for all channels of the board. Bit[3] of register 0x1n88 will be set to 0. Poll this bit until it returns to 1.

Channels Shutdown

This register allows to switch on all the channels of the board after they have been switched off by the automatic shutdown procedure. Channels must be switched on only once the board exits the temperature protection condition.
NOTE: bit[0] is forced to 1 while the board remains in the temperature protection condition.
NOTE: it is not recommended to use this register to shutdown the channels (bit[0] = 1) when the board is out of the temperature protection condition.

Address	0x80BC
Mode	W
Attribute	C

Bit	Description
[0]	Channels Shutdown. Options are: 0 = no shutdown command is issued; 1 = a shutdown command is issued.
[31:1]	Reserved

Acquisition Control

This register manages the acquisition settings.

Address	0x8100
Mode	R/W
Attribute	C

Bit	Description
[1:0]	Start/Stop Mode Selection (default value is 00). Options are: 00 = SW CONTROLLED. Start/stop of the run takes place on software command by setting/resetting bit[2] of this register; 01 = S-IN/GPI CONTROLLED (S-IN for VME, GPI for Desktop/NIM). Acquisition must be armed by setting bit[2] = 1, then the run can optionally START/STOP ON LEVEL or START ON EDGE according to bit[11] (NOTE: the START ON EDGE option is implemented from ROC FPGA fw revision 4.22 on); 10 = FIRST TRIGGER CONTROLLED. If the acquisition is armed (i.e. bit[2] = 1), then the run starts on the first trigger pulse (rising edge on TRG- IN); this pulse is not used as input trigger, while actual triggers start from the second pulse. The stop of Run must be SW controlled (i.e. bit[2] = 0); 11 = LVDS CONTROLLED (VME only). It is like option 01 but using LVDS (RUN) instead of S- IN. The LVDS can be set using registers 0x811C and 0x81A0.
[2]	Acquisition Start/Arm (default value is 0). When bits[1:0] = 00, this bit acts as a Run Start/Stop. When bits[1:0] = 01, 10, 11, this bit arms the acquisition and the actual Start/Stop is controlled by an external signal. Options are: 0 = Acquisition STOP (if bits[1:0]=00); Acquisition DISARMED (others); 1 = Acquisition RUN (if bits[1:0]=00); Acquisition ARMED (others).
[3]	Reserved.
[5:4]	Reserved
[6]	PLL Reference Clock Source (Desktop/NIM only). Default value is 0. Options are: 0 = internal oscillator (50 MHz); 1 = external clock from front panel CLK-IN connector. NOTE: this bit is reserved in case of VME boards.
[7]	Reserved.
[8]	LVDS I/O Busy-In Enable (VME only). Default value is 0. This bit must be enabled to let the board accept the Busy signal as input on the LVDS I/Os. Options are: 0 = disabled; 1 = enabled. NOTE: this bit is supported only by VME boards and meaningful only if the LVDS new features are enabled (bit[8]=1 of register 0x811C), the LVDS I/O mode is set to nBusy/nVeto (see register 0x81A0), and the LVDS I/Os are set as inputs (see register 0x811C).
[9]	LVDS I/O Veto Enable (VME only). Default value is 0. The LVDS I/Os can be programmed to accept a Veto signal as input, or to transfer it as output. Options are: 0 = disabled (default); 1 = enabled. NOTE: this bit is supported only by VME boards and meaningful only if the LVDS new features are enabled (bit[8]=1 of register 0x811C). Register 0x81A0 should also be configured for nBusy/nVeto.
[10]	Reserved.

[11]	LVDS I/O RunIn Enable Mode (VME only) and START ON EDGE Enable for S-IN/GPI CONTROLLED Mode. - If LVDS CONTROLLED MODE is set (bit[1:0] = 0b11) and acquisition is armed (bit[2] = 1), this bit let the LVDS I/Os be set to accept a RunIn signal to control the acquisition upon two options. One is start/stop on level, where the start of the RUN is given at RunIn signal level high and the stop at RunIn signal level low. The other is start on edge, where the start of the RUN is given on the rising edge of the RunIn signal, while the Stop must be only on software command.: 0 = starts on RunIn level (default); 1 = starts on RunIn rising edge. NOTE: this bit is meaningful only if the LVDS new features are enabled (bit[8]=1 of register 0x811C). Register 0x81A0 must also be configured for nBusy/nVeto. NOTE: this register is valid from ROC FPGA fw revision 4.16 on. - If S-IN/GPI CONTROLLED Mode is set (bit[1:0] = 0b01) and acquisition is armed (bit[2] = 1): 0 = Start/Stop run on S-IN/GPI level (default); 1 = Start run on S-IN/GPI rising edge (stop must be by software command: bit[2] = 0). NOTE: options bit[11] = 1 is valid from ROC FPGA fw revision 4.22 on.
[12]	VetoIn as veto for TRG-OUT (VME boards only). When the LVDS VetoIn signal is enabled (bit[9] = 1 in the 0x8100 register), this bit permits to use VetoIn to inhibit the triggers on TRG-OUT connector. The duration of the veto signal on TRG- OUT can be optionally extended by a time value set in the 0x81C4 register. Such function is useful in particular cases of synchronization of a multi-board system. Options are: 0 = VetoIn not used (default) 1 = VetoIn used for TRG-OUT inhibit NOTE: this bit is reserved in case of Desktop and NIM digitizers or ROC FPGA firmware rel. <= 4.16 .
[31:13]	Reserved.

Acquisition Status

This register monitors a set of conditions related to the acquisition status.

Address	0x8104
Mode	R
Attribute	C

Bit	Description
[1:0]	Reserved.
[2]	Acquisition Status. It reflects the status of the acquisition and drivers the front panel 'RUN' LED. Options are: 0 = acquisition is stopped ('RUN' is off); 1 = acquisition is running ('RUN' lits).
[3]	Event Ready. Indicates if any events are available for readout. Options are: 0 = no event is available for readout; 1 = at least one event is available for readout. NOTE: the status of this bit must be considered when managing the readout from the digitizer.
[4]	Event Full. Indicates if at least one channel has reached the FULL condition. Options are: 0 = no channel has reached the FULL condition; 1 = the maximum number of events to be read is reached.
[5]	Clock Source. Indicates the clock source status. Options are: 0 = internal (PLL uses the internal 50 MHz oscillator as reference); 1 = external (PLL uses the external clock on CLK-IN connector as reference).
[6]	Reserved.
[7]	PLL Unlock Detect. This bit flags a PLL unlock condition. Options are: 0 = PLL has had an unlock condition since the last register read access; 1 = PLL has not had any unlock condition since the last register read access. NOTE: flag can be restored to 1 via read access to register 0xEF04.
[8]	Board Ready. This flag indicates if the board is ready for acquisition (PLL and ADCs are correctly synchronized). Options are: 0 = board is not ready to start the acquisition; 1 = board is ready to start the acquisition. NOTE: this bit should be checked after software reset to ensure that the board will enter immediately in run mode after the RUN mode setting; otherwise, a latency between RUN mode setting and Acquisition start might occur.
[14:9]	Reserved.
[15]	S-IN (VME boards) or GPI (DT/NIM boards) Status. Reads the logical level on S-IN (GPI) front panel connector.
[16]	TRG-IN Status. Reads the logical level on TRG-IN front panel connector.
[18:17]	Reserved.
[19]	Channels Shutdown Status. This bit monitors the shutdown of the channels according to bit[8] of register 0x1n88 and the procedure described at 0x81C0 register. Options are: 0 = channels are ON; 1 = channels are in shutdown.

[23:20]	Bits[23:20] (bits[21:20] in case of DT, NIM and 8-channel VME versions) monitor the temperature status of the board channels. Each bit refers to a 4- channel mezzanine, i.e. bit[20] refers to channels 3-0, bit[21] to channels 7-4, and so on. When at least one of the channels in the mezzanine exceeds the 70°C limit (85°C in case of x725S/x730S models), the relevant bit is set automatically to 1. As soon as at least one of these bits becomes 1, the board enters the temperature protection condition which causes the automatic channel turn-off and the acquisition RUN stop (if it was on): 1. Bit[19] becomes 1. 2. Bit[2] of register 0x8100 is automatically set to 0. Data possibly stored at the moment can be readout in any case. When all the bits[23:20] (bits[21:20]) become 0, the board exits the temperature protection condition. This means that the channel temperature reached at least 61°C (74°C in case of x725S/x730S models). The user has then to turn on the board channels and the acquisition RUN (if necessary): 1. Bit[0] of register 0x81C0 must be set to 0 (bit[19] of register 0x8104 becomes 0). 2. Bit[2] of register 0x8100 must be set to 1.
[31:24]	Reserved. NOTE: in case of DT, NIM and 8-channel VME boards, bits[31:22] are reserved.

Software Trigger

Writing this register causes a software trigger generation which is propagated to all the enabled channels of the board.

Address	0x8108
Mode	W
Attribute	C

Bit	Description
[31:0]	Write whatever value to generate a software trigger.

Global Trigger Mask

This register sets which signal can contribute to the global trigger generation.

Address	0x810C
Mode	R/W
Attribute	C

Bit	Description
[7:0]	Bit n corresponds to the trigger request from couple n that participates to the global trigger generation (n = 0,...,3 for DT, NIM and 8-channel VME boards; n = 0,...,7 for 16-channel VME boards). Options are: 0 = trigger request does not participate to the global trigger generation; 1 = trigger request participates to the global trigger generation. Couple n corresponds to the two consecutive channels 2n and 2n+1: couple 0 is channel 0 and channel 1, couple 1 is channel 2 and channel 3, and so on. The trigger request from the couple can be programmed through register 0x1n84 to be the AND/OR/one of the channels. NOTE: in case of DT, NIM and 8-channel VME boards, only bits[3:0] are meaningful, while bits[7:4] are reserved.
[19:8]	Reserved. NOTE: in case of DT, NIM and 8-channel VME Boards, bits[19:4] are reserved.
[23:20]	Majority Coincidence Window. Sets the time window for the majority coincidence in units of the Trigger Clock (8 ns for 730 and 16 ns for 725). Majority level must be set different from 0 through bits[26:24].
[26:24]	Majority Level. Sets the majority level for the global trigger generation. For a level m, the trigger fires when at least m+1 of the enabled trigger requests (bits[7:0] or [3:0]) are over-threshold inside the majority coincidence window (bits[23:20]). NOTE: The majority level must be smaller than the number of channel enabled via bits[7:0] mask (or [3:0]).
[28:27]	Reserved.
[29]	LVDS Trigger (VME boards only). When enabled, the trigger from LVDS I/O participates to the global trigger generation (in logic OR). Options are: 0 = disabled; 1 = enabled.
[30]	External Trigger (default value is 1). When enabled, the external trigger on TRG-IN participates to the global trigger generation in logic OR with the other enabled signals. Options are: 0 = disabled; 1 = enabled.
[31]	Software Trigger (default value is 1). When enabled, the software trigger participates to the global trigger signal generation in logic OR with the other enabled signals. Options are: 0 = disabled; 1 = enabled.

Front Panel TRG-OUT (GPO) Enable Mask

This register sets which signal can contribute to generate the signal on the front panel TRG-OUT LEMO connector (GPO in case of DT and NIM boards).

Address	0x8110
Mode	R/W
Attribute	C

Bit	Description
[7:0]	This mask sets the trigger requests participating in the TRG-OUT (GPO) signal. Bit n corresponds to the trigger request from couple n (n=0,...,3 in case of DT, NIM and 8-channel VME boards; n = 0,..., 7 in case of 16-channel VME boards). Options are: 0 = Trigger request does not participate to the TRG-OUT (GPO) signal; 1 = Trigger request participates to the TRG-OUT (GPO) signal. Couple n corresponds to the two consecutive channels 2n and 2n+1: couple 0 is channel 0 and channel 1, couple 1 is channel 2 and channel 3, and so on. The trigger request from the couple can be programmed through register 0x1n84 to be the AND/OR/one of the two channels. NOTE: In case of DT, NIM and 8-channels VME boards, only bits[3:0] are meaningful while bis[7:4] are reserved.
[9:8]	TRG-OUT (GPO) Generation Logic. The enabled trigger requests (bits [7:0] or [3:0]) can be combined to generate the TRG-OUT (GPO) signal. Options are: 00 = OR; 01 = AND; 10 = Majority; 11 = Reserved.
[12:10]	Majority Level. Sets the majority level for the TRG-OUT (GPO) signal generation. Allowed level values are between 0 and 7 for VME boards, while between 0 and 3 for DT, NIM and 8-channel VME boards. For a level m, the trigger fires when at least m+1 of the trigger requests are generated by the enabled couples of channels (bits [7:0] or [3:0]) .
[28:13]	Reserved.
[29]	LVDS Trigger Enable (VME boards only). LVDS connectors programmed as inputs (according to registers 0x811C and 0x81A0) can participate in the TRG-OUT (GPO) signal generation, in logic OR with the other enabled signals. Options are: 0 = disabled; 1 = enabled.
[30]	External Trigger (default value is 1). When enabled, the external trigger on TRG-IN can participate in the TRG-OUT (GPO) signal generation in logic OR with the other enabled signals. Options are: 0 = disabled; 1 = enabled.
[31]	Software Trigger (default value is 1). When enabled, the software trigger can participate in the TRG-OUT (GPO) signal generation in logic OR with the other enabled signals. Options are: 0 = disabled; 1 = enabled.

LVDS I/O Data

This register allows to read out the logic level of the LVDS I/Os if the LVDS pins are configured as outputs, and to set the logic level of the LVDS I/Os if the pins are configured as inputs.
NOTE: this register is supported by VME boards only.

Address	0x8118
Mode	R/W
Attribute	C

Bit	Description
[15:0]	LVDS I/O Data (VME boards only). It is the logic level of the corresponding nth LVDS I/O to read out or write, according to its direction (0x811C, bit[5:2]). A write operation sets the corresponding pin logic state if configured as output, while a read operation returns the logic state of the corresponding pin if configured as input. In case of Old LVDS I/O Features (0x811C, bit[8] = 0), the general purpose I/O option must be set (0x811C, bit[7:6] = 00). In case of New LVDS I/O Features (0x811C, bit[8] = 1), REGISTER mode must be set (0000 option in the 0x81A0 register).
[31:16]	Reserved.

Front Panel I/O Control

This register manages the front panel I/O connectors. Default value is 0x000000.

Address	0x811C
Mode	R/W
Attribute	C

Bit	Description
[0]	LEMO I/Os Electrical Level. This bit sets the electrical level of the front panel LEMO connectors: TRG-IN, TRG-OUT (GPO in case of DT and NIM boards), S-IN (GPI in case of DT and NIM boards). Options are: 0 = NIM I/O levels; 1 = TTL I/O levels.
[1]	TRG-OUT Enable (VME boards only). Enables the TRG-OUT LEMO front panel connector. Options are: 0 = enabled (default); 1 = high impedance. NOTE: this bit is reserved in case of DT and NIM boards.
[2]	LVDS I/O [3:0] Direction (VME boards only). Sets the direction of the signals on the first 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. NOTE: this bit is reserved in case of DT and NIM boards.
[3]	LVDS I/O [7:4] Direction (VME boards only). Sets the direction of the second 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. NOTE: this bit is reserved in case of DT and NIM boards.
[4]	LVDS I/O [11:8] Direction (VME boards only). Sets the direction of the third 4- pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. NOTE: this bit is reserved in case of DT and NIM boards.
[5]	LVDS I/O [15:12] Direction (VME boards only). Sets the direction of the fourth 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. NOTE: this bit is reserved in case of DT and NIM boards.
[7:6]	LVDS I/O Signal Configuration (VME boards only). Valid for old LVDS I/O features only (0x811C, bit[8] = 0). Options are: 00 = general purpose I/Os: LVDS I/Os work as register; I/O direction is configured through bit[5:2]; the logic level is read out or set in the 0x8118 register. 01 = programmed I/Os: direction and function of the LVDS signals are fixed (see the tabled signal pinout in the digitizer User Manual). 10 = pattern mode: LVDS signals are inputs and their value is written into the header PATTERN field of the event (see the digitizer User Manual); 11 = reserved. NOTE: these bits are reserved in case of DT and NIM boards.
[8]	LVDS I/O New Features Selection (VME boards only). Options are: 0 = LVDS old features; 1 = LVDS new features. The new features options can be configured through register 0x81A0. Please, refer to the User Manual for all details. NOTE: LVDS I/O New Features option is valid from motherboard firmware revision 3.8 on. NOTE: this bit is reserved in case of DT and NIM boards.

[9]	LVDS I/Os Pattern Latch Mode (VME boards only). Options are: 0 = Pattern (i.e. 16-pin LVDS status) is latched when the (internal) global trigger is sent to channels, in consequence of an external trigger. It accounts for post-trigger settings and input latching delays; 1 = Pattern (i.e. 16-pin LVDS status) is latched when an external trigger arrives. NOTE: this bit is reserved in case of DT and NIM boards.
[10]	TRG-IN control. The board trigger logic can be synchronized either with the edge of the TRG-IN signal, or with its whole duration. Note: this bit must be used in conjunction with bit[11] = 0. Options are: 0 = trigger is synchronized with the edge of the TRG-IN signal; 1 = trigger is synchronized with the whole duration of the TRG-IN signal.
[11]	TRG-IN to Mezzanines (channels). Options are: 0 = TRG-IN signal is processed by the motherboard and sent to mezzanine (default). The trigger logic is then synchronized with TRG-IN; 1 = TRG-IN is directly sent to the mezzanines with no mother board processing nor delay. This option can be useful when TRG-IN is used to veto the acquisition. NOTE: if this bit is set to 1, then bit[10] is ignored.
[13:12]	Reserved.
[14]	Force TRG-OUT (GPO). This bit can force TRG-OUT (GPO in case of DT and NIM boards) test logical level if bit[15] = 1. Options are: 0 = Force TRG-OUT (GPO) to 0; 1 = Force TRG-OUT (GPO) to 1.
[15]	TRG-OUT (GPO) Mode. Options are: 0 = TRG-OUT (GPO) is an internal signal (according to bits[17:16]); 1= TRG-OUT (GPO) is a test logic level set via bit[14].
[17:16]	TRG-OUT (GPO) Mode Selection. Options are: 00 = Trigger: TRG- OUT/GPO propagates the internal trigger sources according to register 0x8110; 01 = Motherboard Probes: TRG-OUT/GPO is used to propagate signals of the motherboards according to bits[19:18]; 10 = Channel Probes: TRG-OUT/GPO is used to propagate signals of the mezzanines (Channel Signal Virtual Probe); 11 = S-IN (GPI) propagation.
[19:18]	Motherboard Virtual Probe Selection (to be propagated on TRG- OUT/GPO). Options are: 00 = RUN/delayedRUN: this is the RUN in case of ROC FPGA firmware rel. less than 4.12. This probe can be selected according to bit[20]. 01 = CLKOUT: this clock is synchronous with the sampling clock of the ADC and this option can be used to align the phase of the clocks in different boards; 10 = CLK Phase; 11 = BUSY/UNLOCK: this is the board BUSY in case of ROC FPGA firmware rel. 4.5 or lower. This probe can be selected according to bit[20].
[20]	According to bits[19:18], this bit selects the probe to be propagated on TRG- OUT . If bits[19:18] = 00, then bit[20] options are: 0 = RUN, the signal is active when the acquisition is running and it is synchronized with the start run. This option must be used to synchronize the start/stop of the acquisition through the TRG- OUT->TR-IN or TRG-OUT->S-IN (GPI) daisy chain. 1 = delayedRUN. This option can be used to debug the synchronization when the start/stop is propagated through the LVDS I/O (VME boards). If bits[19:18] = 11, then bit[20] options are: 0 = Board BUSY; 1 = PLL Lock Loss. NOTE: this bit is reserved in case of ROC FPGA firmware rel. 4.5 or lower. NOTE: this bit corresponds to BUSY/UNLOCK for ROC FPGA firmware rel. less than 4.12.
[22:21]	Pattern Configuration. Configures the information given by the 16-bit PATTERN field in the header of the event format (VME only). Options are: 00 = PATTERN: 16-bit pattern latched on the 16 LVDS signals as one trigger arrives (default); Other options are reserved.
[31:23]	Reserved.

Channel Enable Mask

This register enables/disables selected channels to participate in the event readout. Disabled channels are not operative.
WARNING: this register must not be modified while the acquisition is running.

Address	0x8120
Mode	R/W
Attribute	C

Bit	Description
[15:0]	Channel Enable Mask. Bit n can enable/disable channel n to participate in the event readout. Options are: 0 = disabled; 1 = enabled. NOTE: bits[15:8] are reserved in case of DT, NIM and 8-channel VME boards.
[31:16]	Reserved.

ROC FPGA Firmware Revision

This register contains the motherboard FPGA (ROC) firmware revision information.
The complete format is:
Firmware Revision = X.Y (16 lower bits)
Firmware Revision Date = Y/M/DD (16 higher bits)
EXAMPLE 1: revision 3.08, November 12th, 2007 is 0x7B120308.
EXAMPLE 2: revision 4.09, March 7th, 2016 is 0x03070409.
NOTE: the nibble code for the year makes this information to roll over each 16 years.

Address	0x8124
Mode	R
Attribute	C

Bit	Description
[7:0]	ROC Firmware Minor Revision Number (Y).
[15:8]	ROC Firmware Major Revision Number (X).
[31:16]	ROC Firmware Revision Date (Y/M/DD).

Voltage Level Mode Configuration

When the Voltage Level Mode is enabled (bit[2:0] = 100 (bin) of register 0x8144), this register sets the DAC value to be provided on the front panel MON/Sigma output LEMO connector: 1 LSB = 0.244 mV, terminated on 50 Ohm.
NOTE: this register is supported by VME boards only.

Address	0x8138
Mode	R/W
Attribute	C

Bit	Description
[11:0]	DAC Voltage Setting (VME boards only). The corresponding output value is multiplied by 0.244 mV.
[31:12]	Reserved

Software Clock Sync

At power-on, a Sync command is issued by the firmware to the ADCs to synchronize all of them to the clock of the board. In the standard operating, this command is not required to be repeated by the user.
A write access to this register (any value) forces the PLL to re-align all the clock outputs with the reference clock.
EXAMPLE: in case of Daisy chain clock distribution among VME boards, during the initialization and configuration, the reference clocks along the Daisy chain can be unstable and a temporary loss of lock may occur in the PLLs; although the lock is automatically recovered once the reference clocks return stable, it is not guaranteed that the phase shift returns to a known state. This command allows the board to restore the correct phase shift between the CLK-IN and the internal clocks.
NOTE: this register is supported by VME boards only.
NOTE: the command must be issued starting from the first to the last board in the clock chain.
NOTE: if a Sync command is intentionally issued, the user must consider that a new channels calibration procedure is needed for a correct board operating (see 0x809C).

Address	0x813C
Mode	W
Attribute	C

Bit	Description
[31:0]	Write whatever value to generate a Sync command.

Board Info

This register contains the specific information of the board, such as the digitizer family, the channel memory size and the channel density.

Address	0x8140
Mode	R
Attribute	C

Bit	Description
[7:0]	Digitizer Family Code. Options are: 0x0E = 725 digitizer family; 0x0B = 730 digitizer family.
[15:8]	Channel Memory Size Code. Options are: 0x01 = 640 kS acquisition memory per channel; 0x08 = 5.12 MS acquisition memory per channel.
[23:16]	Equipped Channels Number. Options are: 0x10 = 16 channels (VME boards); 0x08 = 8 channels (DT, NIM and 8-channel VME boards). NOTE: if this number is lower than the physical channels number, there could be a communication problem with some of the mezzanines.
[31:24]	Reserved.

Analog Monitor Mode

This register selects which output mode is provided on the MON/Sigma front panel LEMO connector.
NOTE: this register is supported by VME boards only.

Address	0x8144
Mode	R/W
Attribute	C

Bit	Description
[2:0]	Analog Monitor Mode (VME boards only). Options are: 000 = Trigger Majority mode; 001 = Test mode; 010 = reserved; 011 = Buffer Occupancy mode; 100 = Voltage Level mode; Others = reserved. Please, refer to the digitizer User Manual for a detailed description.
[31:3]	Reserved.

Event Size

This register contains the current available event size in 32-bit words. The value is updated after a complete readout of each event.

Address	0x814C
Mode	R
Attribute	C

Bit	Description
[31:0]	Event Size (32-bit words).

Time Bomb Downcounter

This is a down counter value. If the value is constant, the firmware license is enabled and the current firmware can be used without any time limitation. If the value decreases with time, the firmware will stop working (no possibility to enter RUN mode) after 30 minutes after module power-on. If the value is 0, the time bomb has expired, and module is not allowed to enter in RUN mode without power cycling the module.

Address	0x8158
Mode	R
Attribute	C

Bit	Description
[31:0]	Down counter value. If this value is constant the DPP firmware is licensed

Fan Speed Control

This register manages the on-board fan speed in order to guarantee an appropriate cooling according to the internal temperature variations.
NOTE: from revision 4 of the motherboard PCB (see register 0xF04C of the Configuration ROM), the automatic fan speed control has been implemented, and it is supported by ROC FPGA firmware revision greater than 4.4 (see register 0x8124).
Independently of the revision, the user can set the fan speed high by setting bit[3] = 1. Setting bit[3] = 0 will restore the automatic control for revision 4 or higher, or the low fan speed in case of revisions lower than 4.
NOTE: this register is supported by Desktop (DT) boards only.

Address	0x8168
Mode	R/W
Attribute	C

Bit	Description
[2:0]	Reserved: Must be 0.
[3]	Fan Speed Mode. Options are: 0 = slow speed or automatic speed tuning; 1 = high speed.
[5:4]	Reserved: Must be 1.
[31:6]	Reserved: Must be 0.

Run/Start/Stop Delay

This register sets the delay in the Start Run of the board whether the command is issued by software, or by an input single-ended (via S-IN/GPI or TRG-IN connectors) or differential (via LVDS I/O connector) signal. This delay especially occurs in the daisy chain propagation of the run signal in a multi-board system. The latency, mainly due to the cable length and the board's internal circuitry, can be compensated by properly delaying the start of run for each board in the chain. The delay value to set is usually zero for the last board and rises going backwards along the chain.

Address	0x8170
Mode	R/W
Attribute	C

Bit	Description
[7:0]	Delay value in steps of 16 ns for 730 and 32 ns for 725.
[31:8]	Reserved.

Board Failure Status

This register monitors a set of board errors. In case of a failure, bit[26] in the second word of the event format header is set to 1 during data readout (refer to the digitizer User Manual for event structure description). Reading at this register checks which kind of error occurred.
NOTE: in case of problems with the board, the user is recommended to contact CAEN for support.

Address	0x8178
Mode	R
Attribute	C

Bit	Description
[3:0]	Reserved.
[4]	PLL Lock Loss. Options are: 0 = no error; 1 = PLL Lock Loss occurred.
[5]	Temperature Failure. Options are: 0 = no error; 1 = Temperature Failure occurred (i.e. at least one channel is in over-temperature condition).
[6]	ADC Power Down. Options are: 0 = no error; 1 =ADC Power Down occurred (i.e. at least one channel is in power down mode due to an automatic over-temperature protection).
[31:7]	Reserved.

Disable External Trigger

The External Trigger on TRG-IN connector can be disabled through this register. Any functionality related to TRG-IN is disabled as well.

Address	0x817C
Mode	R/W
Attribute	C

Bit	Description
[0]	Options are: 0: external trigger enabled; 1: external trigger disabled.
[31:1]	Reserved

Trigger Validation Mask

Sets the trigger validation logic

Address	0x8180+(4n), n=couple index
Mode	R/W
Attribute	G

Bit	Description
[7:0]	Bit n corresponds to the trigger request from couple of channels n (n=0,...,7) which participates to the generation of the trigger validation signal. Couple n corresponds to the two consecutive channels 2n and 2n+1, i.e. couple 0 is channel 0 and channel 1, couple 1 is channel 2 and channel 3, etc. The trigger request from the couple can be programmed as the local shaped trigger from register 0x1n84, choosing among the options: AND/OR/one of the channels.
[9:8]	Operation Mask. Sets the logic operation among the enabled trigger request signals. Options are: 00: OR; 01: AND; 10: majority; 11: reserved.
[12:10]	Sets the majority level. For a level m the majority fires when at least m+1 trigger requests are high.
[27:13]	Reserved
[28]	LVDS I/O Global Trigger: when enabled (VME form factor only) the global trigger from LVDS I/O participates to the trigger validation generation (in logic OR). Options are: 0: disabled; 1: enabled.
[29]	LVDS I/O Individual Trigger: when enabled (VME form factor only) the individual trigger from LVDS I/O participates to the trigger validation generation (in logic OR). Options are: 0: disabled; 1: enabled.
[30]	External Trigger: when enabled the external trigger from TRG-IN front panel connector participates to the trigger validation generation (in logic OR). Options are: 0: disabled; 1: enabled.
[31]	Software Trigger: when enabled the software trigger participates to the trigger validation generation (in logic OR). Options are: 0: disabled; 1: enabled.

Front Panel LVDS I/O New Features

If the LVDS I/O new features are enabled (bit[8] = 1 of 0x811C), this register programs the functions of the front panel LVDS I/O 16-pin connector. It is possible to configure the LVDS I/O pins by group of four (4).
Options are:
1) 0000 = REGISTER, where the four LVDS I/O pins act as register (read/write according to the configured input/output option);
2) 0001 = TRIGGER, where each group of four LVDS I/O pins can be configured to receive an input trigger for each channel (DPP Firmware only), or to propagate out the trigger request;
3) 0010 = nBUSY/nVETO, where each group of four LVDS I/O pins can be configured as inputs (0 = nBusyIn, 1 = nVetoIn, 2 = nTrigger In, 3 = nRun In) or as outputs (0 = nBusy, 1 = nVeto, 2 = nTrigger Out, 3 = nRun);
4) 0011 = LEGACY, that is to say according to the old LVDS I/O configuration (i.e. ROC FPGA firmware revisions lower than 3.8), where the LVDS can be configured as 0 = nclear TTT, and 1 = 2 = 3 = reserved in case of input LVDS setting, while they can be configured as 0 = Busy, 1 = Data ready, 2 = Trigger, 3 = Run in case of output LVDS setting.
Please refer to the Front Panel LVDS I/Os section of the digitizer User Manual for detailed description.
NOTE: LVDS I/O new features are supported from ROC FPGA firmware revision 3.8 on.
NOTE: this register is supported by VME boards only.

Address	0x81A0
Mode	R/W
Attribute	C

Bit	Description
[3:0]	LVDS I/O pins[3:0] Configuration.
[7:4]	LVDS I/O pins[7:4] Configuration.
[11:8]	LVDS I/O pins[11:8] Configuration
[15:12]	LVDS I/O pins[15:12] Configuration.
[16]	This bit permits selecting whether the nTrigger signal, when configured as output (in nBusy/nVeto LVDS I/O mode), is a copy of the signal sent on the TRG- OUT connector or a copy of the acquisition common trigger. Options are: 0 = nTrigger output is a copy of TRG-OUT signal 1 = nTrigger output is a copy of the acquisition common trigger. NOTE: this bit is reserved for ROC FPGA firmware revisions less than 4.9.
[31:17]	Reserved.

Buffer Occupancy Gain

If the Buffer Occupancy Mode is selected (bit[2:0] = 011 of 0x8144), the LEMO MON/Sigma output connector provides a voltage level whose amplitude increases in fixed steps exactly with the number of events in the event buffer. Each step of the output voltage level is 0.976 mV. A gain can be applied to the step by this register. Allowed values are in the range [0:A]. The default value, 0, means no gain applied while writing 0xn means that the fixed step is $0.976*2^n$ mV.
NOTE: this register is supported from ROC FPGA firmware revision 4.9 on.
NOTE: this register is supported by VME boards only.

Address	0x81B4
Mode	R/W
Attribute	C

Bit	Description
[3:0]	Buffer Occupancy Gain.
[31:4]	Reserved.

Extended Veto Delay

This register is valid for VME boards only and set the duration of the Extended VetoIn signal for trigger inhibit on TRG-OUT when bit[12]=1 of 0x8100 register. Such function is useful in particular cases of synchronization of a multi-board system.
NOTE: This register is valid from ROC FPGA fw revision 4.16 on.

Address	0x81C4
Mode	R/W
Attribute	C

Bit	Description
[15:0]	Extended VetoIn duration value in units of Trigger Clock (8 ns for 730 and 16 ns for 725).
[31:16]	Reserved.

Readout Control

This register is mainly intended for VME boards, anyway some bits are applicable also for DT and NIM boards.

Address	0xEF00
Mode	R/W
Attribute	C

Bit	Description
[2:0]	VME Interrupt Level (VME boards only). Options are: 0 = VME interrupts are disabled; 1,..,7 = sets the VME interrupt level. NOTE: these bits are reserved in case of DT and NIM boards.
[3]	Optical Link Interrupt Enable. Options are: 0 = Optical Link interrupts are disabled; 1 = Optical Link interrupts are enabled.
[4]	VME Bus Error / Event Aligned Readout Enable (VME boards only). Options are: 0 = VME Bus Error / Event Aligned Readout disabled (the module sends a DTACK signal until the CPU inquires the module); 1 = VME Bus Error / Event Aligned Readout enabled (the module is enabled either to generate a Bus Error to finish a block transfer or during the empty buffer readout in D32). NOTE: this bit is reserved (must be 1) in case of DT and NIM boards.
[5]	VME Align64 Mode (VME boards only). Options are: 0 = 64-bit aligned readout mode disabled; 1 = 64-bit aligned readout mode enabled. NOTE: this bit is reserved (must be 0) in case of DT and NIM boards.
[6]	VME Base Address Relocation (VME boards only). Options are: 0 = Address Relocation disabled (VME Base Address is set by the on-board rotary switches); 1 = Address Relocation enabled (VME Base Address is set by register 0xEF0C). NOTE: this bit is reserved (must be 0) in case of DT and NIM boards.
[7]	Interrupt Release mode (VME boards only). Options are: 0 = Release On Register Access (RORA): this is the default mode, where interrupts are removed by disabling them either by setting VME Interrupt Level to 0 (VME Interrupts) or by setting Optical Link Interrupt Enable to 0; 1 = Release On Acknowledge (ROAK). Interrupts are automatically disabled at the end of a VME interrupt acknowledge cycle (INTACK cycle). NOTE: ROAK mode is supported only for VME interrupts. ROAK mode is not supported on interrupts generated over Optical Link. NOTE: this bit is reserved (must be 0) in case of DT and NIM boards.
[8]	Extended Block Transfer Enable (VME boards only). Selects the memory interval allocated for block transfers. Options are: 0 = Extended Block Transfer Space is disabled, and the block transfer region is a 4kB in the 0x0000 - 0x0FFC interval; 1 = Extended Block Transfer Space is enabled, and the block transfer is a 16 MB in the 0x00000000 - 0xFFFFFFFC interval. NOTE: in Extended mode, the board VME Base Address is only set via the on-board [31:28] rotary switches or bits[31:28] of register 0xEF10. NOTE: this register is reserved in case of DT and NIM boards.
[31:9]	Reserved.

Readout Status

This register contains information related to the readout.

Address	0xEF04
Mode	R
Attribute	C

Bit	Description
[0]	Event Ready. Indicates if there are events stored ready for readout. Options are: 0 = no data ready; 1 = event ready.
[1]	Reserved.
[2]	Bus Error (VME boards) / Slave-Terminated (DT/NIM boards) Flag. Options are: 0 = no Bus Error occurred (VME boards) or no terminated transfer (DT/NIM boards); 1 = a Bus Error occurred (VME boards) or one transfer has been terminated by the digitizer in consequence of an unsupported register access or block transfer prematurely terminated in event aligned readout (DT/NIM). NOTE: this bit is reset after register readout at 0xEF04.
[3]	VME FIFO Flag. Options are: 0 = VME FIFO not empty; 1 = VME FIFO is empty.
[31:4]	Reserved.

Board ID

The meaning of this register depends on which VME crate it is inserted in.
In case of VME64X crate versions, this register can be accessed in read mode only and it contains the GEO address of the module picked from the backplane connectors; when CBLT is performed, the GEO address will be contained in the Board ID field of the Event header (see the User Manual for further details).
In case of other crate versions, this register can be accessed both in read and write mode, and it allows to write the correct GEO address (default setting = 0) of the module before CBLT operation. GEO address will be contained in the Board ID field of the Event header (see the User Manual for further details).
NOTE: this register is supported by VME boards only.

Address	0xEF08
Mode	R/W
Attribute	C

Bit	Description
[4:0]	GEO Address (VME boards only).
[31:5]	Reserved.

MCST Base Address and Control

This register configures the board for the VME Multicast Cycles.
NOTE: this register is supported by VME boards only.

Address	0xEF0C
Mode	R/W
Attribute	C

Bit	Description
[7:0]	These bits contain the most significant bits of the MCST/CBLT address of the module set via VME, that is the address used in MCST/CBLT operations.
[9:8]	Board Position in Daisy chain. Options are: 00 = board disabled; 01 = last board; 10 = first board; 11 = intermediate board.
[31:10]	Reserved.

Relocation Address

If address relocation is enabled through register 0xEF00 (bit[6] = 1), this register sets the VME Base Address of the module.
NOTE: this register is supported by VME boards only.

Address	0xEF10
Mode	R/W
Attribute	C

Bit	Description
[15:0]	These bits contain the A31...A16 bits of the address of the module. If bit[6] = 1 of 0xEF00, they set the VME Base Address of the module.
[31:16]	Reserved.

Interrupt Status/ID

This register contains the STATUS/ID that the module places on the VME data bus during the Interrupt Acknowledge cycle.
NOTE: this register is supported by VME boards only.

Address	0xEF14
Mode	R/W
Attribute	C

Bit	Description
[31:0]	STATUS/ID (VME boards only).

Interrupt Event Number

This register sets the number of events that causes an interrupt request. If interrupts are enabled, the module generates a request whenever it has stored in memory a Number of Events > INTERRUPT EVENT NUMBER.

Address	0xEF18
Mode	R/W
Attribute	C

Bit	Description
[9:0]	INTERRUPT EVENT NUMBER.
[31:10]	Reserved.

Aggregate Number per BLT

This register sets the maximum number of complete aggregates which has to be transferred for each block transfer (via VME BLT/CBLT cycles or block readout through Optical Link).

Address	0xEF1C
Mode	R/W
Attribute	C

Bit	Description
[9:0]	Number of complete aggregates to be transferred for each block transfer (BLT).
[31:10]	Reserved.

Scratch

This register can be used to write/read words for test purposes.

Address	0xEF20
Mode	R/W
Attribute	C

Bit	Description
[31:0]	SCRATCH.

Software Reset

All the digitizer registers can be set back to their default values on software reset command by writing any value at this register, or by system reset from backplane in case of VME boards.

Address	0xEF24
Mode	W
Attribute	C

Bit	Description
[31:0]	Whatever value written at this location issues a software reset. All registers are set to their default values (actual settings are lost).

Software Clear

All the digitizer internal memories are cleared:
- automatically by the firmware at the start of each run;
- on software command by writing at this register;
- by hardware (VME boards only) through the LVDS interface properly configured.

A clear command does not change the registers actual value, except for resetting the following registers:
- Event Stored;
- Event Size;
- Channel / Group n Buffer Occupancy.

This register resets also the trigger time stamp.

Address	0xEF28
Mode	W
Attribute	C

Bit	Description
[31:0]	Whatever value written at this location generates a software clear.

Configuration Reload

A write access of any value at this location causes a software reset, a reload of Configuration ROM parameters and a PLL reconfiguration.

Address	0xEF34
Mode	W
Attribute	C

Bit	Description
[31:0]	Write whatever value to perform a software reset, a reload of Configuration ROM parameters and a PLL reconfiguration.

Configuration ROM Checksum

This register contains information on 8-bit checksum of Configuration ROM space.

Address	0xF000
Mode	R
Attribute	C

Bit	Description
[7:0]	Checksum.
[31:8]	Reserved.

Configuration ROM Checksum Length BYTE 2

This register contains information on the third byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address	0xF004
Mode	R
Attribute	C

Bit	Description
[7:0]	Checksum Length: bits[23:16].
[31:8]	Reserved.

Configuration ROM Checksum Length BYTE 1

This register contains information on the second byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address	0xF008
Mode	R
Attribute	C

Bit	Description
[7:0]	Checksum Length: bits[15:8].
[31:8]	Reserved.

Configuration ROM Checksum Length BYTE 0

This register contains information on the first byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address	0xF00C
Mode	R
Attribute	C

Bit	Description
[7:0]	Checksum Length: bits[7:0].
[31:8]	Reserved.

Configuration ROM Constant BYTE 2

This register contains the third byte of the 3-byte constant.

Address	0xF010
Mode	R
Attribute	C

Bit	Description
[7:0]	Constant: bits[23:16] = 0x83.
[31:8]	Reserved.

Configuration ROM Constant BYTE 1

This register contains the second byte of the 3-byte constant.

Address	0xF014
Mode	R
Attribute	C

Bit	Description
[7:0]	Constant: bits[15:8] = 0x84.
[31:8]	Reserved.

Configuration ROM Constant BYTE 0

This register contains the first byte of the 3-byte constant.

Address	0xF018
Mode	R
Attribute	C

Bit	Description
[7:0]	Constant: bits[7:0] = 0x01.
[31:8]	Reserved.

Configuration ROM C Code

This register contains the ASCII C character code (identifies this as CR space).

Address	0xF01C
Mode	R
Attribute	C

Bit	Description
[7:0]	ASCII 'C' Character Code.
[31:8]	Reserved.

Configuration ROM R Code

This register contains the ASCII R character code (identifies this as CR space).

Address	0xF020
Mode	R
Attribute	C

Bit	Description
[7:0]	ASCII 'R' Character Code.
[31:8]	Reserved.

Configuration ROM IEEE OUI BYTE 2

This register contains information on the third byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Address	0xF024
Mode	R
Attribute	C

Bit	Description
[7:0]	IEEE OUI: bits[23:16].
[31:8]	Reserved.

Configuration ROM IEEE OUI BYTE 1

This register contains information on the second byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Address	0xF028
Mode	R
Attribute	C

Bit	Description
[7:0]	IEEE OUI: bits[15:8].
[31:8]	Reserved.

Configuration ROM IEEE OUI BYTE 0

This register contains information on the first byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Address	0xF02C
Mode	R
Attribute	C

Bit	Description
[7:0]	IEEE OUI: bits[7:0].
[31:8]	Reserved.

Configuration ROM Board Version

This register contains the board version information.

Address	0xF030
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Version Code. Options are: 0xF0 = V1725/VX1725/DT5725/N6725; 0xF1 = V1725B/VX1725B/DT5725B/N6725B; 0xF2 = V1725C/VX1725C; 0xF3 = V1725D/VX1725D; 0xF4 = V1725S/VX1725S/DT5725S/N6725S; 0xF5 = V1725BS/VX1725BS/DT5725BS/N6725BS; 0xF6 = V1725CS/VX1725CS; 0xF7 = V1725DS/VX1725DS; 0xC0 = V1730/VX1730/DT5730/N6730; 0xC1 = V1730B/VX1730B/DT5730B/N6730B; 0xC2 = V1730C/VX1730C; 0xC3 = V1730D/VX1730D; 0xC4 = V1730S/VX1730S/DT5730S/N6730S; 0xC5 = V1730BS/VX1730BS/DT5730BS/N6730BS; 0xC6 = V1730CS/VX1730CS; 0xC7 = V1730DS/VX1730DS.
[31:8]	Reserved.

Configuration ROM Board Form Factor

This register contains the information of the board form factor.

Address	0xF034
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Form Factor CAEN Code. Options are: 0x00 = VME64; 0x01 = VME64X; 0x02 = Desktop; 0x03 = NIM.
[31:8]	Reserved.

Configuration ROM Board ID BYTE 1

This register contains the MSB of the 2-byte board identifier.

Address	0xF038
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Number ID: bits[15:8].
[31:8]	Reserved.

Configuration ROM Board ID BYTE 0

This register contains the LSB information of the 2-byte board identifier.

Address	0xF03C
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Number ID: bits[7:0].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 3

This register contains information on the fourth byte of the 4-byte hardware revision.

Address	0xF040
Mode	R
Attribute	C

Bit	Description
[7:0]	PCB Revision: bits[31:24].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 2

This register contains information on the third byte of the 4-byte hardware revision.

Address	0xF044
Mode	R
Attribute	C

Bit	Description
[7:0]	PCB Revision: bits[23:16].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 1

This register contains information on the second byte of the 4-byte hardware revision.

Address	0xF048
Mode	R
Attribute	C

Bit	Description
[7:0]	PCB Revision: bits[15:8].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 0

This register contains information on the first byte of the 4-byte hardware revision.

Address	0xF04C
Mode	R
Attribute	C

Bit	Description
[7:0]	PCB Revision: bits[7:0].
[31:8]	Reserved.

Configuration ROM FLASH Type

This register contains information on which FLASH type (storing the FPGA firmware) is present on-board.

Address	0xF050
Mode	R
Attribute	C

Bit	Description
[7:0]	FLASH Type. Options are: 0x00 = 8 Mb FLASH; 0x01 = 32 Mb FLASH; 0x02 = 64 Mb FLASH. NOTE: for x730 and x725 digitizers, this byte must be 0x01; for x730S and x725S models, it must be 0x02.
[31:8]	Reserved.

Configuration ROM Board Serial Number BYTE 1

This register contains information on the MSB of the board serial number.

Address	0xF080
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Serial Number: bits[15:8].
[31:8]	Reserved.

Configuration ROM Board Serial Number BYTE 0

This register contains information on the LSB of the board serial number.

Address	0xF084
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Serial Number: bits[7:0].
[31:8]	Reserved.

Configuration ROM VCXO Type

This register contains information on which type of VCXO is present on-board.

Address	0xF088
Mode	R
Attribute	C

Bit	Description
[31:0]	VCXO Type Code. Options for VME Digitizers are: 0 = AD9510 with 1 GHz; 1 = AD9510 with 500 MHz (not programmable); 2 = AD9510 with 500 MHz (programmable). Options for Desktop/NIM Digitizers are: Reserved (value = 0).

2 DPP-PSD Memory Organization

Each channel has a fixed amount of RAM memory to save the events. The memory is divided into a programmable number of buffers (also called “aggregates”), where each buffer contains a programmable number of events. For the 725 and 730 families each buffer is shared between two channels, i.e. channel 0 and channel 1, channel 2 and channel 3, etc. The event format is programmable as well. The board registers involved are the following:

- “Aggregate Organization” (*Nb*), address 0x800C: defines how many aggregates can be contained in the memory ($n_{aggr} = 2^{Nb}$).
- “Number of Events per Aggregate” (*Ne*), address 0x1n34: defines the number of events contained in one aggregate. The maximum allowed value is 1023.
- “Record Length” (*Ns*), address 0x1n20: defines the number of samples for the waveform acquisition, when enabled (*rec_len = Ns * 8* for 720, DT5790, 725, and 730 series, and *rec_len = Ns * 12* for 751 series.
- “Board Configuration”, address 0x8000: defines the acquisition mode and the event data format.

Note: Those who need to write their own DAQ software, must take care to choose the Ne value according to the event and buffer size, as explained in the examples in the next section.

Information about the use of these parameters in the CAENDigitizer library can be found in **[RD1]**. According to the programmed event format, an event can contain a certain number of samples of the waveform, one trigger time stamp, the two charges Q_{short} and Q_{long}, and the Baseline/Extras information.

725 and 730 series

The following section describes the structure of the memory organization of 725 and 730 series. The physical memory inside the board is made of memory locations, each of 128-bit (16B). In terms of location occupancy:

Trigger Time Stamp = 1 location;

Waveform (if enabled) = 1 location every 8 samples;

Charges (QL and QS) and EXTRAS = 1 location.

Fig.**2.1** shows the data format as saved into the physical memory for 725 and 730 series. Since two channels share the same buffer, one bit is reserved to store the channel number, where 0 corresponds to the odd channel of the couple, and 1 to the even channel.

Note: Fig. **2.1** refers to the event storage into the physical memory of the board. Data are then organized in a different format for the event readout. The event readout format is shown in the **Event Data Format** section.

As previously said, the “Record Length” and the “Board Configuration” settings determine the event size; the user must calculate the number of event per buffer (*Ne*) and the number of buffers (2^{Nb}) accordingly. When the board runs in List Mode, the event memory contains only two locations, one for the Trigger Time Tag and one for the Charge and Baseline. Therefore it is very small and it is suggested to use a big value for Ne to make the buffer size as big as at least a few KB. Small buffer size results in low readout bandwidth. The only drawback of setting high values for *Ne* is that the events are not available for the readout until the buffer is complete; hence there is some latency between the arrival of a trigger and the readout of the relevant event data. Conversely, when the board runs in Oscilloscope Mode, especially when the record length is large, it is more convenient to keep *Ne* low (typically 1).

Example1: suppose that the mixed mode is enabled and Ns is set to 400 samples:
Event size (in locations) = 1(Time_Stamp) + *Ns*/8(Waveform) + 1(Charge_EXTRA) = 52 loc. Suppose to set *Ne* = 60 (number of events per buffer), hence: buffer_size (in locations) = 52 * 60 = 3120 loc. Supposing that the memory board is made of 128k loc./ch, the number of buffers will be: 128k/3120 = 42 (buffers). This value corresponds to the maximum number of buffers that the memory can contain. However, since the programmable value must be a power of two, the user has to choose the closest number smaller than 42 which can be represented as a power of two, that is 2^5 =

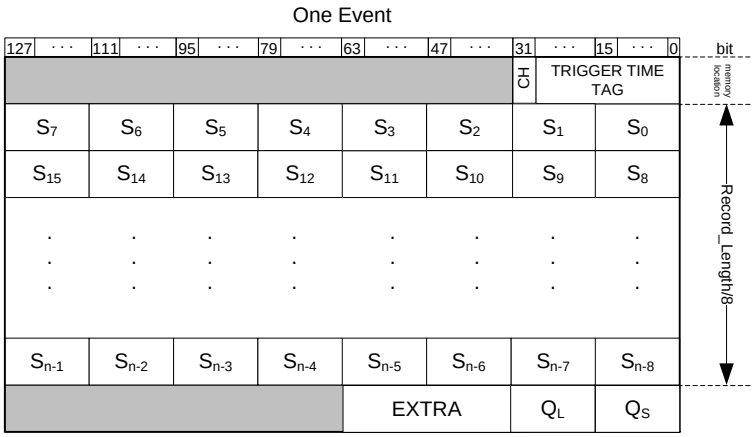

Fig. 2.1: Data organization into the Internal Memory of x725 and x730 digitizer.

32 (i.e. *Nb* = 5 has to be written in the "Aggregate Organization" register).

Example2: suppose that the mixed mode is enabled and *Ns* is set to 24 samples: Event size (in locations) = 1(Time_Stamp) + *Ns*/8(Waveform) + 1(Charge_EXTRAS) = 5 loc. Having a small event size, it is convenient to divide the memory into few buffers of bigger size to store a large number of events. Suppose to have set *Nb* = 3, so that the number of buffers is 8. Supposing that the board memory option is made of 64k locations, each buffer consists in 64k/8 = 8k locations and so the resulting number of event per aggregate should be: *Ne* = 8k/5 = 1639. **IMPORTANT**: in this case, the real number of events stored per aggregate is 1023, due to the register length constraint already mentioned.

Event Data Format

The data format provided by the firmware is grouped into aggregates of events. Each aggregate of channels is then grouped into the board aggregate, and finally into block transfer. Those who need to write their own acquisition software must take care of the following sections.

Channel Aggregate Data Format for 725 and 730 series

The Channel Aggregate is composed by the set of Ne events, where Ne is the programmable number of events contained in one aggregate (see the previous section). The structure of the Channel Aggregate of two events (EVENT 0 and EVENT 1) for 725 and 730 series is shown in Fig. **2.2**, where:

DT: Dual trace enabled flag (1 = enabled, 0 = disabled)

EQ: Charge enabled flag, must be 1

ET: Time Tag enabled flag, must be 1

EE: Extras enabled flag

ES: Waveform (samples) enabled flag

EX: Extras option enabled flag:

Note: to enable the "EXTRAS" word set bit[17] of register 0x8000.

000 = the word "EXTRAS" will be read as:

[31 : 16] = extended time stamp: those 16 bits must be read as the most significant bits of the time stamp, which becomes a 31+16=47 bit number;

"CHANNEL AGGREGATE" DATA FORMAT

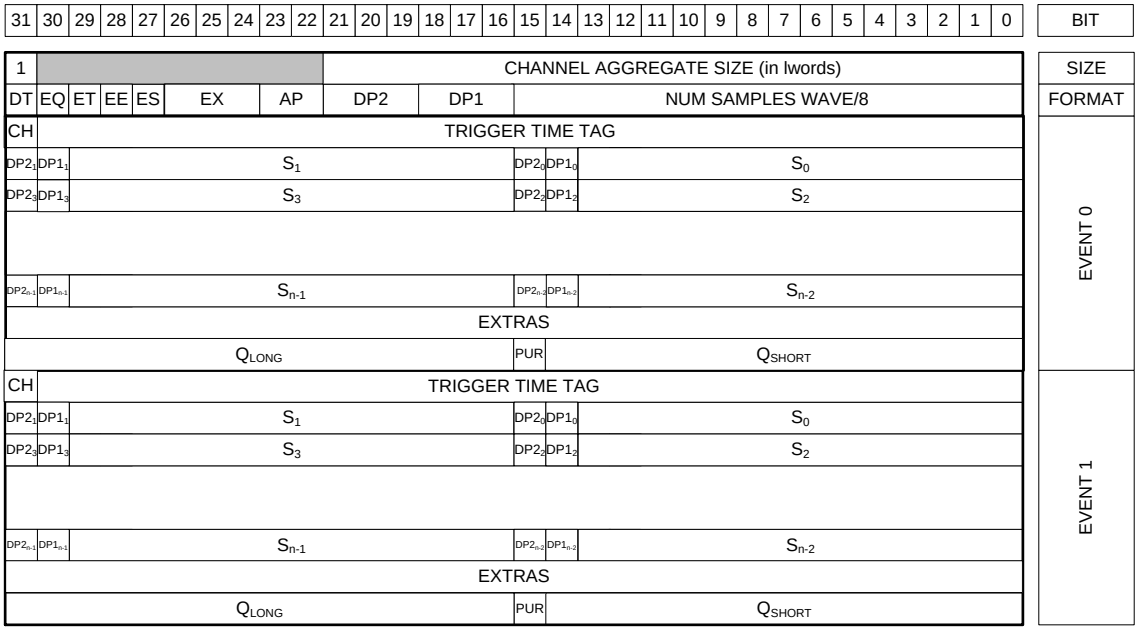

Fig. 2.2: Channel Aggregate Data Format scheme for 725-730 series.

[15 : 0] = the baseline value multiplied by 4.

001 = = the word "EXTRAS" will be read as:

[31 : 16] = extended time stamp: those 16 bits must be read as the most significant bits of the time stamp, which becomes a 31+16=47 bit number;

[15 : 0] = flags, where bit[15]: Trigger Lost (the first event after a trigger lost has this flag set); bit[14]: Over-range (identifies an event saturating inside the gate - clipping); bit[13]: 1024 trigger counted (every 1024 counted events this flag is high); bit[12]: N lost trigger counted (every N counted lost events this flag is high, where N is set from bits[17:16] of register 0x1n84);

010 = the word "EXTRAS" will be read as:

[31 : 16] = extended time stamp: those 16 bits must be read as the most significant bits of the time stamp, which becomes a 31+16=47 bit number;

[15 : 10] = flags, where bit[15]: Trigger Lost (the first event after a trigger lost has this flag set); bit[14]: Over-range (identifies an event saturating inside the gate - clipping); bit[13]: 1024 trigger counted (every 1024 counted events this flag is high); bit[12]: N lost trigger counted (every N counted lost events this flag is high, where N is set from bits[17:16] of register 0x1n84);

[9 : 0] = fine time stamp (T_{fine} – see the definition in **[RD2]**).

100 = the word "EXTRAS" will be read as:

[31 : 16] = Lost Trigger Counter;

[15 : 0] = Total Trigger Counter.

101 = the word "EXTRAS" will be read as:

[31 : 16] = CFD Sample After the Zero Crossing (SAZC);

[15 : 0] = CFD Sample Before the Zero Crossing (SBZC).

111 = the word "EXTRAS" will be read as the fixed value of 0x12345678 (debug use only).

AP: Analog Probe selection. For 725 and 730 series possible selections are:

If DT = 0:

00 = "Input";

01 = "CFD";

If DT = 1:

00 = "Input" and "Baseline";

01 = "CFD" and "Baseline";

Note: The CFD trace is available only if the discrimination mode is CFD (bit[6] = 1 of register 0x1n80). If discrimination mode is LED (bit[6] = 0 of register 0x1n80), the CFD trace becomes the Smoothed Input.

10 = “Input” and “CFD”.

DP1: Digital Virtual Probe 1 selection among:

000 = “Long Gate”;

001 = “Over Threshold”, digital signal that is 1 when the input signal is over the requested threshold;

010 = “Shaped TRG”, logic signal generated by a channel in correspondence with its local self- trigger. It is used to propagate the trigger to the other channels of the board and to other external boards, as well as to feed the coincidence trigger logic (refer to **[RD3]**);

011 = “TRG Val. Acceptance Win.”, logic signal corresponding to the time window where the coincidence validation is accepted. The validation enables the event dump into the memory (see **[RD3]**);

100 = “Pile Up“, logic pulse set to 1 when a pile up event occurred (not implemented);

101 = “Coincidence“, logic pulse set to 1 when a coincidence occurred (refer to **[RD3]**);

110 = reserved;

111 = “Trigger”.

DP2: Digital Virtual Probe 2 selection among:

000 = “Short Gate”;

001 = “Over Threshold”, digital signal that is 1 when the input signal is over the requested threshold;

010 = “TRG Validation”, digital signal that is 1 when a coincidence validation signal comes from the mother board FPGA (refer to **[RD3]**);

011 = “TRG HoldOff”, logic signal generated by a channel in correspondence with its local self- trigger. Other triggers are inhibited for the overall Trigger Hold-Off duration;

100 = “Pile Up“, logic pulse set to 1 when a pile up event occurred (to be implemented);

101 = “Coincidence“, logic pulse set to 1 when a coincidence occurred (refer to **[RD3]**);

110 = reserved;

111 = “Trigger”.

Note: Digital Virtual Probes can be disabled by setting bit[31] of register 0x8000.

NUM SAMPLES WAVE/8 corresponds to the number of words to be read in the event related to the waveform / 4 (2 samples per word)

CH: since two consecutive channels share the same buffer, the CH flag identifies if the even channel or the odd channel participated to the event (0 for even, 1 for odd).

DPi_m (i=1, 2; m=0, 1, …,n-1): Digital Virtual Probe value i for sample m. $DP1_m$ is the value of the probe written in DP1 flag. $DP2_m$ is the value of the probe written in DP2 flag.

$S_{m'}$ (m'=0, 2, 4, …, n-2): Even Samples of the analog probe (whose flag is stored in AP) at time t=m'.

$S_{m''}$ (m''=1, 3, 5, …, n-1): Odd Samples of the analog probe (whose flag is stored in AP) at time t=m''.

If DT=1, Sm'' corresponds to the second analog probe at time t=m''- 1.

For example if DT= 1, and the analog probe selection is “Input” – “Baseline”, Sm’ will corresponds to the “Input” sample at time m', while $S_{m''}$ will corresponds to the “Baseline” at the same time m' (= m''-1).

$Q_{short/long}$: integrated charge value in the short/long gate

PUR: detect an event whose energy is not correctly evaluated. This might be the case of a pile-up event or of an event saturating inside the gate (see bit[24] of register 0x1n84)

Note: when the **"Dual Trace"** option is enabled, half of the samples are used to store the baseline. Therefore only the remaining half samples are used for the input waveform. In the plot visualization each input sample is duplicated to keep the same granularity. Those who need to acquire waveform with full resolution, should disable the dual trace option. For example, in CoMPASS, select the "NONE" option for "Analog Probe 2" **[RD2]**.

Board Aggregate Data Format

For each readout request (occurring when at least one channel has available data to be read) the "interface FPGA (ROC)" reads one aggregate from each enabled channel memory. No more than one aggregate per channel is read each time. The sample of Channel Aggregates is the Board Aggregate. If one channel has no data, that channel does not come into the Board Aggregate. The data format when all 16 channels of a VME have available data, is as shown in Fig. **2.3**, where:

"BOARD AGGREGATE" DATA FORMAT for 725 and 730 series

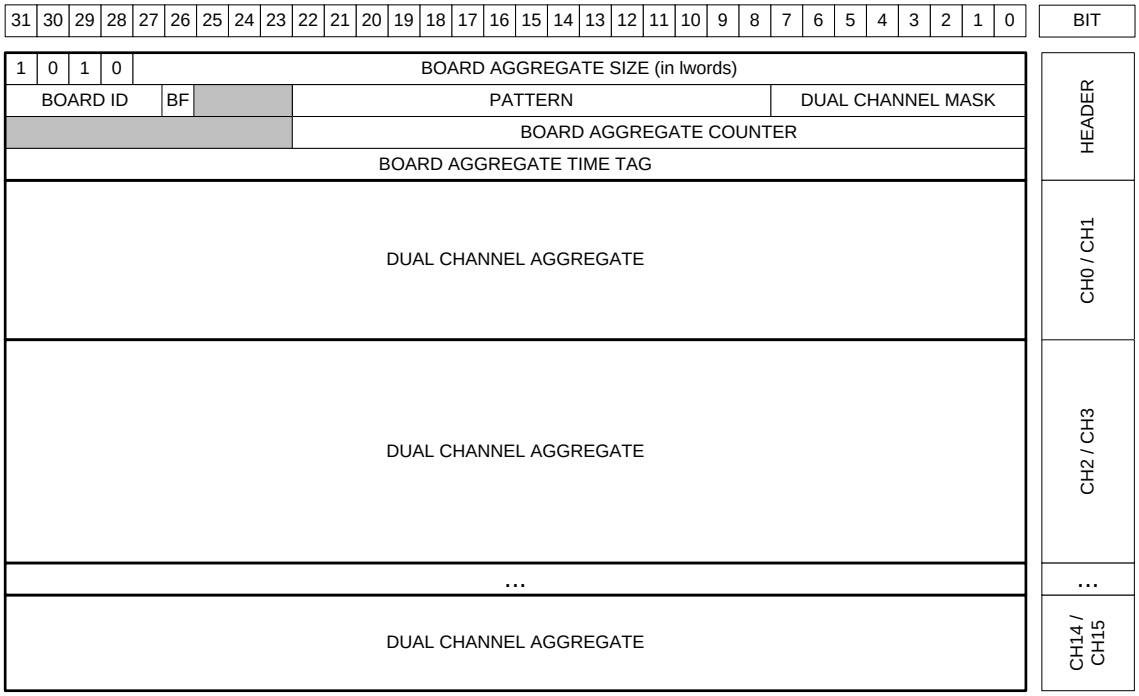

Fig. 2.3: Board Aggregate Data Format scheme for 725-730 series.

BOARD AGGREGATE SIZE: total size of the aggregate

BOARD ID: corresponds to the GEO address of the board. In case of VX boards this number is automatically set for each board. In case of VME boards this value is by default = 0 for all boards. It is possible to set the Board ID through register 0xEF08. The GEO address is quite useful in case of concatenate BLT (CBLT) read.

BF: Board Fail flag. This bit is set to "1" because of a hardware problem, as for example the PLL unlock. The user can investigate the problem checking the Board Failure Status register 0x8178, or contacting CAEN support (refer to Chapter **Technical Support**).

Note: BF bit is meaningful only for ROC FPGA firmware revision greater than 4.5. It is reserved for previous releases.

PATTERN: is the value read from the LVDS I/O (VME only);

DUAL CHANNEL MASK: corresponds to the couple of channels participating to the Board Aggregate (725 and 730 only);

BOARD AGGREGATE COUNTER: counts the board aggregate. It increases with the increase of board aggregates;

BOARD AGGREGATE TIME TAG: is the time of creation of the aggregate (this does not correspond to any physical quantity).

Data Block

The readout of the digitizer is done using the Block Transfer (BLT, refer to **[RD1]**); for each transfer, the board gives a certain number of Board Aggregates, consisting in the Data Block. The maximum number of aggregates that can be transferred in a BLT is defined by the Aggregate Number per BLT. In the final readout, each Board Aggregate comes consecutively. In case of n Board Aggregates, the Data Block is as in Fig. **2.4**

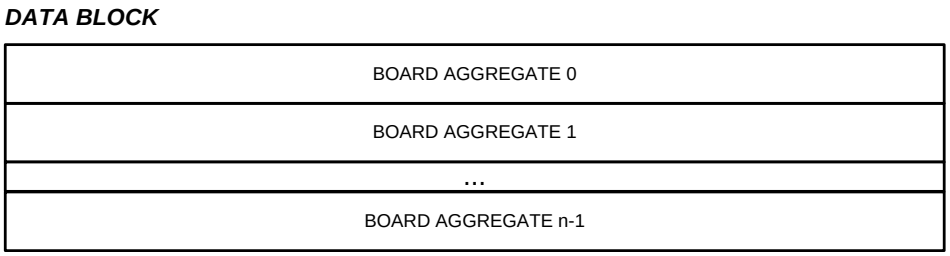

Fig. 2.4: Data Block scheme.

3 Technical Support

To contact CAEN specialists for requests on the software, hardware, and board return and repair, it is necessary a MyCAEN+ account on www.caen.it:

https://www.caen.it/support-services/getting-started-with-mycaen-portal/

All the instructions for use the Support platform are in the document:

A paper copy of the document is delivered with CAEN boards.
The document is downloadable for free in PDF digital format at:

https://www.caen.it/wp-content/uploads/2022/11/Safety_information_Product_support_W.pdf

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