Rev. 1 - Nov 29th, 2021

A2795

Liquid Argon TPC Readout Board

CAEN
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User Manual
UM2580

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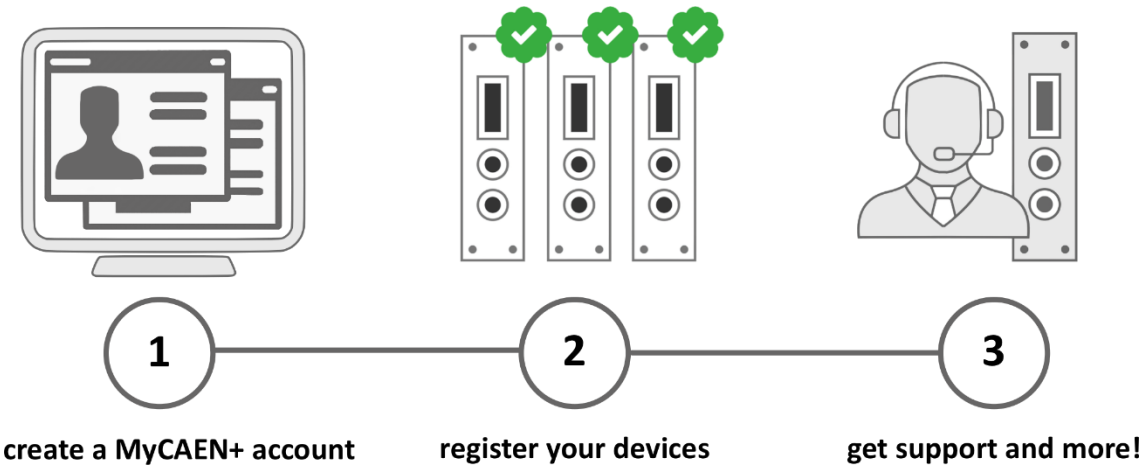

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Purpose of this Manual

This User Manual contains the full description of the A2795 CAEN board.

Change Document Record

Date	Revision	Changes
October 24th, 2019	00	Initial release
November 29th, 2021	01	Fixed the NPO of the document

Symbols, abbreviated terms and notation

DAQ	Data Acquisition
FFT	Fast Fourier Transform
MEB	Multi Event Buffer
SerDes	Serializer/Deserializer
TPC	Time Projection Chamber

Reference Documents

N.A.

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1. Introduction

The **A2795** is a board for the acquisition of 64 analog input channels and 12-bit / 2.5MSPS analog-to-digital conversion. For this purpose, there are 8 sockets on-board to install analog preamplifiers suited for the typical input signals coming from Liquid Argon TPC detectors. It represents the evolution of the previous A2792 board developed by CAEN for the Swiss Federal Institute of Technology in Zurich (ETH), resulting from the experience and the expertise gained in the development of the ICARUS acquisition system, still in use, based on CAEN V791 and V789 boards. The A2795 has been designed to be used in different kind of experiments sharing similar characteristics but requiring particular specifications of signal preamplification.

The A2795 allows the analog inputs to be directly connected to the connectors of the flanges of the TPC chambers without need of additional interconnection cables. Such design solution gives important advantages in terms of costs and performances, particularly for the noise of the charge preamplifiers (stray capacitance reduction) which are typically used in this field of application.

The main features of the board are listed below:

- The analog front-end for the input signal conditioning consists in 8 sockets which host modules with up to 8 channels each; the modules implement the electronic circuitry for the input signal conditioning. This modular design simplifies both the application of future different signal conditioning solutions and the maintenance or the update of the current one on the same board.
- Such design solution makes also possible to use the A2795 for the configuration of the charge preamplifiers in “cold conditions”, where the circuitry sensitive to the electric noise is placed directly within the detector, or in a cryogenic environment, while the board will be filled with voltage preamplifying modules to adapt the output levels of the preamps to the input dynamics of the ADCs.
- The high modularity of the A2795 allows it to be used into crates containing up to 16 boards (1024 channels), optimizing the spaces and system costs.
- A dedicated communication protocol, called TTLink, allows the synchronization and circulation of the main operating commands between a number of A2795s intra and inter-crate virtually infinite.
- The board mounts a single next-generation Altera Cyclone V GX low power FPGA to reduce power consumption and so the heating. Built-in SerDes features a scalable speed to support future protocol developments and/or faster data transfer speeds.
- The sizing of the FPGA's internal resources is such that the occupancy of the features currently implemented does not exceed 25% of the total. Ample space remains so available for adding new features in the future.
- The board communicates on multimode fiber optics, 62.5/125 µm at 1.25 Gb/s, using a proprietary CAEN communication protocol, called CONET2. It is possible to maximize the data transfer bandwidth with point-to-point connections from the DAQ to each A2795 or reduce the overall interconnection costs by using a single fiber up to a maximum of eight (8) A2795 connected in Daisy-chain.
- The use of optical fibers as an interconnection mean allows the connection between high-speed boards up to 200m avoiding the generation of ground loops.
- The DAQ requires the use of CAEN PCIe A3818 cards (1, 2 or 4 optical link CONET2 Master lanes) which are not provided with the A2795.
- Firmware upgrades of the on-board FPGA can be done directly remotely via optical fiber.

2. Technical Specifications

NUMBER OF CHANNELS	64 for a single A2795 board	
PREAMPLIFIERS	8 sockets to host piggyback preamplifier modules with 8 channels on each module	
DC-OFFSET ADJUSTMENT	Programmable 0 ÷ +3.3V by 16-bit DAC for the offset adjustment of the preamplifier output	
ADC RESOLUTION	12-bit (FSR = 3.3V, 1 LSB = 0.805861 mV)	
SAMPLING FREQUENCY	2.5 MHz	
DIGITAL MEMORY	2Mx36bit, programmable in terms of number of buffers and size: from 16 buffers of 4096 samples each (default) up to 4096 buffers of 16 samples each	
TRIGGER IN	Global trigger common to all the channels by: ▪ TTLink ▪ Front panel LEMO connector ▪ Software command	
TRIGGER OUT	Local Trigger (for Induction and Collection separately) from all channels in the same crate sent by the MASTER card via front panel LEMO connector	
TRIGGER TIME STAMP	32-bit counter, synchronous with the sampling clock	
TEST PULSE	▪ External: by front panel LEMO connector, common to all the 64 channels ▪ Internal: by FPGA, different from even to odd channels	
OPTICAL LINK	▪ Transfer rate: 1.25 Gb/s ▪ Maximum data throughput: 80MB/s ▪ Daisy-chain capability: 1 up to 8 boards	
POWER REQUIREMENTS	External Power Supply (A2795 without preamps) +9.0V ±5%, 0.3A (analog power) -5.0V ±10%, 0.0A (analog power) +3.3V ±5%, 0.9A (digital power)	Available Analog Power Supplies for Preamps +7.0V, 1.5A +3.3V, 0.32A +2.5V, 0.25A -2.5V, 0.3A

Tab. 2.1: Specifications Table

3. Hardware Description

The figure below shows the functional block diagram of the A2795 board:

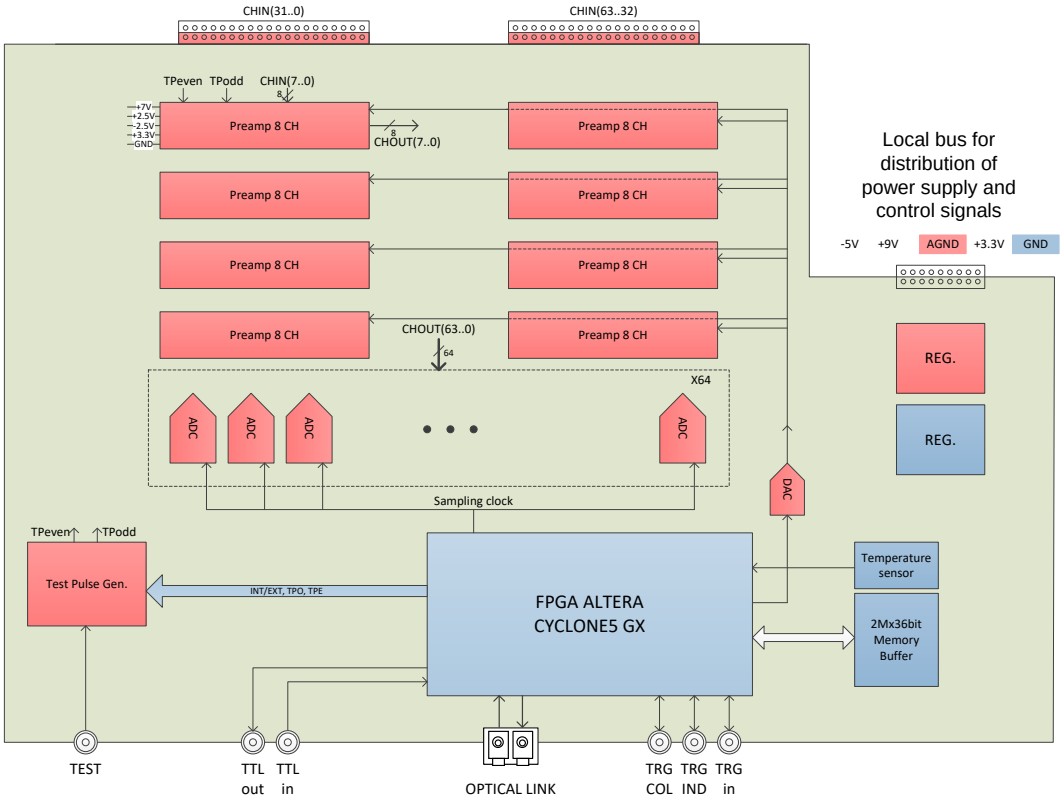

Fig. 3.1: Functional block diagram of the A2795 board

Analog Front-End Block

Input Connections

The input to the 64 preamps of the analog signals from the detector consists in No.2 connectors, 40x2 double-face Card Edge type, for interconnection with Samtec HSEC8-140-01-x-S-01-DV-A connectors. These connectors must be present on the diaphragm of separation between the TPC and the outside world. Usually, the diaphragm is also identified as flange as it is considered to be in solidarity with the mechanics, necessary the vacuum sealing and fixing with the TPC.

The pinout of the two analog input connectors is shown in **Tab. 3.1** below.

Connector: CH[0..31]			
Pin	Signal	Pin	Signal
1	GND	2	GND
3	GND	4	GND
5	GND	6	GND
7	IN0	8	GND
9	IN1	10	GND
….	….	….	GND
67	IN30	68	GND
69	IN31	70	GND
71	GND	72	GND
73	GND	74	GND
75	GND	76	GND
77	GND	78	GND
79	GND	80	GND

Connector: CH[32..63]			
Pin	Signal	Pin	Signal
1	GND	2	GND
3	GND	4	GND
5	GND	6	GND
7	IN32	8	GND
9	IN33	10	GND
….	….	….	GND
67	IN62	68	GND
69	IN63	70	GND
71	GND	72	GND
73	GND	74	GND
75	GND	76	GND
77	GND	78	GND
79	GND	80	GND

Tab. 3.1: Pinout of the input analog connectors

Preamp Modules

The charge preamps are not present on the board. On top side of the A2795 PCB, there are sockets for housing 8 piggyback preamp modules hosting 8 channels each.

Each socket, DIL 34x2 type with female socket contacts PRECIDIP 315-87-1xx-41-003101 type or equivalent, is prepared to interface with preamp modules with the following electromechanical characteristics:

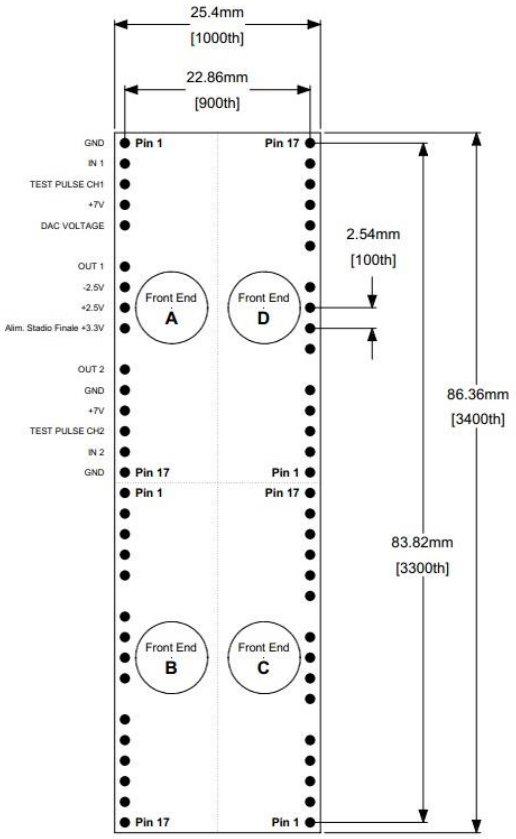

Fig. 3.2: Connector for the preamp modules – Top View

Pin Number (A,B,C,D section)	Pin Name	Type
1	GND	Pwr GND
2	IN1	Analog Input CH1
3	TEST PULSE CH1	In Test Pulse CH1 [0..+330mV]
4	+7V	In Pwr +7V
5	DAC	In DAC Offset [0..+3,3V]
6	GND	Pwr GND
7	OUT1	Out CH1 [0..+3,3V]
8	-2,5V	In Pwr -2,5V
9	+2,5V	In Pwr +2,5V
10	+3,3V	In Pwr +3,3V
11	nc	Non connect
12	OUT2	Out CH2 [0..+3,3V]
13	GND	Pwr GND
14	+7V	In Pwr +7V
15	TEST PULSE CH2	In Test Pulse CH2 [0..+330mV]
16	IN2	Analog Input CH2
17	GND	Pwr GND

Tab. 3.2: Pinout of the connector for the preamp modules

The preamp module plugged into the socket of the A2795 must respect the following mechanical size constraints:

- Referring to the top side of the A2795 PCB, the quote of the components on the bottom of the preamp module must be ≥ 5 mm.
- Referring to the top side of the A2795 PCB, the quote of the components on the top of the preamp module must be ≤ 11 mm.

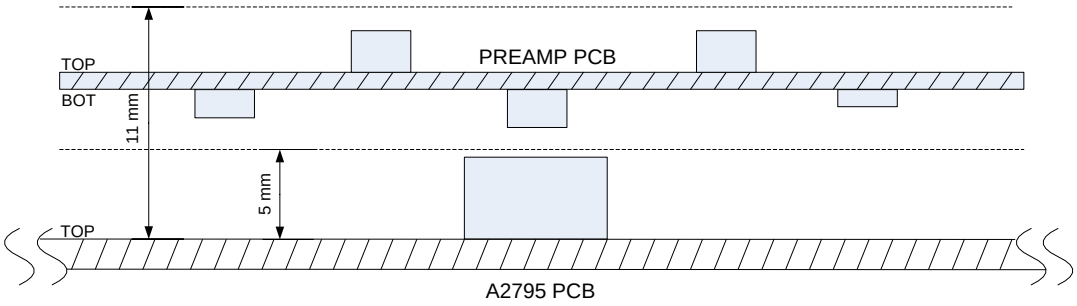

Fig. 3.3: Preamp module mechanical constraints

Given the high sensitivity of the charge preamps, a metal screen appropriately drilled for ventilation needs is provided on the board for the full coverage of the 8 modules. Such screen is removable to facilitate the replacement of the modules.

ADC

The 64 analog voltage signals coming out of the preamp modules are sampled by a 64 Low Power ADCs (AD7276BUJZ), SAR type, 12-bit @ 2.5MHz, with a dynamic input range of 0..+3.3V.

The synchronous operation of the 64 ADCs, guaranteed by the FPGA's driving, allows a precise and systematic temporal reconstruction between the signals of the acquired channels. By means of connections and the TTLink protocol, the sync is extended to all A2795s in the same crate and to A2795s of different crates. Please, refer to Sect. **TTLink (Timing and Trigger Link)**.

The AD7276BUJZ converter does not have an internal Vref that establishes the input dynamic range but uses its own power supply directly. Since all ADCs are powered by a single regulator, it is guaranteed by design that all 64 converters will have exactly the same input dynamics and therefore the same weight in Volts as the LSB (nominally equal to 3300/4096 = 0.857 mV).

The analog input of each converter is preceded by an op-amp as ADC input buffer Anti-Aliasing Low Pass filter, and as a bandwidth limitation to reject the noise outside the signal interest band. This filter limits the bandwidth to 155 KHz (-3 dB).

The quality of the converter in use, the low noise of the regulator and an accurate layout of the A2795 led to an overall electrical noise below 1 LSB

DAC Channel Offset

In order to preserve the entire dynamic range of the ADC either for positive, negative polarity or bipolar signals, there are 2 channels of a 16-bit DAC, controlled by the FPGA, providing a DC offset voltage level common to the two groups of preamps [0..31] and [32..63] (see **Fig. 3.1**).

The voltage levels have a swing of 0..3.3V on a high-impedance load.

Test Pulse Int./Ext.

The A2795 has a Pulse Test system to verify that the preamps are working properly. The source of the pulse test signal can be Internal to the board or External via a connector placed on the front panel. Selecting the Pulse Test source is controlled by the FPGA by means of relay.

Type	Connector	Signal Type	Input Electrical Specification	Channel Input Voltage Range	Note
TP Ext.	LEMO EPL.00.250.NTN	INPUT	0.. +3.3V with Z_{in}= 10KΩ	0..330mV	1:10 Attenuation to 64 input preamplifiers
TP_EVEN Int.	n.a.	Internal DAC Out	n.a.	20..150mV	Default: 100mV, 500ns rise time, 2kHz square wave
TP_ODD Int.	n.a.	Internal DAC Out	n.a.	20..150mV	Default: 100mV, 500ns rise time, 2kHz square wave

Tab. 3.3: Electrical specifications of the Test Pulse

Internal Test Pulse

This mode is intended to qualitatively verify the proper functioning of the preamps present on the board without having to physically access the board itself, very useful function to use when the boards are already installed in the experiment.

The internal pulse test source involves the distinct driving of two groups of 32 even (TP_EVEN) and odd channels (TP_ODD) by a voltage signal consisting of a 2-kHz square wave and a programmable amplitude via 16-bit DAC in the range 20..150 mV_{pp}.

The default pulse is 100-mV_{pp} amplitude and has a rise time of about 500 ns on a high-impedance load.

External Test Pulse

This mode is intended to quantitatively test and measure the characteristics of preamps housed on the board by means of an external source, typically a signal generator.

The input consists of a coaxial connector on the front panel of the board and the signal reaches all 64 preamps. The Input voltage range is [0..+3.3V], DC-coupled, and has an input impedance of 10 kΩ. It is important to note that the input stage attenuates the signal by 1:10. The maximum voltage swing at the preamps input will then be [0..330mV].

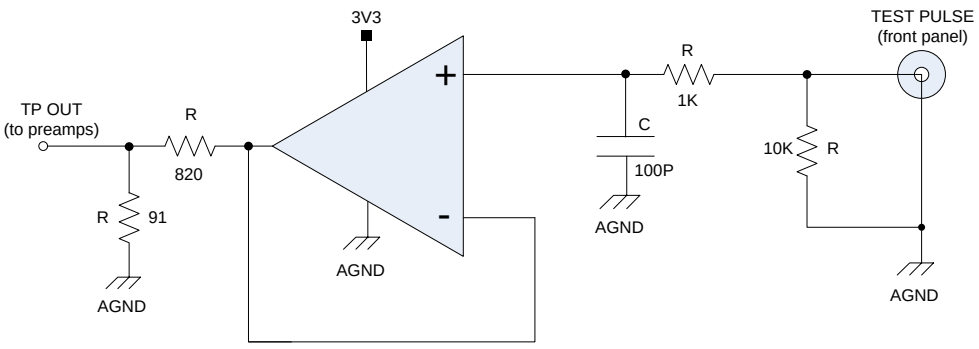

Fig. 3.4: External Test Pulse simplified schematic

FPGA

A single FPGA, Altera Cyclone V GX 5CGXBC4C6F27C7N, is responsible for managing all the main functions of the board. This kind of FPGA ensures low consumption and therefore limits the heat generation, as well as hosts a high-speed SerDes in order to interface directly to the optical link for communication and readout.

The following figure shows the various FPGA interfaces with the sub-parts of the board:

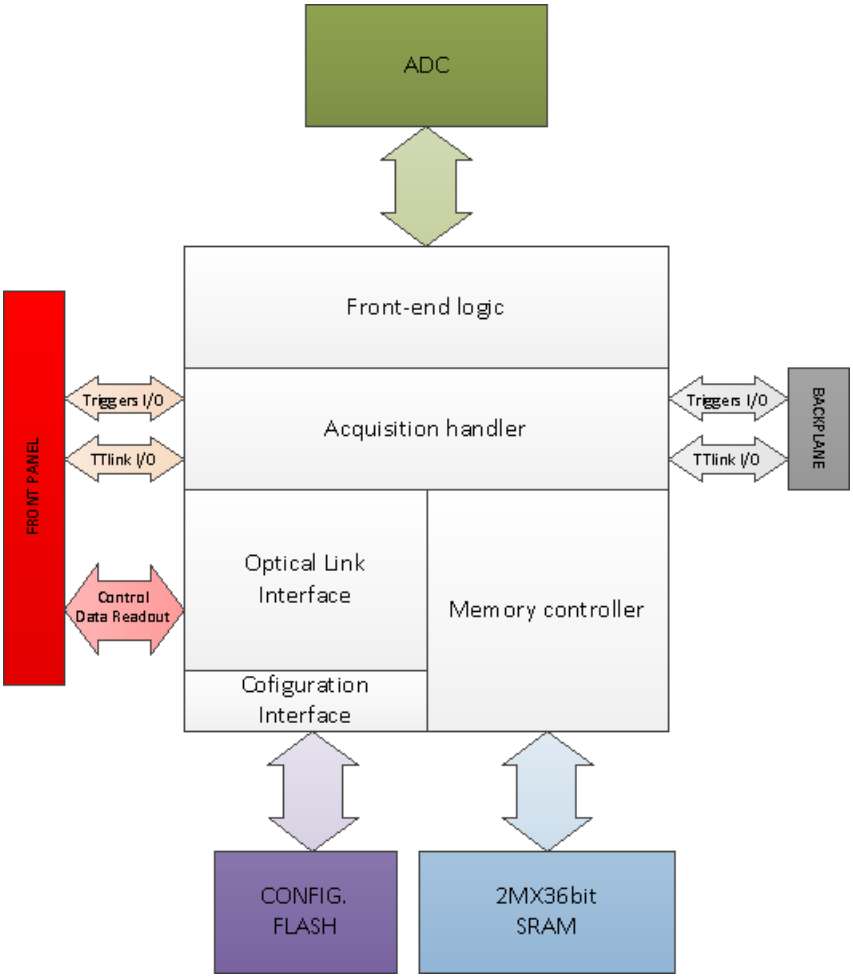

Fig. 3.5: FPGA interfaces

ADC & Memory Buffer

The FPGA is directly interfaced to 64 ADCs and takes care of the data capture, synchronization, and continuous data storage in a 2Mx36bit external memory which is software programmable in terms of number and size of buffers per channel. Each channel totally has at least 144 KB available (see Sect. **Event Acquisition and Storage**).

Backplane

The interface with the backplane allows the propagation of the TTLink signal and then the distribution of the sync and commands necessary for the acquisition by the master A2795 to all other A2795 slaves present in the crate.

The master A2795 is identified as it is inserted into the Slot 0 of the Crate and that position is ensured by 4 bits of identification on the backplane connectors, in binary encoding (Slot 0 must have encoding 0000b, and so on).

On the backplane are also propagated the signals of Collection and Induction Trigger Out, which connect in logical OR all the A2795 in the crate. See Sect. **TTLink (Timing and Trigger Link)** and Sect. **Trigger Logic** for details.

Front Panel

The front panel hosts an input LEMO connector for the physical Trigger and two output LEMO connectors, TRG_COL and TRG_IND (see Sect. **Trigger Logic**).

The panel laso hosts two specific connections for the management of the intra-crate TTLink network (TTLink-IN and TTLink_OUT). See Sect. **TTLink (Timing and Trigger Link)** for a description on how the intra-crate TTLink network works.

Optical Link

The front panel also houses the connector for the optical link.

The optical link interface of the A2795 board currently implements the proven CONET2 CAEN proprietary protocol which allows to reach a continuous data transfer rate up to 80MB/s with a channel bandwidth of 1.25Gb/s.

Since the speed capabilities of the SerDes within the FPGA can reach a maximum of 3.125Gb/s, more performing protocols and/or transmission speeds can potentially be developed in the future. See Sect. **Readout Logic via CONET (Chainable Optical Network)** for details.

Backplane

The board mounts a 10x3 pin male connector type Harting 09251306919, or equivalent, for connections to the crate backplane.

The interconnection for the TTLink, Collection Trigger and Induction Trigger signals makes use of M-LVDS differential transceivers type SN65MLVD200AD to minimize electrical noise generated during their activity.

As a result of the electrical features of these signals, the backplane PCB will have to be made by differential connections with 100Ω Z_{diff} and provide a termination network at the line ends as shown in **Fig. 3.6**.

A SPARE signal is also available to use for future uses. To manage this signal, a Single Ended LVTTL transceiver is provided with drive capability on 50 Ω both Totem Pole and Open collector from the A2795 inserted in the SLOT 0.

It is therefore necessary to foresee on the backplane PCB the realization of this track with an impedance of Z0 = 50 Ω and a termination network at the end of the line as shown in **Fig. 3.6**.

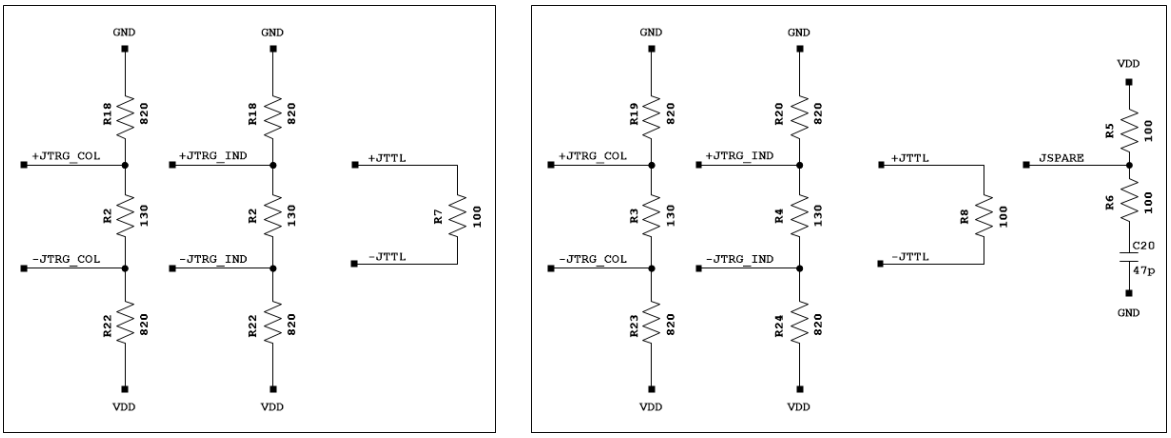

Fig. 3.6: Network terminations on the Backplane

In order the A2795 to work properly, 4 pins, JSLOT_ID [3..0] are also required on the backplane, to identify the physical location of the slot by binary encoding (Slot 0 = 0000b), where:

- Logical 0 = GND
- Logical 1 = 3.3V or float (Pull-up expected on the A2795)

The power supplies needed for the A2795 are +9 V and -5 V for the analog section, and +3.3 V for digital circuitry.

Tab. 3.4 summarizes the signals on the connector, their arrangement and their electrical specifications.

Pin	Signal Name	Type	Note
A1	+JTTL	I/O M-LVDS	TTLink
A2	-JTTL	I/O M-LVDS	TTLink
A3	+JTRG_COL	I/O M-LVDS	Collection Trigger
A4	-JTRG_COL	I/O M-LVDS	Collection Trigger
A5	VDD	Digital Power	
A6	GND	Return Power	
A7	-5V	Analog Power	
A8	GND	Return Power	
A9	GND	Return Power	
A10	+9V	Analog Power	
B1	JSLOT_ID0	I LVTTL	Bit0 Slot ID decode; Pullup on board
B2	JSLOT_ID1	I LVTTL	Bit1 Slot ID decode; Pullup on board
B3	JSLOT_ID2	I LVTTL	Bit2 Slot ID decode; Pullup on board
B4	JSPARE	I/O LVTTL	Output OC or TP
B5	VDD	Digital Power	
B6	GND	Return Power	
B7	-5V	Analog Power	
B8	GND	Return Power	
B9	GND	Return Power	
B10	+9V	Analog Power	
C1	+JTRG_IND	I/O M-LVDS	Induction Trigger
C2	-JTRG_IND	I/O M-LVDS	Induction Trigger
C3	JSLOT_ID3	I LVTTL	Bit3 Slot ID decode; Pullup on board
C4	GND	Return Power	
C5	VDD	Digital Power	
C6	GND	Return Power	
C7	-5V	Analog Power	
C8	GND	Return Power	
C9	GND	Return Power	
C10	+9V	Analog Power	

Tab. 3.4: Backplane connector pinout

Front Panel

There are connectors on the A2795 front panel and monitoring LEDs necessary for the correct operation and status of the board.

In particular, the optical transceiver of the SFP electromechanical standard allows possible replacements and/or upgrades in time without need of hardware changes on the board.

The A2795 currently uses SFP Finisar FTLF8524P2BNV transceiver.

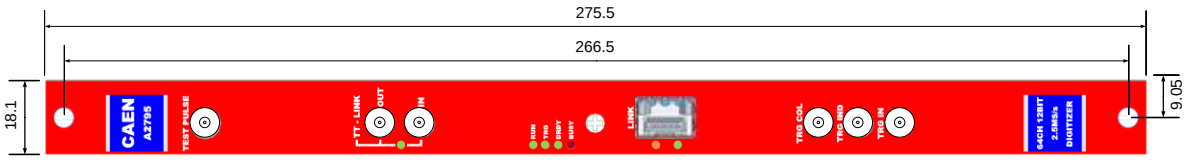

Fig. 3.7: A2795 front panel view (quotes in millimeters)

Label	Type	Signal Type/Color	Electrical Specification	Input Imp. (R_{in})/ Output Load (RL)	Label
PULSE TEST	LEMO EPL.00.250.NTN	Input	0..3,3 V	10 kΩ	1:10 Attenuation
TTLINK OUT	LEMO EPL.00.250.NTN	Output	LVTTL	50 Ω	Totem Pole type
TTLINK IN	LEMO EPL.00.250.NTN	Input	LVTTL	50 Ω	
TRG COL	LEMO EPL.00.250.NTN	Output	LVTTL	50 Ω	Totem Pole type
TRG IND	LEMO EPL.00.250.NTN	Output	LVTTL	50 Ω	Totem Pole type
TRG IN	LEMO EPL.00.250.NTN	Input	LVTTL	50 Ω	
RUN	Led	GREEN			Active capture
TRG	Led	GREEN			Trigger received
DRDY	Led	GREEN			Data Ready: Memory Resident Captured Event
BUSY	Led	RED			Memory buffer Full
LINK	Optical Link	I/O	SFP Optical Link		
	CAGE LED1	GREEN			Fiber connection present
	CAGE LED2	ORANGE			Data transmission

Tab. 3.5: Front Panel I/Os and LEDs table

Power and Voltage Monitor

The A2795 is powered through the backplane connector which must host 3 supply lines for digital and analog circuitry.

The board is equipped with only linear regulators to avoid harmful interferences due to the noise from the sensitive part of the charge preamps.

The regulators selection was anyway based on maximizing the characteristic parameters for the different use case of analog and digital lines (Low Drop and Fast Transient Response for digital lines; Low Drop, Low Noise and High PSRR for analog lines).

+3.3V

Digital power supply: directly powers the +3.3V circuitry on the board and through regulators some FPGA I/O and Core tensions.

The overall consumption of this line depends on the logic implemented in the FPGA and on its operating speed (see **Tab. 3.6**).

+9V

Analog power supply: does not directly feed any circuit of the board. It is connected to those linear regulators deputed to generate all the lower analog supply voltages needed by the board. Since most of them are dedicated exclusively to the preamp section, the overall consumption on the 9V line strongly depends on the preamp used (see **Tab. 3.6**).

-5V

Analog power supply: does not directly feed any circuit of the board. It is connected to the input of the linear controller dedicated to the generation of the lower analog supply voltages needed by the board. Since it is dedicated exclusively to the preamp section, the overall consumption of the -5V line depends on the preamp used (see **Tab. 3.6**).

Backplane Input Power	Input Tolerance	Type	A2795 Load (no preamp)	Voltage available for Preamps	Max. Current (I_{max}) available for Preamps	Notes
+9V	+8.2V ÷ +9.5V	Analog	0.3A			
				+7V	1.5A	
				+3.3V	0.32A	I_{max} depends on the ventilation of the crate
				+2.5V	0.25A	I_{max} depends on the ventilation of the crate
-5V	-4.0V ÷ -5.5V	Analog	0A			
				-2.5V	0.3A	I_{max} depends on the ventilation of the crate
+3.3V	+3.15V ÷ +3.45V	Digital	0.9A			Measured with the current firmware (firmware dependent)

Tab. 3.6: Power Consumptions

There are two “Voltage Supervisor” circuits on the board for +3.3V and +9V input voltages, connected in logical OR with each other They act when the voltages fall below the minimum allowed limit; the board turns on again as soon as the voltages come back over that minimum. This protects the board in case of malfunctioning or component failures due to any instability on the power voltages that the board itself may experience.

The board also hosts a “Power Sequence” circuit which makes possible for the boards in the crate to power on progressively according to the slot in which they are inserted (however after the two voltages of +3.3V and +9V have reached at least their minimum levels required for a stable operation), limiting the power-up current transients.

Mechanics

PCB

The A2795 board has been developed on an FR4 PCB with a thickness of 1.6mm ±10% with a chemical gold finish.

Fig. 3.8 shows the board dimensions in millimeters (mm).

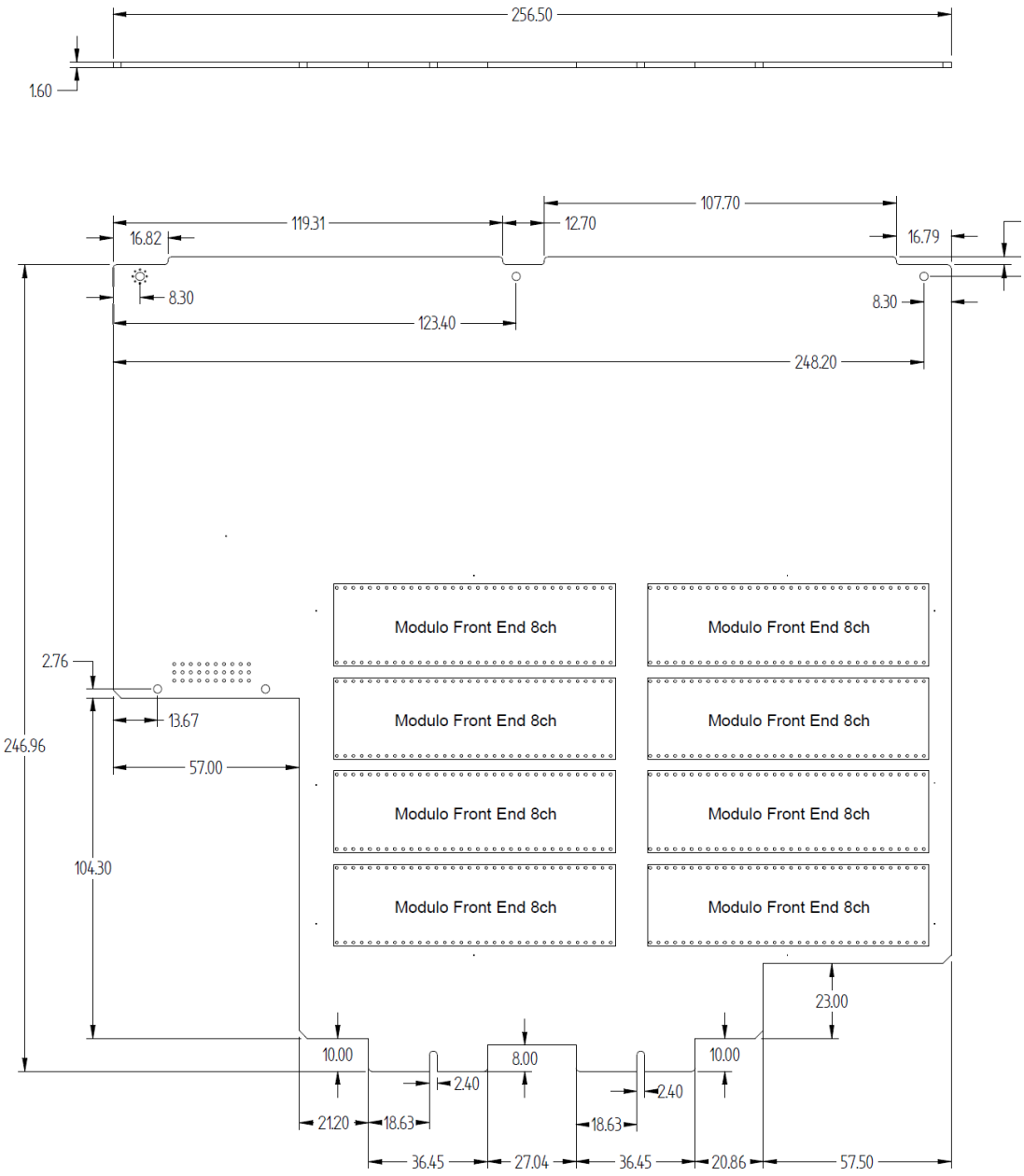

Fig. 3.8: Dimensions of the A2795 mechanics

On the longitudinal sides of the board there is a respect area of 3 mm from the board edges where there are no tracks or components because of the sliding guides normally present in the crate.

The two Edge Card connectors are realized with particular care to the interconnection with the flange: the surface finish of the contacts is in electrolyte gold and follows the specifications indicated by the manufacturer itself (see **Fig. 3.9** from Samtec).

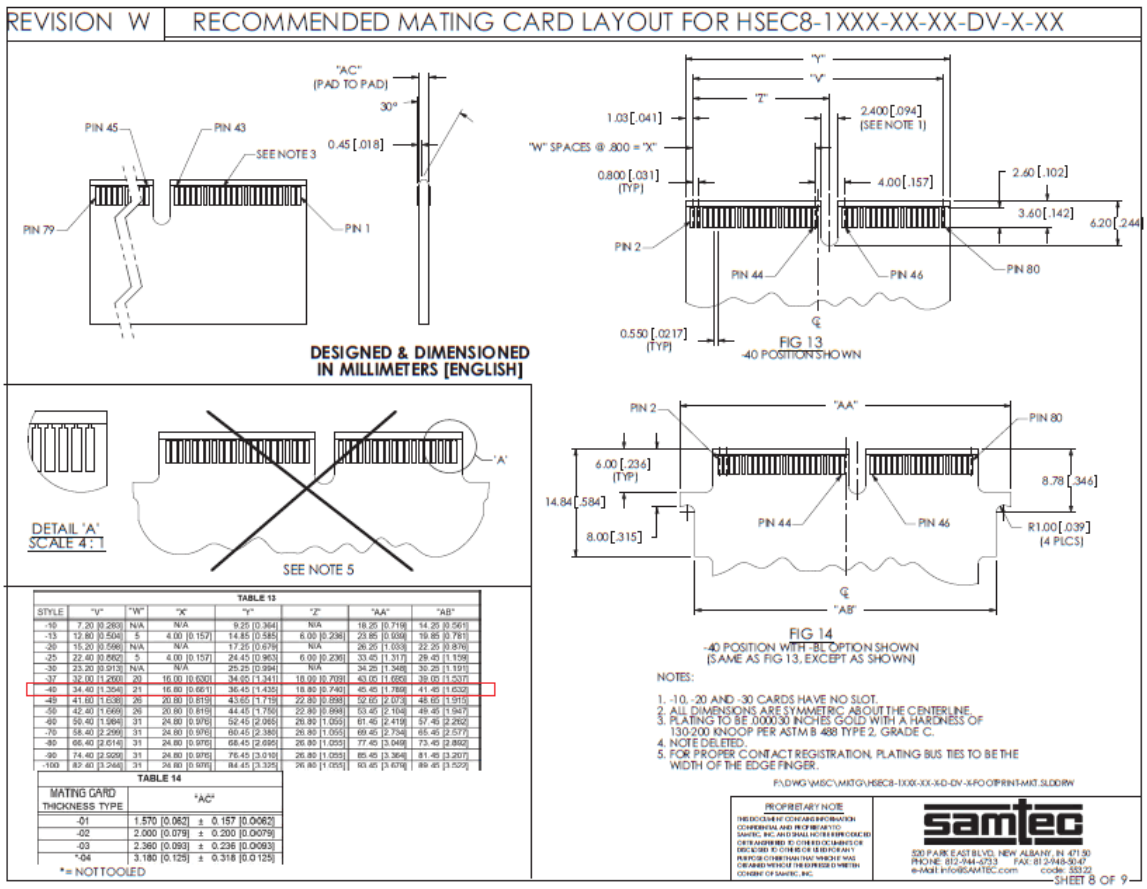

Fig. 3.9: Design specifications of the Edge Card connectors

The work on the PCB routing and lay-up was also taken in good care. Particularly, all the high-speed tracks on the board were treated as transmission lines and were therefore calculated at controlled impedance, taking advantage of the experience of previous board developments with sub nanosecond leading edge.

Front panel

The A2795 is designed to be used in crate with a center-to-center distance between bards of 18.25 mm.

The front panel in aluminum is 275.50 mm x 18.10 mm x 2.5 mm.

Fig. 3.10: Front panel mechanics

Other front panel mechanics specifications:

- No. 3 angular Fischer mod. VS3 for fixing the front panel to the PCB.
- No. 2 fixed type handles Fischer mod. GLK 03, required for insertion and extraction.
- No .2 thumbscrews Fischer mod. RS 1 for mechanical fixing to the crate.

Shielding

Due to the high sensitivity of the charge preamps typically used for capturing signals from TPC, the 8-module area on top side of the A2795 board is equipped with a removable metal screen and electrically connected to GND. This screen is mechanically fixed to a frame on the board by means of two screws and is equipped with grates on the vertical side for internal ventilation of the preamp modules.

The height of the screen related to the top side of the board is 12.5mm.

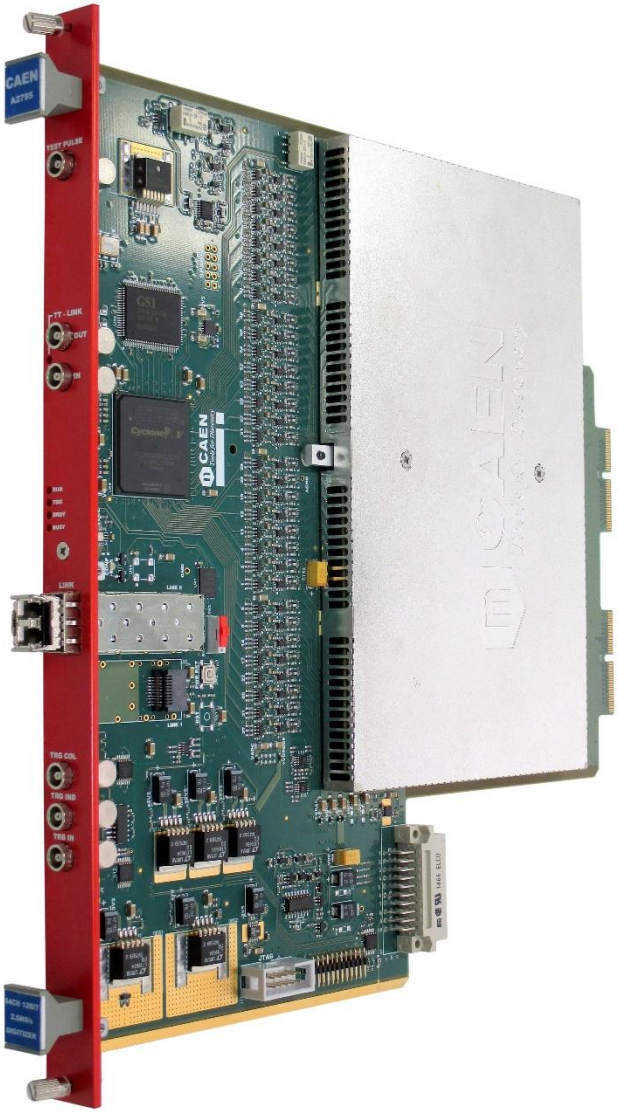

Fig. 3.11: View of the A2795 shield

Ventilation and Temperature Monitor

The arrangement of the components on the A2795 requires the board to be operated in those kind of crates with forced ventilation where the fresh air reaches the boards in the lower and/or lower lateral part, then almost touch the group of preamps and flows out from the crate through two exit openings on the two upper side parts, near the front panel of the boards.

The group of charge preamps, whose electrical performance is sensitive to temperature, is then placed in the coolest part of the board.

For the same reason, high-power components are placed near those parts of the crate where the airflow is higher.

Two temperature sensors operated by the FPGA are also on the board, whose temperatures are constantly read out via optical links in the status data of the board.

The two sensors are placed:

- within the group of preamp modules, to get an indication of the average air temperature inside the shield;
- directly in contact with the regulator, which is the component dissipating more power than the others.

These expedients help in the fine-tuning of the crate and in the power selection of the fan unit by the end-user, according also to the preamps that will be used with the A2795. In fact, absolute temperatures are not predictable a priori as they depend on how the crate and the airflow of its fan unit group are realized.

The operating environmental temperature range of the A2795 is 0 ÷ 40 °C with uncondensed humidity of 10 ÷ 90%.

4. Acquisition and Readout Logic

Event Acquisition and Storage

The A2795 works as Waveform Digitizer of the outputs of the preamps (**Fig. 3.1**): the serial lines of the 64 ADCs are connected to the CYCLONE V FPGA, which continuously reads the digitized samples and writes them, in parallel for all channels, in an array of circular memory buffers (Multi Event Buffers).

When the trigger arrives (see Sect. **Trigger Logic**), the FPGA saves the current buffer (that is, an acquisition windows hereafter called "event") along with the time of the trigger arrival ("timestamp") and the event number. The acquisition continues in the next buffer with no deadtime.

The number and size of circular buffers can be programmed by register, according to the following table:

Number of Buffers	Buffer Size (Samples)	(Time)
16 (default)	4K	1.638400 ms
32	2K	819.2 us
64	1K	409.6 us
128	512	204.8 us
256	256	102.4 us
512	128	51.2 us
1024	64	25.6 us
2048	32	12.8 us
4096	16	6.4 us

Tab. 4.1: Buffer organization of the A2795 digital memory

The events stored can then be read out by means of an optical connection (see Sect. **Optical Link**).

Functionally, the Multi Event Buffer is organized as a FIFO: events are read out in the same time order as they were written.

The format of each event is described in **Fig. 4.1** below.

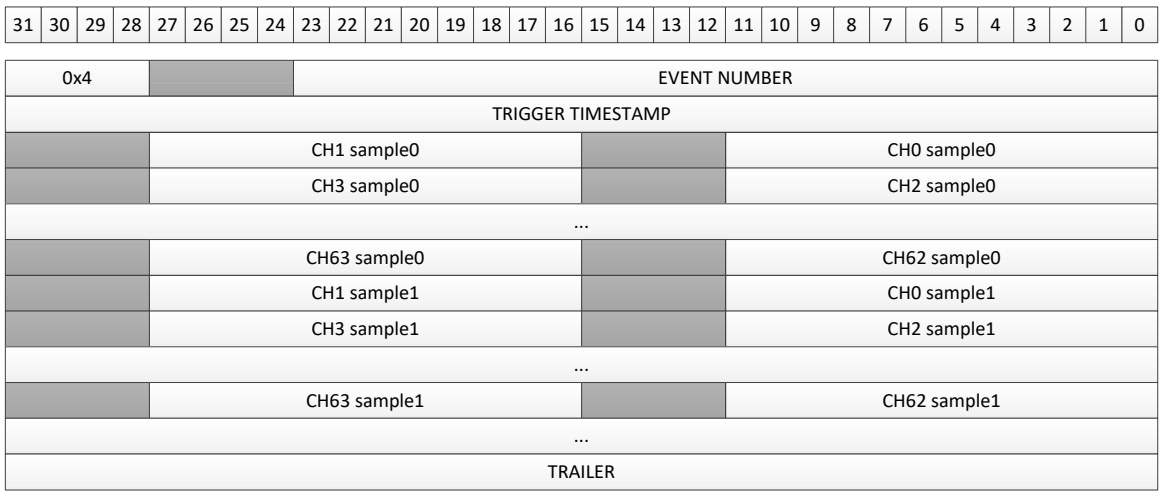

Fig. 4.1: A2795 event structure

TTLink (Timing and Trigger Link)

A system of A2795 boards is totally scalable, which means that it is possible to acquire synchronized data from multiple boards in the same crate but also from multiple crates.

This is possible thanks to a serial link (1 wire) on which a single A2795 (TTLink MASTER) sends a 10MHz clock with modulated duty cycle.

This signal is firstly used to synchronize the sampling clocks of all ADCs on all the boards receiving it (each one called TTLink SLAVE), but also to propagate a set of synchronous commands to all connected boards.

The TTLink duty cycle modulation allows to encode each clock period by one bit (see figure), so that the TTLink a 10Mb transmission is implemented on the TTLink. The bit stream is grouped into 4-bit frames: each frame has an opcode representing a command.

Each TTLink SLAVE internally generates the ADC sampling clock by synchronizing to the TTLink frame at a frequency of 2.5 MHz. The alignment to the 4-bit frame is done by initializing the frame with appropriate COMMA opcodes.

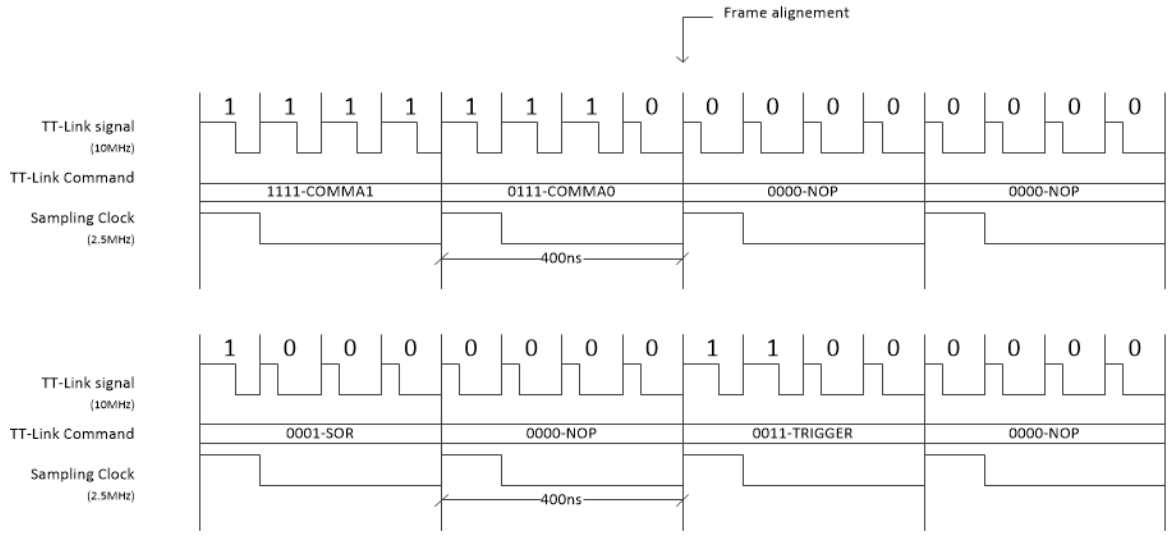

Fig. 4.2: TTLink signal

The implemented opcodes are described in **Tab. 4.2** below.

Opcode	Encoding	Function
Nop	0000	No Operation (IDLE state)
Sor	0001	Start of Run
Eor	0010	End of Run
GTRG, IN	0011	Global Trigger
COMMA1	1111	Comma 1 (frame alignment command)
COMMA0	0111	Comma 0 (frame alignment command)

Tab. 4.2: TTLink opcodes

COMMA1 and COMMA0 must be sequentially generated. If the master is a A2795, the board itself sends COMMA1 and COMMA0 over the backplane upon software command (bit[20] described in Sect. **Single Shot SW**).

It is important to note that the TTLink MASTER itself does not synchronize on the signal generated by it, but on the TTLink signal propagated it back, quite like any TTLink SLAVE.

All the boards in a system (either within the same or multiple crates) so behave like TTLink SLAVE from the synchronization point of view.

Synchronizing A2795s in the same Crate via TTLink

Fig. 4.3 shows the backplane connections of the A2795 boards within a single crate, especially the TTLink connection.

The A2795 in slot 0 is the TTlink MASTER, as it generates the TTLink signal on the backplane; all the boards in the crate, including the MASTER, get synchronized on the TTLink signal sensed from the backplane.

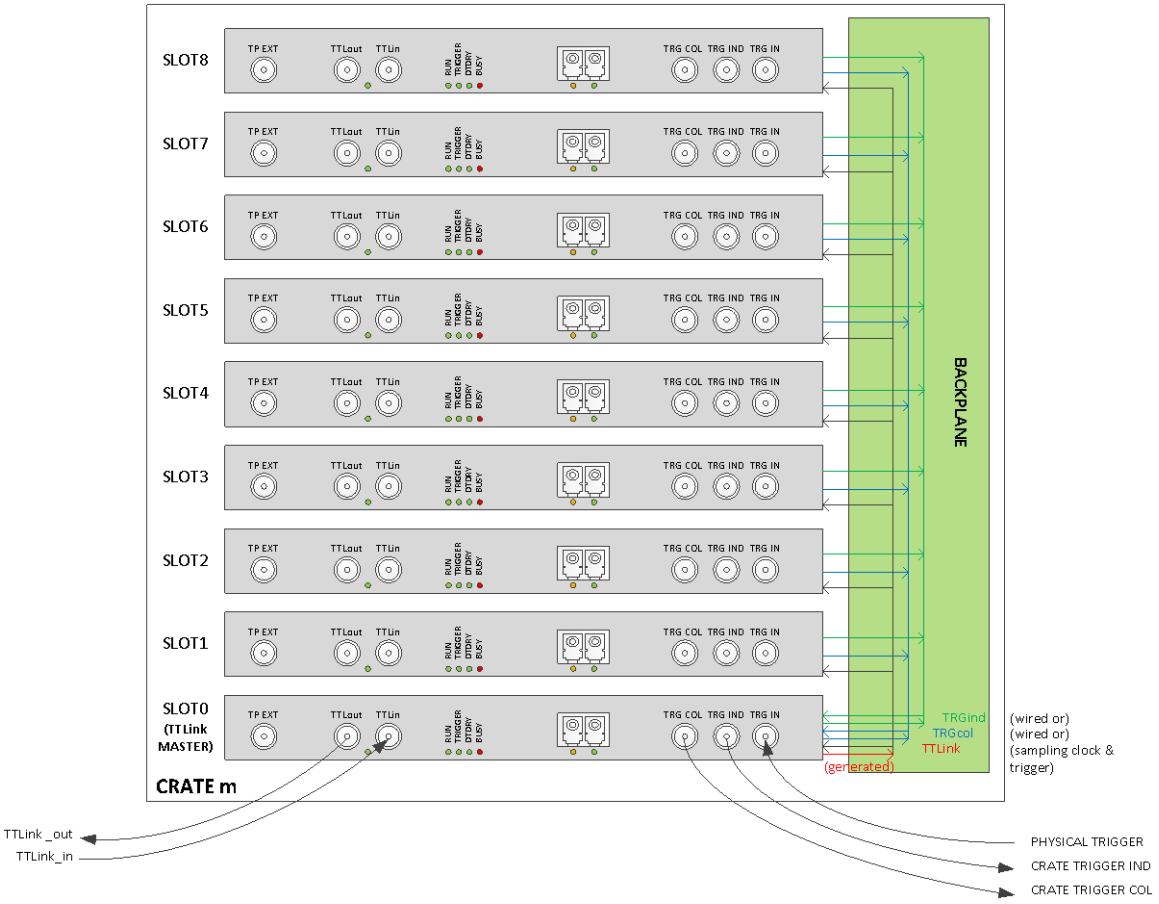

Fig. 4.3: Backplane connections in a single crate

It is so guaranteed that all cards in the crate are synchronous, with regard to both the sampling clock and the acquisition start/stop and trigger opcodes.

NOTE: The TTLink signal propagated on the backplane by the A2795 in SLOT 0 is always obtained by propagating the signal it receives on its front panel TTLink_IN input.

This input can be generated by the crate MASTER board itself on its TTLink_OUT front panel output (which must then be closed on TTLink_IN through a coaxial cable), or it can come from a MASTER outside the crate (see Sect. **Synchronizing Multiple Crates).**

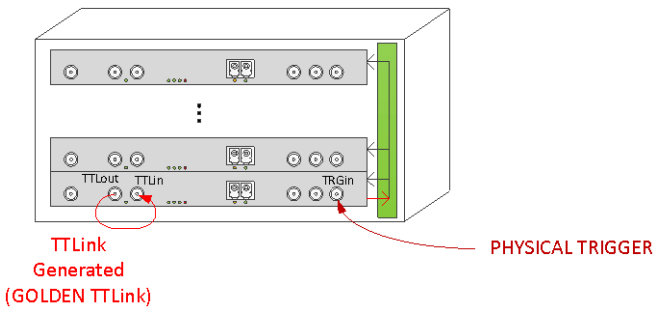

Fig. 4.4: TTLink_OUT to TTLink_IN connection on the MASTER in the crate

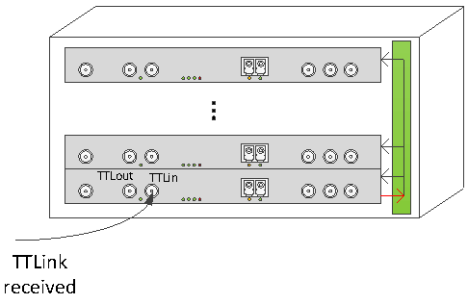

Fig. 4.5: Propagation of TTLink_IN from external MASTER to backplane

Synchronizing Multiple Crates

In case of multiple crates, the TTLink signal is distributed by means of coaxial cables that connect the boards of each SLOT 0. Although different connection modes are possible, there will be always only one board of the system generating the TTLink signal (hereafter called GOLDEN TTLink).

The GOLDEN TTLink MASTER can be any of the A2795 cards which is into SLOT 0 of a crate (possibly, even not a A2795). In any case, the GOLDEN TTLink MASTER must be the board that receives the PHYSICAL TRIGGER of the system, which is then propagated synchronously on the TTLink to all boards in the system.

A set of possible connections are described in next figures (**Fig. 4.6**, **Fig. 4.7**, **Fig. 4.8**, **Fig. 4.9**):

- **Fig. 4.6** shows the TTLink connection of multiple crates in parallel, using a fan-out board. By this mode, the phase difference between the TTLink signals on the different crates is reduced to zero simply by connecting the crates to the fan-out board using cables of the same length.
- **Fig. 4.7** shows the possibility to connect multiple crates in TTLink Daisy chain: since each board in SLOT 0 of a crate GENERATES by default a TTLink signal on its front panel TTLink_OUT output, it must be programmed by register to PROPAGATE on TTLink_OUT the signal received on its TTLink_IN. Although connecting the crates in TTLink Daisy chain guarantees the synchronization of all the boards, there is necessarily a mismatch between the TTLink signals of the different crates, which depends on to the length of the connection cables.
- **Fig. 4.8** shows a possible mixed connection. Under the same number of crates, this mode reduces the number of fan-out board outputs that provide the same GOLDEN TTLink compared to the mode in **Fig. 4.6**.
- **Fig. 4.9** shows another possible example of mixed connection.

It is clear from the figures that whatever is the board generating the GOLDEN TTLink, which is distributed to all the boards in the system, that board must be the one that receives the front panel the physical trigger signal on its front panel TRG_IN input.

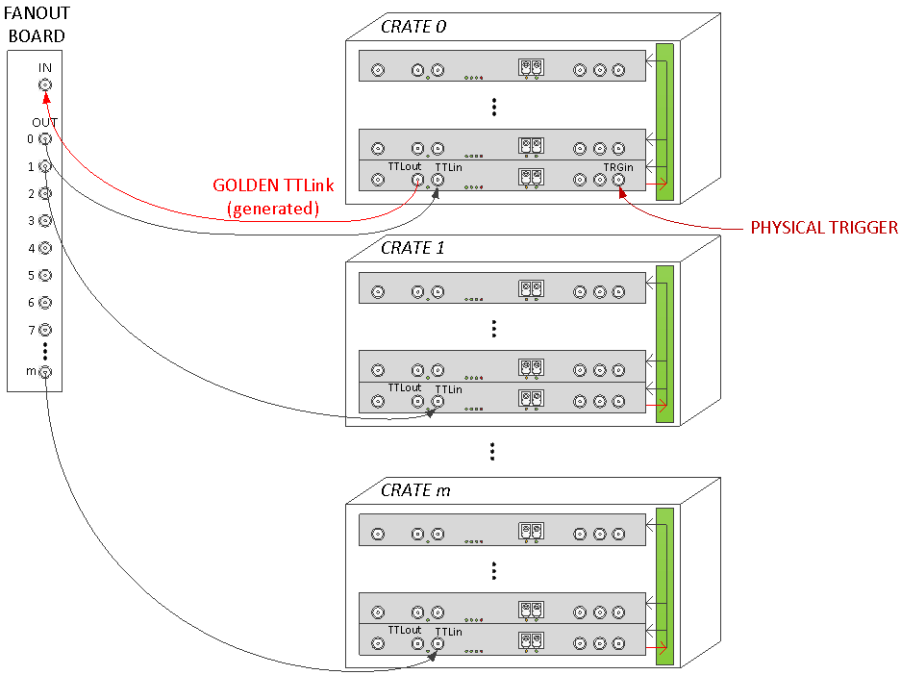

Fig. 4.6: TTLink: connecting multiple crates with fan-outs

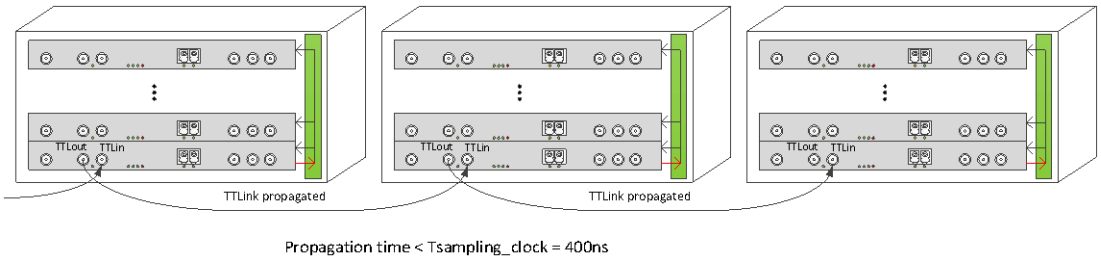

Fig. 4.7: TTLink: Daisy-chain connection between multiple crates

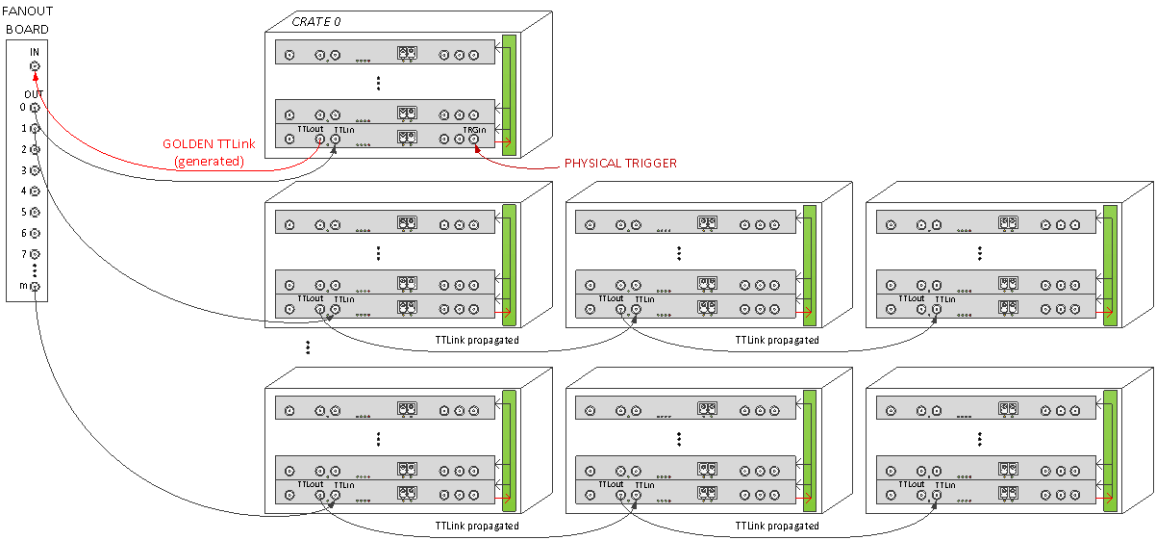

Fig. 4.8: TTLink: mixed connection example #1

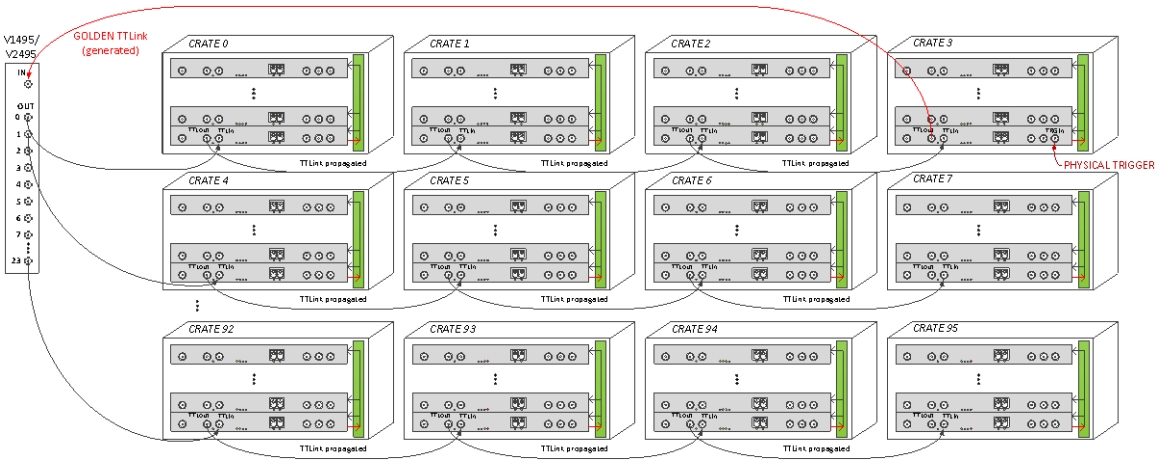

Fig. 4.9: TTLink: mixed connection example #2

Acquisition START/STOP

At the power-on, each A2795 board is in an *idle mode*: acquisition is off (ADC outputs are not read out and no data is written into the MEB).

After the TTLink of all the boards in a system has been aligned to the frame by sending COMMA commands, all the boards step into the *aligned mode*, which means that they can generate signals for the synchronous sampling and readout of the ADCs.

It is now possible to set the boards in *RUN mode*: the sampling clock is so sent to the ADCs, the readout samples are written to memory, and triggers are accepted. At the start of the acquisition, the counter of the trigger timestamp of the board is reset.

In a system with multiple A2795 boards, the acquisition must start at the same time on all the boards (so that the timestamps are aligned). For this reason, the Start Of Run (SOR) command is normally given via TTLink, simultaneously to all boards.

When the GOLDEN TTLink MASTER receives the SOR software command (via optical link), it propagates the SOR to all boards (as described in the previous section), so starting the acquisition simultaneously.

Similarly, acquisition can be stopped simultaneously on all boards using an End Of Run (EOR) command.

It is also possible to give the start and stop of the acquisition to a single board by software command via optical link of the board itself. In such a way that all the boards in the crate are set to RUN one by one, samples will be still acquired in aligned mode, but timestamps will be asynchronous.

Trigger Logic

As described in Sec. **Event Acquisition and Storage**, the trigger of the A2795 board defines a time window where the input waveform of all channels is acquired. A programmable value of input samples is saved before and after the trigger (N_{pre} and N_{post} respectively, where N_{pre} is defined as BufferSize - N_{post}), as shown in Fig. 2.10

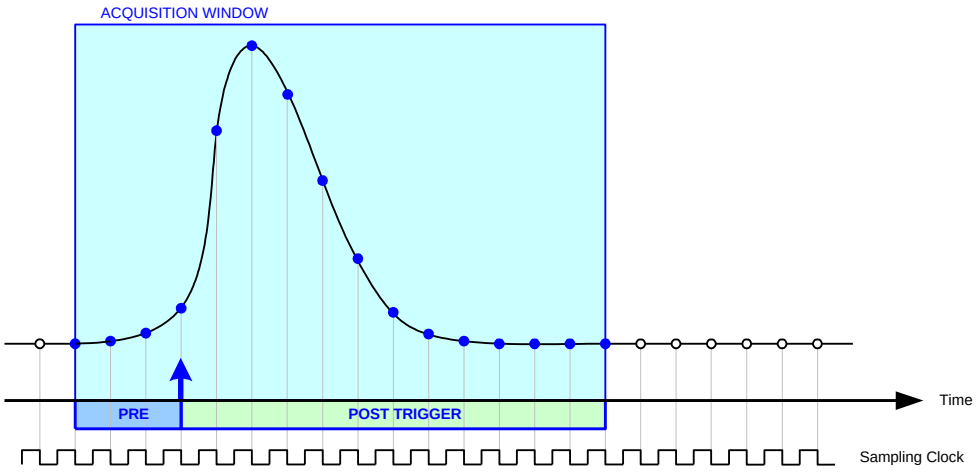

Fig. 4.10: Example of acquisition window with Buffer Size = 16 and Post Trigger = 12

Other triggers occurring in the same acquisition are rejected by the board. Samples of the other waveform are anyway acquired, but they are not identified by a trigger.

Each A2795 board can accept different trigger sources:

- Software Trigger, which is mainly intended for debug purposes. The trigger is sent via software to a single board through optical link.
- Software Trigger via TTLink. The software trigger is sent to the GOLDEN TTLink MASTER, which propagates the trigger to all the other boards of the TTLink system. All boards then receive a synchronous trigger.
- Hardware Trigger on TRG IN front panel connector: the trigger signal is fed into the TRG IN front panel connector of the GOLDEN TTLink MASTER board, which propagates the trigger to all the other boards of the TTLink system. All boards then receive a synchronous trigger.

Triggers are not accepted before the system is not correctly initialized (ARM trigger state).

Trigger OUT Logic

Each A2795 board is prepared for propagating two Trigger OUT signals to the backplane, called “Collection” and “Induction” signals. Such signals are connected in logic OR among all the A2795 boards of the crate, therefore all boards receive them. Although supported at hardware level, no logic is currently implemented, except for testing purposes.

Collection and Induction signals can be also propagated on the board front panel through the LEMO connectors TRG_COL and TRG_IND respectively.

According to the desired configuration, it is possible to select the following configurations:

- Status of TRG_COL and TRG_IND for each A2795 individually;
- Status of TRG_COL and TRG_IND of the whole crate (logic OR of all the A2795 boards in the crate); this information can be retrieved in the front panel connectors of the A2795 MASTER board (slot 0 of the crate).

Readout Logic via CONET (Chainable Optical Network)

CAEN A3818 is a PC controller compliant with the standard PCI Express v2.0, that can be plugged into x8 and x16 slots of the PC. Through the A3818, it is possible to communicate to the boards through optical link. A maximum of 4 links is available, as shown in **Fig. 4.11**. The communication is based on CONET, which is a CAEN proprietary optical protocol. The protocol is bi-directional and the A3818 acts as master, with a maximum transfer rate of 1.25 Gb/s.

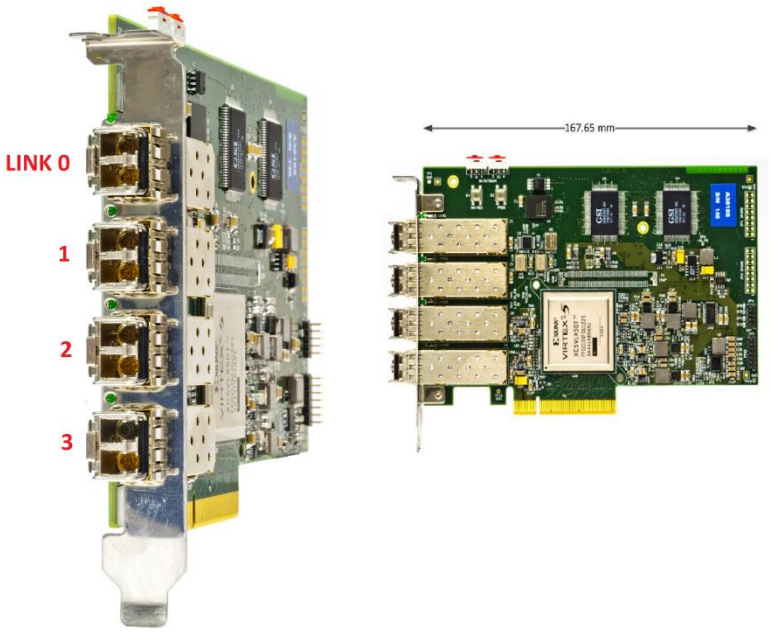

Fig. 4.11: CAEN A3818 optical controller

Up to eight CONET slave nodes can be connected in Daisy chain on each link of the A3818 card optical controller. Therefore, up to thirty-two CAEN A2795 boards can be controlled by the four links of a single A3818 card, which means the simultaneous management of 2048 channels in total.

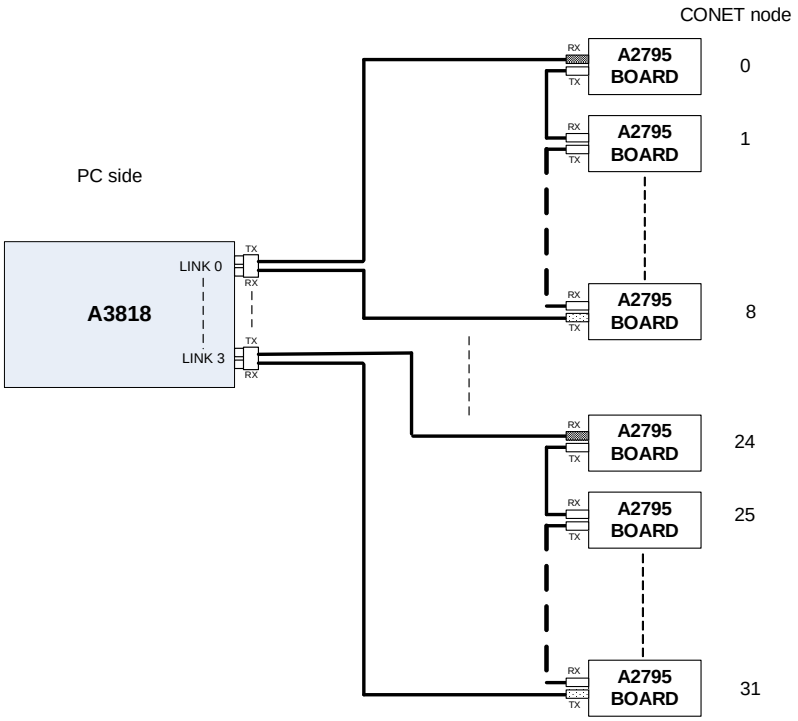

Fig. 4.12: Schematic example of single A3818 maximum Daisy chain capability

Fig. 4.13 shows 8 A2795 boards connected in daisy chain to a single link of the A3818.

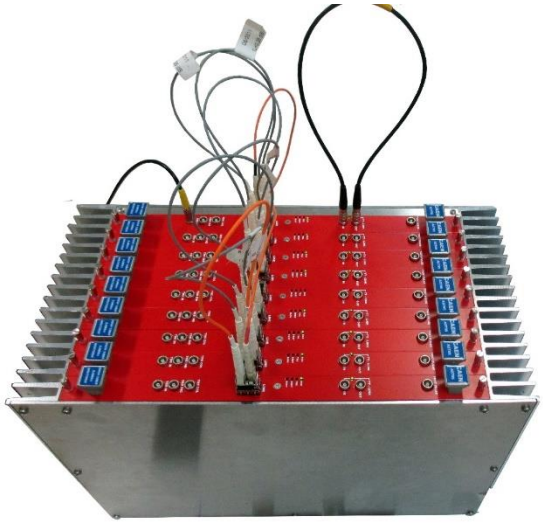

Fig. 4.13: 8 CAEN A2795 boards connected in optical Daisy chain

Fig. 4.14 reports an example of Daisy chain connection of multiple A2795 boards distributed in 9-board crates. The selection of the 8 boards to be Daisy-chained has no constraint.

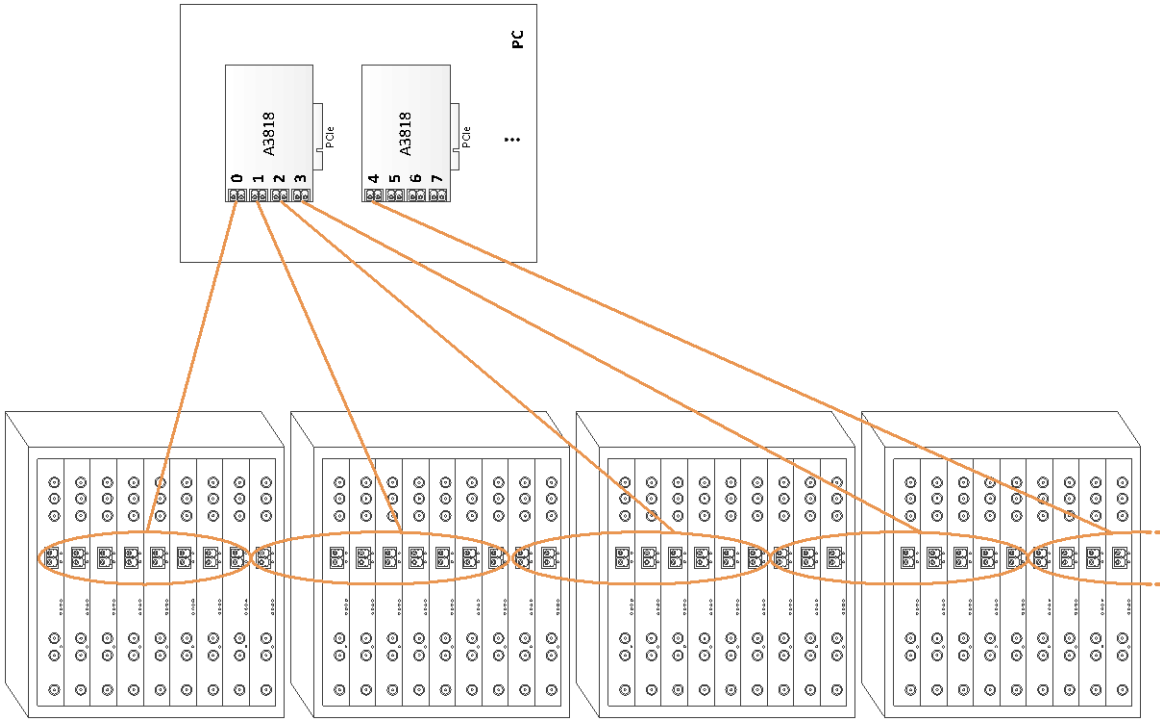

Fig. 4.14: Example of connection of multiple 9-board crates into groups of 8-daisy chained A2795 boards

Fig. 4.15 reports in details how to perform the optical connections between boards in a single crate.

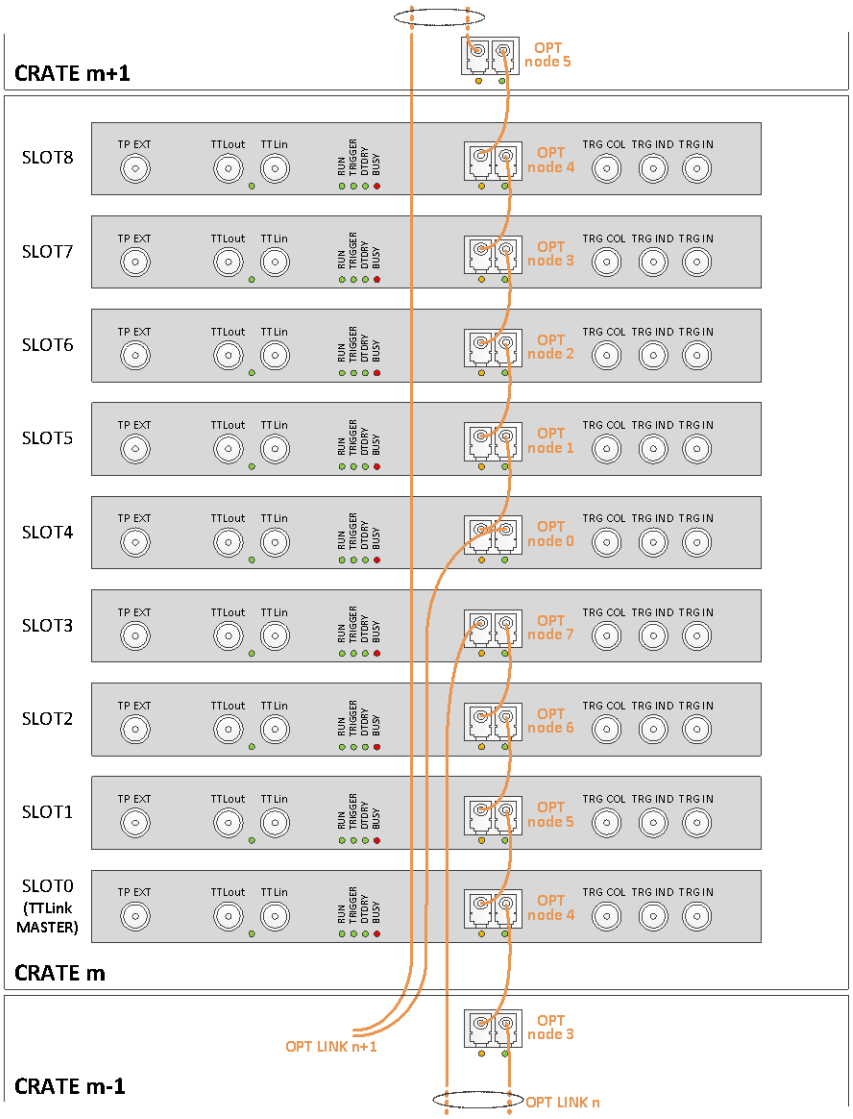

Fig. 4.15: Example of connection of multiple A2795 boards in the same crate via optical link

5. Firmware Upgrade

The FPGA ALTERA CYCLONE V firmware implements the acquisition and readout of the A2795 board, and it can be upgraded writing a configuration file in the FLASH memory of the board itself. The file is an Altera Raw Programming Data format (*.*rpd* extension).

Two kinds of FPGA firmware can be uploaded in the Flash memory, called “Factory” and “Application” firmware. In addition, two different copies of the Application firmware can be uploaded on the memory itself, called “Standard” and “Backup” firmware (see **Fig. 5.1**).

The “Factory” firmware is mainly intended for basic functionality of boot and recovery.

The “Application” firmware implements the acquisition and readout of the board and it can be upgraded by the user by overwriting the flash via optical link.

At the board power-on, the FPGA reads the image of the Factory firmware to start booting. Then it loads the Application firmware, choosing between Standard and Backup image according to the specific switch selection (BKP or STD position of the switch in **Fig. 5.2**). In the unlikely event that the Application image is not present or corrupted, the FPGA remains in Factory mode. In Factory mode, the optical link communication is still guaranteed, thus allowing the user to upgrade the Application firmware to recover the board functioning.

The A2795 Upgrade software allows the user to upgrade and/or verify the two copies of the Application firmware, while the factory firmware can be overwritten by CAEN only.

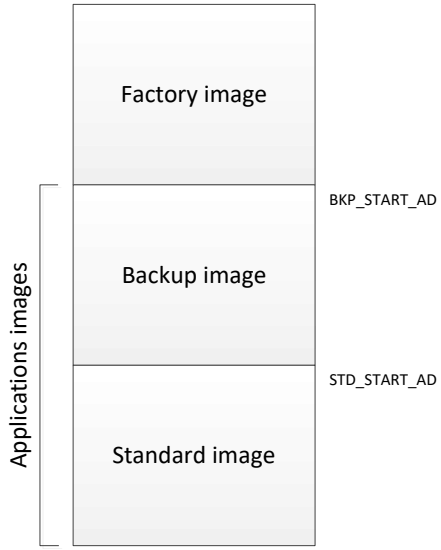

Fig. 5.1: Scheme of the FLASH memory structure with the firmware images

Fig. 5.2: Switch for the selection of Backup (left) and Standard (right) Application firmware

6. Control Software

CAEN provides a software package for A2795 containing:

- A3818 driver for the controller installation
- A low-level library (CAENComm) to access the A2795 boards through the CONET communication interface (optical link)
- Demo codes to manage the communication and acquisition of the A2795 board
- A2795Upgrader software for firmware upgrades

The structure of the software layers is represented in **Fig. 6.1**.

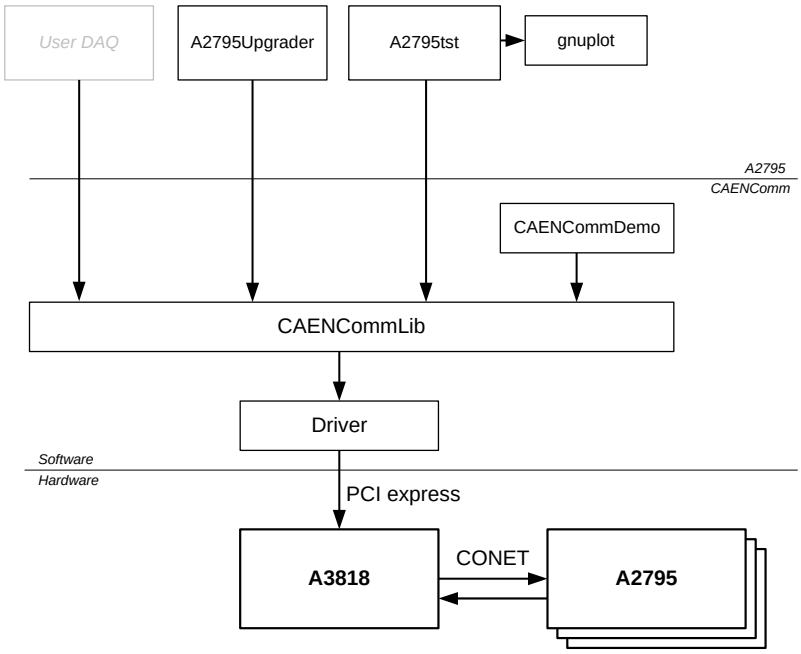

Fig. 6.1: A2795 software layers

Driver for A3818 PCIe Controller

Windows® (version 7 or higher, 32-64 bit) and Linux® (kernel 2.6 or higher) drivers are available for the A3818.

The latest driver version is available for free download at the A3818 *Downloads* page on CAEN web site (**login required**).

CAENComm Library

The CAENComm library contains low-level functions to get access to the CAEN communication interfaces through proprietary protocols for optical link and USB. In case of the A2795 baord, it makes use of the CONET optical link.

The CAENComm library installation package for Windows® and Linux®, as well as the relevant documentation, is available for free download at the CAENComm *Downloads* page on CAEN web site (**login required**).

CAENComm Demo Software (Manual Controller)

A Manual Controller is available In the CAENComm library package under the Samples subfolder. This is a demo (Java® or LabVIEW™) that allows the user to open the communication with the A2795 board and execute simple commands like Read, Write, and BLTRead.

Fig. 6.2: Java version of the CAENComm Demo software

A2795Upgrader

As described in Chap. 5, the A2795Upgrader allows the user to upgrade and/or verify the firmware of the A2795 FPGA through optical link. The firmware upgrade corresponds to a configuration file write, which is a binary file from Altera in the **.rpd* extension.

This software allows the user to open the communication with a A2795 board and write the configuration file in the memory flash through optical link.

A2795tst

The A2795tst software is a simple C code application for the readout of the A2795 boards. The program can be easily compiled for Windows and Linux platforms.

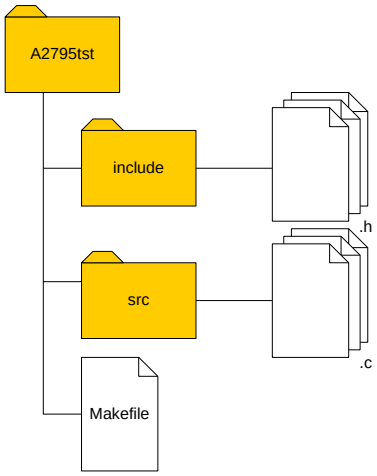

Fig. 6.3: Structure of the A2795sts program folders

The user can modify the demo code to get access to any number of A2795 boards. The current version of the software requires the topology of the optical network, that is the link number of the A3818 which is used for the communication and the number of Daisy chained A2795 boards connected through that specific link.

```
Usage: A2795tst <conet link> <conet node number>
```

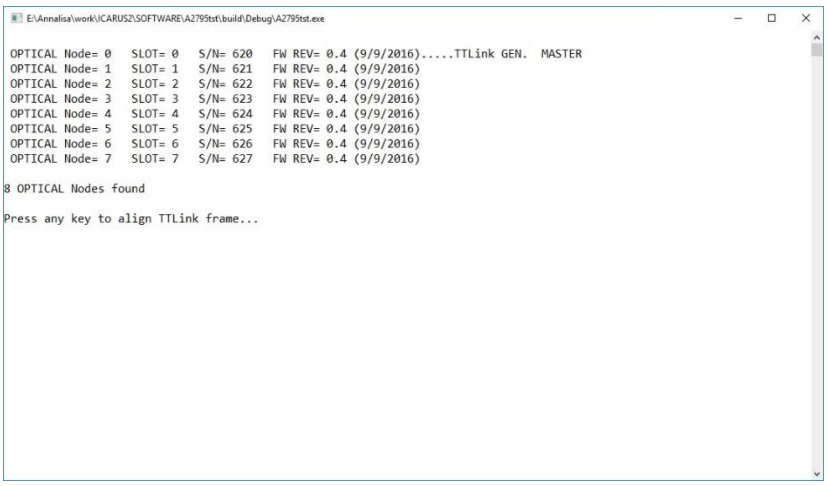

Fig. 6.4: Initialization and identification of the optical Daisy chained boards by A2795tst

The software can initialize and identify the boards found in the optical chain defined by <conet link> and it returns an error if it finds less boards than what defined in <conet node number>.

After the initialization, it is possible to press any key to perform the “TTLink Alignment”, which returns a simple menu (see **Fig. 6.5**) where the user can:

- Select a specific board in the optical chain to communicate with (conet node)
- Get access in read/write mode to the selected board through the Manual Controller
- Set the acquisition status in RUN mode either in case of a single board or multiple synchronized boards via TTTLink (see Sect. **Acquisition START/STOP**)
- Control the data acquisition

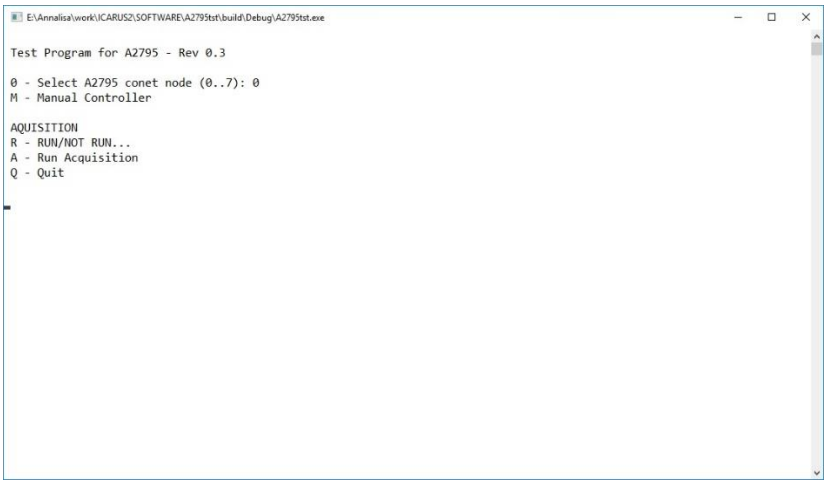

Fig. 6.5: A2795tst main menu

The program reads the events as acquired by the A2795 board and provides few examples of data analysis, such as the RMS noise calculation, FFT, and histograms.

The A2795sts software does not make use of graphical user interfaces, anyway it is possible to plot the events by means of the freeware third-party gnuplot graphing utility (http://www.gnuplot.info), Linux and Windows compliant.

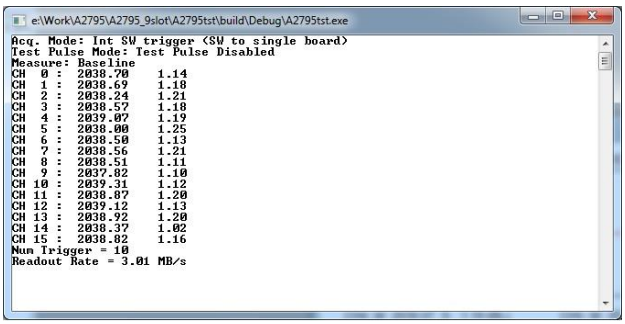

Fig. 6.6: RMS noise calculation by A2795tst for a group of 16 channels

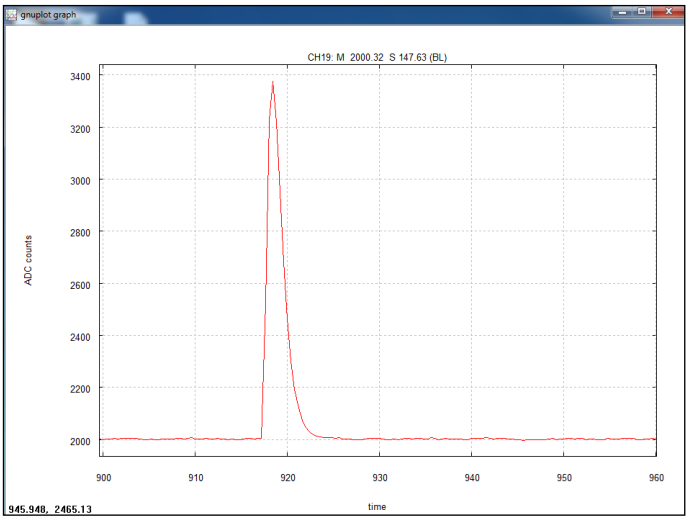

Fig. 6.7: Waveform plot by gnuplot utility

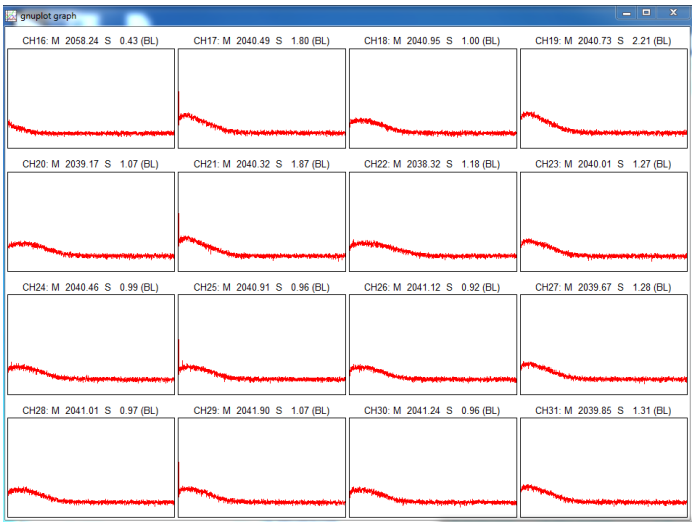

Fig. 6.8: 16-channel FFT plot by gnuplot utility

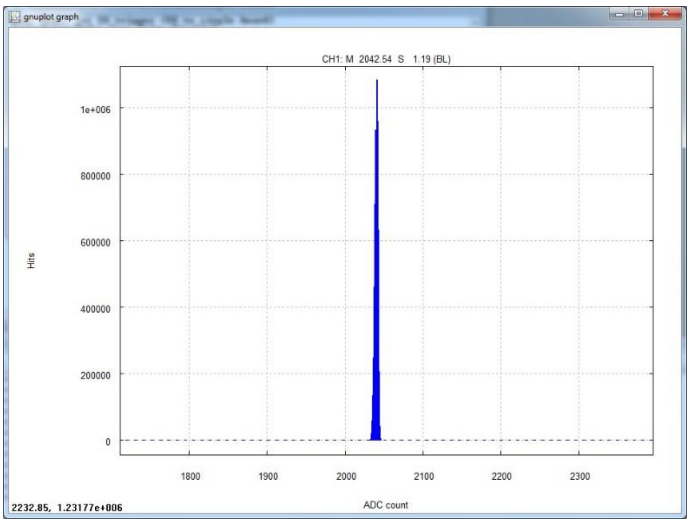

Fig. 6.9: Histogram plot by gnuplot utility

7. A2795 Registers

The A2795 has a set of 32-bit registers that can be read and/or written through the optical link. **Tab. 7.1** reports the register address map, indicating also the register access Type (R = read only, W = write only, R/W = read and write), the number of significant bits, whether the register is initialized or not after a Reset (power ON, LinkReset or SW reset) or after a Clear (SW clear), the Default value after the initialization and the Function of the register.

Register name		Address	Mode	RES	CLR	Default
Multi Event Buffer (MEB) Readout Data		0x0000	R	*	*	-
Firmware Revision		0x1000	R			-
Acquisition Control		0x1004, 0x1008 (BitSet), 0x100C (BitClear)	R/W	*		0x00000000
Test		0x1014	R/W	*		0x0F0F0F0F
Status		0x1018	R			-
Post Trigger		0x1020	R/W	*		0x00000000
Single Shot SW		0x1028	W			
DAC Control		0x1034	R/W	*		0x00000000
DAC Reading		0x1040 – 0x104C	R	*		
Board Temperature		0x1108	R			
Test Pulses Control		0x1200	R/W	*		0x00030009
Configuration ROM	model	0x2000 ÷ 0x2003	R			
	sernum	0x2004 ÷ 0x2007	R			
	opr_year	0x2008 ÷ 0x200B	R			
	opr_num	0x200C ÷ 0x200F	R			

Tab. 7.1: A2795 register address map

Multi Event Buffer (MEB) Readout Data

A read access to the MEB address, either in single mode or block transfer, causes the readout of the data from the Multi Event Buffer.

Address: 0x0000
Bits: [31:0]
Access Mode: R

Firmware Revision

Returns the firmware revision and build date.

Address: 0x1000

Bits: [31:0]

Access Mode: R

Bit	Description
[15:0]	Firmware Revision: the format if XX.YY, where XX and YY are the major and minor Revision Numbers (2 bytes each)
[31:16]	Realization Date: The format is YMDD, where Y is the year (0 stands for 2016), M is the month (from 0x1 to 0xC) and DD is the day (number that must be interpreted as a decimal). Example: 0x0214 is the 14th of February 2016

Acquisition Control

There are three ways to write the content of the Control Register:

- Normal Write (at address 0x1004). where the content of the register is fully overwritten by the new data.
- Bit Set Mode (at address 0x1008), where writing '1' in one bit will set that bit; writing '0' leaves the bit unchanged.
- Bit Clear Mode (at address 0x100C) where writing '1' in one bit will clear that bit; writing '0' leaves the bit unchanged.

The use of the Bit Set/Clear modes are recommended when concurrent processes can access the register; this prevents a process to operate on the content of the register while another process has already changed it. The read access to the Control Register can be done at any address.

Address: 0x1004, 0x1008 (BitSet), 0x100C (BitClear)
Bits: [31:0]
Access Mode: R/W

Bit	Description
[3:0] 0x0000000F Default: 0	Buffer Organization: number of buffers in which the memory is divided (see **Tab. 7.2**)
[4] 0x00000010 Default: 0	Force Acquisition Run: normally, the acquisition is started at the same time in all the A2795s by means of a command sent through the TT-Link. However, it is possible to force one board to start the acquisition setting this bit. 0: The acquisition start/stop is controlled by TT-Link 1: The acquisition is forced to be running
[6:5]	Reserved.
[7] 0x00000080 Default: 0	Master Inhibit Trigger. 0: Triggers sent through the TT-Link Master are enabled 1: Triggers sent through the TT-Link Master are disabled
[8] 0x00000100 Default: 0	Test Pattern Enable. 0: Test pattern is disabled. Data are real samples coming from the ADCs 1: Test Pattern is enabled: Data from the ADCs are replaced by a triangular wave ranging from 0x000 to 0xFFF and back to 0x000
[9] 0x00000200 Default: 0	SRAM test Enable (reserved). 0: Acquisition mode 1: Test mode (only for CAEN test)
[10] 0x00000400 Default: 0	Front Panel TT-Link propagation Enable. 0: TTLink_OUT font panel signal generated by the Master 1: TTLink_OUT font panel signal propagated fom TTLink_IN
[27:11]	Reserved
[29:28] 0x30000000 Default: 0	I/O test Enable (reserved). 0: Acquisition mode 1: Test mode (only for CAEN test)
[30]	Reserved
[31] 0x80000000 Default: 0	EventOne test Enable (reserved). 0: Acquisition mode 1: Test mode (only for CAEN test)

The A2795 has 2 M x 36 bit of SRAM memory. One channel sample takes 12 bits. This means that each board sample (for 64 channels) takes 22 words x 36 bits.

The memory is organized in a certain number of circular buffers, according to the table below.

Bit [3:0]	# of buffers	Buffer Size	
		in samples	in time
0	16	4K	1,638400 ms
1	32	2K	819,2 us
2	64	1K	409,6 us
3	128	512	204,8 us
4	256	256	102,4 us
5	512	128	51,2 us
6	1024	64	25,6 us
7	2048	32	12,8 us
8	4096	16	6,4 us
others	not allowed		

Tab. 7.2: Buffer Organization Table

Test

This register may have different meanings:

- It can be used as a 32-bit scratch register to verify the regular access from the Optical Link to the A2795.
- Setting of the Internal Test (only for CAEN test).

Address: 0x1014
Bits: [31:0]
Access Mode: R

Bit	Description
[31:0]	Read it to verify the optical link access

Status

This register reports the status of the acquisition.

Address: 0x1018
Bits: [31:0]
Access Mode: R

Bit	Description
[3:0]	Slot ID: slot number in which the board is plugged (from 0 to 8)
[4]	Acquisition Running. 0: The acquisition is stopped 1: The acquisition is running
[5]	Data ready. 0: The board has no data 1: The board has data
[6]	Acquisition busy. 0: The board has available buffers 1: The board has no available buffer
[31:7]	Reserved

Post Trigger

The Post Trigger Register (13 bits) allows the user to set the position of the trigger inside the acquisition window, that is the number of samples following the trigger.

Address: 0x1020
Bits: [31:0]
Access Mode: R/W

Bit	Description
[12:0]	Post trigger samples
[31:13]	Reserved

Single Shot SW

This register is used to send SW commands to the A2795 board. Each bit of the register corresponds to a specific action; writing a word to this register causes the execution of the actions related to those bits that are '1' in the word. It is possible to set multiple bits, thus giving the possibility to cause the simultaneous execution of multiple actions. The bits above 16 are dedicated to send commands through the TT-Link. These bits must be used only in the board that is Master of the TT-Link. Using them in the other boards, will not have any effect.

Address: 0x1028
Bits: [31:0]
Access Mode: W

Bit	Description
[0]	Reset: this command causes the following actions. • Stops the acquisition (if it is running) • Clears all data and counters • Reset the Trigger Time Tag • Set to their default value all the registers with '•' in the column RES of **Tab. 7.1**
[1]	Clear: this command causes the following actions. • Stops the acquisition • Clears all data and counters • Reset the Trigger Time Tag
[2]	Board Trigger: send a trigger to the A2795
[3]	Reserved
[4]	Board Trigger IND Test Pulse
[5]	Board Trigger COL Test Pulse
[15:6]	Reserved
[16]	TT-Link Start of Run (SOR)
[17]	TT-Link End of Run (EOR)
[18]	TT-Link Global Trigger
[19]	Reserved
[20]	TT-Link Send Comma. This command allows the TT-Link slave boards to initialize the state machines that receive the TT-Link and decode the commands
[21]	TT-Link Trigger IND Test Pulse
[22]	TT-Link Trigger COL Test Pulse
[31:23]	Reserved

DAC Control

A write access to the DAC Control Register (19 bits) causes the programming of one of the 4 DAC (16 bits) on the board; more in detail, the bits [18..16] select the DAC to be programmed. The bits [15..0] representing the value to be written into the DAC.

DAC A [18..16] = 000	*INTERNAL Test Pulse Amplitude, CH ODD*	These DACs adjust the Amplitude of the Test Pulses. The output of the DACs can range from 0V (0x0000) to 3.3V (0xFFFF). The default value after a reset or power-on is 0x7000.
DAC B [18..16] = 001	*INTERNAL Test Pulse Amplitude, CH EVEN*	
DAC C [18..16] = 010	*DAC Offset CH[31..00]*	These DACs adjust the DC level of the output of the preamplifiers. The output of the DACs can range from 0V (0x0000) to 3.3V (0xFFFF). The default value after a reset or power-on is 0x8000.
DAC D [18..16] = 011	*DAC Offset CH[63..32]*	
ALL DACs [18..16] = 111	*Program all the DACs with the value of bits [15..0] of the DAC Control Register.*	

A read access to this register returns the content of the register as stored in the FPGA (it doesn't correspond to a real reading of the analog voltage).

Address: 0x1034
Bits: [31:0]
Access Mode: R/W

Bit	Description
[15:0]	DAC value
[18:16]	DAC selection. Options are. 000 = DAC A 001 = DAC B 010 = DAC C 011 = DAC D 111 = ALL.DACs
[31:19]	Reserved

DAC Reading

A read access to these registers returns the last value programmed for the correspondent DAC, as stored in the FPGA (it doesn't correspond to a real reading of the analog voltage).

Address: 0x1040, 0x1044, 0x1048, 0x104C
Bits: [31:0]
Access Mode: R

Bit	Description
[31:0]	DAC value

Board Temperature

The card is equipped with two temperature sensors: the FPGA reads the two sensors constantly and writes the value read in the temperature register.

Address: 0x1108
Bits: [31:0]
Access Mode: R

Bit	Description
[7:0]	Temperature sensor 1 value
[15:8]	Reserved
[32:16]	Temperature sensor 2 value
[31:24]	Reserved

Test Pulses Control

A write access to the Test Pulses Control register causes the programming of some relays on the board for the generation of internal test pulses or to accept external test pulses.

The mask definition for the Test Pulses Control Register is shown in the table below.

Disable Test Pulses	0x00030009
Enable External Test Pulses	0x00030006
Enable Internal Test Pulses	0x00030005
Internal test pulses for CH ODD	0x00050030
Internal test pulses for CH EVEN	0x00060030

Address: 0x1200
Bits: [18:16] [5:0]
Access Mode: W

Configuration ROM

Address: 0x2000 ÷ 0x200F

Bits: [7:0]

Access Mode: R

Model	0x2000	Board Model
Sernum	0x2004	Serial Number
Opr_year	0x2008	Production Year
Opr_num	0x200C	Production Number

8. Technical Support Service

CAEN makes available the technical support of its specialists for requests concerning the software and hardware. Use the support form available at the following link:

https://www.caen.it/support-services/support-form/

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