725 Digitizer Family

16/8 Ch. 14-bit 250 MS/s Digitizer

APPLICATIONS

- **Nuclear and Particle Physics**
- **Dark Matter and Astroparticle Physics**
- **Fast Neutron spectroscopy**
- **Homeland Security**

FORM FACTOR

VME64   VME64X   NIM   DESKTOP

FUNCTIONS

ICH WV TS TDC QDC CFD PHA PSD ZS DAW

Maximum flexibility

APPLICATION NOTES

- AN5157
- AN5995
- GD2783
- GD2827

Overview

The 725 is a family of CAEN Waveform Digitizers able to perform basic waveform recording and run online advanced algorithms (DPP) for digital pulse processing: charge integration and pulse shape discrimination with constant fraction timing, pulse height analysis, zero-length encoding, and dynamic acquisition window. The wide selection of DPP algorithms supported by this family makes the 725 a "must-have" for any kind of nuclear physics application. Data is read by a Flash ADC, 14-bit resolution and 250 MS/s sampling rate, which is well suited for mid-fast signals as the ones coming from liquid or inorganic scintillators coupled to PMTs or Silicon Photomultipliers, but also for high precision detectors as Silicon or HPGe coupled with charged sensitive preamplifiers. The acquisition can be channel independent and it is possible to make coincidence/anti-coincidence logic among different channels and external veto/gating. Multiple boards can be synchronized to build up complex systems.

In case of DPP mode, data can be saved in time-stamped list mode to support higher input rates and improving the throughput performances. Piled-up events can be rejected or saved for offline analysis. The acquisition in DPP mode is fully controlled by the CoMPASS and MC^{2}Analyzer software, which manage the algorithm parameters, build the plots and saves the relevant energy, time, and PSD spectra. In case of waveform recording mode, the user can take advantage of the CAENScope and WaveDump software to access and save the waveforms.

Libraries and demo software in C and LabView are available for integration and customization of specific acquisition systems. 725 family comes in three form factors: VME (16 or 8 input channels), NIM (8 input channels) and Desktop (8 input channels). The communication to and from the board is provided through the following interfaces: USB (Desktop and NIM form factors), VMEbus (VME form factor), and Optical Link (all form factors).

Features

- 14-bit @ 250 MS/s
- Analog inputs on MCX coax. connectors
- VME64/VME64X (16/8 ch.), NIM (8 ch.) and Desktop (8 ch.) modules
- 0.5 and 2 Vpp software selectable input dynamic range with programmable DC offset adjustment
- Algorithms for Digital Pulse Processing (DPP)
- VME, USB and Optical Link communication interfaces
- Multi-board synchronization features
- Daisy chain capability
- Demo software tools, Control Software for waveform recording and DPP firmware, C and LabVIEW libraries

| Firmware	Software	ICH	WV	TS	TDC	QDC	CFD	PHA	PSD	ZS	DAW
WAVEFORM RECORDING	WAVE DUMP CAEN / SCOPE CAEN		•	•							
DPP PSD	CoMPASS CAEN	•	•	•	•	•	•		•		
DPP PHA	MC² CAEN / CoMPASS CAEN	•	•	•	•			•			
DPP ZLE PLUS	ZLE⁺ CAEN		•	•						•	
DPP DAW	DAW CAEN	•	•	•							•

Principle of Operation

CAEN Waveform Digitizers are devices able to continuously acquire analog input signals, which are sampled by fast ADCs and stored into digital memories where they are avaiable for readout through different communication interfaces (USB, VMEBus, Optical Link). Depending on the FPGA firmware, the digitizer can work like an oscilloscope to acquire raw waveforms, or perform online processing to calculate parameters such as pulse height, charge, time stamp, pulse shape discrimination. In the latter case, the output data is a time-stamped list of parameters. Data reductions and zero suppression algorithms are also available. Digitization in CAEN digitizers is based on two main technics: **Flash ADC** and **Switched Capacitor Arrays**. Flash ADC are the fastest A/D converters, where the sampling and the analog-to-digital conversion are made practically at the same time. Flash ADC are so not affected by dead-time due to conversion. In the Switched Capacitor Arrays, the sampling and the A/D conversion take place at different times, thus introducing a dead-time. Despite of the dead-time, the Switched Capacitor Array Digitizers are able to sample the input pulse at very high frequency, up to 5 GS/s, with high channel density, while the highest Flash ADC frequency is 4 GS/s with a quite low number of channels. If compared to a commercial digital oscilloscope, the waveform digitizer presents a list of differences which make it an advanced instrument for many applications:

- waveform recording with no dead-time due to conversion (Flash ADC digitizers)
- Independent channel self-triggering and event acquisition
- On-line digital pulse processing (DPP) algorithms
- Data reduction
- Multi-board synchronization for system scalability
- Communication interfaces with high bandwidth readout

The benefits of the digital approach are great stability and reproducibility, ability to reprogram and adjust the algorithms to the application, ability to preserve the information of the signal along the entire acquisition chain, flexibility, better correction of baseline fluctuation, pile-up, ballistic deficit, etc.. All in one board.

CAEN Digitizer block diagram:

- A motherboard which contains one FPGA for the readout interfaces and the services, and defines the form factor.
- One or more daughterboards which define the type of digitizer and contain the signal conditioning input stage, the ADCs, the FPGA for the data processing and the memories.
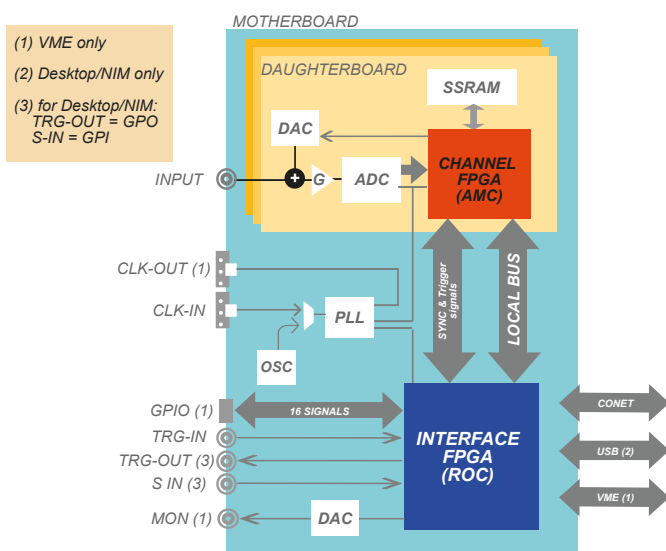
Firmware Upgrade

CAEN has made a big effort in dev

The user can install a DPP algorit methods that go beyond the simp

Firmware

Waveform Recording Firmware

Time windowed waveform recording
Dead-timeless acquisition
Multi-buffer memories
Multi-board synchronization

Software

CAEN Digitizer readout application

Digitizer Software for Signal Inspection and waveform recording

Features

ICH	**WV**	**TS**
TDC	QDC	CFD
PHA	PSD	ZS
D		

Feature Acronyms Legend

ICH (**Independent channels**): the trigger and acquire data inde can be corelated using a user (anti) coincidence logic criteri

TDC (**Time to Digital Converter**): stamp information from the fast digital discriminator filte resolution (sub-ns resolution

**PHA** (**Pulse Height Analysis**): pul exponential signals or comin sensitive preamplifier

DAW (**Dynamic Acquisition Wind** acquisition of a dynamically a number of ADC samples

...veloping algorithms for the Digital Pulse Processing (DPP).

...hm on the FPGA of the digitizer (firmware upgrade), run it on-line and implement new acquisition
...ple waveform recording.

725 / 730 Digitizer Family

CAEN Upgrader Software

Firmware Upgrade Tool
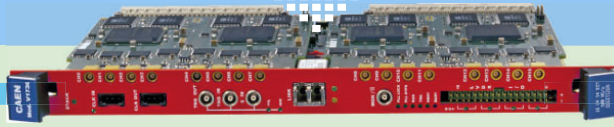
Pulse Height Analysis

Digitizer running DPP-PHA firmware becomes a digital replacement of Shaping Amplifier and Peak Sensing ADC (Multi-Channel Analyzer) by means of digital trapezoidal filters.

CoMPASS CAEN — Multiparametric DAQ Software for Physics Applications

MC² CAEN — Digital MCA Data Acquisition and Analysis Software

ICH	WV	TS
TDC	QDC	CFD
PHA	PSD	ZS
DAW		

Pulse Shape Discrimination

Digitizer running DPP-PSD firmware becomes a digital replacement of dual gate QDC, discriminator and gate generator.

CoMPASS CAEN — Multiparametric DAQ Software for Physics Applications

ICH	WV	TS
TDC	QDC	CFD
PHA	PSD	ZS
DAW		

Zero Length Encoding
New

Digitizer running DPP-ZLE firmware becomes able to transfer digitized waveforms in compressed mode thanks to an enhanced Zero Suppression algorithm.

ZLE⁺ CAEN — Software interface for DPP-ZLEplus management

ICH	WV	TS
TDC	QDC	CFD
PHA	PSD	ZS
DAW		

Dynamic Acquistion Window
New

Digitizer running DPP-DAW firmware allows the user to acquire data from each channel independently and to adapt the acquisition window to the real pulse duration (over-threshold).

DAW CAEN — Software interface for DPP-DAW management

ICH	WV	TS
TDC	QDC	CFD
PHA	PSD	ZS
DAW		

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WV (**Waveforms**): acquisition of a programmable number of ADC samples (raw waveforms)

QDC (**Charge to Digital Converter**): gated integrator (charge)

PSD (**Pulse Shape Discrimination**): particle discrimination via double gated integration

TS (**Timestamp**): trigger coarse time stamp with low resolution (10-20 ns)

CFD (**Constant Fraction Discriminator**): digital Constant Fraction Discriminator with programmable delay and fraction. Works in combination with TDC

ZS (**Zero Suppression**): acquisition of a programmable number of ADC samples with zero suppression

Technical Specifications

GENERAL

Form Factor
1-unit wide, 6U VME64/VME64X
1-unit wide NIM
154x50x164 mm^3 (WxHxD) Desktop

ANALOG INPUT

Channels
16/8 channels, single ended (VME)
8 channels, single ended (NIM, Desktop)

Impedance
50 Ω

Connector
MCX

Full Scale Range (FSR)
2 Vpp (0.5 Vpp software selectable)

Bandwidth
125 MHz

Offset
Programmable DAC for DC offset adjustment. Range: ±1 V @ 2 Vpp, ±0.25 V @ 0.5 Vpp

DIGITAL CONVERSION

Resolution
14 bits

Sampling rate
250 MS/s simultaneously on each channel

ADC CLOCK GENERATION

Clock source: internal/external
On-Board PLL provides ADC sampling clock generation from an internal (50 MHz loc. oscillator) or external reference (50 MHz or 62.5 MHz; other options on request) on front panel CLK-IN connector.

MEMORY

640 kS/ch or 5.12 MS/ch Multi-Event Buffer divisible into 1 ÷ 1024 buffers with independent read and write access. Programmable event size and pre- /post-trigger

TRIGGER

Trigger source
Self-trigger: channel over/under threshold for either Common or Individual (DPP firmware only) trigger generation
External-trigger: Common by TRG-IN or Individual by LVDS connectors (DPP firmware only)
Software-trigger: Common by software command

Trigger propagation
TRG-OUT (VME) / GPO (NIM, Desktop) digital output

Trigger Time Stamp
Waveform recording firmware/DPP-DAW/DPP-ZLE: 31-bit counter, 16ns resolution, 17 s range(*); 48-bit extension by firmware
DPP-PHA/PSD: 31-bit counter, 4 ns resolution, 8 s range; 47-bit extension by firmware; 10-bit and 4 ps fine time stamp by digital CFD; 64-bit extension by software

SYNCHRONIZATION

Clock propagation
Daisy chain (VME only) through CLK-IN/CLK-OUT connectors
One-to-many clock distribution from an external clock source
Clock Cable delay compensation

Acquisition Synchronization
Sync Start/Stop through digital I/O (S-IN, TRG-IN or GPI input, TRG-OUT or GPO output)
External Trigger Time Stamp reset

LVDS I/O (VME only)

16 general purpose LVDS I/Os controlled by FPGA
Busy, Data Ready, Memory Full, Individual Trg-Out and other functions can be programmed
An Input Pattern from the LVDS I/Os can be associated to each trigger as an event marker

ANALOG MONITOR (VME only)

12-bit/125 MHz DAC FPGA controlled output with four operating modes:
Trigger Majority / Test Pulses / Memory Occupancy / Voltage Level

COMMUNICATION INTERFACE

Optical Link
CAEN CONET proprietary protocol,up to 80 MB/s transfer rate
Daisy chainable: it is possible to connect up to 8/32 ADC modules to a single Optical Link Controller (Mod.A2818/A3818)

VME
VME 64X compliant
Data transfer mode: BLT32, MBLT64 (70 MB/s using CAEN Bridge), CBLT32/64, 2eVME, 2eSST (up to 200 MB/s)

POWER CONSUMPTIONS

Desktop: 2.5 A @ +12 V
NIM: 5 A @ +6 V, 300 mA @ -6 V

VME:	V1725	V1725x
	5.2 A @ +5 V	TBD
	750 mA @ +12 V	
	-12 V not used	

Ordering Options

Code	Description	Form Factor
WDT5725SXAAA	DT5725S - 8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE	Desktop
WDT5725SBXAA	DT5725SB - 8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE	Desktop
WN672S5XAAAA	N6725S - 8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE	NIM
WN6725SBXAAA	N6725SB - 8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE	NIM
WV1725SXAAAA	V1725S - 16 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE	6U-VME64
WV1725SBXAAA	V1725SB - 16 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE	6U-VME64
WV1725SCXAAA	V1725SC - 8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE	6U-VME64
WV1725SDXAAA	V1725SD - 8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE	6U-VME64
WVX1725SXAAA	VX1725S - 16 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE	6U-VME64X
WVX1725SBXAA	VX1725SB - 16 Ch. 14 bit 250 MS/s Digitizer: 5.12MSch, CE30, SE	6U-VME64X
WVX1725SCXAA	VX1725SC - 8 Ch. 14 bit 250 MS/s Digitizer: 640kS/c, CE30, SE	6U-VME64X
WVX1725SDXAA	VX1725SD - 8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE	6U-VME64X
WFWDPPTFAA25	DPP-PHA - Digital Pulse Processing for Pulse Height Analysis (16 ch x725)	6U-VME64 VME64X
WFWDPPTFAD25	DPP-PHA - Digital Pulse Processing for Pulse Height Analysis for (8ch x 725)	ALL
WFWDPPNGAA25	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (16 ch x725)	6U-VME64 VME64X
WFWDPPNGAD25	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (8ch x725)	ALL
WFWDPPTWAA25	DPP-DAW - Digital Pulse Processing with Dynamic Acquisition Windows (16ch x725)	6U-VME64 VME64X
WFWDPPTWAD25	DPP-DAW - Digital Pulse Processing with Dynamic Acquisition Windows (8ch x725)	ALL
WFWDPPZLAA25	DPP-ZLEplus - Digital Pulse Processing Zero Length Encoding for (16ch x725)	6U-VME64 VME64X
WFWDPPZLAD25	DPP-ZLEplus - Digital Pulse Processing Zero Length Encoding for (8ch x725)	ALL
WFWDPPS2501A	DPP-SUP - Super Licence for 16ch x 725 Digital Pulse Processing	6U-VME64 VME64X
WFWDPPS2501D	DPP-SUP - Super Licence for 8ch x 725 Digital Pulse Processing	ALL

Accessories

A2818
PCI CONET Controller

A3818
PCI Express CONET2 Controller

A654
MCX to LEMO Cable Adapter

A659
MCX to BNC Cable Adapter

A317
Clock Distribution Cable

A318
SE to Differential Clock Cable Adapter

AI2700
Optical Fiber Series

Cables for CONET Optical Link Networks

DT4700
Clock Generator and FAN-OUT

(*) Trigger Logic and Trigger Time Stamp counter operate at 125 MHz (i.e. 8 ns or 2 ADC clock cycles), while the counter value is read at a frequency of 62.5 MHz (i.e. 16 ns).