CAEN Electronic Instrumentation

740 Digitizer Family

64/32 Ch. 12-bit 62.5 MS/s Digitizer

APPLICATIONS

- Nuclear and Particle Physics
- Neutrino Physics
- Spectroscopic Imaging
- Homeland Security

FORM FACTOR

VME64 VME64X NIM DESKTOP

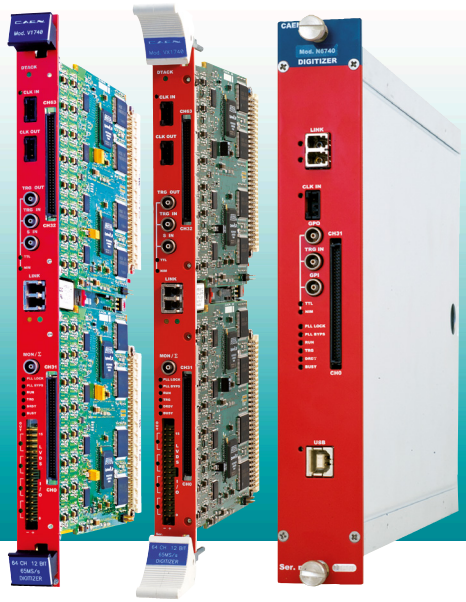
FUNCTIONS

ICH WV TS QDC

Very high channel density

APPLICATION NOTES

- AN6308
- GD2783
- GD2827



Overview

The 740 is a high channel density CAEN Waveform Digitizer family able to perform basic waveform recording and run online advanced algorithms (DPP) of charge integration. Both the elevate number of channels per board (32 for Desktop and NIM form factor, 64 for VME) and the DPP algorithm make the board a digital replacement of a traditional QDC. Data is read by a Flash ADC, 12-bit resolution and 62.5 MS/s sampling rate, which is well suited for mid-slow signals as the ones coming from inorganic scintillators coupled to PMTs, gaseous detectors and others. Sampling rate can be further reduced using the decimation feature. The acquisition can be channel independent and externally vetoed/gated. Multiple boards can be synchronized to build up complex systems.

In case of DPP mode, data can be saved in time-stamped list mode to support higher input rates and improving the throughput performances. The acquisition in DPP mode is fully controlled by the CoMPASS software (Coming Soon), which manages the algorithm parameters, builds the plots and saves the relevant energy and time spectra. In case of waveform recording mode, the user can take advantage of the CAENScope and WaveDump software to access and save the waveforms. Libraries and demo software in C and LabView are available for integration and customization of specific acquisition systems.

740 family comes in three form factors: VME (64 input channels), NIM (32 input channels) and Desktop (32 input channels). The communication to and from the board is provided through the following interfaces: USB (Desktop and NIM form factors), VMEbus (VME form factor), and Optical Link (all form factors).

Features

- 12-bit @ 62.5 MS/s
- Analog inputs on ERNI SMC connectors
- VME64/VME64X (64 ch.), NIM (32 ch.) and Desktop (32 ch.) modules
- 2 or 10 Vpp input dynamic range with programmable DC offset adjustment
- Sampling rate decimation factor (software selectable)
- Algorithms for Digital Pulse Processing (DPP)
- VME, USB and Optical Link communication interfaces
- Multi-board synchronization features
- Daisy chain capability
- Demo software tools, Control Software for waveform recording and DPP firmware, C and LabVIEW libraries

Firmware	Software	ICH	WV	TS	QDC
WAVEFORM RECORDING	WAVE DUMP CAEN		•	•	
DPP QDC	QDC CAEN / CoMPASS CAEN	•	•	•	•

DPP-QDC firmware is supported by x740D version only

Principle of Operation

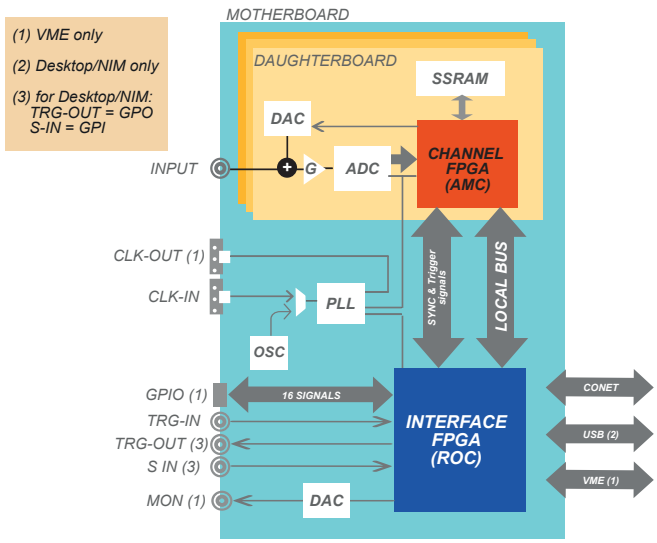
CAEN Waveform Digitizers are devices able to continuously acquire analog input signals, which are sampled by fast ADCs and stored into digital memories where they are avaiable for readout through different communication interfaces (USB, VMEBus, Optical Link). Depending on the FPGA firmware, the digitizer can work like an oscilloscope to acquire raw waveforms, or perform online processing to calculate parameters such as pulse height, charge, time stamp, pulse shape discrimination. In the latter case, the output data is a time-stamped list of parameters. Data reductions and zero suppression algorithms are also available. Digitization in CAEN digitizers is based on two main technics: **Flash ADC** and **Switched Capacitor Arrays**. Flash ADC are the fastest A/D converters, where the sampling and the analog-to-digital conversion are made practically at the same time. Flash ADC are so not affected by dead-time due to conversion. In the Switched Capacitor Arrays, the sampling and the A/D conversion take place at different times, thus introducing a dead-time. Despite of the dead-time, the Switched Capacitor Array Digitizers are able to sample the input pulse at very high frequency, up to 5 GS/s, with high channel density, while the highest Flash ADC frequency is 4 GS/s with a quite low number of channels. If compared to a commercial digital oscilloscope, the waveform digitizer presents a list of differences which make it an advanced instrument for many applications:

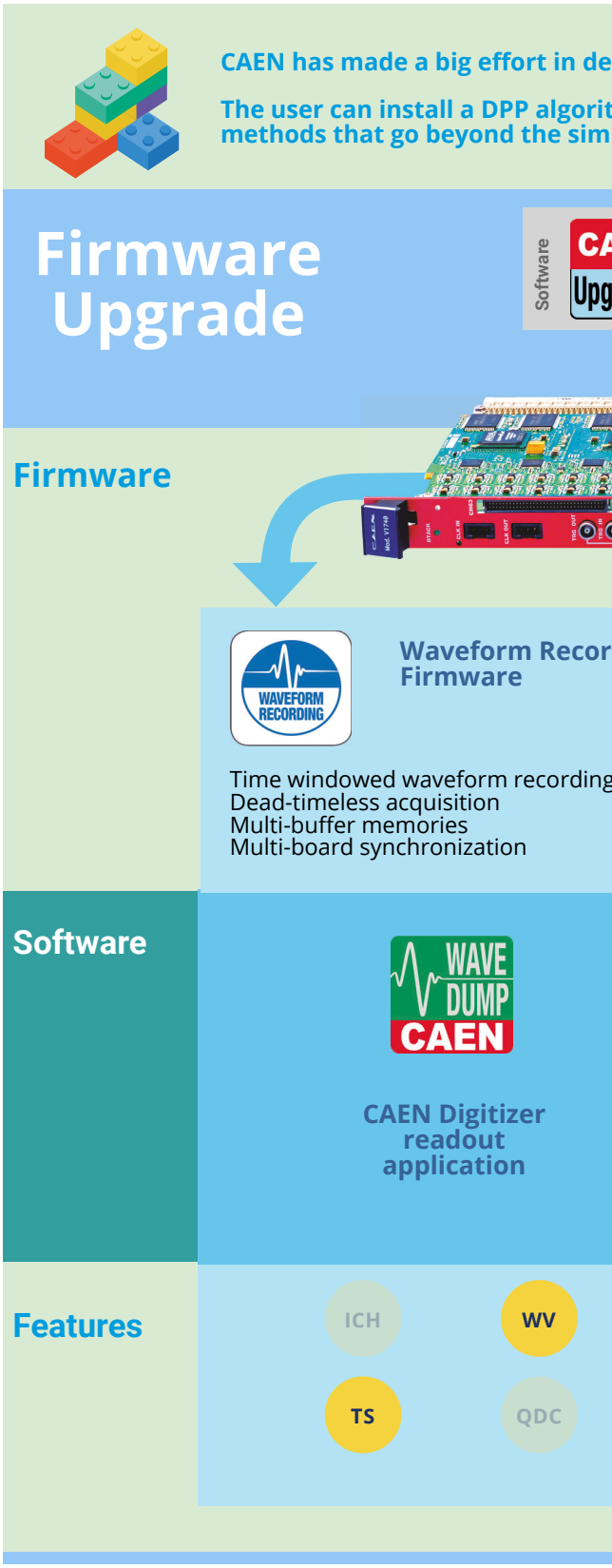
- Waveform recording with no dead-time due to conversion (Flash ADC digitizers)
- Independent channel self-triggering and event acquisition
- On-line digital pulse processing (DPP) algorithms
- Data reduction
- Multi-board synchronization for system scalability
- Communication interfaces with high bandwidth readout

The benefits of the digital approach are great stability and reproducibility, ability to reprogram and adjust the algorithms to the application, ability to preserve the information of the signal along the entire acquisition chain, flexibility, better correction of baseline fluctuation, pile-up, ballistic deficit, etc.. All in one board.

CAEN Digitizer block diagram:

- A motherboard which contains one FPGA for the readout interfaces and the services, and defines the form factor.





- One or more daughterboards which define the type of digitizer and contain the signal conditioning input stage, the ADCs, the FPGA for the data processing and the memories.

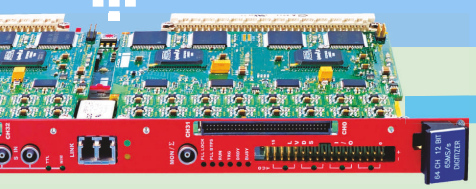
veloping algorithms for the Digital Pulse Processing (DPP).

thm on the FPGA of the digitizer (firmware upgrade), run it on-line and implement new acquisition
ple waveform recording.

740 Digitizer Family

AEN
rader

Firmware Upgrade Tool



ding

DPP QDC

Charge to Digital converter

Digital solution equivalent to Single Gate QDC + Dicriminator + gate Generator

CoMPASS CAEN

Multiparametric DAQ Software for Physics Applications

QDC CAEN

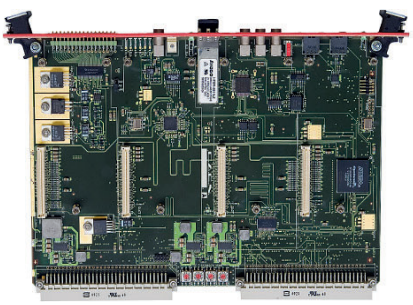
Demo Software for DPP-QDC Management

ICH WV TS QDC

DPP-QDC firmware is supported by x740D version only

Feature Acronyms Legenda

- **ICH** — (**Independent channels**): the channels can trigger and acquire data independently and can be corelated using a user-defined (anti) coincidence logic criteria
- **WV** — (**Waveforms**): acquisition of a programmable number of ADC samples (raw waveforms)
- **TS** — (**Timestamp**): trigger coarse time stamp with low resolution (10-20 ns)
- **QDC** — (**Charge to Digital Converter**): gated integrator (charge)



MOTHERBOARD

DAUGHTERBOARD

Technical Specifications

GENERAL

Form Factor

1-unit wide, 6U VME64/VME64X

1-unit wide NIM

154x50x164 mm^3 (WxHxD) Desktop

ANALOG INPUT

Channels

64 channels, single ended (VME); 32 channels, single endend (NIM)

32 channels, single endend (Desktop) or 16 channels by auxiliary on-board connectors

Impedance

50 Ω (2 Vpp), 1 kΩ (10 Vpp)

Connector

ERNI SMC Dual Row 68pin (VME, NIM and Desktop)

MCX auxiliary (Desktop)

Full Scale Range (FSR)

2 or 10 Vpp (by ordering code)

Bandwidth

30 MHz

Offset

Programmable DAC for DC offset adjustment per each 8-channel group

Range: ±1 V @ 2 Vpp, ±5 V @ 10 Vpp

DIGITAL CONVERSION

Resolution

12 bits

Sampling rate

62.5 MS/s simultaneously on each channel (65 MS/s using external clock)

16.1 MS/s minimum by hardware downsampling (*)

488 kS/s minimum by firmware decimation (8-step programmable)

ADC CLOCK GENERATION

Clock source: internal/external

On-Board PLL provides ADC sampling clock generation from an internal (50 MHz loc. oscillator) or external reference (50 MHz or 62.5 MHz; other options on request) on front panel CLK-IN connector.

MEMORY

192 kS/ch or 1.5 MS/ch Multi-Event Buffer divisible into 1 ÷ 1024 buffers with independent read and write access. Programmable event size and pre- /post-trigger

TRIGGER

Trigger sources

Self-trigger: channel over/under threshold for either Common or Individual (DPP firmware only) trigger generation

External-trigger: Common by TRG-IN or Individual by LVDS connectors (DPP firmware only)

Software-trigger: Common by software command

Trigger propagation

TRG-OUT (VME) / GPO (NIM and Desktop) digital output

Trigger Time Stamp

Waveform recording firmware: 31-bit counter, 16 ns resolution, 17 s range(**); 48-bit extension by firmware

DPP-QDC Firmware: 32-bit counter, 16 ns resolution, 68 s range; 48-bit extension by firmware; 64-bit extension by software

SYNCHRONIZATION

Clock propagation

Daisy chain (VME only) through CLK-IN/CLK-OUT connectors

One-to-many clock distribution from an external clock source

Clock Cable delay compensation

Acquisition Synchronization

Sync Start/Stop through digital I/O (S-IN, TRG-IN or GPI input, TRG-OUT or GPO output)

External Trigger Time Stamp reset

LVDS I/O (VME only)

16 general purpose LVDS I/Os controlled by FPGA

Busy, Data Ready, Memory full, Individual Trig-Out and other functions can be programmed An Input Pattern from the LVDS I/Os can be associated to each trigger as an event marker

ANALOG MONITOR (VME only)

12-bit/125 MHz DAC FPGA controlled output with four operating modes: Trigger Majority / Test Pulses / Memory Occupancy / Voltage Level

COMMUNICATION INTERFACE

Optical Link

CAEN CONET proprietary protocol, up to 80 MB/s transfer rate

Daisy chainable: it is possible to connect up to 8/32 ADC modules to a single Optical Link Controller (Mod. A2818/A3818)

USB (NIM and Desktop direct, VME via V1718 bridge)

USB 2.0 compliant (transfer rate up to 30 MB/s)

VME

Data transfer mode: BLT32, MBLT64 (70 MB/s using CAEN Bridge), CBLT32/64, 2eVME, 2eSST (up to 200 MB/s)

POWER CONSUMPTIONS

Desktop: 1.9 A @ 12 V (Typ.)

NIM: 3.9 A @ +6 V, 420 mA @ -6 V

VME: 4.5 / 4.9 A @ +5 V, 250 mA @ +12 V, -12 V not used

(**) Trigger Logic and Trigger Time Stamp counter operate at 125 MHz (i.e. 8 ns or 1/2 ADC clock cycles), while the counter value is read at a frequency of 62.5 MHz (i.e. 16 ns).

Ordering Options

Code	Description	Form Factor
WDT5740XAAAA	DT5740 - 32 Ch. 12 bit 62.5 MS/s Digitizer: 192kS/ch, EP3C16, SE	Desktop
WDT5740CXAAA	DT5740C - 10Vpp input 32 Ch. 12 bit 62.5MS/s Digitizer: 192kS/ch, EP3C16, SE	Desktop
WDT5740DXAAA	DT5740D - 32 Ch. 12 bit 62.5 MS/s Digitizer: 192kSch, EP3C40, SE	Desktop
WN6740DXAAAA	N6740D - 32 Ch. 12 bit 62.5 MS/s Digitizer: 192kS/ch, EP3C40, SE	NIM
WN6740XAAAAA	N6740 - 32 Ch. 12 bit 62.5 MS/s Digitizer: 192kS/ch, EP3C16, SE	NIM
WN6740CXAAAA	N6740C - 10Vpp input 32 Ch. 12 bit 62.5 MS/s Digitizer: 192kS/ch, EP3C16, SE	NIM
WV1740XAAAAA	V1740 - 64 Ch. 12 bit 62.5 MS/s Digitizer: 192kS/ch, EP3C16, SE	6U-VME64
WV1740AXAAAA	V1740A - 10Vpp input 64ch 12bit 62.5MS/s Digitizer: 1.5 MS/ch, EP3C16, SE	6U-VME64
WV1740BXAAAA	V1740B - 64 Ch. 12 bit 62.5 MS/s Digitizer: 1.5 MS/ch, EP3C16, SE	6U-VME64
WV1740CXAAAA	V1740C - 10Vpp input 64ch 12bit 62.5MS/s Digitizer: 192kS/ch, EP3C16, SE	6U-VME64
WV1740DXAAAA	V1740D - 64 Ch. 12 bit 62.5 MS/s Digitizer: 192kS/ch, EP3C40, SE	6U-VME64
WVX1740XAAAA	VX1740 - 64 Ch. 12 bit 62.5 MS/s Digitizer: 192kS/ch, EP3C16, SE	6U-VME64X
WVX1740AXAAA	VX1740A - 10Vpp input 64 Ch. 12 bit 62.5 MS/s Digitizer: 1.5 MS/ch, EP3C16, SE	6U-VME64X
WVX1740BXAAA	VX1740B - 64 Ch. 12 bit 62.5 MS/s Digitizer: 1.5 MS/ch, EP3C16, SE	6U-VME64X
WVX1740CXAAA	VX1740C - 10Vpp input 64 Ch. 12 bit 62.5 MS/s Digitizer: 192 KS/ch, EP3C16, SE	6U-VME64X
WVX1740DXAAA	VX1740D - 64 Ch. 12 bit 62.5 MS/s Digitizer: 192kSch, EP3C40, SE	6U-VME64X
WFWDPPQDCAAA	DPP-QDC- Digital Pulse Processing for Time Stamped Digital QDC (64ch x740D)	6U-VME64 VME64X
WFWDPPQDCAAA	DPP-QDC - Digital Pulse Processing for Time Stamped Digital QDC (32ch x740D)	Desktop NIM

Accessories

A746D
32 Channel Adapter for LEMO connector

A746B
64 Channel Adapter for LEMO connector

A746E
32ch Adapter for Lemo connector

A2818
PCI CONET Controller

A3818
PCI Express CONET2 Controller

A654
MCX to LEMO Cable Adapter

A659
MCX to BNC Cable Adapter

A317
Clock Distribution Cable

A318
SE to Differential Clock Cable Adapter

AI2700

Optical Fiber Series

Cables for CONET Optical Link Networks

DT4700

Clock Generator and FAN-OUT

(*) The minimum value may depend on the digitizer model, on the firmware or on the hardware downsampling mode (refer to AN6308 - Downsampling measurement with CAEN Digitizer 720/724/740/751 families)

CAEN
Tools for Discovery

CAEN SpA
Via Vetraia 11
55049 – Viareggio Italy
Tel +39.0584.388.398
Fax +39.0584.388.959
info@caen.it www.caen.it