Rev. 0 - 28/10/1993

C420

8 Channel Peak Sensing ADC

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User Manual
UM4950

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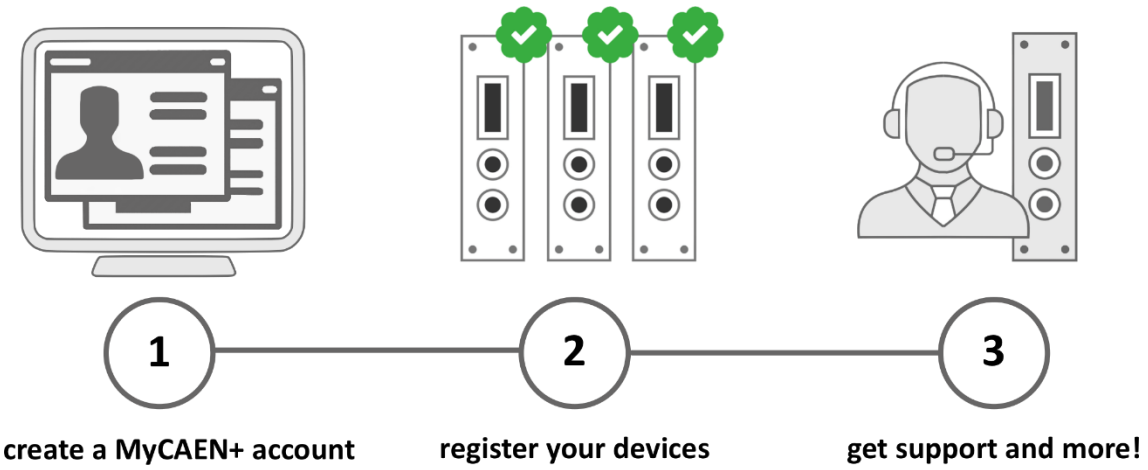

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Technical Information Manual

Revision n. 0

28 October 1993

MOD. C 420

8 CHANNEL PEAK-SENSING ADC

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1. DESCRIPTION

1.1. FUNCTIONAL DESCRIPTION

The CAEN Model C420 8 CHANNEL PEAK-SENSING ADC is a single width CAMAC module provided with 8 independent channels, able to detect and convert the peak value of the analog signals fed to the associated input connectors. The channels are divided in two groups (A and B) of 4 channels each, and each group has a single external trigger input.

The basic structure of the circuit is a multi-stretcher configuration [1] built around a high speed conversion module, i.e. the board can store up to eight simultaneous pulses that will be converted in a fast sequence controlled by a micro programmed logic (see fig. 1.1).

For each channel the associated linear gate stretcher detects the peak-value of the input signal during the programmed gate width (Rise Time Protection) and holds that value till the end of the conversion phase.

The linear gate stretcher can be triggered for each channel in three different ways:

- auto-trigger: the Rise Time Protection starts when the signal on the analog input is higher than a fixed pre-threshold of about 100 mV;

- external sampling trigger: the Rise Time Protection is triggered by an external pulse (NIM/TTL level);

- software sampling trigger: the Rise Time Protection is triggered by a software command that can be issued at the same time to all channels.

When the sampling mode by external pulse is enabled, a front panel switch selector allows the triggering of the two groups of channels (A and B) by the same pulse.

Each channel has a window discriminator whose thresholds, low and high, can be programmed via CAMAC. The conversion of a signal is possible if its peak is higher than the low threshold and lower than the high one, otherwise the stretcher is cleared to zero immediately at the end of the programmed Rise Time Protection.

The micro programmed logic sequencer continuously checks the status of the stretchers and when it finds one with a valid signal to be converted, i. e. at the end of the relevant programmed Rise Time Protection, sends this signal to the ADC via the analog multiplexer and enables the ADC block to start its conversion.

The conversion module is based on a ‘two steps subrange’ concept: an overall resolution of 12 bits is obtained using two 8 bit flash ADC’s. Moreover a sliding scale compensation technique [2] has been implemented to improve the differential Non-linearity.

The converted data are stored into eight 12 bit Data Registers (one per channel) that can be accessed by CAMAC. If the Data Register of a channel is busy, the signal on the stretcher will not be converted.
The unit can accept either square wave, gaussian or semigaussian positive pulses with rise time greater than 1 μs. It can also convert constant or very slow signals working in sampling mode, using either an external trigger, sent to the TRG connectors located on the front panel, or the software trigger to start the Rise Time Protection.

All the features of the unit are completely controllable via software for each channel through the CAMAC bus; amongst them there are the following:

- enabling and disabling of the acquisition for a given channel;
- linear gate stretcher trigger mode selection (auto trigger, external trigger, software trigger);
- Data Register reset: this can be accomplished automatically after a data read operation with a F2 CAMAC Function or by a CAMAC C, Z, F9 command;
- setting of the linear gate opening time (Rise Time Protection) from 1 μs to 15 μs;
- setting of the low and high thresholds of the window discriminator (8 bit data) between 0 V and 4 V;
- selection of the self-test mode: by means of an internal analog switch, each channel can be driven by a signal generated by an internal DAC; this makes possible a full functionality test of the board.

(This module is designed in collaboration with the INFN MILANO)

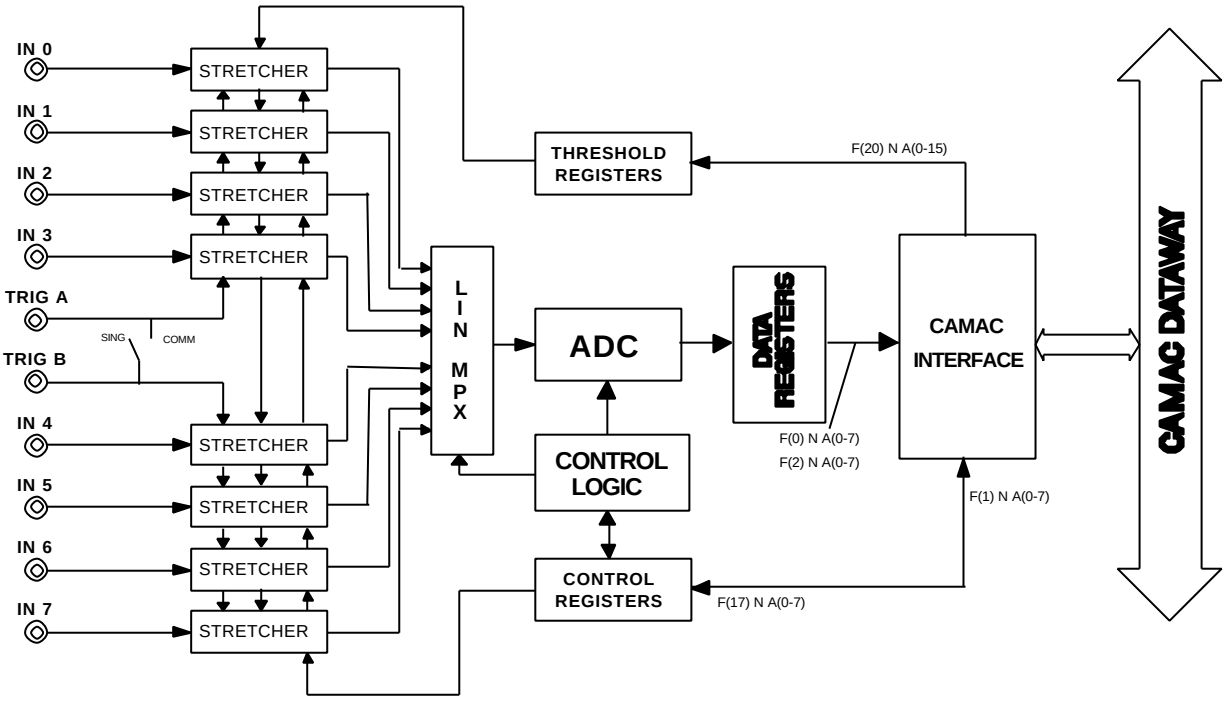

Fig. 1.1: C420 Block Diagram Errore. Il segnalibro non è definito.

2. SPECIFICATIONS

2.1. PACKAGING

1-unit wide CAMAC module.

2.2. EXTERNAL COMPONENTS

CONNECTORS:

- No 8, "IN" LEMO 00 type; input signals connectors from CH0 to CH7.

- No 2, "TRG" LEMO 00 type ; external trigger signals connectors (NIM/TTL level) TRG A and TRG B.

DISPLAYS:

- No 1, "DRDY" green LED; it lights up when the Data Register of at least one channel contains valid data.

SWITCHES:

- No 1, "TRG SEL" two position lever switch; if the sampling mode by external trigger is selected, it is possible to send the same trigger pulse to all channels (switch on COMM) or two independent pulses, one for each group of channels (A or B, switch on SING).

2.3. CHARACTERISTICS OF THE SIGNALS

INPUTS

- Input signals to be converted (CH0 to CH7): the module accepts both positive square wave pulses (min. width 1 μs) and positive gaussian or semigaussian shaped pulses with rise-time variable from 1 μs to 15 μs. 1 KΩ impedance, DC coupling.

- Triggers (TRG A and TRG B): can be NIM or TTL. NIM level, 50 Ω impedance. TTL level, 1 KΩ impedance. 30 ns minimum width.

2.4. PERFORMANCES AND TEST RESULTS

- Maximum Input Voltage: 4.0 V.

- Rise Time Protection: Selectable from 1 μs to 15 μs.

- Resolution: 12 Bits.

- Usable Range: 0.15 V to 3.75 V (90% of Full Range, due to sliding scale).

- Differential Non-linearity Error: ±1%

- Integral Non-linearity Error: ±2 LSB (±0.05%)

- Conversion Time per Channel: 1.2 μs

2.5. POWER REQUIREMENTS

+ 12 V	630 mA
- 12 V	600 mA
+ 6 V	1.7 A
- 6 V	150 mA

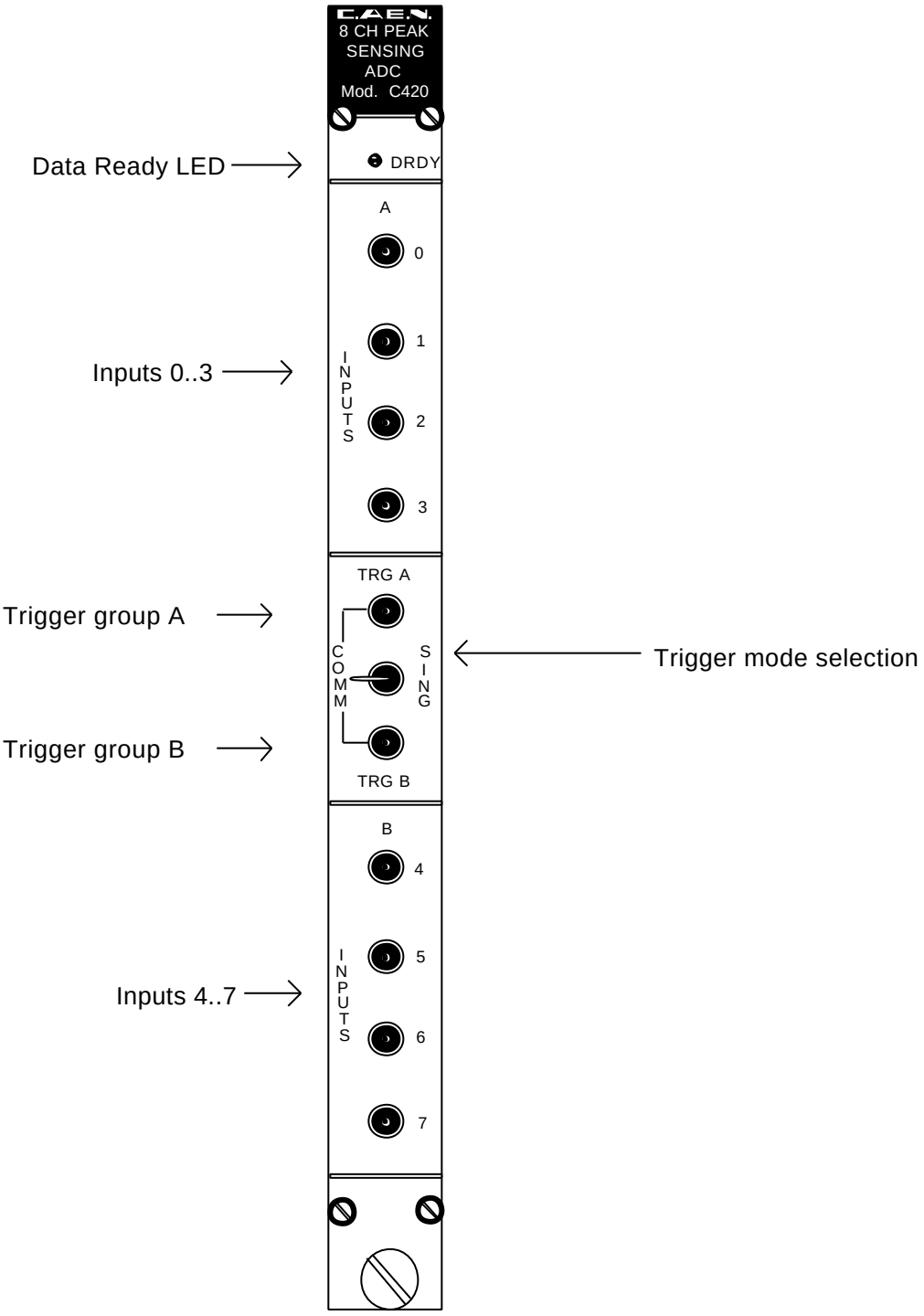

Fig. 2.1: C420 Front Panel Errore. Il segnalibro non è definito.

3. OPERATING MODES

3.1. GENERAL INFORMATION

The CAEN Model C420 8 CHANNEL PEAK-SENSING ADC allows the analog-to-digital conversion of up to 8 independent signal sources. The inputs can be either square wave, gaussian or semigaussian positive pulses.

The peak values fed in input are converted into a 12-bit word stored into a Data Register (one per channel) readable via CAMAC. As soon as one word has been stored the LAM signal (if enabled) becomes true, and the conversion values can be read performing the appropriate CAMAC functions sequence.

Each channel is provided with two 8-bit Threshold Registers (Low and High) for the window discriminator threshold setting, and an 8-bit Control Register for the enabling of the channel, the trigger mode selection and the Rise Time Protection setting. One bit of the Control Register in Read mode is the Data Ready bit (its value is 1 if the channel has valid data in the Data Register).

An additional register (one for all the channels) is the 8-bit Pattern of Data Ready Register: each bit of this register is the Data Ready bit.

The following paragraphs describe the various operations that can be done via CAMAC to perform an ADC conversion.

3.2. MOD. C420 RESET

It is possible to reset the C420 by performing a Z command. After this operation, the C420 is initialized; this causes the following:

- the Control Registers are cleared;
- the Data Registers are cleared;
- the LAM is cleared and disabled;
- the Pattern of Data Ready is cleared.
- the LED of Data Ready is cleared.

The reset operation doesn’t affect the content of the Threshold Registers.

3.3. SETTING THE THRESHOLDS

For each channel of the C420 there are two 8 bit Threshold Registers storing the window discriminator threshold values. The threshold values can be programmed in a range from 0 to 4.0 V.

In order to write Low and High Threshold for each channel, the User must perform two F(20) N CAMAC functions. The chosen value of the threshold is sent to the CAMAC WRITE Lines W<1..8> according to the subaddress value, e. g. F(20) N A (0) writes the Low Thr. for Ch. 0, F(20) N A (1) the High Thr. for Ch. 0, F(20) N A (2) the Low Thr. for Ch. 1, and so on.

3.4. ENABLE/DISABLE LAM GENERATION

It is possible to enable/disable the C420 LAM generation in the following ways:

ENABLE by performing an F(26) N Function;

DISABLE by performing an F(24) N Function;

by performing a Z Command.

At power-on the LAM generation is disabled.

3.5. SETTING THE CONTROL REGISTERS

Various features of the module are selectable via the Control Registers:

- enabling/disabling of the channel;
- setting of the trigger mode (auto trig., ext. trig., softw. trig);
- selection of self test mode;
- setting of the Rise Time Protection.

The structure of the Control Register of each channel is assigned as follows:

W1	Not used in Write Mode. Data Ready bit in Read Mode
W2	1: Enable Channel; 0: Disable Channel.
W3	Trigger Mode selection: see below.
W4	Trigger Mode selection: see below.
W5	Rise Time Protection: Least Significant Bit.
W6	Rise Time Protection.
W7	Rise Time Protection.
W8	Rise Time Protection: Most Significant Bit.

W4	W3	Mode
0	0	Auto Trigger
0	1	Ext. Trigger
1	0	Soft. Trigger
1	1	Test

To write into the Control Register for each channel, the User has to perform an F(17) N CAMAC Function, the subaddress indicating which channel is selected, e. g. F(17) N A(2) for channel 2, and the chosen value of the Control word is sent to the module via the CAMAC WRITE Lines W<1..8>.

The width of the Rise Time Protection can be set via the bits 5 to 8 of the Control Register in a range from 1 μs to 15 μs in steps of 1 μs. Binary values 0000 and 0001 correspond both to a 1 μs setting of the RTP.

An F(1) N A (0÷7) CAMAC Function performs a readout of the Control Register. In a Read Control Register operation, bit 1 of the Control Register (R1) is the Data Ready bit for the selected channel: its value is 1 if the channel has valid data in the Data Register.

According to the chosen configuration of the Control Register, four different acquisition modes are possible for each channel:

- Auto trigger;
- External trigger;
- Software trigger;
- Test mode.

In Auto trigger mode, the triggering of the linear gate stretcher is automatic at the fixed pre-threshold crossing. The module simply converts the peak value of a signal fed in input whenever it lies between the Low and High Threshold values. This is done only if the Data Register is empty.

In External trigger mode, the User needs to connect the trigger inputs to an external signal source. Triggering of the linear gate stretcher is given by the external trigger input.

In Software Trigger mode, the module waits for an F(25) N CAMAC Function to trigger the linear gate stretcher.

Also in Test mode the module waits for an F(25) N CAMAC Function, but the ADC converts automatically the High Threshold value of each enabled channel, and no external input is needed.

3.6. WAITING FOR THE END OF ACQUISITION

Once all settings have been performed, the module is ready for an acquisition. In order to check if an acquisition has occurred, several operations can be performed:

a) - Enable LAM with an F(26) N A(0) CAMAC Function before the beginning of the acquisition;
- Perform a Q test on an F(8) N CAMAC Function.

b) - Perform a Q test on an F(27) N CAMAC Function

c) - Perform a Q test on an F(1) N A(8) CAMAC Function.
If Q response is true, the Read Lines R<1..8> contain the Pattern of Data Ready, an 8 bit register whose bits are the Data Ready bits of each channel, i. e. R1 is the Data Ready bit of channel 0, R8 the Data Ready bit of channel 7.

d) - Perform a test on the first bit (R1) of the Control Register with an F(1) N A(0÷7) CAMAC Function. For each channel, this is the Data Ready bit of the selected channel.

Operating modes a) and b) are not selective of the channel that has acquired, while modes c) and d) are selective, i. e. the User can decide to acquire only a channel that contains valid data. For modes a), b) and c) the Q response is the logical OR of the Data Ready bits of all channels.

3.7. READING THE DATA

Once an acquisition has terminated, the User can read out the converted values in the following ways:

a) by performing an F(0) N A(i) CAMAC Function for the i-th channel. This operation reads the 12 bit Data Register of the i-th channel.

b) by performing an F(2) N A(i) CAMAC Function for the i-th channel. This operation reads and clears the Data Register and resets the Data Ready bit of the i-th channel.

After a readout of the Data Register with an F(2) N CAMAC Function, the channel is ready for a new acquisition.

If, on the contrary, an F(0) N Function has been performed, the User must first clear the Data Register with an F(2) N Function. The module is then ready to acquire with the same settings. If desired, the User can change the settings with a reset of the module, using a Z operation, and after that an F(17) N operation to write on the Control Register. The module is ready to acquire with the new settings.

4. CAMAC FUNCTIONS

The standard CAMAC Functions listed in Table 4.1 allow the user to perform the required control and readout operations on the C420 module.

X response is generated for each valid function.

Q response is generated for each valid function unless otherwise specified.

Table 4.1 Mod. C420 CAMAC Functions Errore. Il segnalibro non è definito.

F(0) N A(0¸7)	Reads the Data Register on R1..R12.
F(1) N A(0¸7)	Reads the Control Register on R1..R8.
F(1) N A(8)	Reads pattern of Data Ready on R1..R8.
F(2) N A(0¸7)	Reads the Data Register on R1..R12 and clears channel.
F(8) N *	Q response if LAM is enabled and Or-Data-Ready of all channels is true.
F(9) N *	Clears the module.
F(17) N A(0¸7)	Writes the Control Register on W1..W8.
F(20) N A(0¸15)	Writes Low and High Threshold on W1..W8. (A(0)=LowThCh0; A(1)=HighThCh0;....A(14)=LowThCh7; A(15)=HighThCh7)
F(24) N *	Disables LAM.
F(25) N *	Software Trigger.
F(26) N *	Enables LAM.
F(27) N *	Tests status. Q response if Or-Data-Ready of all channels is true.
C	Same as F(9) N.
Z	Resets the module

* Any value of the address lines is valid.

4.1. F(0) N A(0¸7) FUNCTION (Read Data Register)

This CAMAC Function reads the 12 bit Data Register and doesn't clear the channel contents; subaddresses 0 through 7 select the different channels (0 through 7). For each channel the Data Register contains the converted values of the detected peak.

4.2. F(1) N A(0¸7) FUNCTION (Read Control Register)

This CAMAC Function reads the 8 bit Control Register; subaddresses 0 through 7 select the different channels (0 through 7). See paragraph 4.7 for the contents of the Control Register (F(17) N A(0-7) FUNCTION).
The first bit of the Control Register in Read Mode is the Data Ready bit for the selected channel, i. e. it is true when the Data Register contains valid data.

4.3. F(1) N A(8) FUNCTION (Read Pattern of Data Ready)

This CAMAC Function reads the Pattern of Data Ready, an 8 bit register whose bits are the Data Ready bits of each channel, i. e. R1 is the Data Ready bit for channel 0, R8 the Data Ready bit for channel 7. The Q response is the logical OR of the Data Ready bits of all channels. If Q response is true, the Read Lines R<1..8> contain the Pattern of Data Ready

4.4. F(2) N A(0 ¸ 7) FUNCTION (Read and Clear Channel)

This CAMAC Function reads the 12 bit Data Register and clears the channel contents; subaddresses 0 through 7 select the different channels (0 through 7). For each channel the Data Register contains the converted values of the detected peak.
This CAMAC Function causes the following:

- the Data Register of the channel is cleared;
- the Data Ready bit of the channel is cleared.
- the LED of Data Ready is cleared.

4.5. F(8) N FUNCTION (Test Or-Data Ready)

This CAMAC Function performs a test of the LAM line. The Q response is the logical OR of the Data Ready bits of all channels only if the LAM has been enabled.

4.6. F(9) N, C (Clear Module)

This CAMAC Function clears the module; this causes the following:

- the Data Register is cleared;
- the LAM is cleared;
- the Pattern of Data Ready is cleared.
- the LED of Data Ready is cleared.

4.7. Z (Reset Module)

This CAMAC Function resets the module; this causes the following:

- the Control Register is cleared
- the Data Register is cleared;
- the LAM is cleared and disabled;
- the Pattern of Data Ready is cleared.
- the LED of Data Ready is cleared.

4.8. F(17) N A(0¸7) FUNCTION (Write Control Register)

This CAMAC Function writes on the 8 bit Control Register; subaddresses 0 through 7 select the different channels (0 through 7). For each channel the Control Register sets the enabling of the channel (W2), the Trigger mode selection (W3, W4) and the Rise Time Protection (W5 through W8) according to the following tables:

W1	Not used in Write Mode. Data Ready bit in Read Mode
W2	1: Enable Channel; 0: Disable Channel.
W3	Trigger Mode selection: see below.
W4	Trigger Mode selection: see below.
W5	Rise Time Protection: Least Significant Bit.
W6	Rise Time Protection.
W7	Rise Time Protection.
W8	Rise Time Protection: Most Significant Bit.

W4	W3	Mode
0	0	Auto Trigger
0	1	Ext. Trigger
1	0	Soft. Trigger
1	1	Test

The first bit of the Control Register is not used in Write Mode.

4.9. F(20) N A(0¸15) FUNCTION (Write Low & High Threshold)

This CAMAC function writes Low and High Threshold for each channel; the chosen value of the threshold is sent to the CAMAC WRITE Lines W<1..8> according to the subaddress value, e. g. F(20) N A (0) writes the Low Thr. for Ch. 0, F(20) N A (1) the High Thr. for Ch. 0, F(20) N A (2) the Low Thr. for Ch. 1, and so on.

4.10. F(24) N FUNCTION (Disable LAM Generation)

This CAMAC function disables the LAM generation.

4.11. F(25) N FUNCTION (Software Trigger)

This CAMAC function sends a trigger to the linear gate stretcher. It must be performed if the chosen operating modes are:

- Software trigger;

- Test mode.

4.12. F(26) N FUNCTION (Enable LAM Generation)

This CAMAC function enables the LAM generation; it must be performed after a Reset operation (Z) because this operation disables the LAM generation.

4.13. F(27) N FUNCTION (Test Status)

This CAMAC Function performs a test of the status of the module. The Q response is the logical OR of the Data Ready bits of all channels.

5. EXAMPLE OF A SIMPLE ACQUISITION

CAUTION: *turn OFF the CAMAC crate before inserting or removing the module.*

1. Insert the C420 module into the CAMAC crate, then turn the crate itself ON.

2. Perform a Z CAMAC command: the LAM signal is set to false condition.

3. Connect the signal sources to the C420 input connectors (CH0÷CH7).

4. Connect the "TRG" connectors to a signal source (NIM/TTL level) if sampling mode by external trigger is requested.

5. Perform an F(20) N A (0÷15) CAMAC function to write Low and High Threshold for each channel via the W1..W8 lines; e. g. F(20) N A (0): Low Thr. Ch. 0, F(20) N A (1): High Thr. Ch. 0, F(20) N A (2): Low Thr. Ch. 1, and so on.

6. Perform an F(26) N CAMAC Function to enable LAM generation.

7. Perform an F(17) N A (0÷7) CAMAC Function to write on the Control Register for each channel via the W1..W8 lines, e. g. F(17) N A(5) for channel 5. The structure of the Control Register is described in 3.5.

   If desired, the User can read back the content of the Control Register as a check with an F(1) N A (0¸7).

8. Activate the signals to be converted (and the TRG signal if external trigger is chosen).

9. Perform an F(8) N A(0) CAMAC function until Q = 1 (Q response if Or-Data Ready is true, i. e. if any channel has a valid datum).

10. Perform an F(2) N A(0÷7) CAMAC function to read and clear the Data Register of the chosen channel (0 through 7) on the R1..R12 read lines.

    If all the readings are performed with an F(2) N, the module is ready for a new acquisition (go to step 8).

6. REFERENCES

[1] G. Bassato, et al: A Four Channel ADC on a VME Board, IEEE Trans. Nucl Sci. 37 (2185), 1990.

[2] C. Cottini, E. Gatti, V. Svelto: A Sliding Scale Analog to Digital Converter for Pulse Height Analysis, Proc. Int. Symp. Nucl., Paris, Nov. 1963.

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