CAEN
Tools for Discovery

Electronic Instrumentation

User Manual UM7155

741 Family

Peak Sensing Firmware Registers

Rev. 1 - October 10th, 2024

Purpose of this Manual

The User Manual contains the full description of the 741 Peak Sensing firmware registers for 741 digitizer family. The description is compliant with the firmware revision **4.18_1.00**. For future release compatibility, check in the firmware history files.

Change Document Record

Date	Revision	Changes
June 16th, 2020	00	First release.

Symbols, abbreviated terms and notation

ADC	Analog-to-Digital Converter
AMC	ADC & Memory Controller
DAC	Digital-to-Analog Converter
DC	Direct Current
LVDS	Low-Voltage Differential Signal
ROC	ReadOut Controller
USB	Universal Serial Bus

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1 Registers and Data Format

All registers described in the User Manual are 32-bit wide. In case of VME access, **A24** and **A32** addressing mode can be used.

Reset and Clear

The module's registers can be set back to their default values on software reset command by writing in the Software Reset register or by system reset from backplane, in case of VME boards. In particular, the registers or buffers listed below

- Event Readout Buffer
- Buffer Occupancy
- Event Stored
- Event Size

are also be set back to their default values (registers) or emptied (buffers) by a clear issued:

- automatically by the firmware at the start of each run;
- on software command by writing in the Software Clear register

Register Address Map

The table below reports the complete list of registers that can be accessed by the user. The register names in the first column can be clicked to be redirected to the relevant register description. The register address is reported on the second column as a hex value. The third column indicates the allowed register access mode, where:

R	**Read only**. The register can be accessed in read only mode.
W	**Write only**. The register can be accessed in write only mode.
R/W	**Read and write**. The register can be accessed both in read and write mode.

According to the attribute reported in the fourth column, the following choices are available:

G **Group register**. In case of 741 peak sensing ADC, some registers manage **groups** of channels. Group registers have M instances, where M is the total number of groups. Write access can be performed in single group mode (one group at a time) or broadcast (simultaneous write access to all groups). Read command must be in single group mode.
Single group access can be performed at address 0x1nXY, where n identifies the n^{th} group, while broadcast write can be performed at the address 0x80XY. For example:

- access to address 0x1120 to read/write register 0x1n20 for group 1 of the board. In case of 741 board, group 1 corresponds to channels from 16 to 31 (16 channels per group). The same value is applied to all channels in the same group.
- to write the same value for all groups in the board, access to 0x8020 (broadcast write). To read the corresponding value, access to the individual address 0x1n20.

C **Common register**. Register with this attribute has a single instance, therefore read and write access can be performed at address 0x80XY only.

Register Name	Address	Mode	Attribute
Event Readout Buffer	0x0000 - 0x0FFC	R	C
Amplitude Zero Suppression Threshold	0x1n24, 0x8024	R/W	G
Group n Status	0x1n88	R	G
AMC Firmware Revision	0x1n8C	R	G
Channel Enable Mask of Group n	0x1nA8, 0x80A8	R/W	G
Gate width	0x8020	R/W	C
Peak Sensing Control	0x80E0	R/W	C
Acquisition Control	0x8100	R/W	C
Acquisition Status	0x8104	R	C
Software Trigger	0x8108	W	C
LVDS I/O Data	0x8118	R/W	C
Front Panel I/O Control	0x811C	R/W	C
ROC FPGA Firmware Revision	0x8124	R	C
Event Stored	0x812C	R	C
Software Clock Sync	0x813C	W	C
Board Info	0x8140	R	C
Event Size	0x814C	R	C
Fan Speed Control	0x8168	R/W	C
Memory Buffer Almost Full Level	0x816C	R/W	C
Run/Start/Stop Delay	0x8170	R/W	C
Board Failure Status	0x8178	R	C
Front Panel LVDS I/O New Features	0x81A0	R/W	C
Readout Status	0xEF04	R	C
Board ID	0xEF08	R/W	C
MCST Base Address and Control	0xEF0C	R/W	C
Relocation Address	0xEF10	R/W	C
Scratch	0xEF20	R/W	C
Software Reset	0xEF24	W	C
Software Clear	0xEF28	W	C
Configuration Reload	0xEF34	W	C
Configuration ROM Checksum	0xF000	R	C
Configuration ROM Checksum Length BYTE 2	0xF004	R	C
Configuration ROM Checksum Length BYTE 1	0xF008	R	C
Configuration ROM Checksum Length BYTE 0	0xF00C	R	C
Configuration ROM Constant BYTE 2	0xF010	R	C
Configuration ROM Constant BYTE 1	0xF014	R	C
Configuration ROM Constant BYTE 0	0xF018	R	C
Configuration ROM C Code	0xF01C	R	C
Configuration ROM R Code	0xF020	R	C
Configuration ROM IEEE OUI BYTE 2	0xF024	R	C
Configuration ROM IEEE OUI BYTE 1	0xF028	R	C
Configuration ROM IEEE OUI BYTE 0	0xF02C	R	C
Configuration ROM Board Version	0xF030	R	C
Configuration ROM Board Form Factor	0xF034	R	C
Configuration ROM Board ID BYTE 1	0xF038	R	C
Configuration ROM Board ID BYTE 0	0xF03C	R	C
Configuration ROM PCB Revision BYTE 3	0xF040	R	C
Configuration ROM PCB Revision BYTE 2	0xF044	R	C
Configuration ROM PCB Revision BYTE 1	0xF048	R	C
Configuration ROM PCB Revision BYTE 0	0xF04C	R	C
Configuration ROM FLASH Type	0xF050	R	C
Configuration ROM Board Serial Number BYTE 1	0xF080	R	C
Configuration ROM Board Serial Number BYTE 0	0xF084	R	C
Configuration ROM VCXO Type	0xF088	R	C

Event Readout Buffer

This is the addressing space for the event readout. The event payload is made of 32-bit words; its structure is defined in the User Manual of the board.

Address	0x0000 - 0x0FFC
Mode	R
Attribute	C

Bit	Description
[31:0]	32-bit word of the event.

Amplitude Zero Suppression Threshold

When in zero-suppression mode (bit[17]=1 of register 0x80E0), these registers allow the user to set the channel threshold below which the measured signal amplitude is not included in the data packet. If this is the case, the related bit in the payload channel mask is set to 0.
NOTE: This register sets the same value for groups of 8 channels, where n is the group index.

Address	0x1n24, 0x8024
Mode	R/W
Attribute	G

Bit	Description
[14:0]	Threshold value. Important Note: - If [2:0] is set equal to 0 in the 0x80E0 register, [10:0] bits are dedicated to set threshold value and [14:11] bits are reserved. - If [2:0] is set equal to 1 in the 0x80E0 register, [11:0] bits are dedicated to set threshold value and [14:12] bits are reserved. - If [2:0] is set equal to 2 in the 0x80E0 register, [12:0] bits are dedicated to set threshold value and [14:13] bits are reserved. - If [2:0] is set equal to 3 in the 0x80E0 register, [13:0] bits are dedicated to set threshold value and [14] bit is reserved.
[31:15]	Reserved.

Group n Status

This register contains the status information common to all the channels of group n.

Address	0x1n88
Mode	R
Attribute	G

Bit	Description
[0]	Memory Full.
[1]	Memory Empty.
[2]	If 1, the SPI bus is busy.
[31:3]	Reserved.

AMC Firmware Revision

Returns the Peak Sensing firmware revision (mezzanine level).
To control the mother board firmware revision see register 0x8124.
For example: if the register value is 0xC3218303:
- Firmware Code and Firmware Revision are 131.3;
- Build Day is 21;
- Build Month is March;
- Build Year is 2012.

NOTE: since 2016 the build year started again from 0.

Address	0x1n8C
Mode	R
Attribute	G

Bit	Description
[7:0]	Firmware revision number
[15:8]	Peak Sensing Firmware code equal to 0x20
[19:16]	Build Day (lower digit)
[23:20]	Build Day (upper digit)
[27:24]	Build Month. For example: 3 means March, 12 is December.
[31:28]	Build Year. For example: 0 means 2000, 12 means 2012. NOTE: since 2016 the build year started again from 0.

Channel Enable Mask of Group n

Enable/disable selected channels of group n.
Note: this register must not be accessed while the acquisition is running.

Address	0x1nA8, 0x80A8
Mode	R/W
Attribute	G

Bit	Description
[15:0]	Bit m enables/disables channel m of group n. Options are: 0: disabled; 1: enabled.
[31:16]	Reserved.

Gate width

This register defines the gate width when enabled through register 0x80E0.
WARNING: this register must not be accessed while acquisition is running.

Address	0x8020
Mode	R/W
Attribute	C

Bit	Description
[31:0]	Number of samples of the gate width, where one sample corresponds to 16 ns. Minimum value is 1.

Peak Sensing Control

Management of the Peak Sensing algorithm features

Address	0x80E0
Mode	R/W
Attribute	C

Bit	Description
[2:0]	Spectrum channels: defines the maximum number of channels in the spectrum. Options are: 0 = 16384; 1 = 8192 ; 2 = 4096; 3 = 2048; 4 = 1024.
[3]	Reserved.
[4]	Gate witdh. Options are: 0 = gate width set by register 0x8020. 1 = gate width equal to the external gate duration.
[15:5]	Reserved.
[16]	Sliding scale. Options are: 0 = disabled; 1 = enabled.
[17]	Amplitude Zero Suppression. Options are: 0 = disabled; 1 = enabled. Threshold setting is defined via 0x1n24 register.
[18]	Signal Polarity. Options are: 0 = negative signal; 1 = positive signal.
[19]	Input Range. Options are: 0 = 8 V; 1 = 4 V. Note: when the 4V option is selected, the high-resolution channel mode (bit [2:0]=4) is not available.
[30:20]	Reserved.
[31]	Reserved. Must be 0.

Acquisition Control

This register manages the acquisition settings.

Address	0x8100
Mode	R/W
Attribute	C

Bit	Description
[1:0]	Start/Stop Mode Selection (default value is 00). Options are: 00 = SW CONTROLLED. Start/stop of the run takes place on software command by setting/resetting bit[2] of this register. Other options are reserved.
[2]	Acquisition Start/Stop. Options are: 0 = Acquisition STOP; 1 = Acquisition RUN.
[3]	Reserved.
[5:4]	Reserved
[6]	PLL Reference Clock Source (Desktop/NIM only). Default value is 0. Options are: 0 = internal oscillator (50 MHz); 1 = external clock from front panel CLK-IN connector. NOTE: this bit is reserved in case of VME boards.
[7]	Reserved.
[8]	LVDS I/O Busy-In Enable (VME only). Default value is 0. This bit must be enabled to let the board accept the Busy signal as input on the LVDS I/Os. Options are: 0 = disabled; 1 = enabled. NOTE: this bit is supported only by VME boards and meaningful only if the LVDS new features are enabled (bit[8]=1 of register 0x811C), the LVDS I/O mode is set to nBusy/nVeto (see register 0x81A0), and the LVDS I/Os are set as inputs (see register 0x811C).
[9]	LVDS I/O Veto Enable (VME only). Default value is 0. The LVDS I/Os can be programmed to accept a Veto signal as input, or to transfer it as output. Options are: 0 = disabled (default); 1 = enabled. NOTE: this bit is supported only by VME boards and meaningful only if the LVDS new features are enabled (bit[8]=1 of register 0x811C). Register 0x81A0 should also be configured for nBusy/nVeto.
[12:10]	Reserved.
[13]	Must be 1 to identify the Peak Sensing firmware.
[31:14]	Reserved.

Acquisition Status

This register monitors a set of conditions related to the acquisition status.

Address	0x8104
Mode	R
Attribute	C

Bit	Description
[1:0]	Reserved.
[2]	Acquisition Status. It reflects the status of the acquisition and drivers the front panel 'RUN' LED. Options are: 0 = acquisition is stopped ('RUN' is off); 1 = acquisition is running ('RUN' lits).
[3]	Event Ready. Indicates if any events are available for readout. Options are: 0 = no event is available for readout; 1 = at least one event is available for readout. NOTE: the status of this bit must be considered when managing the readout from the digitizer.
[4]	Event Full. Indicates if the board memory has reached the FULL condition (i.e. maximum number of storable events). Options are: 0 = the board is not FULL; 1 = the board is FULL.
[5]	Clock Source. Indicates the clock source status. Options are: 0 = internal (PLL uses the internal 50 MHz oscillator as reference); 1 = external (PLL uses the external clock on CLK-IN connector as reference).
[6]	Reserved.
[7]	PLL Unlock Detect. This bit flags a PLL unlock condition. Options are: 0 = PLL has had an unlock condition since the last register read access; 1 = PLL has not had any unlock condition since the last register read access. NOTE: flag can be restored to 1 via read access to register 0xEF04.
[8]	Board Ready. This flag indicates if the board is ready for acquisition (PLL and ADCs are correctly synchronized). Options are: 0 = board is not ready to start the acquisition; 1 = board is ready to start the acquisition. NOTE: this bit should be checked after software reset to ensure that the board will enter immediately in run mode after the RUN mode setting; otherwise, a latency between RUN mode setting and Acquisition start might occur.
[14:9]	Reserved.
[15]	REJ Status. Reads the logical level on REJ front panel connector.
[16]	GATE Status. Reads the logical level on GATE front panel connector.
[31:17]	Reserved.

Software Trigger

Writing this register causes a software trigger generation which is propagated to all the enabled channels of the board.

Address	0x8108
Mode	W
Attribute	C

Bit	Description
[31:0]	Write whatever value to generate a software trigger.

LVDS I/O Data

This register allows to read out the logic level of the LVDS I/Os if the LVDS pins are configured as outputs, and to set the logic level of the LVDS I/Os if the pins are configured as inputs.
NOTE: this register is supported by VME boards only.

Address	0x8118
Mode	R/W
Attribute	C

Bit	Description
[15:0]	LVDS I/O Data (VME boards only). It is the logic level of the corresponding nth LVDS I/O to read out or write, according to its direction (0x811C, bit[5:2]). A write operation sets the corresponding pin logic state if configured as output, while a read operation returns the logic state of the corresponding pin if configured as input. In case of Old LVDS I/O Features (0x811C, bit[8] = 0), the general purpose I/O option must be set (0x811C, bit[7:6] = 00). In case of New LVDS I/O Features (0x811C, bit[8] = 1), REGISTER mode must be set (0000 option in the 0x81A0 register).
[31:16]	Reserved.

Front Panel I/O Control

This register manages the front panel I/O connectors. Default value is 0x000000.

Address	0x811C
Mode	R/W
Attribute	C

Bit	Description
[1]	Reserved.
[2]	LVDS I/O [3:0] Direction (VME boards only). Sets the direction of the signals on the first 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. NOTE: this bit is reserved in case of DT and NIM boards.
[3]	LVDS I/O [7:4] Direction (VME boards only). Sets the direction of the second 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. NOTE: this bit is reserved in case of DT and NIM boards.
[4]	LVDS I/O [11:8] Direction (VME boards only). Sets the direction of the third 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. NOTE: this bit is reserved in case of DT and NIM boards.
[5]	LVDS I/O [15:12] Direction (VME boards only). Sets the direction of the fourth 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. NOTE: this bit is reserved in case of DT and NIM boards.
[7:6]	LVDS I/O Signal Configuration (VME boards only). Valid for old LVDS I/O features only (0x811C, bit[8] = 0). Options are: 00 = general purpose I/Os: LVDS I/Os work as register; I/O direction is configured through bit[5:2]; the logic level is read out or set in the 0x8118 register. 01 = programmed I/Os: direction and function of the LVDS signals are fixed (see the tabled signal pinout in the digitizer User Manual). 10 = pattern mode: LVDS signals are inputs and their value is written into the header PATTERN field of the event (see the digitizer User Manual); 11 = reserved. NOTE: these bits are reserved in case of DT and NIM boards.
[8]	LVDS I/O New Features Selection (VME boards only). Options are: 0 = LVDS old features; 1 = LVDS new features. The new features options can be configured through register 0x81A0. Please, refer to the User Manual for all details. NOTE: LVDS I/O New Features option is valid from motherboard firmware revision 3.8 on. NOTE: this bit is reserved in case of DT and NIM boards.
[31:9]	Reserved.

ROC FPGA Firmware Revision

This register contains the motherboard FPGA (ROC) firmware revision information.
The complete format is:
Firmware Revision = X.Y (16 lower bits)
Firmware Revision Date = Y/M/DD (16 higher bits)
EXAMPLE 1: revision 3.08, November 12th, 2007 is 0x7B120308.
EXAMPLE 2: revision 4.09, March 7th, 2016 is 0x03070409.
NOTE: the nibble code for the year makes this information to roll over each 16 years.

Address	0x8124
Mode	R
Attribute	C

Bit	Description
[7:0]	ROC Firmware Minor Revision Number (Y).
[15:8]	ROC Firmware Major Revision Number (X).
[31:16]	ROC Firmware Revision Date (Y/M/DD).

Event Stored

This register contains the number of events currently stored in the Output Buffer.
NOTE: the value of this register cannot exceed the maximum number of available buffers according to the register address 0x800C.

Address	0x812C
Mode	R
Attribute	C

Bit	Description
[31:0]	Number of the current events stored in the Output Buffer.

Software Clock Sync

At power-on, a Sync command is issued by the firmware to the ADCs to synchronize all of them to the clock of the board. In the standard operating, this command is not required to be repeated by the user.
A write access to this register (any value) forces the PLL to re-align all the clock outputs with the reference clock.
EXAMPLE: in case of Daisy chain clock distribution among VME boards, during the initialization and configuration, the reference clocks along the Daisy chain can be unstable and a temporary loss of lock may occur in the PLLs; although the lock is automatically recovered once the reference clocks return stable, it is not guaranteed that the phase shift returns to a known state. This command allows the board to restore the correct phase shift between the CLK-IN and the internal clocks.
NOTE: this register is supported by VME boards only.
NOTE: the command must be issued starting from the first to the last board in the clock chain.

Address	0x813C
Mode	W
Attribute	C

Bit	Description
[31:0]	Write whatever value to generate a Sync command.

Board Info

This register contains the specific information of the board, such as the digitizer family, the channel memory size and the channel density.

Address	0x8140
Mode	R
Attribute	C

Bit	Description
[7:0]	Peak Sensing Family Code: 0x10 = 741 peaksensing family.
[15:8]	Reserved.
[23:16]	Equipped Groups Number. Options are: 0x04 = 4 groups (DT and NIM boards); 0x08 = 8 groups (VME boards). NOTE: if this number is lower than the physical group number, there could be a communication problem with some of the mezzanines.
[31:24]	Reserved.

Event Size

This register contains the current available event size in 32-bit words. The value is updated after a complete readout of each event.

Address	0x814C
Mode	R
Attribute	C

Bit	Description
[31:0]	Event Size (32-bit words).

Fan Speed Control

This register manages the on-board fan speed in order to guarantee an appropriate cooling according to the internal temperature variations.
NOTE: from revision 4 of the motherboard PCB (see register 0xF04C of the Configuration ROM), the automatic fan speed control has been implemented, and it is supported by ROC FPGA firmware revision greater than 4.4 (see register 0x8124).
Independently of the revision, the user can set the fan speed high by setting bit[3] = 1. Setting bit[3] = 0 will restore the automatic control for revision 4 or higher, or the low fan speed in case of revisions lower than 4.
NOTE: this register is supported by Desktop (DT) boards only.

Address	0x8168
Mode	R/W
Attribute	C

Bit	Description
[2:0]	Reserved: Must be 0.
[3]	Fan Speed Mode. Options are: 0 = slow speed or automatic speed tuning; 1 = high speed.
[5:4]	Reserved: Must be 1.
[31:6]	Reserved: Must be 0.

Memory Buffer Almost Full Level

This register allows to set the level for the Almost Full generation. The written value (ALMOST FULL LEVEL) represents the number of buffers that must be full of data before to assert the BUSY signal. This register takes part in the BUSY propagation among multiple boards.
NOTE: if this register is set to 0, the ALMOST FULL is a FULL.
For the Almost Full description, please refer to the Acquisition Synchronization section of the digitizer User Manual.

Address	0x816C
Mode	R/W
Attribute	C

Bit	Description
[10:0]	ALMOST FULL LEVEL.
[31:11]	Reserved.

Run/Start/Stop Delay

This register sets the delay in the Start Run of the board either the command is issued by software, or by hardware through a single-ended (via S-IN/GPI or TRG-IN connectors) or differential (via LVDS I/O connector) input signal. This delay especially occurs in the daisy chain propagation of the run signal in a multi-board system. The latency, mainly due to the cable length and the board's internal circuitry, can be compensated by properly delaying the start of run for each board in the chain. The delay value to set is usually zero for the last board and rises going backwards along the chain.

Address	0x8170
Mode	R/W
Attribute	C

Bit	Description
[7:0]	Delay value in steps of 16 ns.
[31:8]	Reserved.

Board Failure Status

This register informs on the cause of a board fail. In event of a failure, bit[26] in the second word of the event format header is set to 1 during data readout (refer to the event structure description in the User Manual of the digitizer). Reading at this register checks which kind of error occurred. NOTE: in case of problems with the board, the user is recommended to contact CAEN for support.

Address	0x8178
Mode	R
Attribute	C

Bit	Description
[3:0]	Reserved.
[4]	PLL Lock Loss. Options are: 0 = no error; 1 = PLL Lock Loss occurred.
[31:5]	Reserved.

Front Panel LVDS I/O New Features

If the LVDS I/O new features are enabled (bit[8] = 1 of 0x811C), this register programs the functions of the front panel LVDS I/O 16-pin connector. It is possible to configure the LVDS I/O pins by group of four (4).
Options are:
1) 0000 = REGISTER, where the four LVDS I/O pins act as register (read/write according to the configured input/output option);
2) 0001 = GATE, where each group of four LVDS I/O pins can be configured to propagate out the gate signal;
3) 0010 = nBUSY/nVETO, where each group of four LVDS I/O pins can be configured as inputs (0 = nBusyIn, 1 = nVetoIn, 2 = Reserved, 3 = Reserved) or as outputs (0 = nBusy, 1 = nVeto, 2 = nGateOut, 3 = nRun);
4) 0011 = LEGACY, where the LVDS can be configured as 0 = Busy, 1 = Data ready, 2 = Gate, 3 = Run in case of output LVDS setting.
Please refer to the Front Panel LVDS I/Os section of the digitizer User Manual for detailed description.
NOTE: LVDS I/O new features are supported from ROC FPGA firmware revision 3.8 on.
NOTE: this register is supported by VME boards only.

Address	0x81A0
Mode	R/W
Attribute	C

Bit	Description
[3:0]	LVDS I/O pins[3:0] Configuration.
[7:4]	LVDS I/O pins[7:4] Configuration.
[11:8]	LVDS I/O pins[11:8] Configuration.
[15:12]	LVDS I/O pins[15:12] Configuration.
[16]	This bit permits selecting whether the nGate signal, when configured as output (in nBusy/nVeto LVDS I/O mode), is a copy of the signal sent on the TRG-OUT connector or a copy of the acquisition common Gate. Options are: 0 = nGate output is a copy of TRG-OUT signal 1 = nGate output is a copy of the acquisition common gate.
[31:17]	Reserved.

Readout Status

This register contains information related to the readout.

Address	0xEF04
Mode	R
Attribute	C

Bit	Description
[0]	Event Ready. Indicates if there are events stored ready for readout. Options are: 0 = no data ready; 1 = event ready.
[1]	Reserved.
[2]	Bus Error (VME boards) / Slave-Terminated (DT/NIM boards) Flag. Options are: 0 = no Bus Error occurred (VME boards) or no terminated transfer (DT/NIM boards); 1 = a Bus Error occurred (VME boards) or one transfer has been terminated by the digitizer in consequence of an unsupported register access or block transfer prematurely terminated in event aligned readout (DT/NIM). NOTE: this bit is reset after register readout at 0xEF04.
[3]	VME FIFO Flag. Options are: 0 = VME FIFO not empty; 1 = VME FIFO is empty.
[31:4]	Reserved.

Board ID

The meaning of this register depends on which VME crate it is inserted in.
In case of VME64X crate versions, this register can be accessed in read mode only and it contains the GEO address of the module picked from the backplane connectors; when CBLT is performed, the GEO address will be contained in the Board ID field of the Event header (see the User Manual for further details).
In case of other crate versions, this register can be accessed both in read and write mode, and it allows to write the correct GEO address (default setting = 0) of the module before CBLT operation. GEO address will be contained in the Board ID field of the Event header (see the User Manual for further details).
NOTE: this register is supported by VME boards only.

Address	0xEF08
Mode	R/W
Attribute	C

Bit	Description
[4:0]	GEO Address (VME boards only).
[31:5]	Reserved.

MCST Base Address and Control

This register configures the board for the VME Multicast Cycles.
NOTE: this register is supported by VME boards only.

Address	0xEF0C
Mode	R/W
Attribute	C

Bit	Description
[7:0]	These bits contain the most significant bits of the MCST/CBLT address of the module set via VME, that is the address used in MCST/CBLT operations.
[9:8]	Board Position in Daisy chain. Options are: 00 = board disabled; 01 = last board; 10 = first board; 11 = intermediate board.
[31:10]	Reserved.

Relocation Address

If address relocation is enabled through register 0xEF00 (bit[6] = 1), this register sets the VME Base Address of the module.
NOTE: this register is supported by VME boards only.

Address	0xEF10
Mode	R/W
Attribute	C

Bit	Description
[15:0]	These bits contain the A31...A16 bits of the address of the module. If bit[6] = 1 of 0xEF00, they set the VME Base Address of the module.
[31:16]	Reserved.

Scratch

This register can be used to write/read words for test purposes.

Address	0xEF20
Mode	R/W
Attribute	C

Bit	Description
[31:0]	SCRATCH.

Software Reset

All the digitizer registers can be set back to their default values on software reset command by writing any value at this register, or by system reset from backplane in case of VME boards.

Address	0xEF24
Mode	W
Attribute	C

Bit	Description
[31:0]	Whatever value written at this location issues a software reset. All registers are set to their default values (actual settings are lost).

Software Clear

All the digitizer internal memories are cleared:
- automatically by the firmware at the start of each run;
- on software command by writing at this register;
- by hardware (VME boards only) through the LVDS interface properly configured.

A clear command does not change the registers actual value, except for resetting the following registers:
- Event Stored;
- Event Size;
- Channel / Group n Buffer Occupancy.

This register resets also the trigger time stamp.

Address	0xEF28
Mode	W
Attribute	C

Bit	Description
[31:0]	Whatever value written at this location generates a software clear.

Configuration Reload

A write access of any value at this location causes a software reset, a reload of Configuration ROM parameters and a PLL reconfiguration.

Address	0xEF34
Mode	W
Attribute	C

Bit	Description
[31:0]	Write whatever value to perform a software reset, a reload of Configuration ROM parameters and a PLL reconfiguration.

Configuration ROM Checksum

This register contains information on 8-bit checksum of Configuration ROM space.

Address	0xF000
Mode	R
Attribute	C

Bit	Description
[7:0]	Checksum.
[31:8]	Reserved.

Configuration ROM Checksum Length BYTE 2

This register contains information on the third byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address	0xF004
Mode	R
Attribute	C

Bit	Description
[7:0]	Checksum Length: bits[23:16].
[31:8]	Reserved.

Configuration ROM Checksum Length BYTE 1

This register contains information on the second byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address	0xF008
Mode	R
Attribute	C

Bit	Description
[7:0]	Checksum Length: bits[15:8].
[31:8]	Reserved.

Configuration ROM Checksum Length BYTE 0

This register contains information on the first byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address	0xF00C
Mode	R
Attribute	C

Bit	Description
[7:0]	Checksum Length: bits[7:0].
[31:8]	Reserved.

Configuration ROM Constant BYTE 2

This register contains the third byte of the 3-byte constant.

Address	0xF010
Mode	R
Attribute	C

Bit	Description
[7:0]	Constant: bits[23:16] = 0x83.
[31:8]	Reserved.

Configuration ROM Constant BYTE 1

This register contains the second byte of the 3-byte constant.

Address	0xF014
Mode	R
Attribute	C

Bit	Description
[7:0]	Constant: bits[15:8] = 0x84.
[31:8]	Reserved.

Configuration ROM Constant BYTE 0

This register contains the first byte of the 3-byte constant.

Address	0xF018
Mode	R
Attribute	C

Bit	Description
[7:0]	Constant: bits[7:0] = 0x01.
[31:8]	Reserved.

Configuration ROM C Code

This register contains the ASCII C character code (identifies this as CR space).

Address	0xF01C
Mode	R
Attribute	C

Bit	Description
[7:0]	ASCII 'C' Character Code.
[31:8]	Reserved.

Configuration ROM R Code

This register contains the ASCII R character code (identifies this as CR space).

Address	0xF020
Mode	R
Attribute	C

Bit	Description
[7:0]	ASCII 'R' Character Code.
[31:8]	Reserved.

Configuration ROM IEEE OUI BYTE 2

This register contains information on the third byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Address	0xF024
Mode	R
Attribute	C

Bit	Description
[7:0]	IEEE OUI: bits[23:16].
[31:8]	Reserved.

Configuration ROM IEEE OUI BYTE 1

This register contains information on the second byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Address	0xF028
Mode	R
Attribute	C

Bit	Description
[7:0]	IEEE OUI: bits[15:8].
[31:8]	Reserved.

Configuration ROM IEEE OUI BYTE 0

This register contains information on the first byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Address	0xF02C
Mode	R
Attribute	C

Bit	Description
[7:0]	IEEE OUI: bits[7:0].
[31:8]	Reserved.

Configuration ROM Board Version

This register contains the board version information.

Address	0xF030
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Version Code. Options are: 0x55 = V1741/N6741.
[31:8]	Reserved.

Configuration ROM Board Form Factor

This register contains the information of the board form factor.

Address	0xF034
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Form Factor CAEN Code. Options are: 0x00 = VME64; 0x01 = VME64X; 0x02 = Desktop; 0x03 = NIM.
[31:8]	Reserved.

Configuration ROM Board ID BYTE 1

This register contains the MSB of the 2-byte board identifier.

Address	0xF038
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Number ID: bits[15:8].
[31:8]	Reserved.

Configuration ROM Board ID BYTE 0

This register contains the LSB information of the 2-byte board identifier.

Address	0xF03C
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Number ID: bits[7:0].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 3

This register contains information on the fourth byte of the 4-byte hardware revision.

Address	0xF040
Mode	R
Attribute	C

Bit	Description
[7:0]	PCB Revision: bits[31:24].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 2

This register contains information on the third byte of the 4-byte hardware revision.

Address	0xF044
Mode	R
Attribute	C

Bit	Description
[7:0]	PCB Revision: bits[23:16].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 1

This register contains information on the second byte of the 4-byte hardware revision.

Address	0xF048
Mode	R
Attribute	C

Bit	Description
[7:0]	PCB Revision: bits[15:8].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 0

This register contains information on the first byte of the 4-byte hardware revision.

Address	0xF04C
Mode	R
Attribute	C

Bit	Description
[7:0]	PCB Revision: bits[7:0].
[31:8]	Reserved.

Configuration ROM FLASH Type

This register contains information on which FLASH type (storing the FPGA firmware) is present on- board.

Address	0xF050
Mode	R
Attribute	C

Bit	Description
[7:0]	FLASH Type. Options are: 0x00 = 8 Mb FLASH; 0x01 = 32 Mb FLASH.
[31:8]	Reserved.

Configuration ROM Board Serial Number BYTE 1

This register contains information on the MSB of the board serial number.

Address	0xF080
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Serial Number: bits[15:8].
[31:8]	Reserved.

Configuration ROM Board Serial Number BYTE 0

This register contains information on the LSB of the board serial number.

Address	0xF084
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Serial Number: bits[7:0].
[31:8]	Reserved.

Configuration ROM VCXO Type

This register contains information on which type of VCXO is present on-board.

Address	0xF088
Mode	R
Attribute	C

Bit	Description
[31:0]	VCXO Type Code. Options for VME Digitizers are: 0 = AD9510 with 1 GHz; 1 = AD9510 with 500 MHz (not programmable); 2 = AD9510 with 500 MHz (programmable). Options for Desktop/NIM Digitizers are: Reserved (value = 0).

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