CAEN
Tools for Discovery

Electronic Instrumentation

PRELIMINARY

User Manual UM7028

A55CITx

CITIROC Piggyback Board for DT5550W

Rev. 3 - March 2nd, 2022

Purpose of this User Manual

This User Manual contains the full description of the A55CITx Piggyback Boards family for DT5550W.

Change Document Record

Date	Revision	Changes
July 18th, 2019	00	Initial release
February 21st, 2020	01	Revised **DT5550W Readout Software**
June 8th, 2021	02	Revised **DT5550W Readout Software**
March 2nd, 2022	03	General revision

Symbols, abbreviated terms and notation

ADC	Analog to Digital Converter
FPGA	Field Programmable Gate Array
OEM	Original Equipment Manufacturer
OS	Operating system
PHA	Pulse Height Analysis

Reference Document

[RD1] CITIROC 1A Datasheet (available on WeeROC website)

[RD2] UM6697 - DT5550W User Manual

[RD3] UM6377 – A7585 DT5485 User Manual

[RD4] UM5833 – A1702/DT5702 User Manual

[RD5] DS8241 – Remotization kit datasheet

Manufacturer contact

CAEN S.p.A.
Via Vetraia, 11 55049 Viareggio (LU) - ITALY
Tel. +39.0584.388.398 Fax +39.0584.388.959
www.caen.it | info@caen.it

Limitation of responsibility

If the warnings contained in this manual are not followed, CAEN will not be responsible for damage caused by improper use of the device. The manufacturer declines all responsibility for damage resulting from failure to comply with the instructions for use of the product. The equipment must be used as described in the user manual, with particular regard to the intended use, using only accessories as specified by the manufacturer. No modification or repair can be performed.

MADE IN ITALY: We remark that all our boards have been designed and assembled in Italy. In a challenging environment where a competitive edge is often obtained at the cost of lower wages and declining working conditions, we proudly acknowledge that all those who participated in the production and distribution process of our devices were reasonably paid and worked in a safe environment (this is true for the boards marked "MADE IN ITALY", while we cannot guarantee for third-party manufactures).

Index

Purpose of this User Manual 2
Change Document Record 2
Symbols, abbreviated terms and notation 2
Reference Document 2
Manufacturer contact 2
Limitation of responsibility 2
Index 4
List of Figures 5
List of Tables 6
1 Introduction 7
2 Safety Notices 8
3 Block Diagram 10
4 Technical Specifications 11
5 Packaging and compliancy 13
6 PID (Product Identifier) 15
7 Power Requirements 16
8 Cooling Management 17
9 Installing the device 18
10 Hardware Description 19
SiPM connection and biasing 19
Pitch Adapter Kit 21
Temperature Feedback 23
Test Pins 24
Motherboard I/Os 25
11 Functional Description 27
Citiroc-1A 27
SiPM Gain Trimming 27
Charge Measurement 28
Discriminators 30
Test Pulser 30
ASIC Trigger Operation 31
Default trigger logic 33
Veto and validation 33
Readout Modes 34
Photon Counting 34
Analog Multiplexed Readout 35
ASICs configuration 36
12 Firmware and data format 37
13 DT5550W Readout Software 39
Software installation 39
Board Connection 41
Software GUI Description 42
Menu and Control Toolbar 42
Main plots 43
The ASIC Monitor Tab 45
The Scan Tab 45
The Settings Tab 46
Channel specific settings 52

Log Area and DAQ Status Bar 52
How to perform an acquisition **53**
Spectroscopy Data Saving Format **53**
Photon Counting Data Saving Format **55**
How to perform pedestal calculation **56**
How to set uniformity gain **56**
How to remap a detector geometry **57**
14 Multiple boards control **59**
15 Instructions for Cleaning **61**
Cleaning the Touchscreen **61**
Cleaning the air vents **61**
General cleaning safety precautions **61**
16 Device decommissioning **62**
17 Disposal **63**
18 Technical Support **64**

List of Figures

Figure 3.1: block diagram showing the main components of A55CITx (left box) and DT5550W motherboard, as well as their interconnection. 10
Figure 5.1: general view of the DT5550W system, where the piggyback is the upper board. 13
Figure 10.1: general view (left front side, right: rear side) of the A55CIT4 piggyback, shown as example. 19
Figure 10.2: the Hamamatsu S13361-3050AE-08 connected onboard. The grid reports the association between the matrix pixels (A-1 …. H-8) and the ASIC channels (ch0 … ch31). The green-coloured pixels are connected to ASIC A while yellow-coloured pixels are connected to ASIC B. 20
Figure 10.3: SiPM connection scheme to the ASIC and biasing lines 21
Figure 10.4: view of the 64-ch pitch adapters. The strip connectors (each for 32 channels), the External HV LEMO and the P2 jumper are clearly visible. 22
Figure 10.5: dimensions of the pitch adapter. 22
Figure 10.6: SiPM connection scheme to the ASIC and biasing lines when using the pitch adapter kit 23
Figure 10.7: Top: how to plug the pitch adapter on the board's SiPM connector. The connectors are pressure-pluggable. Bottom: general view of a DT5550W with A55CIT4 piggyback and two pitch adapters plugged in. In this configuration, all 128 channels of the DT5550W board are exposed on the strip connectors. 23
Figure 10.8: the user I2C interface on the motherboard, to be used for external temperature sensor connection. 24
Figure 10.9: the test pins of A55CITx boards. 24
Figure 10.10: a typical debugging acquisition made at the oscilloscope using test pins. Yellow: Shaper output. Magenta: the NOR32 time trigger. Blue: Analog LG output. 25
Figure 10.11: the programmable LEMO digital I/Os of the DT5550W 25
Figure 11.1: scheme of the CITIROC 1A ASIC. 27
Figure 11.2: High Gain and Low Gain voltage sensitive Preamplifiers. 28
Figure 11.3: Slow Shaper schematic. 28
Figure 11.4: the Track&Hold operation in CITIROC 1A ASIC. 29
Figure 11.5: Peak detector chronogram. 29
Figure 11.6: Fast Shaper circuit scheme. 30
Figure 11.7: the In_Calib circuit 31
Figure 11.8: the Citiroc-1A trigger scheme 31
Figure 11.9: the Citiroc-1A charge triggering logic system 32
Figure 11.10: scheme of the triggering logic set in the default firmware loaded on DT5550W for A55CITx management. 33
Figure 11.11: readout scheme of DT5550W and ASIC operating in photon counting mode. 34
Figure 11.12: the analog readout scheme of CITIROC 1A, where multiplexed data are available as output. 35
Figure 11.13: scheme of the analog multiplexed readout process 36
Figure 12.1: structure of the data packet sent to the PC using the default firmware. 37
Figure 13.1: general view of the DT5550W Readout Software. In this example, a spectroscopy and imaging acquisition is being performed with A55CIT2 board, using a 64-channel SiPM matrix. 39
Figure 13.2: the "Connection" window at start-up of the DT5550W Readout Software 42

Figure 13.3: the Menu and Control Toolbar of the DT5550W Readout Software, before (top) and during (bottom) acquisition. 42
Figure 13.4: the *ASIC Monitor* Tab for A55CITx Piggyback. The white plot shows the charge multiplexed output....45
Figure 13.5: the *Settings* tab for A55CITx piggyback. The top and bottom area are clearly visible. The top area has different tabs for general configuration and the bottom area has a tab for each ASIC. 46
Figure 13.6: the *Asic General* subtab of the *Settings* tab. 47
Figure 13.7: the *Trigger* subtab of the *Settings* tab. 47
Figure 13.8: the effect of different triggering on imaging acquisition. On the left, with Trigger Mode = Time, and a more intense light on ASIC A, this latter is triggering while ASIC B is not triggering. On the right, with Trigger Mode = OR Time , both ASICs are acquiring. 48
Figure 13.9: the *Timestamp* subtab of the *Settings* tab. 48
Figure 13.10: the *HV* subtab of the *Settings* tab. 49
Figure 13.11: the *Data Processing* subtab of the *Settings* tab. 49
Figure 13.12: the *Monitor* subtab of the *Settings* tab. 50
Figure 13.13: the *Photon Counting* subtab of the *Settings* tab. 51
Figure 13.14: the bottom area of the *Settings* tab, containing the table for ASIC channels specific settings. In this case two ASICs (called A and B) are hosted on the board**.** 52
Figure 13.15: the *Log Area* after board connection. 53
Figure 13.16: the *Start Run* window which opens after the acquisition with data saving is started. 53
Figure 13.17: data saved in binary format for A55CITx board 54
Figure 13.18: an image of a 64-channel SiPM matrix acquired before (left) and after (right) the pedestal calculation. 56
Figure 13.19: the results of pedestal calculation and gain regulation. The image on the right (after compensation of offset and gain) has a more uniform background (deep blue pixels) and small energy differences in neighbouring pixels with respect to the image on the left. 57
Figure 13.20: the *Mapping* tab, to associate the ASIC channels to detector pixels. 57
Figure 14.1: the *Server configuration* window 59

List of Tables

Table 1.1: table of available board models and accessories 7
Table 2.1: operating limits for A55CITx mezzanine connector. 9
Table 4.1: technical specifications of the A55CITx 12
Table 10.1: description of the main components and connectors of the A55CITx board 19
Table 10.2: description of the pitch adapter connectors. 22
Table 10.3: A55CITx test pins description. 25
Table 10.4: assignment of the programmable LEMO digital I/Os in the default firmware for A55CITx management. 26
Table 13.1: saved data format in *Processing Mode* = DECODE EVENTS 55
Table 13.2: saved data format in *Processing Mode* = FULL 55
Table 13.3: saved data format in *Photon Counting Mode* 56

1 Introduction

The A55CITx board is the Piggyback Board for DT5550W, hosting up to four CITIROC 1A WeeROC (*) ASICs. It can be used in conjunction with DT5550W motherboard to perform **high-resolution energy measurements with SiPMs and SiPM matrixes.**

The device is designed to operate in laboratory environment under the supervision of skilled technicians.

The CITIROC 1A is the ideal solution for high density channel systems, aiming to readout SiPM sensors extracting energy, time and positional information. In fact, the CITIROC 1A chip, besides the classical readout chain made of preamp, fast and slow shaper, it also integrates a trigger with a timing resolution better than 100 ps and a Sample&Hold circuit with peak detection. Each CITIROC 1A integrates 32 readout channels.
The A55CITx piggyback is equipped with CAEN module A7585D to be used for SiPM biasing. The A7585D power supply is directly soldered on the PCB.

The CITIROC 1A integrates in a chip an entire readout system, requiring externally only few passive components, two clock lines and a FPGA connected with few lines, which can manage up one hundred ASICs. Therefore, a system exploiting this chip is the best solution for experiments in which the high number of channels requires the reduction of the hardware components, because of geometrical and economic reasons.

The A55CITx Piggyback can be easily plugged onto the DT5550W motherboard to arrange a **complete Data Acquisition System for SiPM with up to 128 channels**. The CITIROCs readout is completely managed by the firmware preloaded on the FPGA hosted by the DT5550W motherboard.

The **DT5550W Readout Software** is the free and open source Windows-based software developed to perform acquisitions with the DT5550W. It works in conjunction with the DT5550W default firmware and it can be modified by the user according to the custom functions implemented in the firmware and for any other need. It allows to perform:

- List event readout and timestamping
- Energy Spectrum measurements
- Imaging with configurable detector shape
- System and ASIC configuration
- ASIC monitor signal probing

For more detailed information, see **[RD2]**.

Available board models and accessories are listed below.

Motherboard	Description	Product Code
DT5550W	DT5550W - WeeROC ASICs Evaluation and DAQ System	WDT5550WXAAA
Piggyback Board Models	**Description**	**Product Code**
A55CIT2	A55CIT2 - Piggyback Board with 2 CITIROC chip	WW55CITI2AA2
A55CIT4	A55CIT4 - Piggyback Board with 4 CITIROC chip	WW55CITI2AA4
Accessories	**Description**	**Product Code**
REMOT5550W	Remotization kit with 2-meters cable for DT5550W	WKREMOT5550W

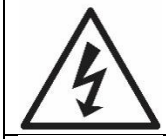
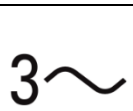
Table 1.1: table of available board models and accessories

(*) https://www.weeroc.com

2 Safety Notices

N.B. Read carefully the "Precautions for Handling, Storage and Installation" document provided with the product before starting any operation.

The following HAZARD SYMBOLS may be reported on the unit:

	Caution, refer to product manual
	Caution, risk of electrical shock
	Protective conductor terminal
	Earth (Ground) Terminal
	Alternating Current
	Three-Phase Alternating Current

The following symbol may be reported in the present manual:

	General warning statement

The symbol could be followed by the following terms:

- **DANGER**: indicates a hazardous situation which, if not avoided, will result in serious injury or death.
- **WARNING**: indicates a hazardous situation which, if not avoided, could result in death or serious injury.
- **CAUTION**: indicates a situation or condition that, if not avoided, could cause physical injury or damage the product and / or its environment.

To avoid potential hazards, use the product only as specified. Only qualified personnel should perform service procedures.
Avoid Electric Overload. To avoid electric shock or fire hazard, do not power a load outside of its specified range.
Avoid Electric Shock. To avoid injury or loss of life, do not connect or disconnect cables while they are connected to a voltage source.

Do Not Operate without Covers. To avoid electric shock or fire hazard, do not operate this product with covers or panels removed.
Do Not Operate in Wet/Damp Conditions. To avoid electric shock, do not operate this product in wet or damp conditions.
Do Not Operate in an Explosive Atmosphere. To avoid injury or fire hazard, do not operate this product in an explosive atmosphere.
Do Not Operate with Suspected Failures. If you suspect this product to be damaged, please contact Technical Support.

The mezzanine connector carries more than 250 I/O lines that can be grouped as:

- Digital 3.3V single ended I/O
- Digital 2.5V single ended I/O
- Digital differential 2.5V LVDS
- Analog differential Input
- Analog Common Mode Output
- I2C
- Power Supply
- Clock output

The following operating limits must be respected:

Net class	Connector	Unit	Min	Max
Digital lines	Mezzanine connector			
	Digital 3.3V	Voltage	0 V	3.5V
		Current		10 mA
	Digital 2.5V	Voltage	0 V	2.7 V
		Current		10 mA
	LVDS	Voltage	0.5 V	2.1 V
		Current		10 mA
		Common Mode		1.25 V
	I2C	Voltage	0	3.5 V
	Analog Differential Input	Voltage	0.45 V	1.55 V
		Common Mode	0.95 V	0.95 V
	Analog Common Mode Output	Current		6 mA
	Power 5V	Current		2 A
	Power 3.3V	Current		2 A
	Power 1.8V	Current		1 A
	Power 4V A	Current		600 mA
	Power -1V A	Current		600 mA
	Clock Output	Differential Impedance	80 Ω	120 Ω

Table 2.1: operating limits for A55CITx mezzanine connector.

WARNING: the piggyback connector lines are directly connected to the FPGA I/O. Violation in maximum absolute rating given in this document will likely destroy the FPGA.

THIS DEVICE SHOULD BE INSTALLED AND USED BY SKILLED TECHNICIAN ONLY OR UNDER HIS SUPERVISION

3 Block Diagram

The A55CITx board is designed to be plugged on the DT5550W motherboard via the mezzanine connector, so that this latter board provides all needed power supply lines, clocks, control and transfer signals. In **Figure 3.1**, the interconnection of the piggyback with the motherboard components is shown.

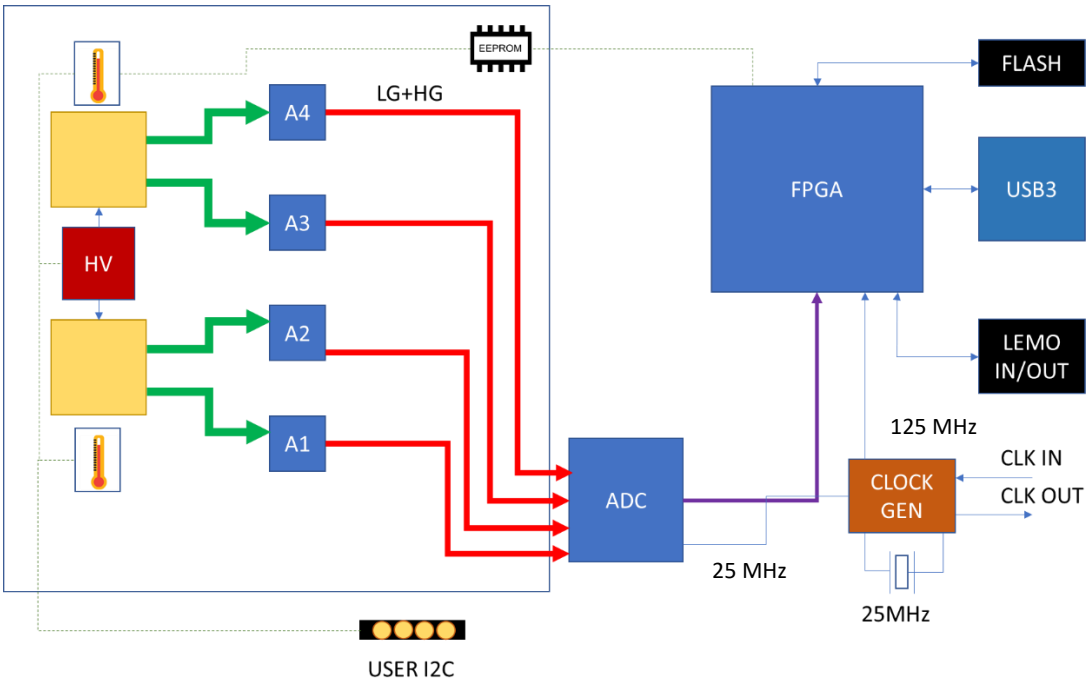


Figure 3.1: block diagram showing the main components of A55CITx (left box) and DT5550W motherboard, as well as their interconnection.

4 Technical Specifications

TECHNICAL	
POWER CONSUMPTION	DT5550W + A55CIT4 piggyback - 0.9A @ 12V (Typ.)
ANALOG INPUT	**Channels** 64 or 128 (=2 or 4 Citiroc-1A) **Connector** Compatible with one or two 64-channel Hamamatsu matrix S13361-3050AE-08 INCLUDED **strip adapter with 2.54 mm pitch**
SIGNAL POLARITY	Positive
SENSITIVITY	Dual range: Low Gain (LG)/High Gain (HG). Channel-by-channel individual setting of the gain value through a CSP feedback capacitor, C_f, adjustable from 25 fF to 1575 fF (25 fF step): - LG = 1.5 pF/C_f (max gain = 60) - HG = 10 × LG = 15 pF/C_f (max gain = 600)
DYNAMIC RANGE	The Citiroc-1A preamplifiers ensure a dynamic range from 160 fC to 400 pC (i.e. from 1 to 2500 photo-electrons with 10^6 SiPM gain)
SHAPING TIME	**Slow Shaper** 7 options from 12.5 ns to 87.5 ns (12.5 ns step) **Fast Shaper** Fixed: 15 ns
ANALOG PROBE	MCX connectors allowing the user to acquire analog signals from a specific, software selectable stage of each Citiroc-1A signal shaping chain: - LG/HG Preamplifier output - LG/HG Slow Shaper output - Fast Shaper output
CALIBRATION INPUT	MCX connectors allowing the user to drive a signal through the charge injection circuit
SELF-TRIGGERS	Programmable 10-bit DAC for common threshold - Minimum threshold: 1/3 photo-electron - Separate trigger line per channel - Programmable 4-bit DAC for channel-by-channel threshold fine adjustment - Logic combination (AND, OR) of triggers for start of A/D conversion and time reference -**Custom combinations** through open FPGA and **SCI-Compiler**
EXTERNAL TRIGGER	From LEMO 4 of the DT5550W motherboard programmable I/Os
HIGH VOLTAGE POWER SUPPLY	Single channel PCB mounted A7585D High Voltage Power Supply: - Common SiPM bias voltage: 20 ÷ 85 V -Vset vs. Vout Accuracy: ±0.2% ±50mV - Individual channel adjustment: 8-bit (2.5V or 4.5V dynamic range) - Max. output bias current: 10 mA - Programmable temperature compensation
ACQUISITION MODES	**Spectroscopy Mode (PHA)** -Simultaneous acquisition of all channels – energy and timestamp - 14-bit A/D conversion - Systematic conversion time ~ *25* µs → Max. trigger rate ~ *40* kHz **Counting Mode** - Channel-by-channel independent counting - Counting window - Maximum counting rate (per channel): ~ *10* Mcps
TIME STAMP	*Default FW*: 0.5 ns resolution TDC for event timetag since the start of the run 6.125 ns resolution for reset-on-T0 timestamp *Custom FW*: Defined by the firmware design
INTERCONNECTION	Mezzanine connector carrying more than 200 analog/digital lines, to connect the A55CITx onto the DT5550W motherboard
SOFTWARE	• **DT5550W Readout Software** to manage the default firmware • **SCI-Compiler** for custom firmware development on the DT5550W motherboard
MECHANICAL	
FORM FACTOR	Desktop bare PCB unit

DIMENSIONS (H/W/L)	Piggyback: 5/160/145 mm^3 (including connectors) Piggyback mounted on DT5550W: 24/152/260 mm^3 (including connectors)
ENVIRONMENTAL	
ENVIRONMENTAL	Indoor use
OPERATING TEMPERATURE	Operating Temperature -20 °C ÷ 50 °C
OPERATING HUMIDITY	25% ÷ 95% RH non condensing
STORAGE TEMPERATURE	-30 °C ÷ +80 °C
STORAGE HUMIDITY	5% ÷ 90% RH non condensing
ALTITUDE	≤2000 m
POLLUTION DEGREE	2
OVERVOLTAGE CATEGORY	II
EMC ENVIRONMENT	Commercial and light industrial
IP DEGREE	IPX0 enclosure, not for wet location
REGULATORY	
COMPLIANCE	• EMC: CE 2014/30/EU Electromagnetic compatibility Directive • Safety: CE 2014/35/EU Low Voltage Directive

Table 4.1: technical specifications of the A55CITx

5 Packaging and compliancy

The A55CITx is a bare piggyback PCB – 5/160/145 mm^3 (including connectors) H/W/L – intended to be mounted on the DT5550W motherboard. The system is provided as OEM device without any enclosure in order to be easily integrated in the final experimental setup. If the A55CITx is purchased together with the DT5550W motherboard, the system is provided already assembled, as shown in **Figure 5.1**

Figure 5.1: general view of the DT5550W system, where the piggyback is the upper board.

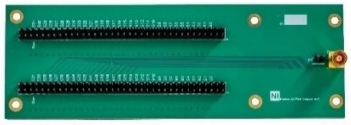
The unit is inspected by CAEN before the shipment, and it is guaranteed to leave the factory free of mechanical or electrical defects.

When receiving the unit, the user is strictly recommended to inspect for any damage which may have occurred during transportation. Particularly, inspect for exterior damages like broken connectors and check that the panel is not scratched or cracked.

All packing material should be held on until the inspection has been completed. If damage is detected, the user must file a claim with the carrier immediately and notify CAEN.

Before installing the unit, make sure to read thoroughly the safety rules and installation requirements (Sec. **Safety Notices** and **Installing the device**), then place the package content onto your bench.

The content of the delivered package standardly consists of the part list shown in the table below (**Table 5.1**). All the official documentation, firmware updates, software tools, and accessories are available on *www.caen.it* at the product web page.

	Part	Description	Qty
	A55CITx piggyback	Weeroc ASICs evaluation and DAQ system	x1
	Dark box	3D-printed dark box with connector for optical fiber, compatible with CAEN SP5601/SP5605 LED Driver kit. It can be used to operate the SiPMs in a light-tight environment and illuminate them with an external light source.	x1 or x2
	2.54 mm pitch adapter	2.54 mm pitch adapter to convert the Ultra Fine Pitch Socket for SiPM connection into a double 2.54 mm strip connector	x1 or x2

	Fixing kit	Nuts and bolts to secure the dark box or pitch adapter to the A55CITx – by default it is already mounted to secure the dark boxes	
	User guide	UM7028 – A55CITx User Manual	x1

Table 5.1: delivered kit.

CAUTION: to manage the product, consult the operating instructions provided.

A55CITx is an ESD sensitive item. Handling without ESD protective covering shall be performed only into approved ESD Protected Area (EPAs)

A55CITx complies with EMC directive only if installed in a CE marked system

It is recommended to:

- Inspect containers for damage during shipment. Report any damage to the freight carrier for possible insurance claims.
- Check that all the components received match those listed on the enclosed packing list. (CAEN cannot accept responsibility for missing items unless we are notified promptly of any discrepancies.)
- Open shipping containers; be careful not to damage contents.
- Inspect contents and report any damage. The inspection should confirm that there is no exterior damage to the unit such as broken knobs or connectors and that the front panel and display face are not scratched or cracked. Keep all packing material until the inspection has been completed.
- If damage is detected, file a claim with carrier immediately and notify CAEN service.
- If equipment must be returned for any reason, carefully repack equipment in the original shipping container with original packing materials if possible. Please contact CAEN service.
- If equipment is to be installed later, place equipment in original shipping container and store in a safe place until ready to install

DO NOT SUBJECT THE ITEM TO UNDUE SHOCK OF VIBRATIONS

DO NOT BUMP, DROP OR SLIDE SHIPPING CONTAINERS

DO NOT LEAVE ITEMS OR SHIPPING CONTAINERS UNSUPERVISED IN AREAS WHERE UNTRAINED PERSONNEL MAY MISHANDLE THE ITEMS

USE ONLY ACCESSORIES WICH MEET THE MANUFACTURER SPECIFICATIONS

6 PID (Product Identifier)

PID is the CAEN product identifier, an incremental number greater than 10000 that is unique for each product. The PID is on a label affixed to the product (**Fig. 6.1**).

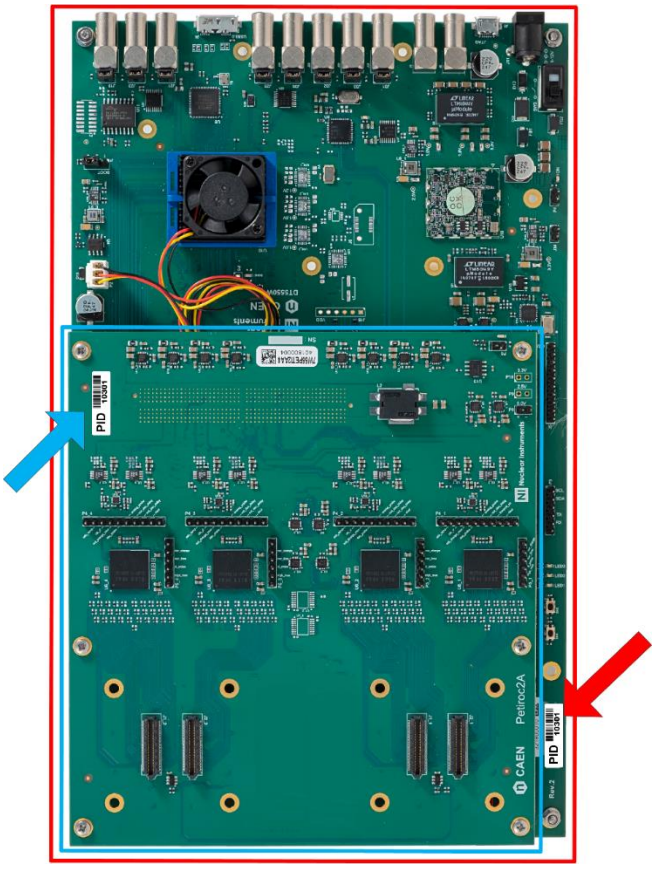


Fig. 6.1: PID location. The blue arrow points to the piggyback board PID.

7 Power Requirements

The A55CITx is powered by the DT5550W motherboard. The motherboard is powered by an external 220-110 V to 12V, 60W AC/DC stabilized power supply provided with the board and included in the delivered kit, together with a standard wall IEC C13 power chord.

Note: using a different power supply source, like battery or linear type, it is recommended the source to provide +12 V and 2A; the power jack is a 2.1 mm type, a suitable cable is the RS 656-3816 type (or similar)

The maximum operating voltage is 12.8V while the minimum is 9V

8 Cooling Management

The A55CITx piggyback board can operate in the temperature range -20 + 50 °C.

The following paragraph refers to the piggyback mounted onto the DT5550W board.

An air flow fan is installed onboard, onto the FPGA of the DT5550W. The user must take in care to provide a proper cooling to the board with external fan if the board is used in an enclosure or if the board is installed in a setup with poor air flow.
Excessive temperature will, in first instance, reduce the performance and the quality of the measurements and can also damage the board.

Please do not stop fan operation to avoid FPGA overheating. If in a single rack tower, multiple units are installed, please consider external fans or rack mounted air conditioning system.

If the board is stored in cold environmental, please check for water condensation before power on.

The board has not been tested for radiation hardness. High energy particle can be source of soft error and can damage the FPGA. If used in strong proton or neutron beams, arrange proper shielding or remote the sensor with a custom cable.

9 Installing the device

- Connect the A55CITx piggyback onto the mezzanine connector of the DT5550W motherboard
- Power on the DT5550W as described in **[RD2]**

If the A55CITx is purchased together with the DT5550W motherboard, the system is provided already assembled, as shown in **Figure 5.1.**

ONLY QUALIFIED PERSONNEL SHOULD PERFORM INSTALLATION, OPERATIONS

DO NOT INSTALL THE EQUIPMENT SO THAT IT IS DIFFICULT TO OPERATE THE ON/OFF SWITCH ONBOARD

IT IS RECOMMENDED THAT THE SWITCH OR CIRCUIT-BREAKER IS NEAR THE EQUIPMENT

THE SAFETY OF ANY SYSTEM THAT INCORPORATES THE DEVICE IS UNDER THE RESPONSIBILITY OF THE ASSEMBLER OF THE SYSTEM

A55CITx is an ESD sensitive item. Handling without ESD protective covering shall be performed only into approved ESD Protected Area (EPAs)

A55CITx complies with EMC directive only if installed in a CE marked system

Do not use the device and contact technical support if one of these situations is verified:
- Enclosure integrity is compromised
- Insulation of HV chord is damaged (if present)
- The indication led or display is not performing as required (e.g. led not working, display with incorrect graphic)
- Fans are not working (if present)

10 Hardware Description

The A55CITx piggyback boards are designed to be plugged onto DT5550W motherboard to build a complete readout system for SiPM (64 or 128 channels).

In the following picture the most important components and connectors on the front and rear side of the A55CIT2 (taken as example for the A55CITx family) are highlighted.

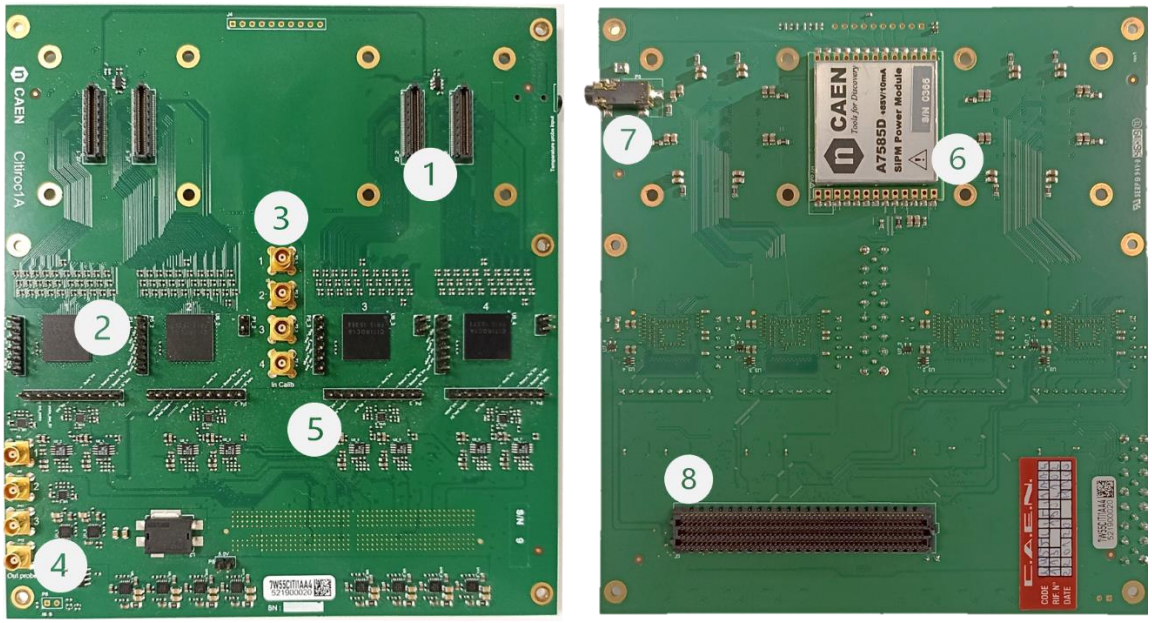


Figure 10.1: general view (left front side, right: rear side) of the A55CIT4 piggyback, shown as example.

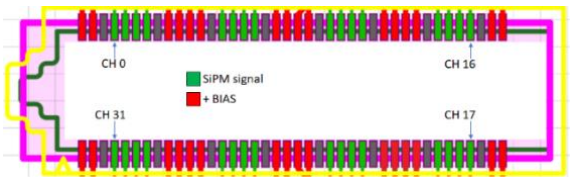
Number	Description
1	**Input connectors** SAMTEC SS4-40-3.00-L-D-K-TR, compatible with 64-channel Hamamatsu matrix S13361-3050AE-08. Each couple of connectors can host a SiPM matrix each. The pinout is the following: 
2	CITIROC ASIC in BGA packaging
3	In_calib – MCX connectors – allows to inject a charge signal from an external pulser in order to calibrate and normalize the pulse response of all channels. Refer to Par. **Test Pulser** for more details
4	Output probe – MCX connectors – refer to Par. **Test Pins** for more details
5	**Test Pins** – 2.54 mm strip – refer to Par. **Test Pins** for more details
6	**A7585D 20-85 V Power Supply** for SiPM biasing
7	Temperature probe input
8	**Mezzanine connector –** SAMTEC SEAM-50-02.0-S-08-2-A-K-TR, 8 column, 64 rows, BGA array connector used to plug the piggyback onto the DT5550W motherboard

Table 10.1: description of the main components and connectors of the A55CITx board

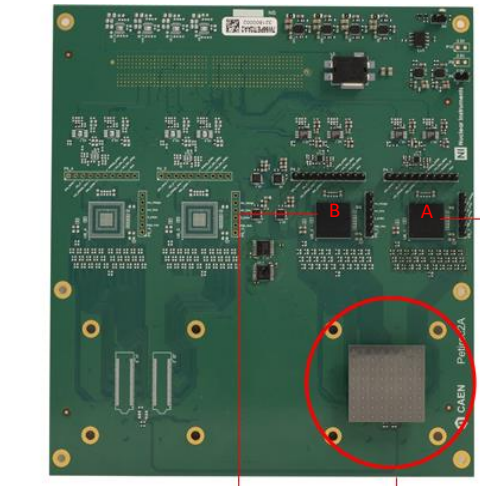
SiPM connection and biasing

It is possible to connect SiPMs to the A55CITx board in three ways:

- use Hamamatsu S13361-3050AE-08 matrix to be connected directly on the onboard Samtec SS4-40-3.0-L-D-K-TR connectors.
- plug the PCB pitch adapter on the board connectors and use the exposed 2.54 mm pitch strip to easily solder any kind of SiPM matrix or array (refer to **Pitch Adapter Kit**). SiPM cathodes must be connected to *Bias* pins, while anodes to S_x pins.

- use a compatible remoting cable to be plugged on the board connectors and design a custom PCB hosting SiPMs – for example CAEN 64-channels Remotization kit **[RD5]**

If connecting a S13361-3050AE-08 Hamamatsu 64-channels matrix directly onboard, the resulting correspondence with the board readout channels is the following:



A-1 ch14	B-1 ch15	C-1 ch16	D-1 ch17	E-1 ch14	F-1 ch15	G-1 ch16	H-1 ch17
A-2 ch13	B-2 ch12	C-2 ch19	D-2 ch18	E-2 ch13	F-2 ch12	G-2 ch19	H-2 ch18
A-3 ch10	B-3 ch11	C-3 ch20	D-3 ch21	E-3 ch10	F-3 ch11	G-3 ch20	H-3 ch21
A-4 ch9	B-4 ch8	C-4 ch23	D-4 ch22	E-4 ch9	F-4 ch8	G-4 ch23	H-4 ch22
A-5 ch6	B-5 ch7	C-5 ch24	D-5 ch25	E-5 ch6	F-5 ch7	G-5 ch24	H-5 ch25
A-6 ch5	B-6 ch4	C-6 ch27	D-6 ch26	E-6 ch5	F-6 ch4	G-6 ch27	H-6 ch26
A-7 ch2	B-7 ch3	C-7 ch28	D-7 ch29	E-7 ch2	F-7 ch3	G-7 ch28	H-7 ch29
A-8 ch1	B-8 ch0	C-8 ch31	D-8 ch30	E-8 ch1	F-8 ch0	G-8 ch31	H-8 ch30

Figure 10.2: the Hamamatsu S13361-3050AE-08 connected onboard. The grid reports the association between the matrix pixels (A-1 …. H-8) and the ASIC channels (ch0 … ch31). The green-coloured pixels are connected to ASIC A while yellow-coloured pixels are connected to ASIC B.

The SiPM bias is provided onboard by the CAEN A7585D Power Supply module, which is extremely low noise (no additional filters needed). The bias lines for SiPMs are grouped eight by eight and connected to the A7585D through a 50 Ω resistance in series, as shown in **Figure 10.3**: SiPM connection scheme to the ASIC and biasing lines**Figure 10.3**. The provided PCB adapter, instead, is equipped with independent filters for each bias line to be fed into the SiPMs.

Since the A7585D feeds the SiPM cathodes with positive high voltage bias (B), the anodes of SiPMs are independently connected to the ASIC input lines (S), accepting positive signals (see **Figure 10.3**). At the ASIC input stage, an 8-bit DAC allows to perform a fine tuning of the bias, individually for each SiPM channel. The voltage can be adjusted in the range 0-4.5 V. This is important in particular to tune the gain of each element, especially when connecting single SiPMs, which can have a spread on the breakdown voltage up to 400 mV. Increasing the DAC value has the effect of lowering the effective bias voltage on the SiPM.

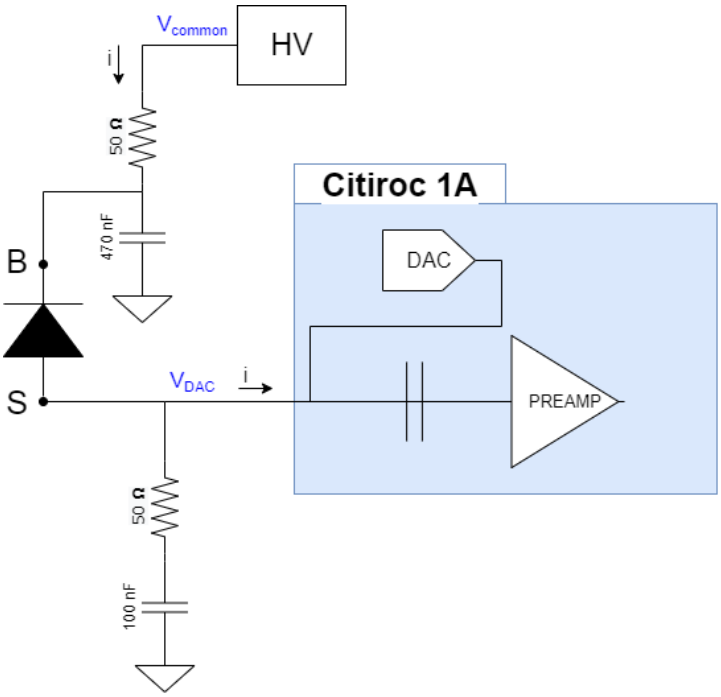


Figure 10.3: SiPM connection scheme to the ASIC and biasing lines

Pitch Adapter Kit

CAEN provides with the A55CITx board, an adapter kit composed by one or two 64-ch PCB boards, to allow the user to easily connect any kind of single SiPM, matrix or array to the board.

The PCB is designed to be pressure-pluggable onto the input connectors available onboard and converts a couple of SAMTEC SS4-40-3.00-L-D-K-TR to a **double 2.54 mm strip connector** (see **Figure 10.4**)**.** In this way, the user can easily mount through-holes 2.54 mm headers on the adapter PCB to connect SiPMs anode/cathode lines. Using two of these PCBs allows to exploit the 128 readout channels of the A55CITx board, exposed on the 2.54 mm pitch strips.

The adapter provides 64 signal readout lines (S_x) and 64 sensor bias (B) lines. Each adapter has two 2.54mm-pitch strip connectors, each one exposing 32 bias/signal couples. Once the adapters are plugged in, the bias can be provided by the A7585D on the A55CITx board itself or externally through the LEMO HV connector available on the adapter. The jumper P2, if inserted, connects the bias pins to the DT5550W High Voltage generator while the LEMO connector is always connected to the Bias pins. The adapter is designed to optimize connections to SiPMs. Each detector has independent bias lines filtered with 1kΩ resistor and 100nF capacitor, as shown in **Figure 10.6**

In order to operate with external bias generator, the jumper P2 should be removed from the pitch adapter, in order to avoid damaging the A55CITx board. External high voltage should not exceed 100V.

Note: the channels pinout indicated on the PCB silkscreen is merely indicative. The effective correspondence with the ASIC channels is defined in the *Mapping* section of the DT5550W Readout Software.

Note: Refer to **Figure 10.7** for instructions to correctly plug the pitch adapter onto the A55CITx.

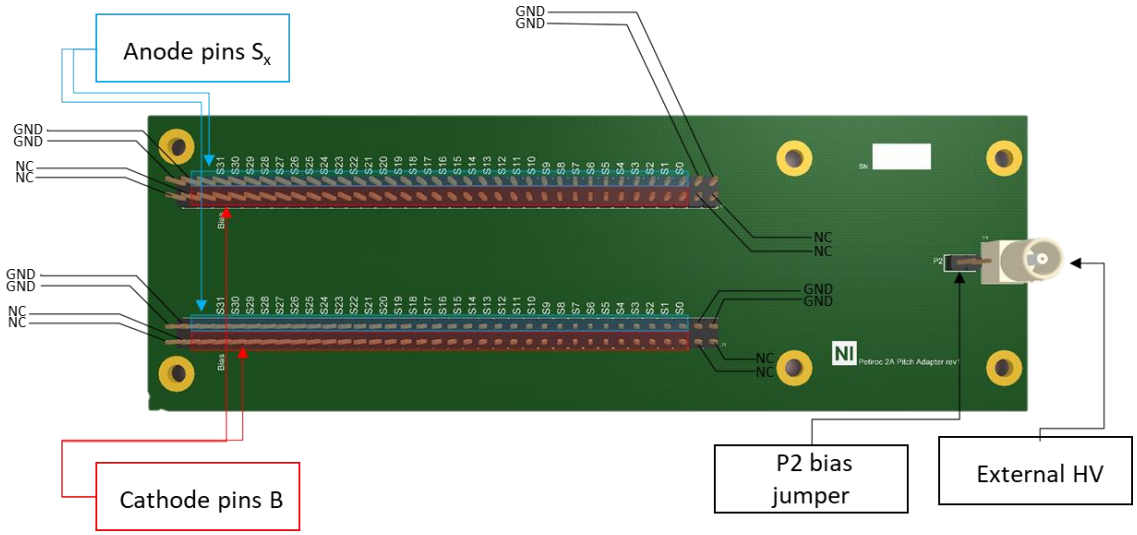


Figure 10.4: view of the 64-ch pitch adapters. The strip connectors (each for 32 channels), the External HV LEMO and the P2 jumper are clearly visible.

Name	Description
Anode pins S_x	**2.54 mm strip – 32 pins.** Connection to ASIC input lines, to wire SiPM anodes. GND = ground
Cathode pins B	**2.54 mm strip – 32 pins.** Connection to High Voltage lines, to wire SiPM cathodes for biasing. NC = not connected
External HV	**LEMO HV.** External High Voltage input for SiPM biasing. Connection to SiPMs cathodes as shown in **Figure 10.6**. The external HV connector is always connected to the Cathode pins B
P2 Jumper	If inserted, connects the Cathode pins B to the DT5550W High Voltage generator

Table 10.2: description of the pitch adapter connectors.

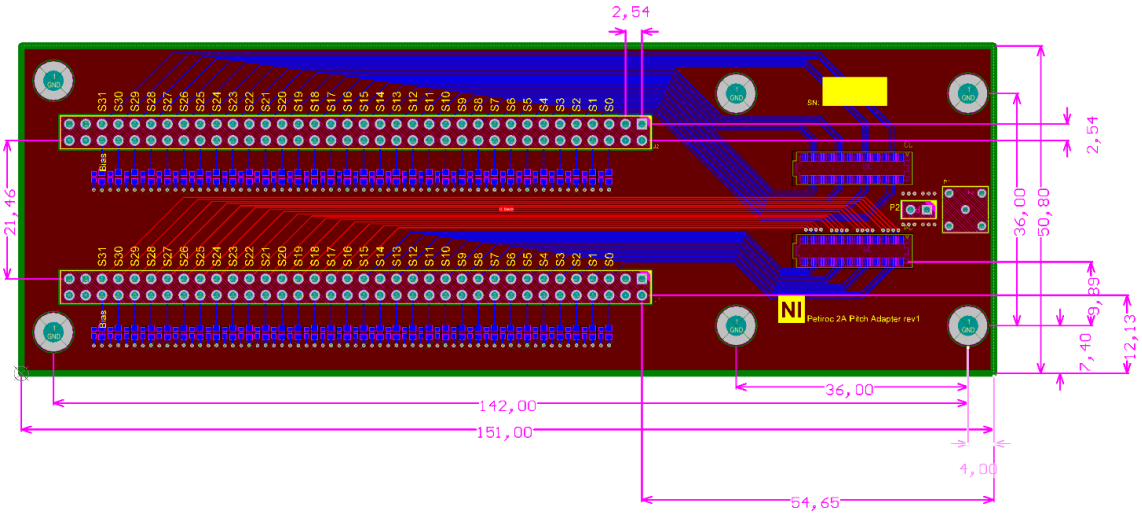


Figure 10.5: dimensions of the pitch adapter.

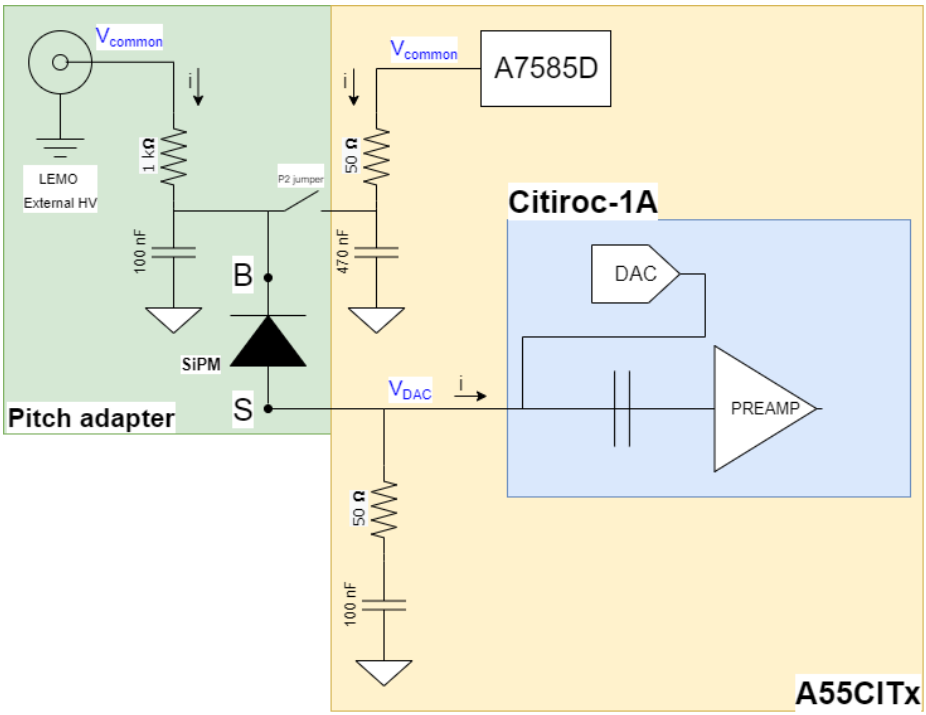


Figure 10.6: SiPM connection scheme to the ASIC and biasing lines when using the pitch adapter kit

Figure 10.7: Top: how to plug the pitch adapter on the board's SiPM connector. The connectors are pressure-pluggable. Bottom: general view of a DT5550W with A55CIT4 piggyback and two pitch adapters plugged in. In this configuration, all 128 channels of the DT5550W board are exposed on the strip connectors.

Temperature Feedback

Near each SiPM connector hosted on the A55CITx board, a temperature sensor is soldered. This sensor is read by the FPGA and the information is used by the DT5550W Readout Software for SiPM bias active compensation during temperature changes.

In case of using SiPMs mounted on an external PCB, it is recommended exploiting the USER I2C bus, available on the motherboard, to read out an external sensor (pinout of I2C on the PCB serigraphy). In this case, in order to use the active bias compensation as defined in the DT5550W Readout Software, the user needs a Texas Instruments TMP100 external sensor, configuring its address at 0x50, bit A0 = GND and A1 = 3.3V.

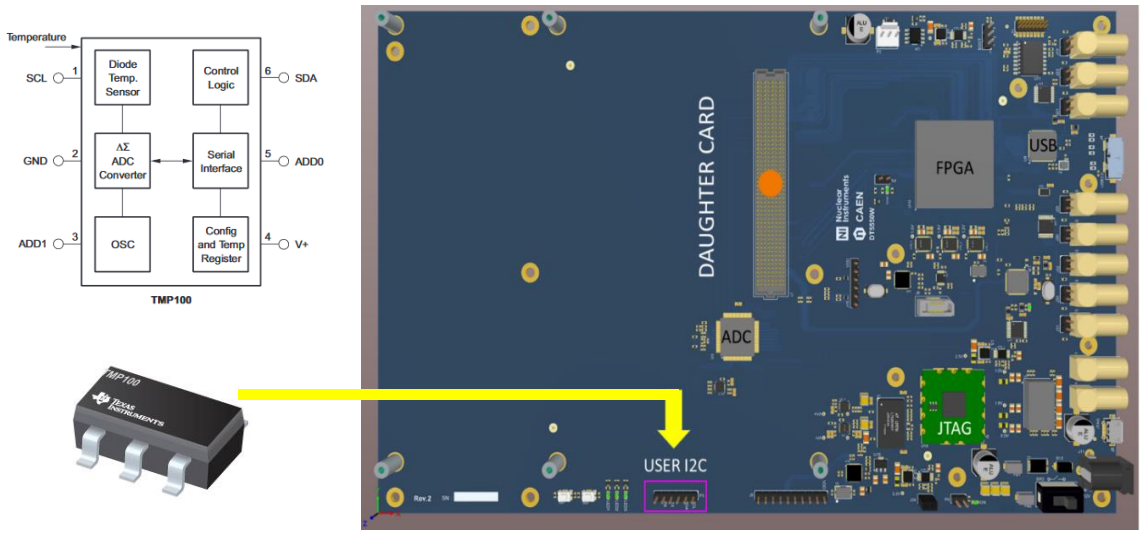


Figure 10.8: the user I2C interface on the motherboard, to be used for external temperature sensor connection.

In general, there are several methods to perform the active SiPM bias compensation, using:

- The average temperature read out by the two sensors soldered on the piggyback PCB, near the matrix connectors. This method is directly supported by DT5550W Readout Software.
- The temperature read by an external sensor. If using a Texas Instruments TMP100 with address 0x50, this method is directly supported by DT5550W Readout Software.
- A temperature read out with any other method (like thermocouples or similar sensors readout). The provided temperature can be passed to the SDK libraries for active bias compensation.

Test Pins

On the sides of each ASIC hosted on the A55CITx board, some test pins are available, to allow the user to debug the internal operation of the chip itself. The name of each pin is reported on the PCB serigraphy (see **Table 10.3** for more details)

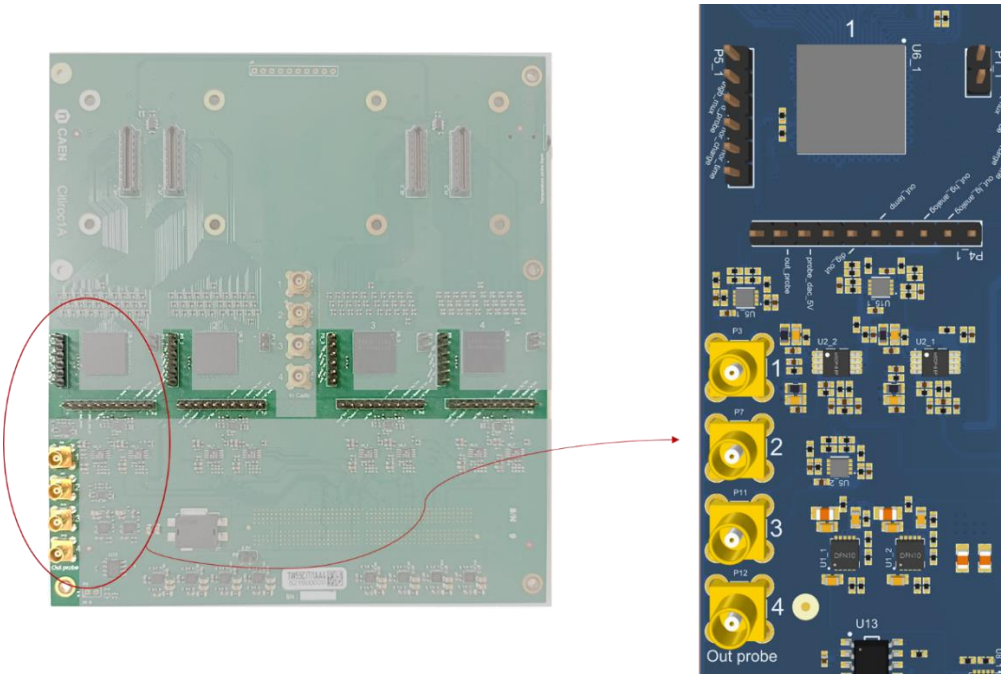


Figure 10.9: the test pins of A55CITx boards.

Pin name	Description
trigb_mux	**OR32 trigger**
d_probe	Internal probe managed by the software. For the selected channel it shows one of the following: • **High gain peak detector status** • **Low gain peak detector status**
nor_time	**NOR32 of the time triggers** (disabled by default, to reduce the noise during the readout)
nor_charge	**NOR32 of the charge triggers**
out_probe	**Analog monitor** probe (Function is software selectable) – refer to Par. **Monitor**
probe_dac_5V	**Input DAC** output channel 0 to 31
hold_lg	Analog memory Hold signal for low gain line
dig_out	**Triggers** multiplexed output
out_temp	ASIC internal **temperature sensor**
out_hg_analog	High Gain **Slow Shaper** multiplexed output
out_lg_analog	Low Gain **Slow Shaper** multiplexed output
Out Probe (MCX connector)	**Analog monitor** probe (Function is software selectable) – refer to Par. **Monitor**

Table 10.3: A55CITx test pins description.

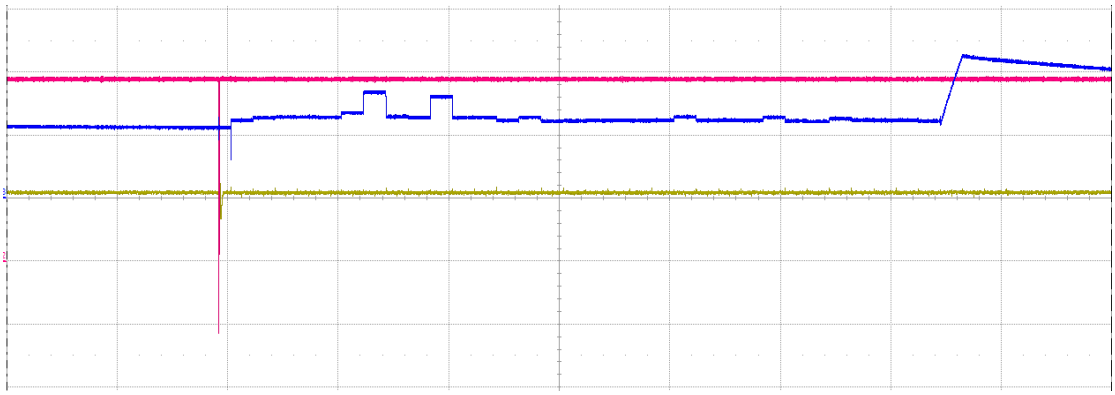


Figure 10.10: a typical debugging acquisition made at the oscilloscope using test pins. Yellow: Shaper output. Magenta: the NOR32 time trigger. Blue: Analog LG output.

Motherboard I/Os

When the A55CITx is mounted onto the DT5550W motherboard running the default firmware to manage the Citiroc-1A chips, the assignment of the 8 programmable LEMO I/Os on the DT5550W motherboard is also defined as shown in the following scheme.

Figure 10.11: the programmable LEMO digital I/Os of the DT5550W

LEMO	Description
A	**CLK IN** - accepts a 25MHz, 3.3V signal, 50 Ω input impedance.
B	**CLK OUT** - provides a 25MHz, 3.3V signal (can be used to drive a 50Ω coaxial cable).
0	RUN/START OUT
1	BUSY OUT
2	TRG OUT
3	T0 OUT
4	EXT TRG
5	VALIDATION/VETO IN
6	RUN/START IN
7	T0 IN

Table 10.4: assignment of the programmable LEMO digital I/Os in the default firmware for A55CITx management.

11 Functional Description

In the following chapter, operation principles and functional descriptions of the DT5550W+ A55CITx module are treated in detail.
The core of the board is the 2 Citiroc-1A ASIC chip **[RD1]**. Citiroc-1A is a 32-channel front-end ASIC designed to readout SiPMs for scientific instrumentation application. The ASIC allows the user to trigger down to 1/3 photo-electron and provides the charge measurement with a good noise rejection and 1% linearity up to 2500 photo-electrons. Citiroc-1A outputs the 32-channel triggers with a high timing resolution (better than 100 ps RMS), even though it does not have an internal TAC/TDC to acquire the timing measurement. However, the FPGA of the DT5550W is programmed for this purpose and a high resolution TDC (0.5 ns) was implemented to calculate the time distance (ΔT) between a reference signal and the input pulses.
The DT5550W embeds a programmable high voltage power supply (20 ÷ 85 V, 10 mA) for the bias of the SiPMs, featuring a feedback loop with the temperature sensor (internal or external) for the compensation of the gain drift. An individual adjustment of the high-voltage is possible using a DAC (internal to each channel) connected to the ASIC inputs, which gives the correction for the non-uniformity of SiPMs.

Citiroc-1A

The A55CITx is based on the functions and readout chains of the Citiroc-1A WeeROC ASIC. A scheme of the chip is given in **Figure 11.1.**

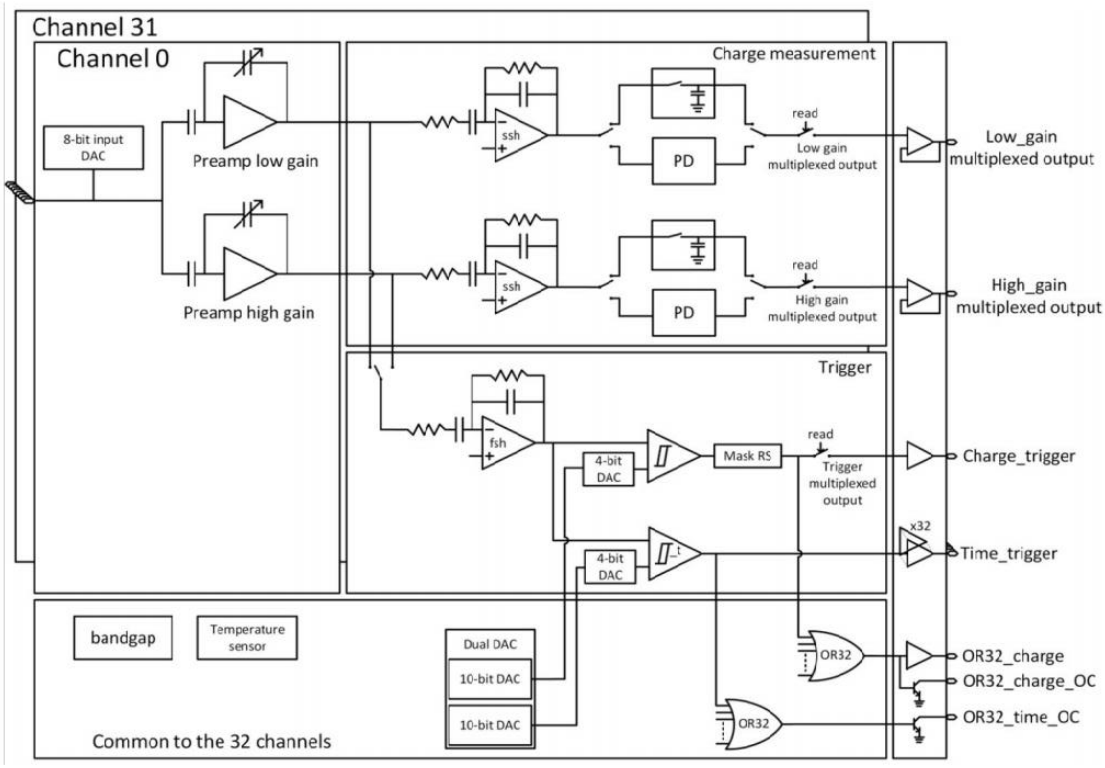


Figure 11.1: scheme of the CITIROC 1A ASIC.

Each of the 32 readout channels available in the chip integrates a classical readout chain made of Preamplifier (one for Low Gain and one for High Gain), Fast and Slow Shaper, a trigger line with a timing resolution better than 100 ps, a Peak Detector circuit and analog output MUX. Moreover, for each channel, a block for the fine bias regulation is available.

SiPM Gain Trimming

The A55CITx embeds a programmable high voltage power supply (A7585D) for the bias of the SiPMs. Moreover, each of the 32 Citiroc-1A inputs features a low power 4.5 V/2.5 V-range software programmable 8-bit DAC to finely adjust the SiPMs individual high voltage in order to correct for gain and noise non- uniformities of systems using several SiPMs.

Note: the value set for the voltage provided by the DAC (V_{DAC}) is subtracted to the common value of the HV:

$$V_{SiPM} = HV - V_{DAC}$$

The Citiroc-1A DAC can only operate as a current sink. It is therefore not possible to measure the DAC voltage by placing a multimeter between the channel pin (anode) and ground. Indeed, this procedure could damage the chip

Charge Measurement

Each channel of Citiroc-1A embeds two channel-by-channel independent programmable variable-gain Preamplifiers ensuring a wide coverage of the dynamic range. Both LG and HG Preamplifiers can be tuned according to the values of the feedback capacitance Cf, which can range from 25 fF to 1575 fF with a step of 25 fF (6 bits). Indeed, the voltage gain is given by the ratio Cin/Cf, with C in = 15 pF for the HG amplification chain and 1.5 pF for the LG one.

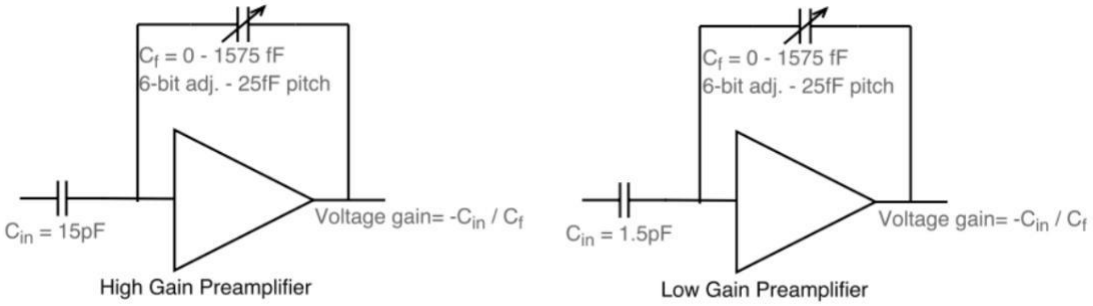


Figure 11.2: High Gain and Low Gain voltage sensitive Preamplifiers.

The amplification chain is then composed of two CR-RC^2 Slow Shapers that are respectively connected on the two Preamplifier outputs for each channel. The peaking time of each Slow Shaper can be tuned from 12.5 ns to 87.5 ns with a 12.5 ns pitch. The peaking time is common to all the 32 channels, even though it can be different between LG Slow Shaper and HG Slow Shaper.

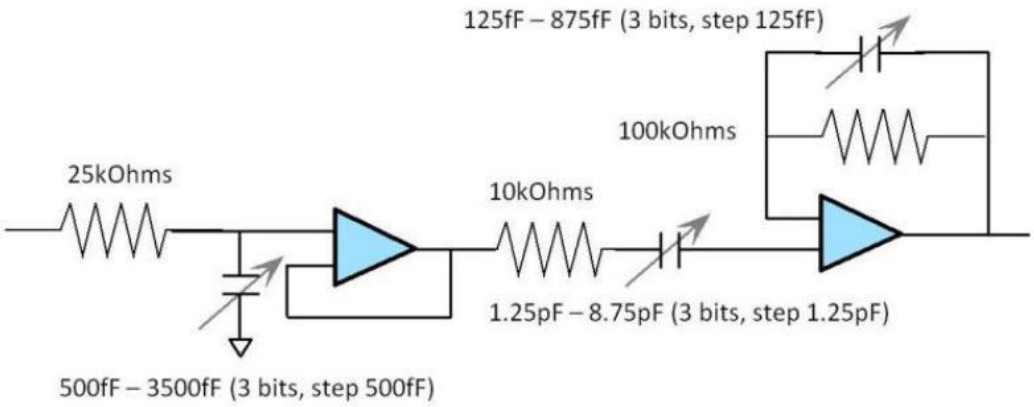


Figure 11.3: Slow Shaper schematic.

The amplitude of the signal from the Slow Shaper output is measured with a peak sensing system, called **Peak Detector**, that automatically stores the highest value of the Slow Shaper after being armed. The Peak Detector allows the user to get the maximum of the peaks for each channel even if those peaks are not precisely defined in time, for example if incident photons come with a delay from channel to channel.

Note: The charge measurement of Citiroc-1A in the A55CITx works with a bunch (global) trigger, either external or generated by a combination of channel individual triggers. As soon as a trigger is issued, all channels start the peak sampling.

The energy of the signal is basically measured basing on the slow shaper output with a **peak sensing** system.

Two peak sensing systems are embedded for each shaper: a **peak detector** that automatically stores the highest value of the slow shaper after being armed, and a **track and hold** that requires an external hold signal at the peaking time. They cannot run concurrently and a slow control bit allows choosing between the two. The selection of the peak sampling solution is independent between low gain and high gain and is common for the 32 channels. The choice of the best peak sampling solution depends on the final application:

- **Track & hold** is more suitable for events where photons are all detected at the same time (few ns spread)
- **Peak detector** is more suitable for events where photons are spread in time (several 10 or 100ns)

The **track & hold** cell of each gain line is controlled by a hold signal. The hold signals must remain high (in hold mode) until the read-out sequence has been completed. The hold signal is active on level.

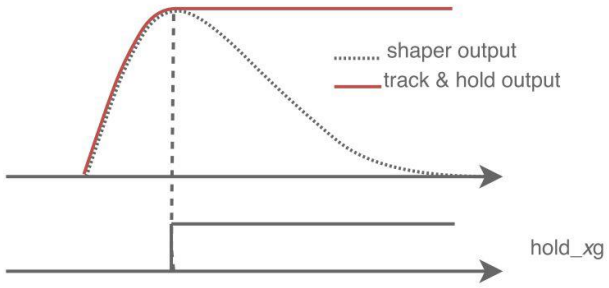


Figure 11.4: the Track&Hold operation in CITIROC 1A ASIC.

It possible to use a **peak detector** to sample the maximum of the shaped signal, in alternative to the track and hold. The peak detector acquisition sequence works in 3 phases:

1. **OFF Phase**: before any trigger, the peak detector is turned off. Upon trigger, the peak detector switches to Peak Sensing Phase.
2. **Peak Sensing Phase**: in this mode, the peak detector memorizes the maximum of the input signal. That mode is kept until the internal logic provides a rising edge on the Hold signal, as it is shown in Fig. **7.5**, the Peak Detector switches to Hold Phase when that signal occurs. The time distance between the trigger and the Hold signal is defined by the Hold Delay parameter (programmable).
3. **Hold Phase**: The rising edge of the Hold signal causes the disconnection of the input of the Peak Detector from the Slow Shaper and ensures that no other input signal is memorized. That phase is used during the serial read-out of the ASIC. The falling edge of the Hold signal will cause the release of the Hold Phase and the Peak Detector will switch back to the OFF Phase for the next acquisition.

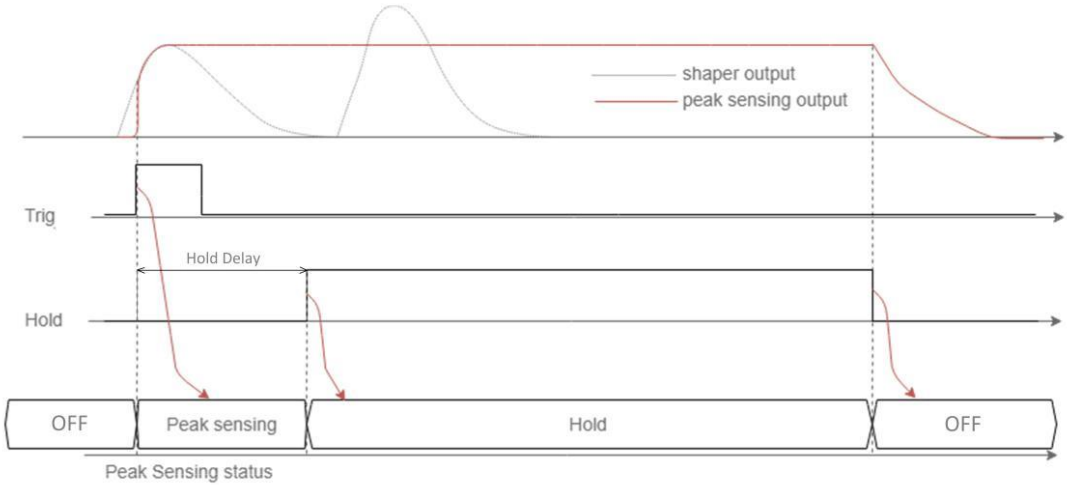


Figure 11.5: Peak detector chronogram.

A proper setting of the Hold Delay parameter is fundamental in order to acquire a correct value for the peak amplitude of the pulse. Indeed, if the trigger arrives too late (beyond the peaking time of the Slow Shaper), the Peak Sensing Detector stores a lower value of the signal. The peaking time of the Slow Shaper depends on the shaping time set but is typically less than 100 ns, so the trigger latency must be small. If, however, the trigger arrives significantly earlier, then it is important to set a Hold Delay value high enough so as not to risk stopping the Peak Sensing Phase when the signal has not yet reached the peak.
To understand how to properly set the Hold Delay parameter, two ways are viable:

- Look at the oscilloscope the Trigger, Hold and Slow Shaper signals and measure the time distance between the Trigger signal and the Slow Shaper peak.
- Perform an Hold Delay Scan

ASICs like Citiroc-1A have not an integrated ADC, they just perform a peak detection operation on each channel. The two analog charge measurements (one from the LG amplification chain and one from the HG amplification chain) from each channel are sent out (via FPGA command) in parallel. The charge measurements from each channel (32 for each Citiroc-1A chip) are then sequentially multiplexed on a single analog output (see **[RD1]** for more details).

Discriminators

Citiroc-1A is an analog ASIC and there is no auto-trigger capability with it. The trigger going out of Citiroc-1A can eventually be sent to a DAQ system where a decision to convert the event in digital or not can be taken (otherwise a trigger external to the Citiroc-1A can be used). The Citiroc-1A trigger chain can be connected either to the LG or to the HG Preamplifier depending on the requested level of trigger. The trigger chain is then composed of a 15 ns peaking-time Fast Shaper which directly receives the signal from one of the two Preamplifiers for each channel.

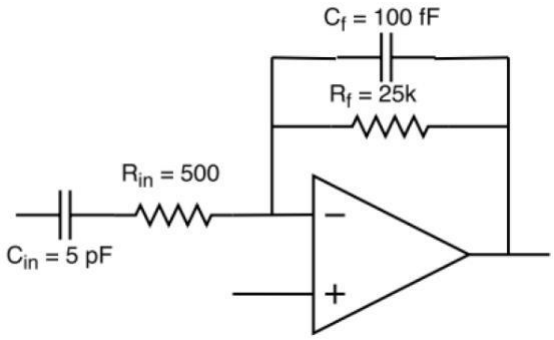


Figure 11.6: Fast Shaper circuit scheme.

The output of the Fast Shaper is fed into two discriminators:

- The **Charge Discriminator** (QD) which provides an ASIC level trigger which is the logic OR of the enabled channels (Q-OR). The Q-OR signal toggles at the first QD trigger. Every time an A/D conversion sequence is started, the logic status (high or low) of the QD trigger of each channel is also transmitted and saved to the data packet, thus allowing the user to determine which channels triggered in the QD line.
- The **Time Discriminator** (TD), which provides accurate event time information on each channel. The 32 discriminator outputs are available on 32 digital outputs connected to the FPGA. The lines are then used for the generation of a bunch trigger signal from a logic combination (AND, OR, custom) of the channel self-triggers and for Photon Counting

More details on the trigger chain of the Citiroc-1A can be found on **[RD1]**

The QD and TD thresholds are common for the 32 channels and are set by two 10-bit DACs. A 4-bit DAC on each discriminator allows adjusting each of the 32 thresholds individually to compensate for non- uniformities

Test Pulser

A test input can be enabled for each channel of the Citiroc-1A chip and can be used for test and calibration purpose. The pulse can be injected using the available In_Calib MCX connectors, one for each ASIC mounted on the A55CITx board (see **Hardware Description**).

The injection test capacitance value is 3 pF and there is no difference between the LG and HG stage when using the test pulse, since the two input capacitors (1.5 pF and 15 pF respectively for LG and HG Preamplifier) are by-passed. The user can select to which channels the test pulse should be transmitted at the same time, by using the Test LG/HG slow controls available in the Readout Software (refer to Par. **Channel specific settings**). Moreover, the test pulse can be transmitted to the LG Preamplifier, to the HG Preamplifier or to both.

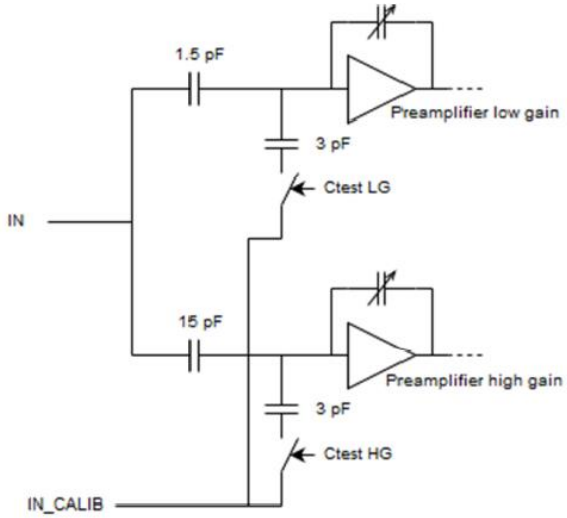


Figure 11.7: the In_Calib circuit

Note: WeeROC suggests connecting the test pulse to one channel at a time **[RD1].**

ASIC Trigger Operation

The CITIROC trigger chain can be connected either to the low gain or the high gain preamplifier depending on the requested level of trigger. The chain is composed of a fast shaper followed by two discriminators:

- The first, defined as “charge discriminator”, provides the trigger (OR32) and is also used for the “hit register”. Discriminator outputs provide an ASIC level trigger (OR32) which is a logic OR of the 32 channels. The OR32 signal toggles at the first charge discriminator trigger. Charge discriminator outputs can be latched by slow control command (“RS_or_discri”). The reset of the latched (if used) triggers is performed by the LVDS signal “Raz_Chn”.
- The second, defined as “time discriminator”, provides the event time information on each channel. The 32 discriminators outputs are available on the trigb[0-31] digital outputs. The logic NOR of the 32 time discriminator is available as an open collector digital output on pin NOR32t_oc.

A 15ns peaking-time fast shaper can either be connected to the high gain preamplifier or to the low gain. That connection is set by slow control. The fast shaper peaking time and gain are not programmable.

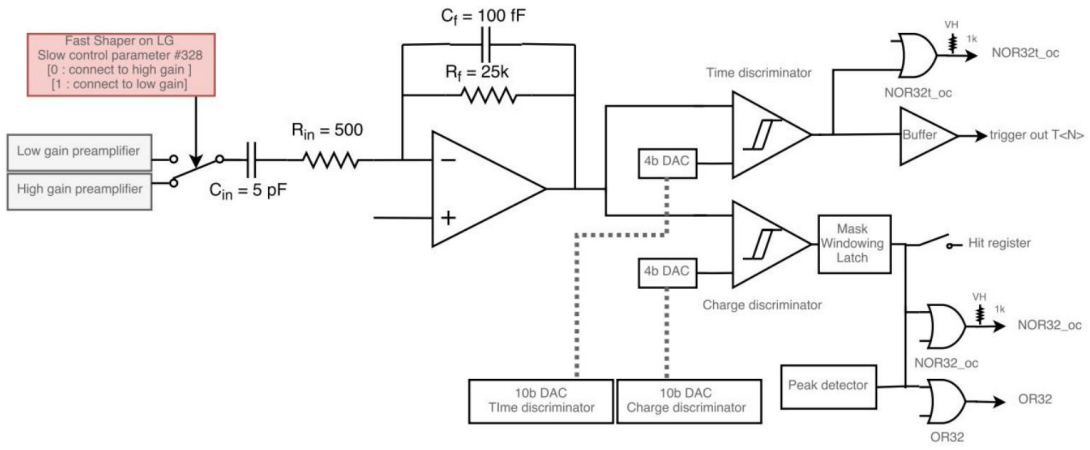


Figure 11.8: the Citiroc-1A trigger scheme

The time trigger is provided externally to the ASIC in order to start the acquisition. NOR time and charge trigger are internally connected to readout circuit. The FPGA uses the trigger information to lock the Peak Stretcher / Sample & Hold and start the readout procedure. The time trigger is also used to perform an accurate timestamp measurement on each channel.

The time trigger signals are given as output on 32 independent lines; the charge trigger information is stored in a register, called HIT, which can be read after each recorded event to know which channels effectively caused the trigger.

The charge trigger can operate in latched or non-latched mode. In latched mode (as set in the default firmware) the trigger signal is stored in a flip-flop until the reset event. The reset can be performed manually through a dedicated reset line (RazChn) or automatically at the end of the acquisition (this latter option is set in the default firmware). In non-latched mode, the comparator output is directly connected to the output pin. This is useful to count the exact number of trigger hits on each channel. Latch is mandatory to obtain the HIT information.

The charge discriminator is followed by a logic system as shown in **Figure 11.9**. That logic system allows the following choice:

- **Mask a channel**: allows inhibiting a charge discriminator channel by channel to quiet a noisy channel for example. That parameter is programmed by slow control.
- **Enable/inhibit trigger during a specific period of time**: that LVDS signal allows enabling all the triggers during a specific time window only if the user know when an event is supposed to occur for example. The signal name on the pin list is ValEvt [ValEvt_p / ValEvt_n].
- **Latch the discriminator output**: allows latching the discriminators output to memorize the trigger status. Triggers can be reset with the RazChn LVDS signal to be ready for the next event(RazChn_p / RazChn_n). Charge discriminators must be latched to use the hit register and shall only be reset after the read sequence.

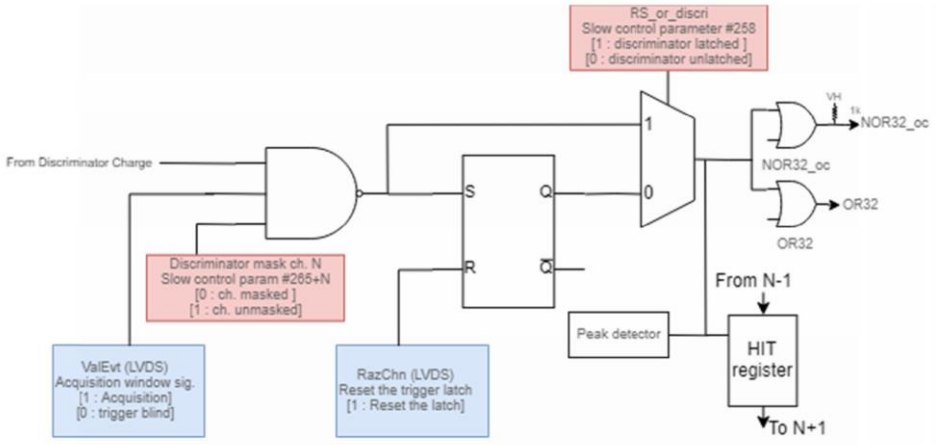


Figure 11.9: the Citiroc-1A charge triggering logic system

Many trigger signals are available at the ASIC outputs and are sent to the DT5550W FPGA, to select some events and reject other ones, basing on a trigger logic. The available triggers are:

- **32 independent time triggers**, one for each channel of the ASIC. The trigger is high when the inverted signal coming from the preamplifier exceed the set trigger threshold. Basing on the input signal polarity, the trigger operates on the rising or falling edge. The time trigger threshold is composed of a coarse part, common to all channels, and a fine part which is adjustable independently for each channel. The time trigger can be vetoed for each channel. In this case the trigger signal for the specific channel is not sent in output and it does not participate to the OR32 logic among the channels. It is possible to disable the trigger outputs on the ASIC pins to reduce the noise but to let them participate to the OR32 logic.
- **NOR32 time trigger.** It is the OR32 of time triggers in inverted logic. It is available as output of the ASIC and it is used internally to generate the “hold” signal to extract the charge information
- **NOR32/OR32 charge trigger.** It is the OR32 of charge triggers in inverted logic. The individual charge triggers are not available as output at the ASIC pins. Only the OR32 is available.
- **Charge Trigger MUX.** It is not a real trigger but a shift register, which contains the independent charge trigger of each channel for the last acquired event. In output, the 32 bits indicating the channels causing the charge triggers are available.

The general trigger of the chip is given by one of the OR signal and validate the acquisition of the event. Upon validation of the event, the FPGA will start the read-out sequence using the serial output read-out providing in parallel the low gain analog value, high gain analog value and trigger status of each channel sequentially. CITIROC 1A will be blind during that read-out sequence.

Default trigger logic

The default trigger logic is implemented in the FPGA firmware of the DT5550W, as shown in **Figure 11.10**. It is possible to set each ASIC to trigger independently using time/charge triggers, or use a global board trigger that is the OR of all the possible triggers (internal, software, external , etc.).

It is also possible to put in logic AND couples of even-odd adjacent channels (0&1, 2&3, …) to perform coincidences

The external trigger can be fed at LEMO4 of the DT5550W motherboard. It can be used for three main purposes:

- verify the ASIC operation without any signal
- pedestal measurements
- imaging trigger for multiple ASICs and boards

The pedestal measurement is fundamental for the ASIC channels equalization. The ASIC can be triggered by an internal generator with programmable frequency (1 kHz by default). At this point, the transferred data are useful to measure the baseline in absence of any input signal.
The imaging trigger is important to tune energy measurements on multiple pixels. For example, we can consider a SiPM matrix connected to two ASICs. If the light on a pixel of the matrix is very low but enough to cause a trigger, for instance, on ASIC 1, also the adjacent pixels will count some charge even if the signal is too low to cause a trigger. Some of these pixels could be connected to ASIC 2 and will be readout since the channel trigger cause the entire ASIC to be readout, while pixels connected to ASIC 2 will not be readout and, therefore, some information are lost.
The imaging trigger, when enabled via software, propagates the trigger generated by an ASIC to all the other ASICs and to other boards, allowing the readout of the entire sensor connected.

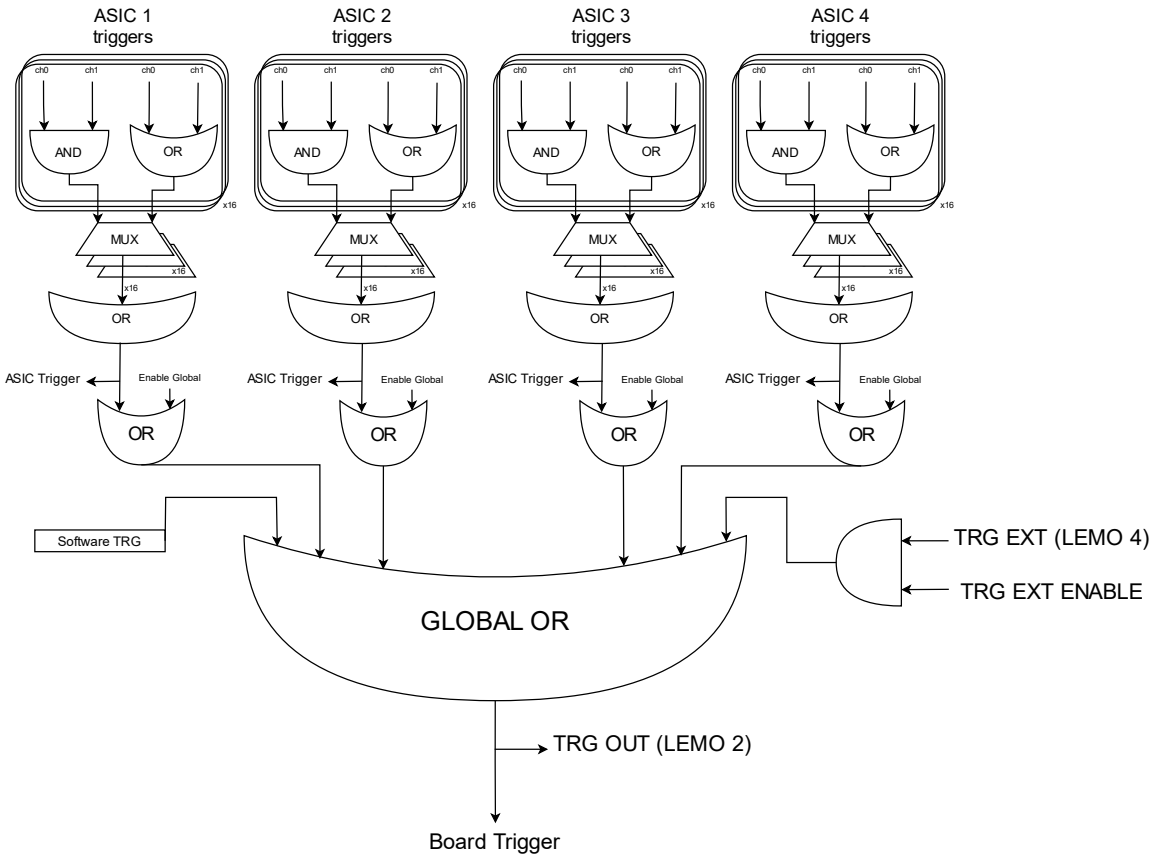


Figure 11.10: scheme of the triggering logic set in the default firmware loaded on DT5550W for A55CITx management.

Veto and validation

In addition to this triggering scheme, it is possible to **veto** some one or more of the ASIC trigger (named as 1,2,3,4) or use an external veto to be fed at LEMO 5 of the DT5550W. This option is enabled by software, as explained in Par. **Trigger.**

It is also possible to enable a **validation** mode. This option allows to mark as validated only the events that are flagged by a low-to-high transition or by a high level level on LEMO 5 of the DT5550W. When the validation mode is enabled, external veto is automatically bypassed and overridden by the validation system behaviour.
Validation mode useful in that situations where you have an external trigger (i.e. a large scintillator) but the processing time for the discriminated signal is too high to drive the external trigger. In fact, in order to capture the peak of the Citiroc-1A slow shaper, an external trigger should feed LEMO 4 after a maximum equal to the slow shaper shaping time with respect to the incident light on SiPMs. With the fastest shaper, this time should be smaller than 12.5ns while with the slowest about 87 ns. This time is too short even for a simple coincidence, considering the propagation delay through cables. The validation mode, instead, allows the system to capture the peak as soon as the internal trigger is fired but the event will be flagged as fake or discarded if the validation does not come within the validation window that can be up to 500 µs. During the validation period, the readout of the ASIC is altered with respect to normal readout. In particular the peak stretcher is frozen with the selected internal trigger, but the readout process is not started until validation. If validation does not come within the validation window, the conversion is aborted, otherwise the packet is transferred to the PC with a flag to identify validation.

Validation can be configured to happen on a High Level (LEVEL H) or on a Low-to-High transition (Edge Pos):

- when LEVEL H is selected, an event is validated whenever the signal on LEMO 5 is logic high
- if Edge Pos is selected, an event is validated whenever LEMO 5 receives a rising edge after 16 ns from the external trigger and before the end of the validation window.

There is an option discard events that are not validated within the validation window. A trace of them is preserved in the *trigger id* and *Validation id* fields that are transferred in each event packet (refer to Chap. **Firmware** for more details). If the option is not selected, the event is converted and transferred even if it is not validated. In this case the event is flagged as not validated in the *flag* field of the packet and the not-validated event counter is increased.

Readout Modes

The Citiroc-1A readout can be performed in two ways (both implemented in the default firmware):

- **Photon Counting**: only the trigger lines are used, in non-latched mode, to count the number of trigger transitions (i.e. the number of events) on each ASIC channel. When using this readout mode, the ASIC clocks are switched off.
  This allows to count events with a frequency of more than 10 MHz

- **Analog Multiplexed Readout – Pulse Height Analysis**: the time trigger lines can be used to implement in the FPGA a trigger logic which is able to select some events. In alternative, if the accurate the time measurement is not important, the time trigger lines can be disabled and only the NOR32 charge trigger can be used to analogically readout the ASIC. This latter way of operation, together with the clocks disabling, minimize the noise and maximize the energy resolution. When using the analog readout, only some dedicated analog lines of the ASIC are used and the charge measurement is performed using the external ADC hosted on the DT5550W motherboard.
  This allows to read out up to 40 kHz/channel.

Photon Counting

If the charge information is not required, it is possible to work in photon counting mode.

In this mode the firmware just counts the transitions of the channel triggers: the ASIC works in fully asynchronous mode and no internal ADC/TDC is enabled. Only the ASIC fast shaper and comparator are used. It is possible to use the photon counting mode to read out the number of photons per channel from the beginning of the run and extract a list (energy of a series of events) in a specific integration window opened by a start signal. The start signal could be generated by an internal periodic signal or by an external signal provided at LEMO6 Run/Start. Our suggestion is to set this window width between 100ns and 4s. The internal start signal frequency could be set between 1Hz and 1MHz.

The readout scheme in photon counting mode is shown below.

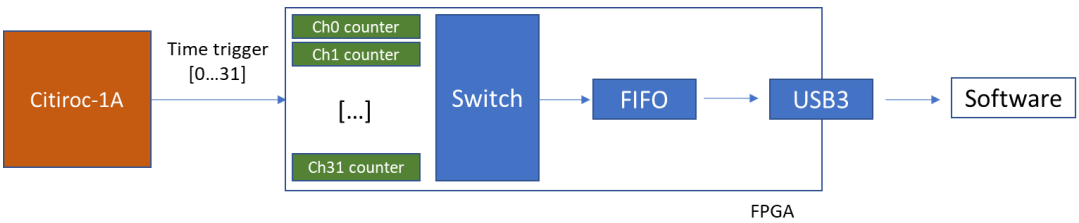


Figure 11.11: readout scheme of DT5550W and ASIC operating in photon counting mode.

Analog Multiplexed Readout

The CITIROC 1A can be read out using its analog multiplexed output through the external 80 MS/s, 14-bit ADC, which is mounted on the DT5550W motherboard. This ADC has 8 channels: the odd channels (1,3,5,7) are connected to the "*charge_hg"* output of the ASICs while (2,4,6,8) are connected to "*charge_lg"*

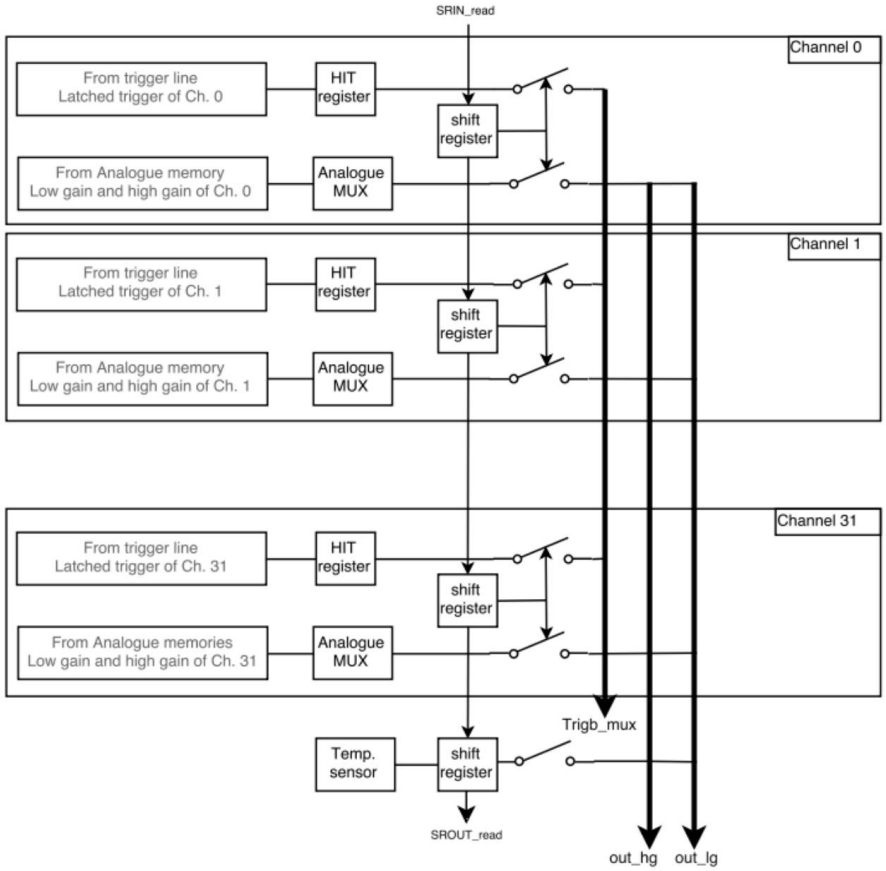


Figure 11.12: the analog readout scheme of CITIROC 1A, where multiplexed data are available as output.

On the "*out_charge_mux"* and "*Trigb_mux"* outputs are available, for all channels, the charge and trigger values stored by the ASIC for the latest event. These data are read out thanks to a shift register which selects a channel at each subsequent clock cycle. There are two digital lines to control the analog shift register:

- *SRIN_read*: user must load a '1' at the beginning of the read procedure to select the first channel
- *Ck_read*: user must generate a few clock cycles equal to the number of channels plus one to shift out the analog information.

The charge analog information is provided on the *out_charge_mux* output. At the same time, on the *Trigb_mux* output, the multiplexed triggers are available, providing a coarse timestamp for the correspondent charge events.

In analog readout mode, the FPGA uses a 0.5ns resolution TDC to extract the event timecode

The analog data conversion is done on the DT5550W motherboard by mean of the 80 MS/s, 14-bit ADC. The charge data are correlated to the channel knowing the number of clock cycles generated from the beginning of the readout process.

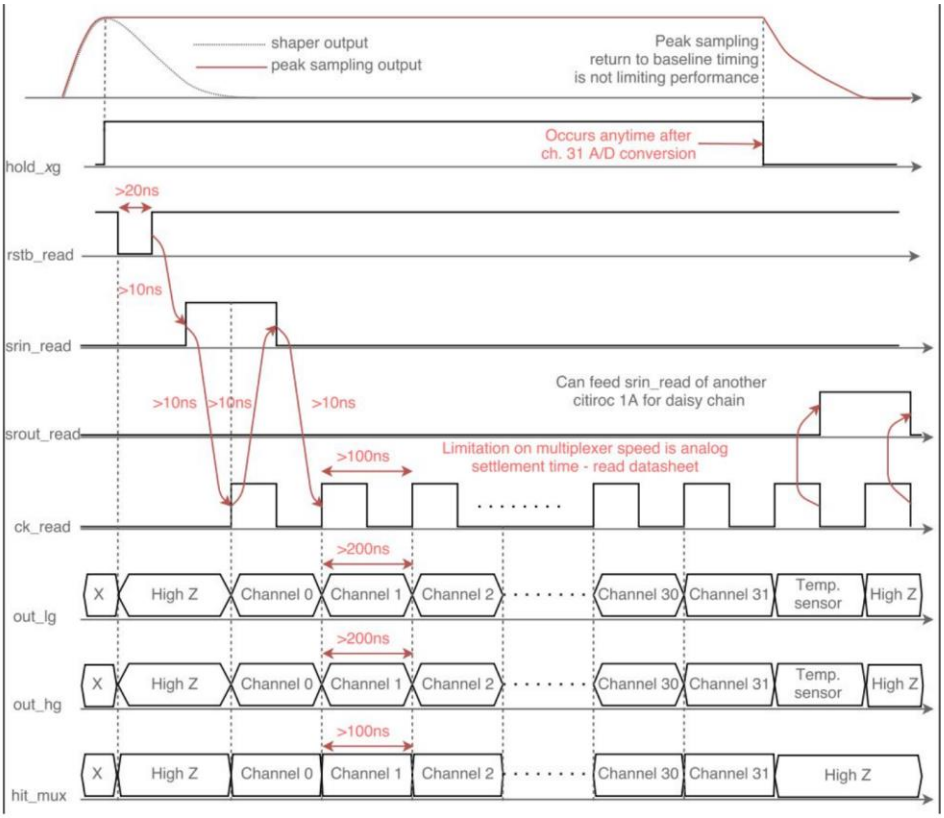


Figure 11.13: scheme of the analog multiplexed readout process

ASICs configuration

The configuration of all the ASICs hosted on the piggyback board is managed by the DT5550W Readout Software, which allows the user to easily set some of the ASICs parameters.
The ASIC is configured via a shift register with 1144 bits. Some parameters are preconfigured, to make the board working correctly in analog readout mode. In any case the Readout Software is distributed as open source code and the user can modify it to access the configuration bits which are not accessible from the software GUI (refer to **[RD1]** for a detailed description of each bit).

The configuration is generated directly by the Readout Software, as a bitstream representing the sequence to be loaded in the ASIC. The bitstream is transferred via USB bus from the PC to the FPGA, which stores it in 32-bit registers; at the beginning of the programming sequence, the FPGA sends the stream to the ASIC to configure it. The FPGA and the Readout Software allows to manage independently the configuration of each ASIC.

12 Firmware and data format

The default firmware version preloaded on DT5550W for A55CITx piggyback allows to perform the following operations:

- Citiroc-1A parameters configuration
- Configuration of the triggering logic as per the scheme in **Figure 11.10**:
  - ASICs trigger signals (by default OR32)
  - External Trigger
  - Veto
  - Validation
- Readout of energy from Citiroc-1A
- Event timestamping
- Photon Counting
- T0/Veto management
- Channel rate measurements
- Data transmission through USB 3.0

Data are transmitted in packets coming from each ASIC. Each packet from each ASIC has the following structure.

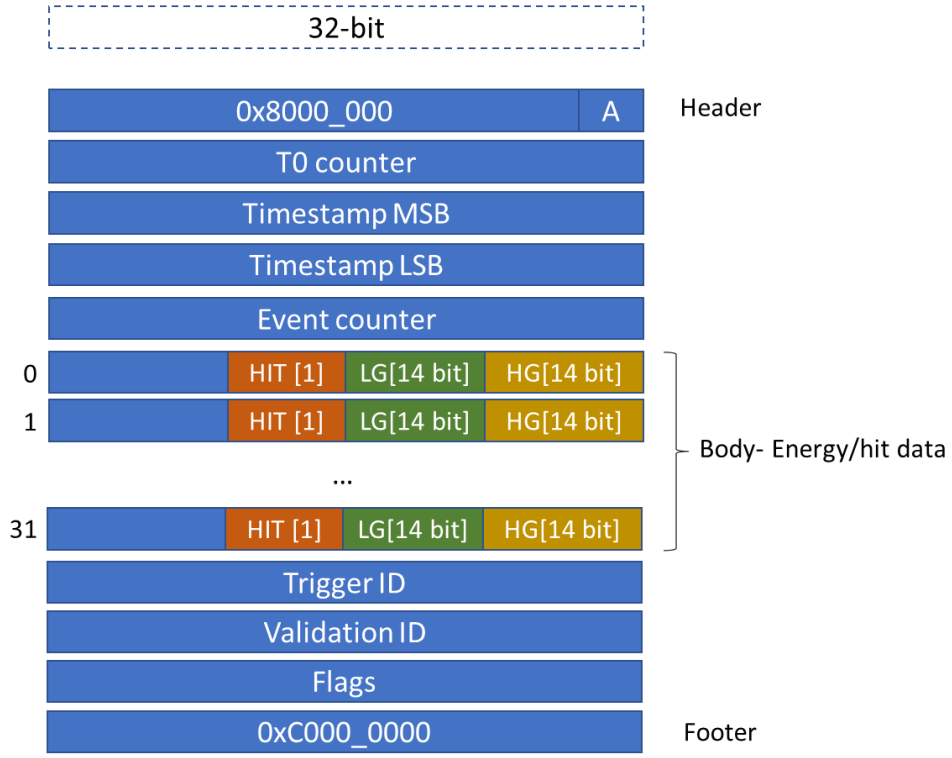


Figure 12.1: structure of the data packet sent to the PC using the default firmware.

- The *header* is used to validate the packet: in absence of the header 0x8000_000, the packet must be discarded. The letter *A* is identifying the ASIC from which the data are coming [A,B,C,D]
- *T0 counter* is the number of T0 cycles
- the *Timestamp* is the time code from the last T0, transmitted as MSB and LSB
- *Event counter* is a common counter to all ASICs and indicates the number of packets sent from the beginning of the run
- The body contains data coming from the ASIC, including Hit flag, Low Gain Energy and High Gain Energy for each channel of the ASIC
- *Trigger ID* is the number of triggers that the specific ASIC generated from the run start up to the moment when the specific packet has been generated (that means when the tigger fired). If global trigger is selected this number should be equal for all ASIC otherwise each ASIC will have an independent value
- *Validation ID* is the value of the validation counter captured when the packet has been generated starting from the start of the run. This counter does not count validated events but the Low->High transitions of the External Validation signal (LEMO 5). The number of this counter can be used to keep synchronization between external

detectors that are triggered by the validation signal, because *validation ID* will be increased even if the ASIC does not trigger on any event. *Validation ID* increases even if the event is not transferred to the PC.

- *Flags*:
  - 0 - validation is off – event validated
  - 1 - validation is on – event validated
  - 2 - event not validated (internal trigger fired but no validation in the validation window)
  - 3 - Fake event (validation event when no internal trigger has been fired in a validation window time before the validation event)
- The *footer* is used to validate the packet: in absence of the footer 0xC000_0000, the packet must be discarded.

Note: the firmware is provided as open source SCI-Compiler project. The user can modify this firmware or write his own code, with the help of SCI-Compiler. The upgrade of the firmware on DT5550W FPGA, can be performed via SCI-Compiler or through the OpenHardwareProgrammer tool. Refer to **[RD2]** for more details.

13 DT5550W Readout Software

DT5550W Readout Software is a **free and open-source** software developed for **Windows OS** to operate **in conjunction with the default firmware** of the DT5550W, in order to provide a ready-to-use solution. The software is common for all A55xxxx piggyback models.

Note: The software is distributed both as compiled application on the CAEN website and as source code. The source code is available at https://github.com/NuclearInstruments/DT5550W. It is written in VB.NET and C# and it can be easily customized by the user to adapt to a custom firmware and for any other need. In order to recompile the DT5550W Readout Software, a free version of Visual Studio .NET 2015 or later must be installed on the user's PC.

Note: the general functionalities of the software are described in DT5550W User Manual **[RD2]**. In this Chapter we recall them briefly and go into more details with the specific functionalities for A55CITx piggyback

The DT5550W Readout Software allows for:

- Simultaneous readout of up to 4 Citiroc-1A ASICs
- Triggering scheme setting
- Parameters scan
- Energy measurements
- Time of flight measurements
- Photon Counting
- Online Cluster reconstruction between multiple ASICs, based on timestamp
- Imaging
- Energy and time spectra plot
- Event list mode readout (energy, time, position)
- Monitor of the analog signals
- High Voltage management
- Data saving in binary and ASCII format

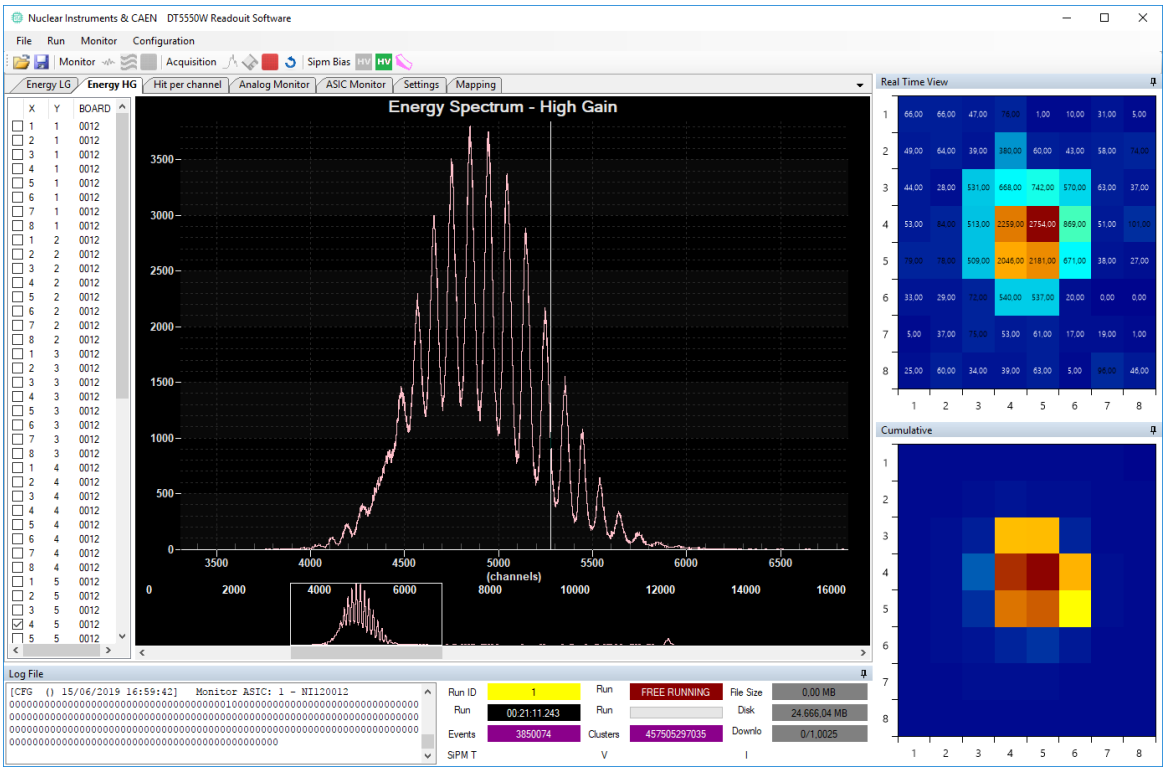


Figure 13.1: general view of the DT5550W Readout Software. In this example, a spectroscopy and imaging acquisition is being performed with A55CIT2 board, using a 64-channel SiPM matrix.

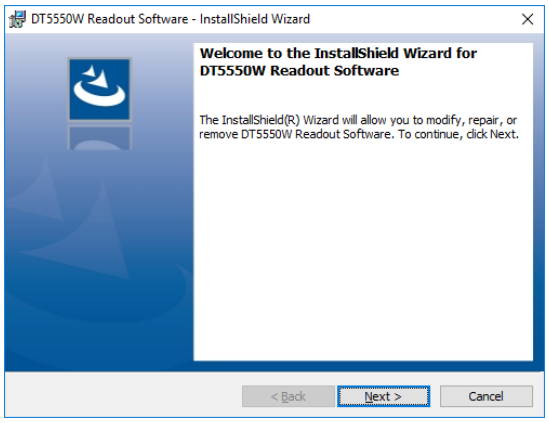
Software installation

DT5550W Readout Software is compliant with Windows 10-64bit

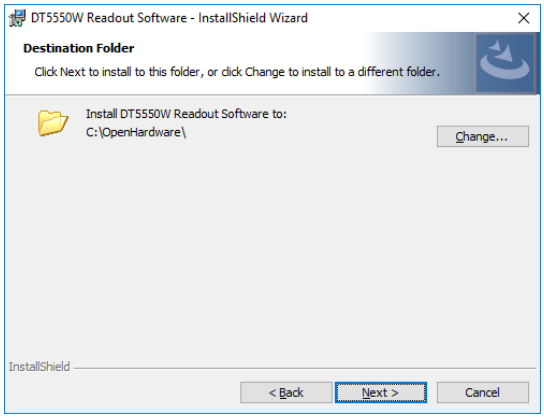
Note: The software is standalone and does not require the prior installation of any library

In order to install the DT5550W Readout Software, follow the steps below:

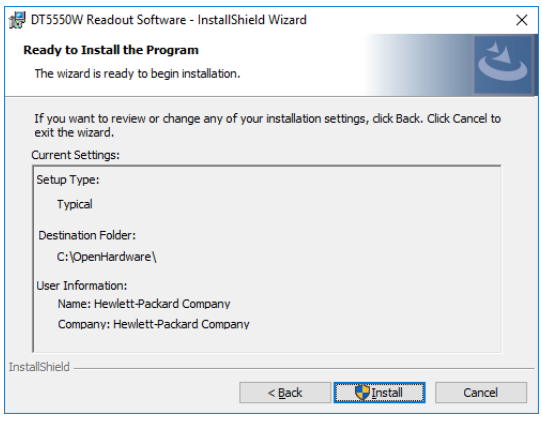
- Download the software package from the DT5550W product page on the CAEN website (**login required**)
- Unzip and run the executable as administrator.
- A setup wizard will start. **Press "Next" to continue.**



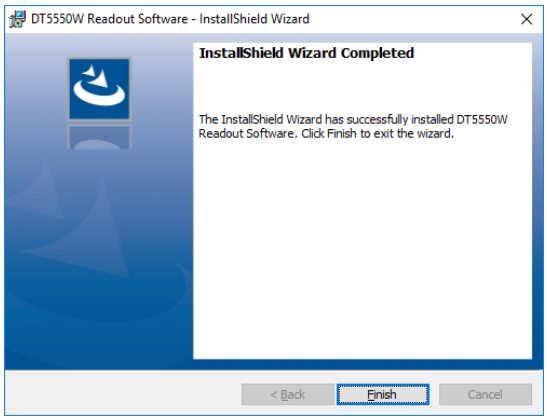
- Choose the destination folder and **press "Next".**



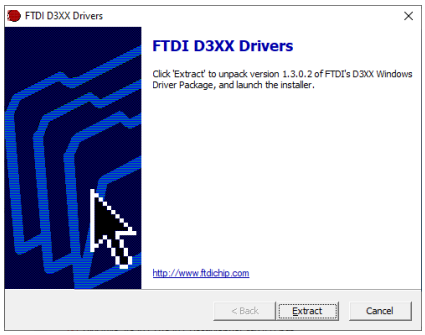
- **Click "Install"** to complete software installation.

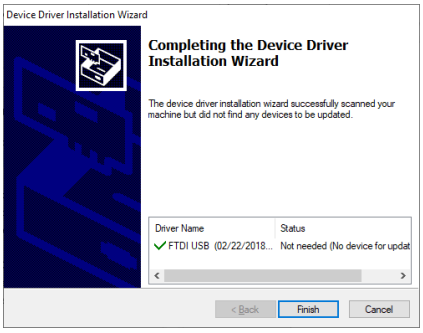


- Wait until installation is completed and press "**Finish**" to complete the setup.



- Follow the instruction to install the FTDI USB drivers





- Now it is possible to launch the DT5550W Readout software from the Windows programs menu.

Board Connection

After launching the software, the “Connection” window will open, and the user is asked to connect a board specifying the connection parameters:

- *Device*: select the PID/Serial Number of the DT5550W to be connected
- *ASIC model*: select Citiroc. In *Auto* mode, the software automatically detects the ASIC type
- *ASIC count:* specify the number of ASICs on your A55CITx. In *Auto* mode, the software automatically detects the number of ASICs mounted on the piggyback board.

Note: the software does not support connection to multiple boards: multiple instances of the software must be opened to manage acquisitions on each board.

Press *Connect* to establish a connection with the specified parameters and *Refresh* to update the list of devices listed in the Combo box.

Figure 13.2: the "Connection" window at start-up of the DT5550W Readout Software

Software GUI Description

Menu and Control Toolbar

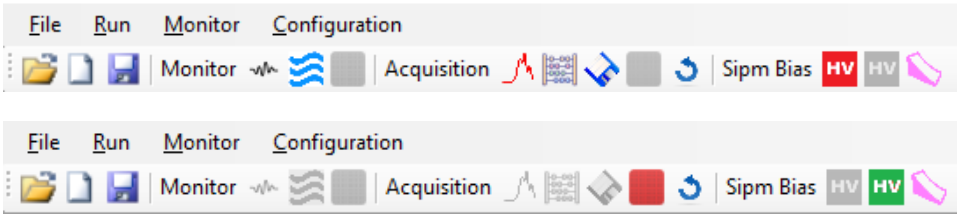


Figure 13.3: the Menu and Control Toolbar of the DT5550W Readout Software, before (top) and during (bottom) acquisition.

The *Menu and Control Toolbar* contains the following buttons:

- Open: open a configuration file
- Save: save a configuration file

Monitor (Oscilloscope acquisition configuration)

- Single Shot: acquire a single waveform in the oscilloscope
- Wave: start continuous acquisition of waveforms on the oscilloscope
- Stop: stop the oscilloscope acquisition

Acquisition

- *Spectrum*: start **Spectroscopy acquisition** according to the ASIC settings (no data saving)
- *Abacus*: start **Photon Counting acquisition** according to the ASIC settings
- Save: start energy/time or photon counting acquisition according to the ASIC settings and dump data on file.
- Stop: stop current acquisition
- Reset: reset the online spectra

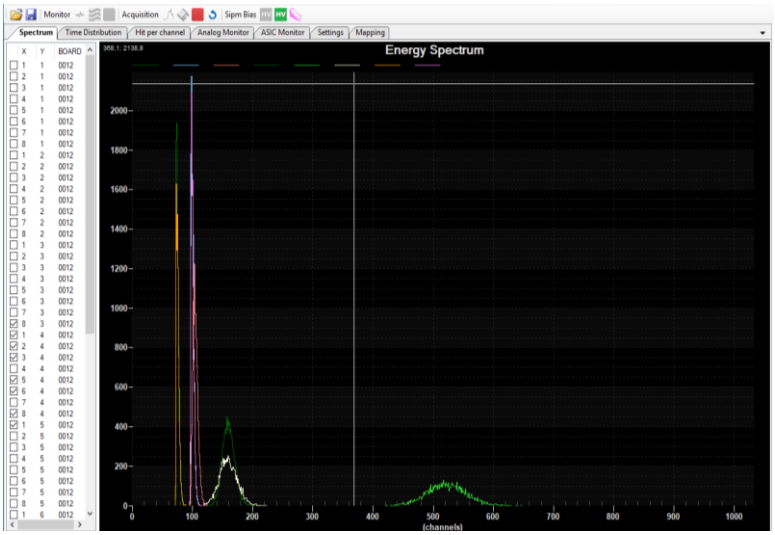
SiPM Bias

- Turns ON/OFF the SiPM Power Supply. The Voltage is selected in the *Settings* tab. It is not possible to change the Voltage status during acquisition.
- *Ramp icon*: open the channel counts monitor

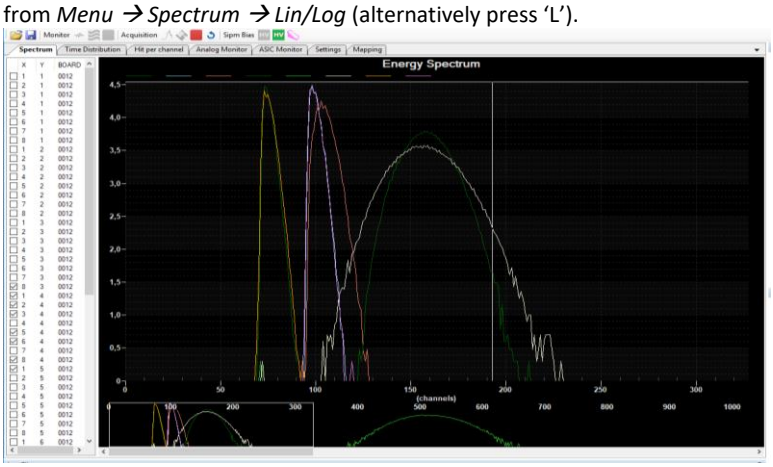
Main plots

The main working area hosts all the tabs related to the ASICs settings, configuration of the acquisition and online plots (spectra, oscilloscope, …). The main available plots are:

- ***EnergyLG/EnergyHG*** shows the Low Gain and High Gain energy spectrum for each board channel. The spectrum of multiple channels can be displayed on the same plot, by checking the relative checkboxes in the channels list on the left of the tab. The channels are listed as element of a matrix (X-Y coordinates) reproducing the detector shape. Also the sum spectrum, realized summing all energy values of all channels. It is possible to set a scaling factor in the *Settings* for this spectrum.

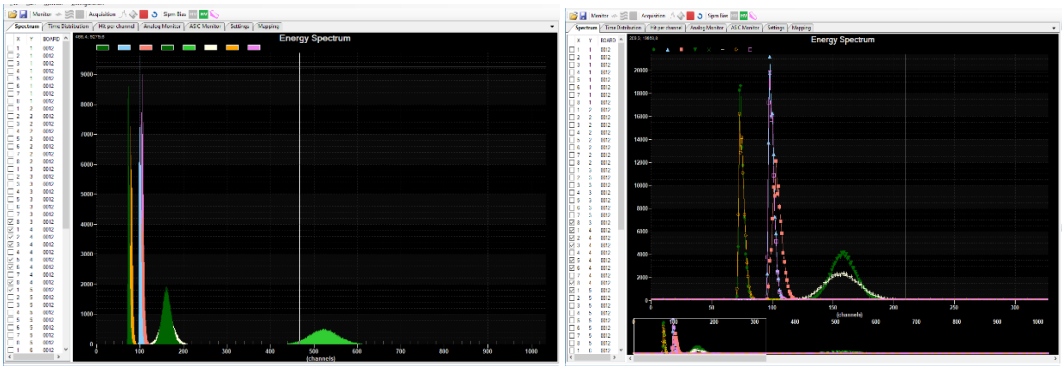


It is possible to zoom in the spectrum with keyboard command and then the mouse to drag on the interested area: rectangular zoom (press 'Z'), horizontal zoom (press 'H'), vertical zoom (press 'V'), unzoom (press 'U'). The spectrum can be displayed in bot linear and semi-log scale. It is possible to switch between the two modes from *Menu* → *Spectrum* → *Lin/Log* (alternatively press 'L').

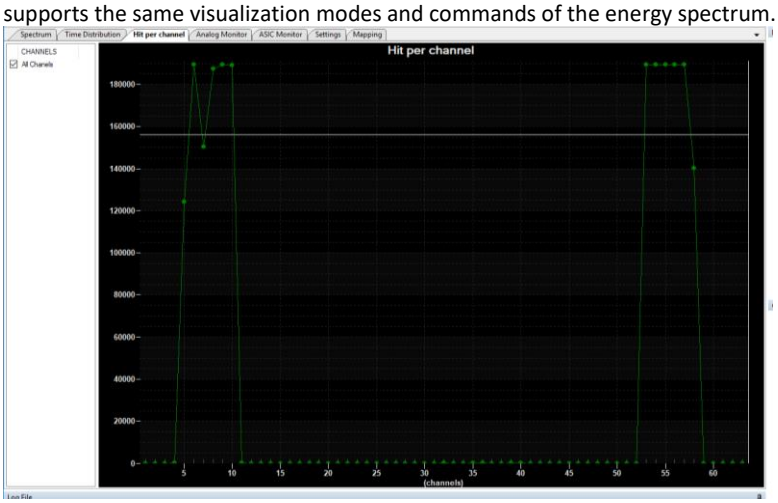


It is also possible to change the plot type: press 'O' to cycle between plot modes. Available plot modes are:

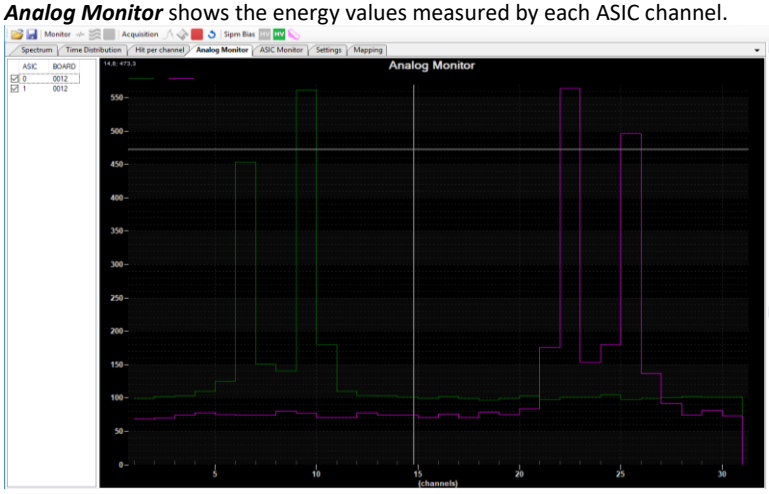
- Step
- Line
- Line with interpolation
- Bar
- Area
- Area with interpolation
- Dot
- Dot with Line
- Dot with interpolation

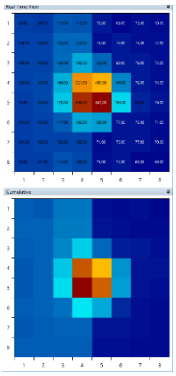


- ***Hit per channel,*** to visualize the number of triggers detected on each channel from the acquisition start. It supports the same visualization modes and commands of the energy spectrum.



- ***Analog Monitor*** shows the energy values measured by each ASIC channel.





- In the ***Imaging*** area, the results of energy acquisition are shown as real-time and cumulative image. The real-time image shows the energy acquired on each channel event by event, while the cumulative image shows the sum of the energy channel by channel, acquired during the entire run. It is possible to ZOOM in the image using the mouse wheel. Press 'a' on the keyboard to perform a zoom to fit.

The ASIC Monitor Tab

The *ASIC Monitor* Tab shows on oscilloscope the *charge_mux* output signal of the selected ASIC, i.e. the charge multiplexed analog output. The signal is synchronous to the following ASIC signals (refer to **[RD1]** for more details), shown in the plot:

- Analog High Gain
- Analog Low Gain
- Hit
- Analog readout clock
- Data In (srin_read)
- Trigger Charge
- Trigger Time
- External Veto (LEMO 5)

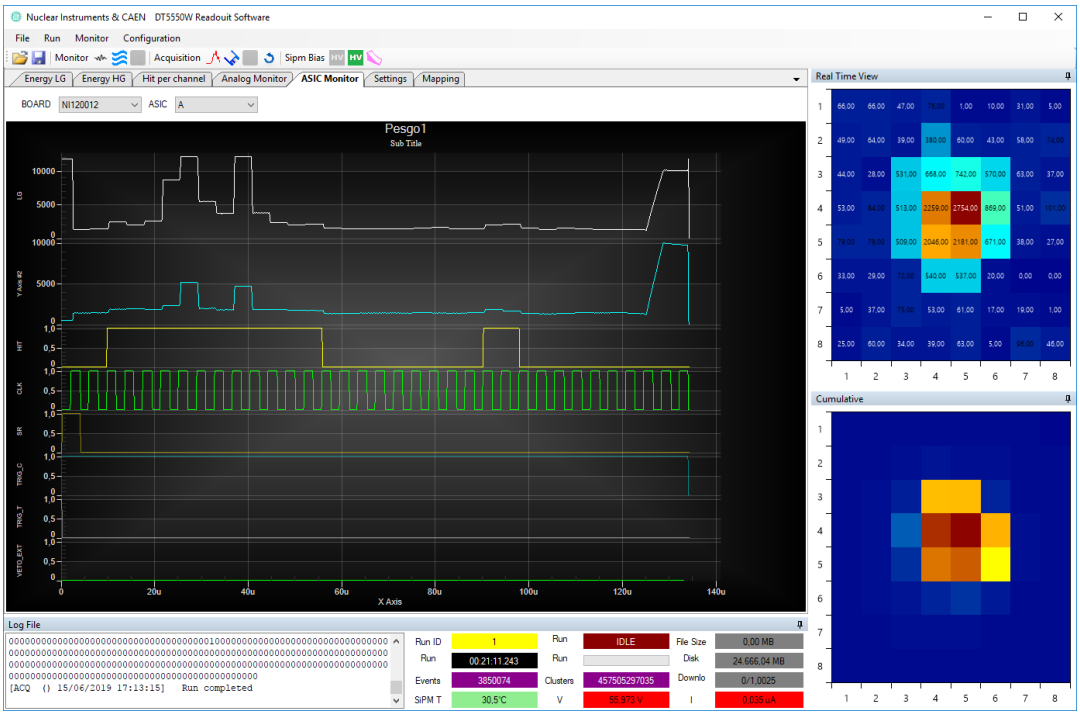


Figure 13.4: the *ASIC Monitor* Tab for A55CITx Piggyback. The white plot shows the charge multiplexed output

The Scan Tab

The *Scan* Tab allows to perform scanning on some of the ASIC parameters in order to tune at best the acquisition settings. The results are shown live time in the Counting Scan plot, where the number of recorded trigger is plotted vs. the time of the scanning (and so vs. the values of the scanned parameter). It is possible to select the parameters to be scanned, the range and steps of the scanning, the acquisition time and it is also possible to dump data on file.

- **Scan Type** allows to select the parameter to be scanned, choosing among the available ones.
- **MIN, STEP and MAX** allows to set the range and the steps for the scanning in bit units
- **sec** allows to define the time for the scanning
- **Start** allows to start the acquisition in scanning mode and dump resulting data on file.

The file format for Scan Data is the following:

```
TIME; PARAMETER_VALUE; CHANNEL[n]; VALUE[n]
0.0421388;300;30;16843009; ……..0;16843009
1.209408;310;30;16843009; ……0;16843009
2.3690355;320;30;16843009; ……..0;16843009
……..
```

- **TIME** is the time in second when that point acquisition star
- **PARAMETER_VALUE** is the value of the scanned parameter
- Follows a list of **asic_channel; value** that are the measured points

The Settings Tab

The *Settings* Tab allows to configure the ASICs and the acquisition parameters.
It is divided in two areas:

- the top area contains the global settings, common to all ASICs, and the DAQ parameters
- the bottom area contains the settings relative to a specific ASIC or channel

The *Apply Settings* button allows to effectively apply the given settings. No parameters can be changed during acquisition.
The *Apply Monitor* button allows to effectively apply the given *Monitor* settings. No parameters can be changed during acquisition.

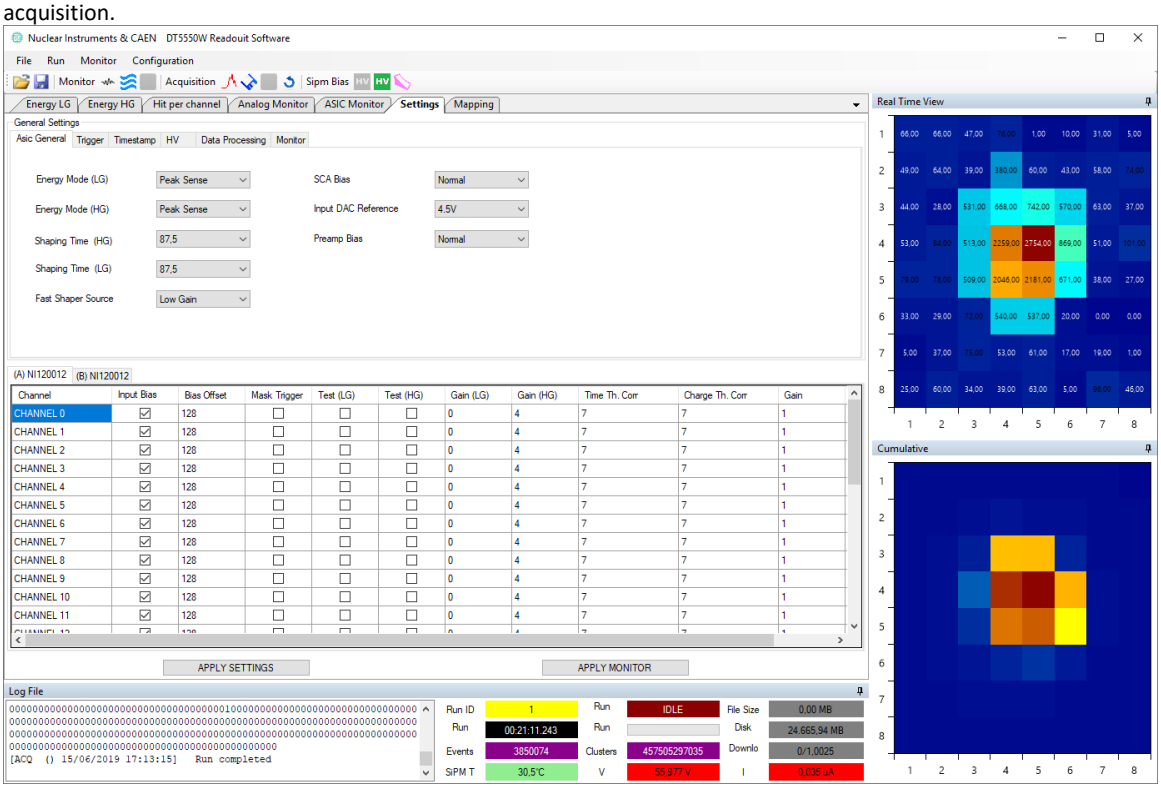


Figure 13.5: the *Settings* tab for A55CITx piggyback. The top and bottom area are clearly visible. The top area has different tabs for general configuration and the bottom area has a tab for each ASIC.

The *top area* is divided in different subtabs:

- ***Asic General***, which allows to configure the ASIC analog input stage
- ***Trigger,*** for ASIC and board trigger management
- ***Timestamp,*** for online time data processing management
- ***HV,*** to set parameters for A7585D soldered on the board
- ***Data Processing,*** for data processing management
- ***Monitor,*** to set parameters related to the analog readout and probe signals
- ***Photon Counting,*** to set the parameters for the photon counting acquisition

The *bottom area* has a tab for each ASIC hosted on the board. Each tab can be used to set the specific settings of each channel, like the offset for fine bias regulation and the trigger threshold.

Asic General

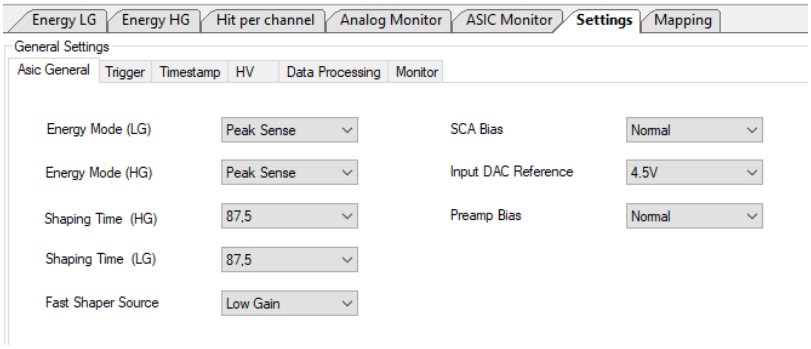


Figure 13.6: the *Asic General* subtab of the *Settings* tab.

This tab contains the settings for the configuration of the analog input stage of the ASIC.

- ***Energy Mode LG*** selects between *Peak Sense* and *Sample and Hold* logic for the Low Gain Amplifier
- ***Energy Mode HG*** selects between *Peak Sense* and *Sample and Hold* logic for the High Gain Amplifier
- ***Shaping Time LG*** selects shaping time for the Low Gain path
- ***Shaping Time HG*** selects shaping time for the High Gain path
- ***Fast Shaper Source*** selects source between low and high gain amplifier for the trigger shaper
- ***SCA bias*** selects between *Normal* and *weak bias* for the output amplifier
- ***Input DAC reference*** selects the input DAC voltage (and range).
- ***Preamp bias*** selects between *Normal* and *weak bias* for the input pre-amplifier

Trigger

This tab contains the settings for the configuration of ASIC and board trigger.

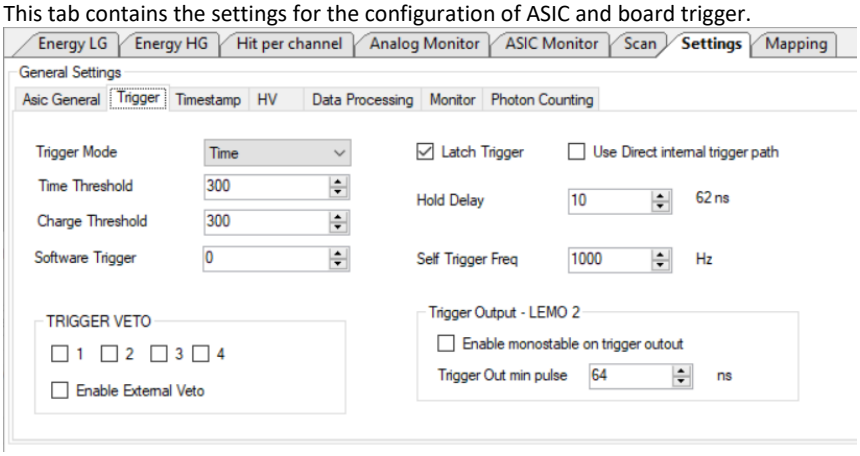


Figure 13.7: the *Trigger* subtab of the *Settings* tab.

- ***Trigger Mode*** selects between
  - Time trigger
  - Charge trigger
  - External trigger (LEMO 4)
  - Common (time), i.e. the logic OR between the time trigger of all ASICs
  - Common charge, i.e. the logic OR between the charge trigger of all ASICs
  - Self-trigger, forced by the software itself
  - 2 Coinc (time), i.e. couples of even-odd adjacent channels (0&1, 2&3, …) are put in logic AND on each ASIC separately. Each ASIC works independently and events can also be partially readout from one ASIC only.
  - Global 2 coinc (time), i.e. couples of even-odd adjacent channels (0&1, 2&3, …) are put in logic AND and the ASICs trigger output are put in OR to build a global trigger.

- ***Time Threshold*** sets the threshold for the time trigger. The value is set in LSB and the correspondent value in photoelectrons varies from ASIC to ASIC. With a Hamamatsu matrix S13361-3050AE-08 and bias voltage 54 V, Time Threshold = 300 results in zero counts in dark environment.
- ***Charge Threshold*** sets the threshold for the charge trigger.
- ***Software Trigger*** sets the threshold for zero suppression.
- ***Self-Trigger Freq*** allows to set the triggering rate of the software trigger.

- ***Trigger Veto*** enables/disables on or more ASICs (named as 1,2,3,4) and allows to use an external veto (on LEMO 4 for the default firmware). When the validation mode is enabled, external veto is automatically bypassed and overridden by the validation system behaviour
- ***Latch Trigger*** enables the latch on the charge trigger inside the ASIC. The Latch must be enabled to obtain the hit information
- ***Use Direct internal trigger path*** allows to send the trigger clock to the peak sensing cell of the ASIC. If disabled, the clock is the FPGA 125 MHz clock.
- ***Hold Delay*** allows to set the delay of the HOLD signal of the ASIC with respect to the trigger, in multiple steps of 6 ns. The resulting delay is shown next to the box.
- ***Trigger Output*** provides the trigger signal as output on LEMO 2. The trigger output is the logic OR of all signals sent to the ASIC trig_ext pin. The trigger can be provided as over threshold signal or shaped with a minimum length programmed by the monostable. In order to enable the monostable, check the *Enable monostable on trigger output* and set the *Trigger out min pulse*.

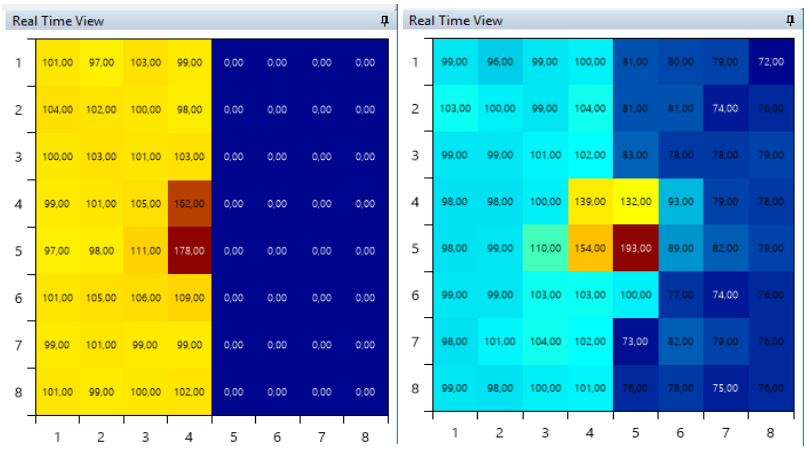


Figure 13.8: the effect of different triggering on imaging acquisition. On the left, with Trigger Mode = Time, and a more intense light on ASIC A, this latter is triggering while ASIC B is not triggering. On the right, with Trigger Mode = OR Time , both ASICs are acquiring.

Timestamp

This tab allows to manage the time data online processing.

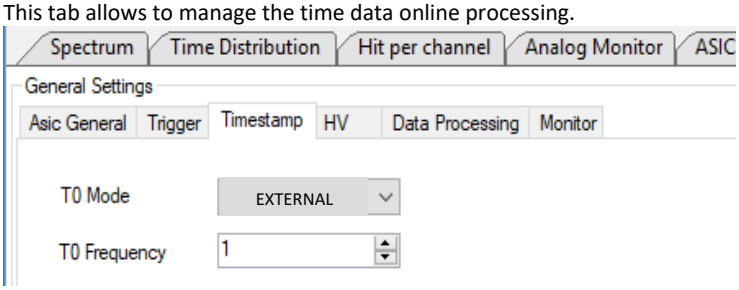


Figure 13.9: the *Timestamp* subtab of the *Settings* tab.

- ***T0 mode*** allows to manage the reference for time measurements. The possible options are:
  - EXTERNAL: T0 is given by an external signal (on LEMO 1 for the default firmware)
  - INTERNAL: T0 is generated by the software with the frequency specified in *T0 Frequency*
- ***T0 Frequency*** sets the frequency of the internal T0, if used.

High Voltage (HV)

This tab allows to adjust the parameters of the A7585D module, mounted on the A55CITx board. The module can supply a voltage between 20 and 85 V with maximum current of 10 mA.

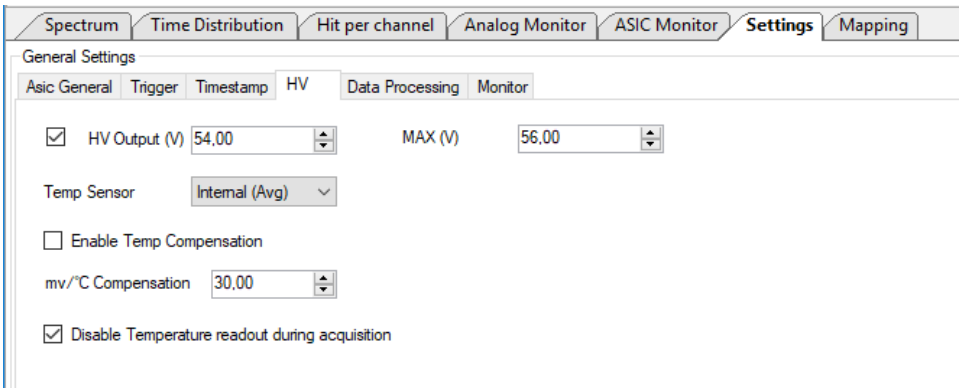


Figure 13.10: the *HV* subtab of the *Settings* tab.

- ***HV Output (V)*** allows to set the voltage value and enable the power supply, by checking the checkbox. When enabling temperature compensation, this is considered the voltage at 25° C.
- ***MAX (V)*** allows to limit the output voltage at the set value (protection against failure or error)
- ***Temp Sensor*** allows to choose the temperature sensor on which the temperature compensation is based. It is possible to choose the average of the two onboard sensors (Internal) or an external sensor.
- ***Enable Temp Compensation****:* if checked, the A7585D output voltage is adjusted depending on the measured temperature. It is needed to specify the *mV/°C compensation* factor.
- ***Disable Temperature readout during acquisition****:* if checked, the temperature sensors are not read out. This is useful since the application of temperature compensation could require 10 ms every 5 s, being the board unable to transmit data during this interval. If the rate is very high the board could enter in busy state. With this option the temperature is read out only with the board not acquiring, to avoid as much as possible the busy state.

Data Processing

This tab allows to set the parameters for the software data processing.

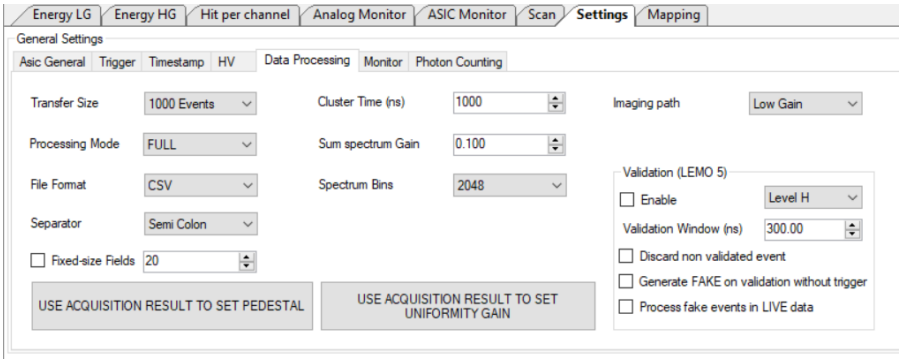


Figure 13.11: the *Data Processing* subtab of the *Settings* tab.

- ***Transfer Size*** is used to set the number of events to be included in each data transmission. The plot on the software are updated at each transmission, therefore the transfer size should be minimal to obtain a nearly real-time update of the plots. On the other hand, small transmissions packets do not exploit efficiently the USB3.0 bandwidth and are suggested only in case of low rate.
- ***Processing Mode*** is used to select the data processing:
  - FULL: events coming from different ASICs are considered correlated a reconstructed in a single cluster.
  - DECODE EVENTS: events coming from different ASICs are considered uncorrelated. Only the cluster of events on the channels of the same ASIC are reconstructed.
  - NONE: no online processing is done. The data must be saved in binary format and processed offline.
- ***Cluster Time***: maximum time distance between two events in order that they can be considered in the same cluster
- ***Sum Spectrum Gain*** sets the multiplying factor to be applied to the energy sum spectrum shown in the Spectrum tab.
- ***Spectrum Bins*** allows to rebin the energy spectrum (from 256 to 8192 bins)
- ***File Format*** allows to choose the file format saved by the software:
  - *CSV:* data are decodified as CSV standard and saved in .data format. When CSV format is selected, the user can choose how to format the output file ***Separator*** among semi colon, colon, space or tab.

If ***fixed-size field*** is selected, each field (excluding tab) will have the specified size.

- *BINARY:* data are not decodified and saved in binary format. The data are the binary which comes along the USB 3.0 bus. The user must implement a script to decode the data, but the raw data saving requires less space on disk.

- ***Imaging Path*** sets whether the image reconstruction shown in the software is extracted from Low Gain or High gain data.
- ***Use Acquisition Result to set Pedestal***: this button allows the user to easily perform the pedestal calculation (refer to Par. **How to perform pedestal calculation**)
- ***Use Acquisition Result to set Uniformity Gain***: this button automatically performs the regulation of the channels gain to uniform the response of sensor's pixels (refer to Par. **How to set uniformity gain**)
- **Validation (LEMO 5)** contains the control for validation mode (refer to Par. **Veto and validation** for more details). It is possible to *Enable* the validation mode, choose if validation must occur on *Level H* or *Edge Pos* and set a *Validation Window*, as explained in Par. **Veto and validation**.
  If the option *discard non validated event* is selected all the events those are not validated within the validation window are discarded. A trace of them is preserved in the *trigger id* and *Validation id* fields that are transferred in each event packet (refer to Chap. **Firmware** for more details). If the option is not selected, the event is converted and transferred even if it is not validated. In this case the event is flagged as not validated in the *flag* field of the packet and the not-validated event counter is increased.
  If option *generate FAKE on validation without trigger* is checked, the FPGA will generate a fake event filled of not converted data. In order to minimize the deadtime on events that do not contains any relevant information, the ASIC readout and the conversion are not started, so that energy, hit and fine TDC data are not relevant in the packet. Checking both *Discard non validated events* and *generate fake events*, files generated by the DT5550W and by another external system that uses the same validation as trigger will not only be aligned by timestamp and trigger id but also aligned by the event position in the files.
  If option *generate FAKE on validation without trigger* is checked and *Process fake events in live data* is selected, the fake events will processed in live view plots. These data usually contain the last event converted by an internal trigger.

Monitor

This tab allows to set the parameters related to the analog readout and probe signals. The settings in this tab can be changed without reprogramming the entire ASIC pressing the general *Apply Settings* button. It is enough to press the *Set* button available in this tab.

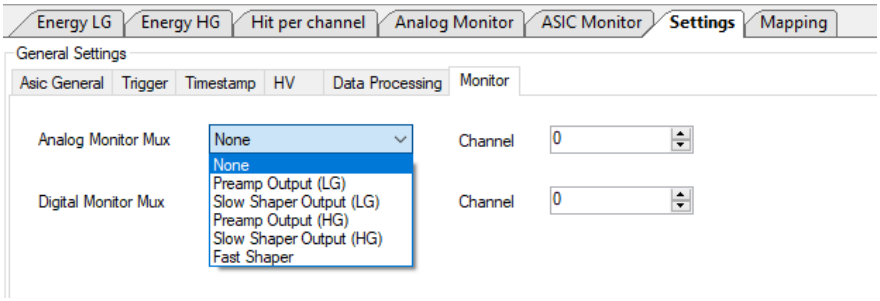


Figure 13.12: the *Monitor* subtab of the *Settings* tab.

- ***Analog Monitor Mux*** selects which Analog ASIC internal signal to be sent on the **Out Probe** connectors (see Par.**Test Pins**)
- ***Digital Monitor Mux*** selects which Digital ASIC internal signal to be sent on the **d_probe** pin (see Par. **Test Pins**)
- ***Channel*** selects the ASIC channel for which the signal specified in *Analog/Digital Monitor Mux* field is shown

Photon Counting

This tab allows to set the parameters to readout the board in Photon Counting mode. The Photon Counting mode acquisition starts when pressing the abacus icon in the bottom toolbar.

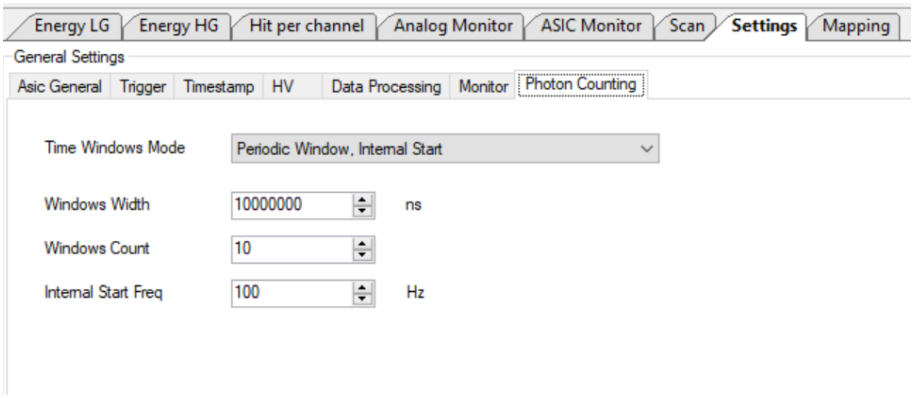
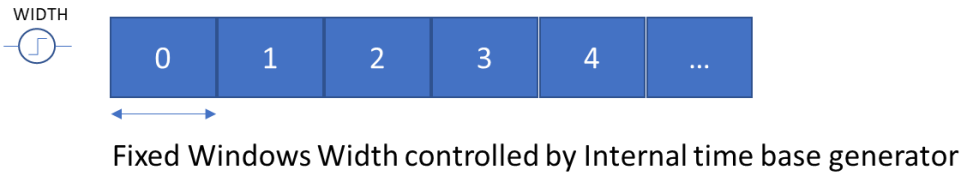


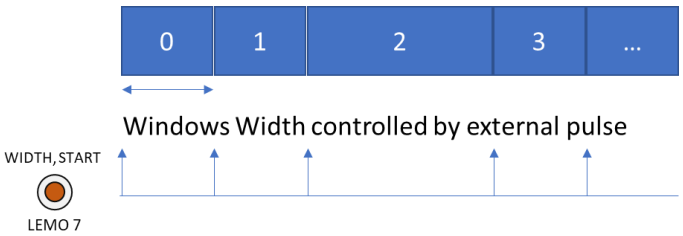
Figure 13.13: the *Photon Counting* subtab of the *Settings* tab.

- ***Time Windows Mode*** selects the way in which events are counted inside a specific time window. There are four working modes:

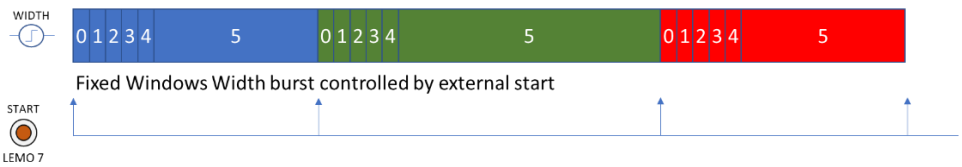
  - *Periodic Window, Internal Start*: programmable fixed windows width controlled by an internal base generator. The board counts the number of triggers from any ASIC channels in each window. Windows are all adjacent without dead time. Please, be aware that, due the USB bandwidth limits, the minimum width in order not to have dead time is 1ms. It is possible to use this mode even with microseconds width windows but is not possible to guarantee the zero deadtime.
    In this mode the **Windows Width** must be set.



  - *Periodic Window, External Start (LEMO7):* The width and the start of the windows is adjusted upon the commutation (rising edge) of the T0 (LEMO 7) signal. All windows are adjacent and the width of the windows is regulated by the period of the external T0 signal. Non periodic signal on T0 are fully supported.
    In this mode no other parameter must be set.



  - *Windows Scan, External Scan Start (LEMO7)*: A programmable number of windows burst is started by the LEMO7 external signal. The width of each window is programable and generated by internal time generator. The last window will be modulated in width in order to fill the space between one start and the subsequent.
    In this mode the **Windows Width** and **Windows Count** must be set.



  - *Windows Scan, Periodic Scan Start*: similar to the previous one, but the start of the burst is generated internally, with no need of any external signal.
    In this mode also the **Internal Start Frequency** must be set

- ***Windows Width*** sets the width of the time windows in ns
- ***Windows Count*** *sets* the number of windows in a burst
- ***Internal Start Frequency*** sets the frequency of the internal signal giving the start of the time windows generation.

Channel specific settings

The bottom area of the *Settings Tab* contains a table to set the ASIC channels specific parameters. Each tab of this area is related to an ASIC hosted on the board and can be used to set parameters like the offset for fine bias regulation and the trigger threshold.

(A) NI120012 (B) NI120012

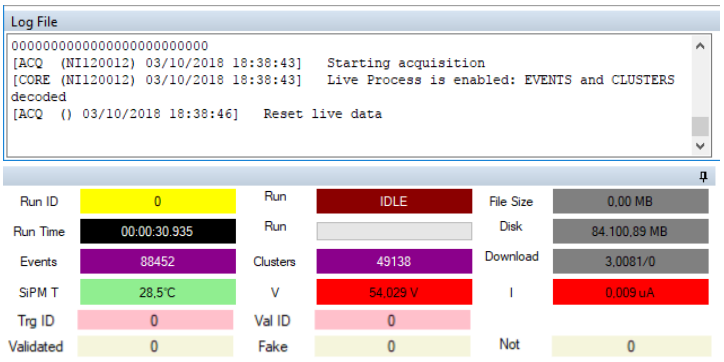
Channel	Input Bias	Bias Offset	Mask Trigger	Test (LG)	Test (HG)	Gain (LG)	Gain (HG)	Time Th. Corr	Charge Th. Corr	Gain
CHANNEL 0	☑	128	☐	☐	☐	0	4	7	7	1
CHANNEL 1	☑	128	☐	☐	☐	0	4	7	7	1
CHANNEL 2	☑	128	☐	☐	☐	0	4	7	7	1
CHANNEL 3	☑	128	☐	☐	☐	0	4	7	7	1
CHANNEL 4	☑	128	☐	☐	☐	0	4	7	7	1
CHANNEL 5	☑	128	☐	☐	☐	0	4	7	7	1
CHANNEL 6	☑	128	☐	☐	☐	0	4	7	7	1
CHANNEL 7	☑	128	☐	☐	☐	0	4	7	7	1
CHANNEL 8	☑	128	☐	☐	☐	0	4	7	7	1
CHANNEL 9	☑	128	☐	☐	☐	0	4	7	7	1
CHANNEL 10	☑	128	☐	☐	☐	0	4	7	7	1
CHANNEL 11	☑	128	☐	☐	☐	0	4	7	7	1

Figure 13.14: the bottom area of the *Settings* tab, containing the table for ASIC channels specific settings. In this case two ASICs (called A and B) are hosted on the board**.**

The parameters configurable from the channel specific settings tabs are:

- *Input Bias*, to enable/disable the ASIC's channel input DAC for fine bias regulation
- *Bias Offset,* to set the 8-bit input DAC value for fine bias regulation. In case of a positive bias given by A7585D module, a higher offset results in a lower bias voltage. The bias can be adjusted in the range ±1 V. The value 128 corresponds to a zero offset and so the bias is not adjusted.
- *Mask Trigger,* to disable the time trigger of the specific channel
- *Test LG,* enable the test pulse for the low gain amplifier
- *Test HG,* enable the test pulse for the high gain amplifier
- *Gain LG,* analog gain of the low gain amplifier (min 0, max 63)
- *Gain HG,* analog gain of the high gain amplifier (min 0, max 63)
- *Time Th. Corr,* to set the individual channel time trigger threshold adjustment. The values of this threshold and the general time threshold are not linearly correlated.
- *Charge Th. Corr,* to set the individual channel charge trigger threshold adjustment. The values of this threshold and the general charge threshold are not linearly correlated.
- *Gain,* to set the energy gain
- *Offset,* to set the pedestal value

Log Area and DAQ Status Bar



In the *Log Area*, are reported all the interactions of the software with the board, included the bitstream sent to the ASICs. In this way, it is possible to capture a configuration to be used on a custom board.

In the *DAQ Status Bar*, the acquisition status and stats are reported, included the high voltage status (when available on the piggyback board) , the piggyback temperature sensors value and validation parameters

After board connection, the *Log Area* shows, in the first lines, the model of the detected piggyback board, the number of ASICs, the serial number and the firmware version loaded on the motherboard.

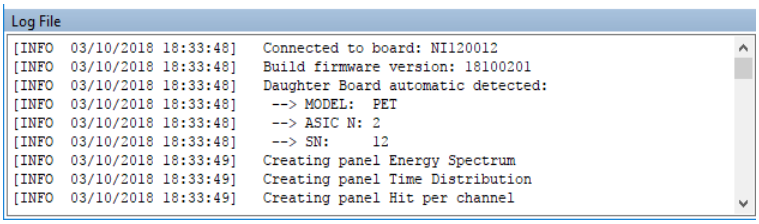


Figure 13.15: the *Log Area* after board connection.

How to perform an acquisition

Before starting an acquisition, the user should set all the relevant parameters in the *Settings* tab.
The acquisition is started pressing the correspondent button in the *Menu and Control Toolbar (Acquisition section)*. The Spectrum icon starts an acquisition without data saving, while the Floppy Disk icon starts an acquisition with data saving in the specified file format.
After pressing the Floppy Disk icon, the *Start Run* window automatically opens. In this menu it is possible to specify the data saving folder and compile the logbook, with the relevant acquisition parameters, the date and other annotations.
It is also possible to set the Target mode for the acquisition: in *Free running* the acquisition must be stop manually, in *Run Time* the user must specify a target time at which the acquisition is stopped, in *Cluster Number* the user must specify the target number of events in a cluster (this latter is available only in *Processing Mode* = FULL).
It is possible to choose the acquisition *Mode* between *Spectroscopy* and *Photon counting*, in order to save energy/time or counts data respectively.

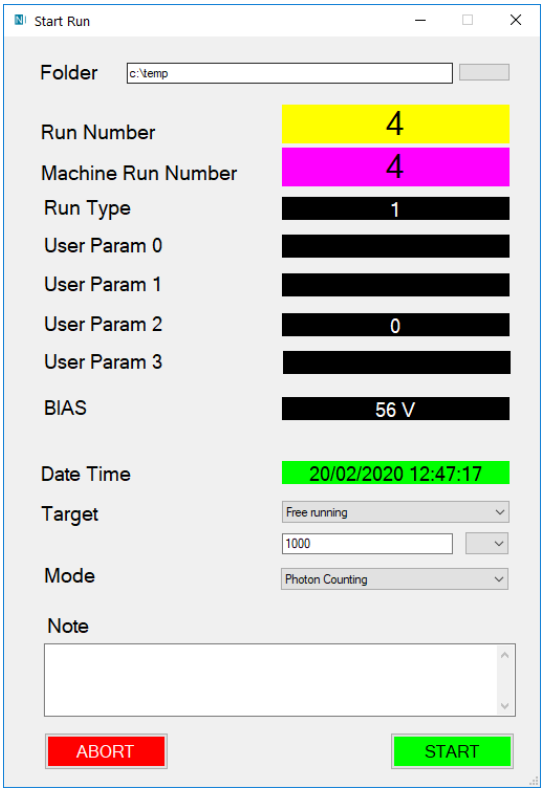


Figure 13.16: the *Start Run* window which opens after the acquisition with data saving is started.

After setting the fields in the *Start Run* window, press 'Start' to effectively start the board acquisition with specified parameters, press 'Abort' to return to the main software window.

After the acquisition is started, the user can visualize on plots the results of the acquisition, using the tabs described in **[RD2]**.

Spectroscopy Data Saving Format

For each Spectroscopy Mode run, two files with the same name and different format are saved:

- a .JSON file, which contains the run information and the entire ASIC configuration. It can be easily decodified via a json parser (available in all modern programming languages) or via strings elaboration.

- a .data or binary file containing the data, depending on the format chosen in the *Data Processing* tab.

The binary file is a direct dump of the data transmitted on USB3.0 bus, without any elaboration. The packet is described in Chap. **Firmware and data format**. It is possible to write a function, for example in C language, to decode the binary data (an example code is given open source at https://github.com/NuclearInstruments/CitirocDecodeC-)

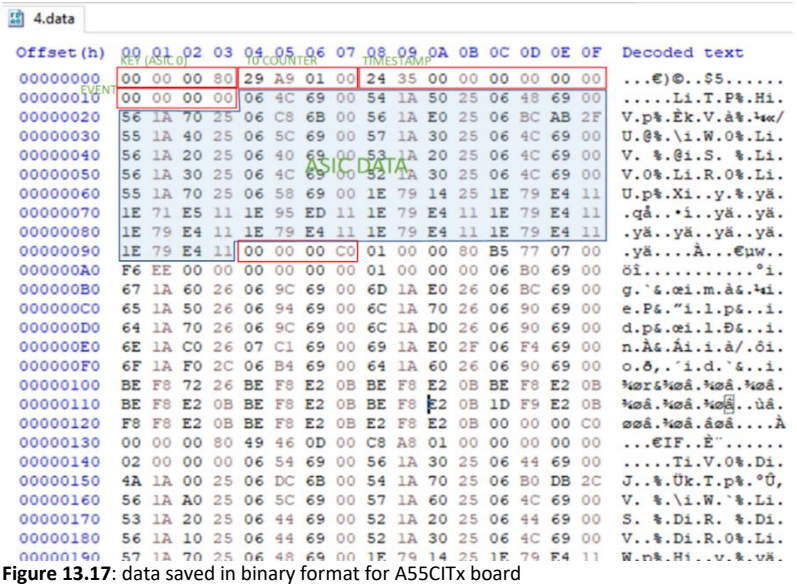


Figure 13.17: data saved in binary format for A55CITx board

The .data file is a textual CSV format. Each line represents an event and each column a decodified field (timestamp, hits, energy LG, energy HG….). Column are separated by ; separator.
The data format is different depending on the Processing Mode. In decoded events mode, each line contains only the data relative to one ASIC; multiple ASIC on the board are processed and saved as completely independent. In full processing mode, the software reconstructs clusters using the event timecode as reference to merge multiple events.

With *Processing Mode* = DECODE EVENTS, the structure of the data file is as follows (the fields are placed in columns in the file and a first header row explains the column field):

Field	Size (Columns)	Description
ID	1	Progressive number (increment by 1 for each row by the software)
ASIC	1	ID of the ASIC on the board (0,1, 2 ...)
EventCounter	1	Progressive number in hardware for each acquisition (acquisition=trigger that can be enqueued in the output FIFO)
RUN_EventTimeCodeLSB	1	Timecode of the event from the start of the acquisition in clock cycles
RUN_EventTimecode_ns	1	Timecode of the event from the start of the acquisition in clock ns. Resolution is 0.5 ns
T0_to_Event_Timecode	1	Timecode of the event from the last T0 in clock cycles
T0_to_Event_Timecode_ns	1	Timecode of the event from the last T0 in ns
Trigger ID	1	Number of triggers that the specific ASIC generated from the run start up to the moment when the specific packet has been generated (that means when the tigger fired)
Validation ID	1	Value of the validation counter captured when the packet has been generated starting from the start of the run. This counter does not count validated events but the Low->High transitions of the External Validation signal (LEMO 5)
FLAG	1	0 - validation is off – event validated 1 - validation is on – event validated 2 - event not validated (internal trigger fired but no validation in the validation window) 3 - Fake event (validation event when no internal trigger has been fired in a validation window time before the validation event)

HIT	32	1/0 vector containing the ASIC hit flag for each channel
CHARGE_LG	32	integer vector containing the charge Low Gain information for each channel
CHARGE_HG	32	integer vector containing the charge High Gain information for each channel

Table 13.1: saved data format in *Processing Mode* = DECODE EVENTS

With *Processing Mode* = FULL, the size of the packet (each row) depends on how many ASICs are merged in a cluster. For example, if an events interact with just one part of the sensor and only one of four ASIC triggers the cluster will contain information relative to just one ASIC and the number of columns will be less than the maximum .The structure of the .csv file is as follows (the fields are placed in columns in the file and a first header row explains the column field):

Field	Size (Columns)	Description
ID_CLUSTER	1	Progressive number (increment by 1 for each row by the software)
CLUSTER_RUN_Timecode_ns	1	Timecode of the cluster from the start of the acquisition in clock ns (the timecode of the cluster is the timecode of the first event of the cluster)
CLUSTER_Timecode_ns	1	Timecode of the event from the last T0 in ns (the timecode of the cluster is the timecode of the first event of the cluster)
NEventsInCluster	1	Number of events (ASICs) present in the cluster
THE FOLLOWING PART IS REPEATED FOR EACH EVENT IN THE CLUSTER		
RUN_EventTimeCodeLSB	1	Timecode of the event from the start of the acquisition in clock cycles
RUN_EventTimecode_ns	1	Timecode of the event from the start of the acquisition in clock ns. Resolution is 0.5 ns
T0_to_Event_Timecode	1	Timecode of the event from the last T0 in clock cycles
T0_to_Event_Timecode_ns	1	Timecode of the event from the last T0 in ns
Trigger ID	1	Number of triggers that the specific ASIC generated from the run start up to the moment when the specific packet has been generated (that means when the tigger fired)
Validation ID	1	Value of the validation counter captured when the packet has been generated starting from the start of the run. This counter does not count validated events but the Low->High transitions of the External Validation signal (LEMO 5)
FLAG	1	0 - validation is off – event validated 1 - validation is on – event validated 2 - event not validated (internal trigger fired but no validation in the validation window) 3 - Fake event (validation event when no internal trigger has been fired in a validation window time before the validation event)
HIT	32	1/0 vector containing the ASIC hit flag for each channel
CHARGE_LG	32	integer vector containing the charge Low Gain information for each channel
CHARGE_HG	32	integer vector containing the charge High Gain information for each channel

Table 13.2: saved data format in *Processing Mode* = FULL

Photon Counting Data Saving Format

For each Photon Counting Mode run, a textual CSV format file is saved. The file is formatted as follows:

Field	Size (Columns)	Description
ROW	1	Progressive number (increment by 1 for each row by the software)
TIME CODE	1	Timecode indicating when the data frame has been queued in the output FIFO
TIME CODE (ns)	1	Timecode indicating when the data frame has been queued in the output FIFO (expressed in ns)
START COUNTER	1	Number of commutation of the start signal on LEMO7 (for synchronization with other boards)

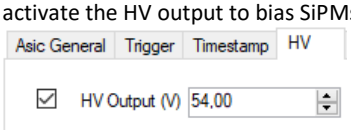
WINDOWS COUNTER	1	ID of the time window in the burst
CH[n]	128	Counts of the n-th channel in the specified time window

Table 13.3: saved data format in *Photon Counting Mode*

How to perform pedestal calculation

The DT5550W Readout Software allows to easily manage the pedestal calculation automatically.
In order to exploit this functionality, the user should :

- remove any light source from the sensors
- activate the HV output to bias SiPMs



- enable the Software Trigger at 1 kHz frequency

At this point, the user can reset the plots view, start the acquisition and acquire for nearly 10 seconds. The acquired image will be extremely non-uniform, with great differences of energy detected by different channels, as shown in **Figure 13.18.**
At this point the user can:

- stop the acquisition
- press the '*Use Acquisition Result to set Pedestal*' button in the *Data Processing* tab and the software will automatically adjust the *Offset* of each channel to uniform at best the pedestal
- press 'Apply Settings'
- start again the acquisition

The result after pedestal calculation is shown in **Figure 13.18,** where the image on the right is detecting, in absence of light, much more uniform energies with respect to the image on the left.

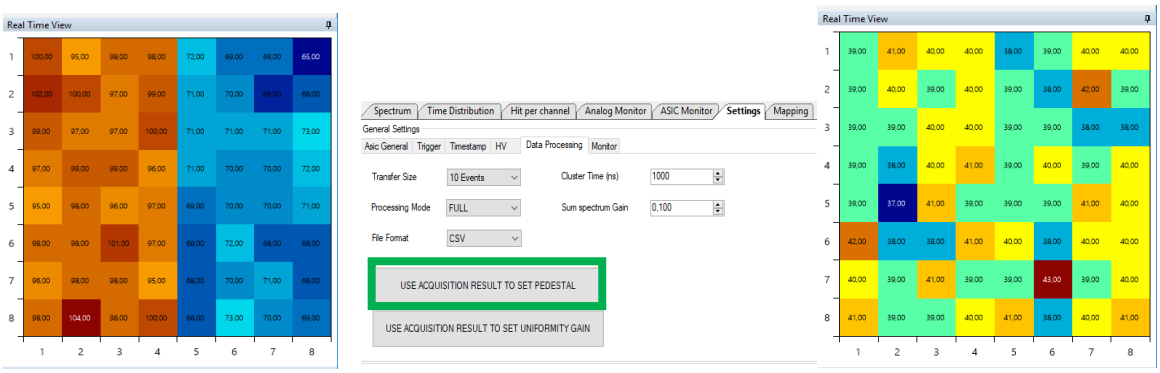
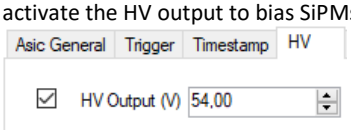


Figure 13.18: an image of a 64-channel SiPM matrix acquired before (left) and after (right) the pedestal calculation.

How to set uniformity gain

The DT5550W Readout Software allows to easily manage the channels gain regulation automatically.
In order to exploit this functionality, the user should :

- illuminate the SiPM with pulsed light in the more uniform possible way, so that each pixel receives the same amount of light
- activate the HV output to bias SiPMs



- operate with the internal ASIC trigger

At this point, the user can reset the plots view, start the acquisition and acquire the time needed to collect a sufficient amount of data.
At this point the user can

- stop the acquisition
- press the '*Use Acquisition Result to set Uniformity Gain*' button in the *Data Processing* tab and the software will automatically adjust the *Gain* coefficient of each channel to uniform at best the energies detected by the matrix pixels
- press 'Apply Settings'
- reset real-time results
- start again the acquisition

In **Figure 13.19,** the results of gain and pedestal compensation are shown, taking as example a 64-channel matrix.

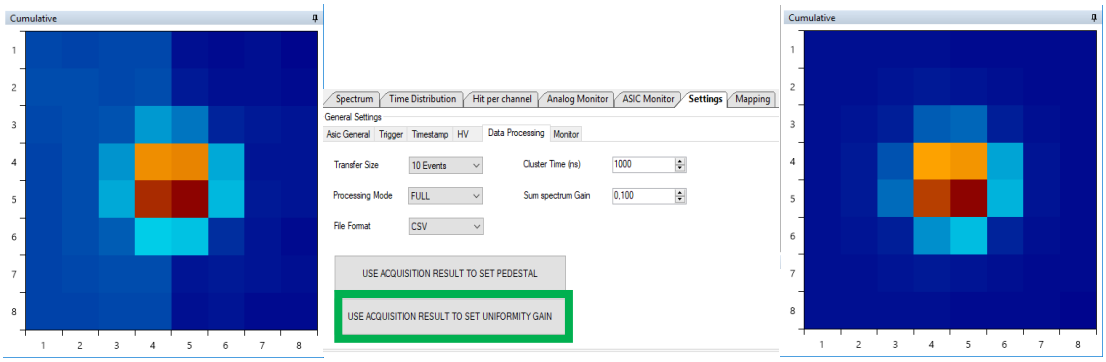


Figure 13.19: the results of pedestal calculation and gain regulation. The image on the right (after compensation of offset and gain) has a more uniform background (deep blue pixels) and small energy differences in neighbouring pixels with respect to the image on the left.

How to remap a detector geometry

In order to map the channels of the ASIC directly on the pixel position of a detector, the DT5550W Readout Software uses a configurable conversion map, which can be set in the *Mapping* tab.

The map is a 2D grid, with configurable dimensions, in order to reproduce the physical shape of the detector. Once the dimensions are established, it is possible to associate each cell of the matrix to a specific ASIC channel in a specific board. All this information is used to reconstruct the image in the *Event Display* area.

It is possible to configure the number of rows and columns of the grid. The Resize button can be used to redefine the dimensions of the grid, the *Default* button restores the standard dimension of the map according to the number of ASICs installed on the piggyback board, the *Board Layout* button restores the default channel-pixel assignment.

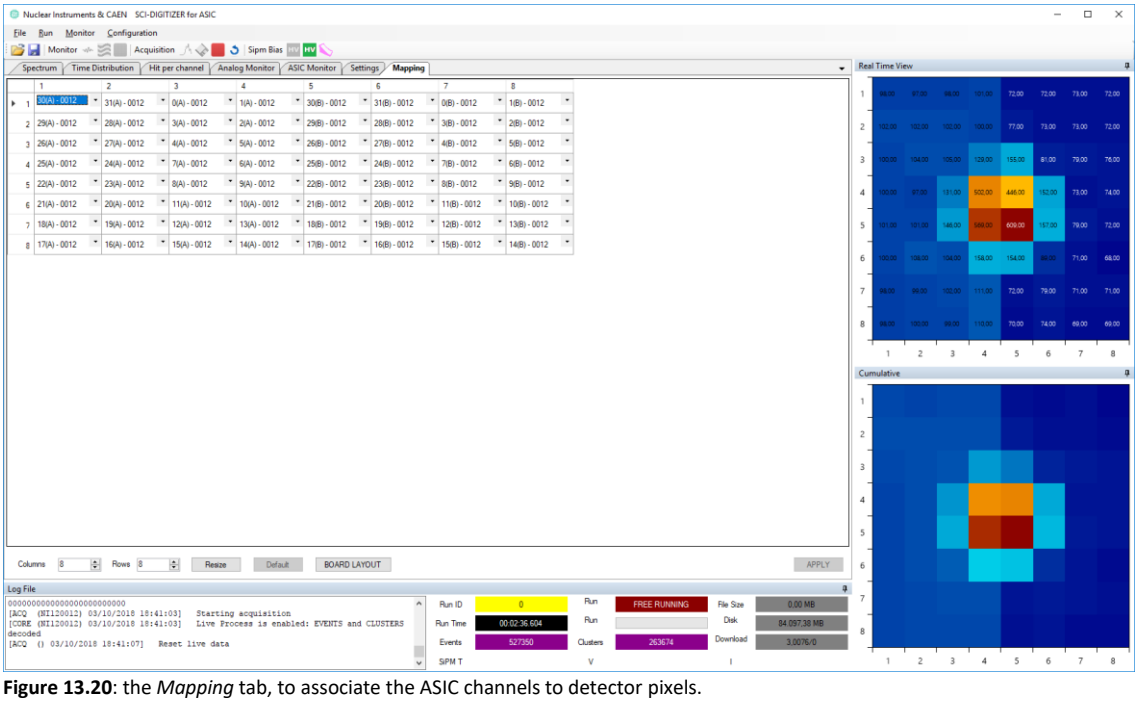
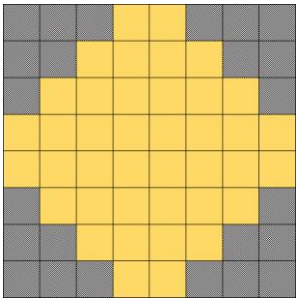


Figure 13.20: the *Mapping* tab, to associate the ASIC channels to detector pixels.

In order to modify the channel-pixel mapping, it is sufficient to click on the desired cell of the grid and select one of the ASIC channels from the combo box. It is possible not to assign any ASIC channel to a cell of the grid: this is particularly useful to obtain a reproduction of a non-square detector. The pixels which are not assigned to any channels will always count a zero energy.

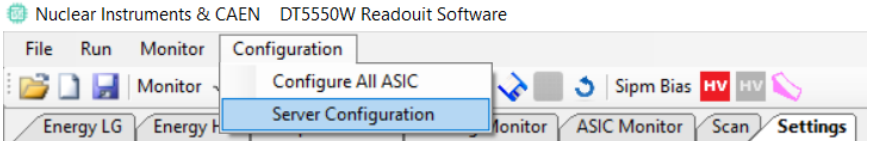


The user must press *Apply* to assign the mapping grid.

14 Multiple boards control

In order to have the possibility to remote control the software and start/stop multiple readout systems, a very simple TCP server has been implemented

From Configuration -> Server Configuration, it is possible to access to the server settings.



The server listens on the TCP port specified for all ethernet switches. It is possible to *Enable Server*, choose the *Server Port* and select the folder where to save data. The folder is overridden if the settings are changed during the run. It is possible to set a *Detector Name* to be prepend in the file name.

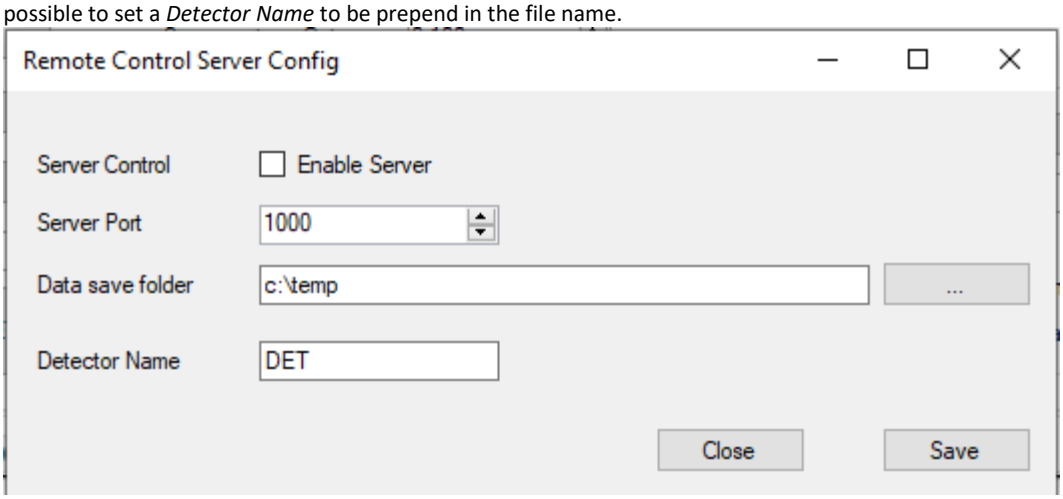


Figure 14.1: the *Server configuration* window

The generated file contains the following information:
DETECTOR NAME
RUN NUMBER (5 digits)
RUN TYPE (5 digits)
TIME OF START (in UTC)

User can develop a client in any programming language that supports TCP raw socket. The protocol supports only two commands - START and STOP - . The configuration is stored in the DT5550W readout application and the software must be configured in the correct way before starting the run. Each command is made of three phases:

- open connection
- send command
- close connection

After each command, it is mandatory to close the connection.

The commands are

START COMMAND

0xFF	0x80	0x00	0x08	RN1	RN0	RT1	RT0	0xEE	0x00	0x00	0x01	T3	T2	T1	T0

STOP COMMAND

0xFF	0x80	0x00	0x08	RN1	RN0	RT1	RT0	0xEE	0x00	0x00	0x01	T3	T2	T1	T0

where,

RN1: Run number MSB byte [15..8]
RN0: Run number LSB byte [7..0]

RT1: Run type MSB byte [15..8]
RT0: Run type LSB byte [7..0]

T3: Run type MSB byte [31..24]
T2: Run type [23..16]
T1: Run type [15..8]
T0: Run type LSB byte [7..0]

Note: a Python example of a client to manage the remote server can be downloaded for free at https://github.com/NuclearInstruments/dt5550w-remote-client

15 Instructions for Cleaning

The equipment may be cleaned with compressed air spray, isopropyl alcohol or deionized water and air dried.

Cleaning the Touchscreen

In order to clean the touchscreen (if present), wipe the screen with a towelette designed for cleaning monitors or with a clean cloth moistened with water.
Do not use sprays or aerosols directly on the screen; the liquid may seep into the housing and damage a component. Never use solvents or flammable liquids on the screen.

Cleaning the air vents

It is recommended to occasionally clean the air vents (if present) on all vented sides of the board. Lint, dust, and other foreign matter can block the vents and limit the airflow. Be sure to unplug the board before cleaning the air vents and follow the general cleaning safety precautions.

General cleaning safety precautions

CAEN recommends cleaning the device using the following precautions:

1) Never use solvents or flammable solutions to clean the board.
2) Never immerse any parts in water or cleaning solutions; apply any liquids to a clean cloth and then use the cloth on the component.
3) Always unplug the board when cleaning with liquids or damp cloths.
4) Always unplug the board before cleaning the air vents (if present)
5) Wear safety glasses equipped with side shields when cleaning the board

16 Device decommissioning

After its intended service, it is recommended to perform the following actions:

- Detach all the signal/input/output cable
- Wrap the device in its protective packaging
- Insert the device in its packaging (if present)

THE DEVICE SHALL BE STORED ONLY AT THE ENVIRONMENT CONDITION SPECIFIED IN THE MANUAL, OTHERWISE PERFORMANCE AND SAFETY WILL BE NOT GUARANTEED

17 Disposal

The disposal of the equipment must be managed in accordance with Directive 2012/19 / EU on waste electrical and electronic equipment (WEEE).

The crossed bin symbol indicates that the device shall not be disposed with regular residual waste.

18 Technical Support

CAEN makes available the technical support of its specialists for request concerning the software and the hardware. Use the support form available at the following link:

https://www.caen.it/support-services/support-form/

CAEN SpA is acknowledged as the only company in the world providing a complete range of High/Low Voltage Power Supply systems and Front-End/Data Acquisition modules which meet IEEE Defaults for Nuclear and Particle Physics. Extensive Research and Development capabilities have allowed CAEN SpA to play an important, long term role in this field. Our activities have always been at the forefront of technology, thanks to years of intensive collaborations with the most important Research Centres of the world. Our products appeal to a wide range of customers including engineers, scientists and technical professionals who all trust them to help achieve their goals faster and more effectively.

CAEN S.p.A.
Via Vetraia, 11
55049 Viareggio
Italy
Tel. +39.0584.388.398
Fax +39.0584.388.959
info@caen.it
www.caen.it

CAEN GmbH
Klingenstraße 108
D-42651 Solingen
Germany
Tel. +49 (0)212 254 4077
Mobile +49 (0)151 16 548 484
Fax +49 (0)212 25 44079
info@caen-de.com
www.caen-de.com

CAEN Technologies, Inc.
One Edgewater Plaza - Suite 101
Staten Island, NY 10305
USA
Tel. +1.718.981.0401
Fax +1.718.556.9185
info@caentechnologies.com
www.caentechnologies.com

CAEN
Tools for Discovery
Electronic Instrumentation

UM7028 - A55CITx User Manual Rev. 3 - March 2nd, 2022
00000-00-DPP00-MUTX