Purpose of this Manual

The User Manual contains the full description of the DPP-PHA firmware registers for 780 family series. The description is compliant with the DPP-PHA firmware revision **4.25_128.78**. For future release compatibility check the firmware history files.

Change Document Record

Date	Revision	Changes
January 22nd, 2019	00	Initial Release.
August 26th, 2019	01	Modified registers Board Configuration, Trigger Hold-Off Width, DPP Algorithm Control, DPP Algorithm Control 2. Added register TRG-IN Counter.
July 10th, 2020	02	Added Chap. DPP-PHA Memory Organization.
March 24th, 2022	03	Modified Chap. DPP-PHA Memory Organization to make it compliant with firmware revision 4.25_128.77.
August 26th, 2022	04	Modified bit[9:8] of DPP Algorithm Control 2 register (0x1nA0). Updated copyrights and Endpage.

Symbols, abbreviated terms and notation

ADC	Analog-to-Digital Converter
AMC	ADC & Memory Controller
DAQ	Data Acquisition
DAC	Digital-to-Analog Converter
DC	Direct Current
DPP	Digital Pulse Processing
DPP-QDC	DPP for Charge to Digital Converter
DPP-PHA	DPP for Pulse Height Analysis
DPP-PSD	DPP for Pulse Shape Discrimination
LVDS	Low-Voltage Differential Signal
MCA	Multi-Channel Analyzer
ROC	ReadOut Controller
USB	Universal Serial Bus

Reference Documents

[RD1] UM1935 - CAENDigitizer User & Reference Manual.

[RD2] UM5960 - CoMPASS User Manual.

[RD3] GD2827 - How to make coincidences with CAEN digitizers.

All CAEN documents can be downloaded at:
`www.caen.it/support-services/documentation-area`

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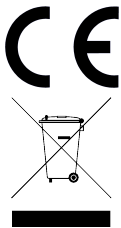
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CAEN ⬡ **Electronic Instrumentation**

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1 Registers and Data Format

All registers described in the User Manual are 32-bit wide. In case of VME access, **A24** and **A32** addressing mode can be used.

Register Address Map

The table below reports the complete list of registers that can be accessed by the user. The register names in the first column can be clicked to be redirected to the relevant register description. The register address is reported on the second column as a hex value. The third column indicates the allowed register access mode, where:

R   **Read only**. The register can be accessed in read only mode.

W   **Write only**. The register can be accessed in write only mode.

R/W   **Read and write**. The register can be accessed both in read and write mode.

According to the attribute reported in the fourth column, the following choices are available:

I   **Individual register**. This kind of register has N instances, where N is the total number of channels in the board. Individual registers can be written either in single mode (individual setting) or broadcast (simultaneous write access to all channels). Read command must be individual.
Single access can be performed at address 0x1nXY, where n is the channel number, while broadcast write can be performed at the address 0x80XY. For example:

- access to address 0x1570 to read/write register 0x1n70 for channel 5 of the board;

- to write the same value for all channels in the board, access to 0x8070 (broadcast write). To read the corresponding value, access to the individual address 0x1n70.

C   **Common register**. Register with this attribute has a single instance, therefore read and write access can be performed at address 0x80XY only.

H   **HV register**. In case of 780 series and DT5790 some registers manage the HV channels of the boards. Read and write access can be performed at address 0x1nXY only, where n=2 corresponds to the HV channel 0 and n=3 corresponds to the HV channel 1.

Register Name	Address	Mode	Attribute
High Voltage VSet	0x1n20 (n=2 for HV-ch0, n=3 for HV-ch1)	R/W	H
High Voltage ISet	0x1n24 (n=2 for HV-ch0, n=3 for HV-ch1)	R/W	H
High Voltage Ramp Up	0x1n28 (n=2 for HV-ch0, n=3 for HV-ch1)	R/W	H
High Voltage Ramp Down	0x1n2C (n=2 for HV-ch0, n=3 for HV- ch1)	R/W	H
High Voltage VMax	0x1n30 (n=2 for HV-ch0, n=3 for HV-ch1)	R/W	H
High Voltage Control	0x1n34 (n=2 for HV-ch0, n=3 for HV-ch1)	R/W	H
Number of Events per Aggregate	0x1n34, 0x8034	R/W	I
High Voltage Status/A639 Firmware Release	0x1n38 (n=2 for HV- ch0, n=3 for HV-ch1)	R	H
Pre Trigger	0x1n38, 0x8038	R/W	I
Data Flush	0x1n3C, 0x803C	W	I
High Voltage VMon/Analog In	0x1n40 (n=2 for HV-ch0, n=3 for HV-ch1)	R	H
Channel n Stop Acquisition	0x1n40, 0x8040	R/W	I
High Voltage IMon/Temperature In	0x1n44 (n=2 for HV-ch0, n=3 for HV-ch1)	R	H
Shaped Trigger Delay	0x1n44, 0x8044	R/W	I
RC-CR2 Smoothing Factor	0x1n54, 0x8054	R/W	I
Input Rise Time	0x1n58, 0x8058	R/W	I
Trapezoid Rise Time	0x1n5C, 0x805C	R/W	I
Trapezoid Flat Top	0x1n60, 0x8060	R/W	I
Peaking Time	0x1n64, 0x8064	R/W	I
Decay Time	0x1n68, 0x8068	R/W	I
Trigger Threshold	0x1n6C, 0x806C	R/W	I
Trigger Hold-Off Width	0x1n74, 0x8074	R/W	I
Peak Hold-Off	0x1n78, 0x8078	R/W	I
Baseline Hold-Off	0x1n7C, 0x807C	R/W	I
DPP Algorithm Control	0x1n80, 0x8080	R/W	I
Shaped Trigger Width	0x1n84, 0x8084	R/W	I
Channel n Status	0x1n88	R	I
AMC Firmware Revision	0x1n8C	R	I
DC Offset	0x1n98, 0x8098	R/W	I
DPP Algorithm Control 2	0x1nA0, 0x80A0	R/W	I
Input Dynamic Range	0x1nB4, 0x80B4	W	I
Trapezoid Baseline Offset	0x1nB8, 0x80B8	R/W	I
Individual Software Trigger	0x1nC0, 0x80C0	W	I
Fine Gain	0x1nC4, 0x80C4	R/W	I
Energy skimming LLD	0x1nC8, 0c80C8	R/W	I
Energy skimming ULD	0x1nCC, 0x8nCC	R/W	I
Derivative Zero Compensation	0x1nD0, 0x80D0	R/W	I
Veto Width	0x1nD4, 0x80D4	R/W	I
TRG-IN Counter	0x1nF0	R	I
Board Configuration	0x8000, 0x8004 (BitSet), 0x8008 (BitClear)	R/W	C
Aggregate Organization	0x800C	R/W	C
Record Length	0x8020	R/W	C
Acquisition Control	0x8100	R/W	C
Acquisition Status	0x8104	R	C
Software Trigger	0x8108	W	C
Global Trigger Mask	0x810C	R/W	C

Front Panel TRG-OUT (GPO) Enable Mask	0x8110	R/W	C
Front Panel I/O Control	0x811C	R/W	C
Channel Enable Mask	0x8120	R/W	C
ROC FPGA Firmware Revision	0x8124	R	C
Board Info	0x8140	R	C
Event Size	0x814C	R	C
Fan Speed Control	0x8168	R/W	C
Run/Start/Stop Delay	0x8170	R/W	C
Board Failure Status	0x8178	R	C
Disable External Trigger	0x817C	R/W	C
Trigger Validation Mask	0x8188 (ch0), 0x818C (ch1)	R/W	I
Readout Control	0xEF00	R/W	C
Readout Status	0xEF04	R	C
Aggregate Number per BLT	0xEF1C	R/W	C
Scratch	0xEF20	R/W	C
Software Reset	0xEF24	W	C
Software Clear	0xEF28	W	C
Configuration Reload	0xEF34	W	C
Configuration ROM Checksum	0xF000	R	C
Configuration ROM Checksum Length BYTE 2	0xF004	R	C
Configuration ROM Checksum Length BYTE 1	0xF008	R	C
Configuration ROM Checksum Length BYTE 0	0xF00C	R	C
Configuration ROM Constant BYTE 2	0xF010	R	C
Configuration ROM Constant BYTE 1	0xF014	R	C
Configuration ROM Constant BYTE 0	0xF018	R	C
Configuration ROM C Code	0xF01C	R	C
Configuration ROM R Code	0xF020	R	C
Configuration ROM IEEE OUI BYTE 2	0xF024	R	C
Configuration ROM IEEE OUI BYTE 1	0xF028	R	C
Configuration ROM IEEE OUI BYTE 0	0xF02C	R	C
Configuration ROM Board Version	0xF030	R	C
Configuration ROM Board Form Factor	0xF034	R	C
Configuration ROM Board ID BYTE 1	0xF038	R	C
Configuration ROM Board ID BYTE 0	0xF03C	R	C
Configuration ROM PCB Revision BYTE 3	0xF040	R	C
Configuration ROM PCB Revision BYTE 2	0xF044	R	C
Configuration ROM PCB Revision BYTE 1	0xF048	R	C
Configuration ROM PCB Revision BYTE 0	0xF04C	R	C
Configuration ROM FLASH Type	0xF050	R	C
Configuration ROM Board Serial Number BYTE 1	0xF080	R	C
Configuration ROM Board Serial Number BYTE 0	0xF084	R	C
Configuration ROM VCXO Type	0xF088	R	C

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High Voltage VSet

Set the channel voltage value (V)

Address	0x1n20 (n=2 for HV-ch0, n=3 for HV-ch1)
Mode	R/W
Attribute	H

Bit	Description
[15:0]	Channel voltage value in steps of 0.1 V. For example to set 2500 V write 25000.
[31:16]	Reserved

High Voltage ISet

Set the maximum current limit that can be supplied by a channel

Address	0x1n24 (n=2 for HV-ch0, n=3 for HV-ch1)
Mode	R/W
Attribute	H

Bit	Description
[15:0]	Set the maximum current in steps of 10 nA (780 series) and 50 nA (DT5790). For example to set 2000 uA, write 40000 for DT5790 and 200000 for 780 series.
[31:16]	Reserved

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High Voltage Ramp Up

Set the ramp up voltage value in V/s

Address	0x1n28 (n=2 for HV-ch0, n=3 for HV-ch1)
Mode	R/W
Attribute	H

Bit	Description
[8:0]	Ramp up in V/s.
[31:9]	Reserved

High Voltage Ramp Down

Set the ramp down voltage value in V/s

Address	0x1n2C (n=2 for HV-ch0, n=3 for HV-ch1)
Mode	R/W
Attribute	H

Bit	Description
[8:0]	Ramp down in V/s.
[31:9]	Reserved

High Voltage VMax

VMax is the hardware value that can be programmed by the user to limit the maximum voltage of a channel. If a value VSet > VMax is erroneously programmed, the HV channels supplies up to VMax and marks bit[6] of register High Voltage Status 0x1n38.

Address	0x1n30 (n=2 for HV-ch0, n=3 for HV-ch1)
Mode	R/W
Attribute	H

Bit	Description
[7:0]	Maximum voltage value in steps of 20 V for 780 series and DT5790, and 2 V for 780SD boards. Note: the VMax resolution of 2 V is supported for HV firmware release greater than 2.2. For HV firmware release less than 2.2 the VMax resolution is 20 V.
[31:8]	Reserved

High Voltage Control

This register manages the high voltage power and monitor mode

Address   0x1n34 (n=2 for HV-ch0, n=3 for HV-ch1)
Mode   R/W
Attribute   H

Bit	Description
[0]	Manages the Power ON/OFF of the HV channel. Options are: 0: HV channel OFF; 1: HV channel ON.
[1]	Manages how the channel shuts down. This setting applies both when the user shuts the channel down and when the channel automatically shuts down due to an alarm (see register High Voltage Status 0x1n38). Options are: 0: kill mode, the HV channel shuts down instantaneously; 1: ramp mode, the HV channel shuts down with a rate of V/s as defined by the HV Ramp Down register, 0x1n2C.
[6:2]	Reserved
[7]	Manages the monitor mode of the HV channel. Options are: 0: Register 0x1n40 used to monitor the HV Channel VMon, register 0x1n44 used to monitor the HV Channel IMon, register 0x1n38 used to monitor the HV Channel Status; 1: Register 0x1n40 used to monitor the Analog In, register 0x1n44 used to monitor the Temperature In, register 0x1n38 used to monitor the A639 Firmware Release.
[31:8]	Reserved

Number of Events per Aggregate

Each channel has a fixed amount of RAM memory to save the events. The memory is divided into a programmable number of buffers, called "aggregates", whose number of events can be programmed by this register. The maximum number of events per aggregate depends on the aggregate size (which is defined by the number of aggregates per memory, 0x800C), and the event size (which is defined by the record length, 0x1n20, the acquisition mode and the event format, 0x8000).

Note: it is usually recommended to keep this value high to optimize the readout, except in case of small input rate, where it is recommended to use a smaller value (even 1). Since the memory cannot be read until the aggregate is full, setting a a small number of events per aggregate makes the events ready to be read in a shorter time scale. Users can also force the readout through the flush register, 0x1n3C.

Address	0x1n34, 0x8034
Mode	R/W
Attribute	I

Bit	Description
[9:0]	Number of events per aggregate.
[31:10]	Reserved.

High Voltage Status/A639 Firmware Release

According to the monitor mode value (bit[7] of register High Voltage Control 0x1n34) this register corresponds to:
1. monitor mode = 0, HV channel status (see the bit description for more details). NOTE: in case of bit[3], bit[9], bit[10] or bit[14] = 1 the HV channel is turned off according to Power Down Mode (see HV Channel Control register, 0x1n34);
2. monitor mode = 1, A639 firmware release. For example, for a firmware release 1.03, the register value is 0x103, where 1 corresponds to the register word high byte, and 3 corresponds to the register word low byte.

Address	0x1n38 (n=2 for HV-ch0, n=3 for HV-ch1)
Mode	R
Attribute	H

Bit	Description
[0]	1 = HV power ON
[1]	1 = HV channel rump up
[2]	1 = HV channel rump down
[3]	1 = HV channel is in Over Current (IMon > ISet)
[4]	1 = HV channel is in Over Voltage (VMon > VSet + 2%)
[5]	1 = HV channel is in Under Voltage (VMon < VSet - 2%)
[6]	1 = HV channel is over Maximum Voltage (Vout > VMax)
[7]	1 = HV channel is over Maximum Current (IMon > hardware maximum IOut)
[8]	1 = Temperature warning. The temperature of the HV channel is greater than 80°C.
[9]	1 = Over Temperature. The temperature of the HV channel is greater than 125°C.
[10]	1 = HV channel is disabled for an active external inhibit.
[11]	1 = Calibration error. There is a calibration error on the HV channel.
[12]	1 = Alarm Reset. The HV channel is resetting the alarms.
[13]	1 = HV channel is shutting down
[14]	1 = Maximum Power. The HV output power is greater than 4 W.
[15]	1 = Fan speed high
[31:16]	Reserved

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Pre Trigger

The Pre Trigger defines the number of samples before the trigger in the waveform saved into memory.

Address	0x1n38, 0x8038
Mode	R/W
Attribute	I

Bit	Description
[10:0]	Number of pre trigger samples +4 samples. Each sample corresponds to 10 ns.
[31:11]	Reserved

Data Flush

Data events are grouped into aggregates of N events each, where N can be programmed through register 0x1n34. As soon as an aggregate reaches N events then it is ready to be read. An aggregate containing a number of events smaller than N cannot be read and must be forced to flush its current data. This is for example the case of low input rate, where the board might appear empty (no data) even if a small amount of events is already stored in the buffer, or at the end of the run where the last aggregate might be incomplete. A write access to this register forces the read of the current incomplete aggregate.

Address   0x1n3C, 0x803C
Mode   W
Attribute   I

Bit	Description
[31:0]	A write access to this register causes the flush of the current aggregate.

High Voltage VMon/Analog In

According to the monitor mode value (bit[7] of register High Voltage Control 0x1n34) this register corresponds to:
1. monitor mode = 0, HV channel VMon;
2. monitor mode = 1, voltage between Pin 3 (EXT_ANALOG) and Pin 1 (GND) of the DB9 connector related to the selected channel.

Address	0x1n40 (n=2 for HV-ch0, n=3 for HV-ch1)
Mode	R
Attribute	H

Bit	Description
[15:0]	If monitor mode = 0, these bits read the HV channel VMon. VMon is equal to the content of the register multiplied by the resolution of 0.1 V. For example, if the register value is 10238, VMon = 1023.8 V. If monitor mode = 1, these bits read the voltage between Pin 3 (EXT_ANALOG) and Pin 1 (GND) of the DB9 connector related to the selected channel. The voltage value is equal to the content of the register multiplied by the inverse of the resolution of 0.001 V.
[31:16]	Reserved

Channel n Stop Acquisition

This register performs the stop acquisition of a single channel n. If bit[0] = 0, then channel n starts the acquisition as the global run is active, together with any other enabled channel. Note that if the global run is not active, writing 0 in this register does not produce any effect. If bit[0] = 1 and the global run is active, then channel n stops the acquisition independently on the other enabled channels.

It is possible to drive the start/stop acquisition independently on each channel by the following steps:
1. Set the individual stop acquisition on each desired channel (bit[0] = 1).
2. Enable the global run through register Acquisition Control 0x8100 (no channel will start the acquisition);
3. Set bit[0] = 0 to start the individual acquisition, then bit[0] = 1 to stop it.
4. When all channels are individually stopped, disable the global run.

Address	0x1n40, 0x8040
Mode	R/W
Attribute	I

Bit	Description
[0]	Options are: 0: Run; 1: Stop.
[31:1]	Reserved

High Voltage IMon/Temperature In

According to the monitor mode value (bit[7] of register High Voltage Control 0x1n34) this register corresponds to:

1. monitor mode = 0, this register provides the monitored current value;

2. monitor mode = 1, this register is used to read the value of the resistance between Pin 8 (EXT_TEMP) and Pin 1 (GND) of the DB9 connector related to the selected channel.

Address	0x1n44 (n=2 for HV-ch0, n=3 for HV-ch1)
Mode	R
Attribute	H

Bit	Description
[15:0]	If monitor mode = 0, these bits provide the monitored current value. The value of Imon is equal to the content of the register multiplied by the resolution (780 series: 10 nA; DT5790: 50 nA). For example, if Imon Reg = 10238 then IMon = 102.38 uA (DT5780). If Imon Reg = 10238 then IMon = 511.9 uA (DT5790). If Monitor Mode = 1, these bits are used to read the value of the resistance between Pin 8 (EXT_TEMP) and Pin 1 (GND) of the DB9 connector related to the selected channel. The resistance value is that of a temperature probe PT100 or PT1000. The resistance value is equal to the content of the register multiplied by the resolution of 0.1 Ohm. For example, if Reg value = 1234, then the resistance value = 123.4 Ohm.
[31:16]	Reserved

Shaped Trigger Delay

Set a programmable delay on the shaped trigger signal. NOTE: the trapezoid peaking is not affected by this register, so for high delay the energy value might have no sense. Indeed, this register is mainly useful to set a veto between two detectors with different timing response, like a fast scintillator and a HPGe. In that case, the delay is applied to the scintillator trigger to match the HPGe, but the energy information from the scintillator is not relevant.

Address	0x1n44, 0x8044
Mode	R/W
Attribute	I

Bit	Description
[15:0]	Delay expressed in steps of 10 ns
[31:16]	Reserved

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RC-CR2 Smoothing Factor

Defines the number of samples of a moving average filter used for the RC-CR2 signal formation.

Address   0x1n54, 0x8054
Mode   R/W
Attribute   I

Bit	Description
[5:0]	Write the desired number of samples. Options are: 0x1: 1 sample; 0x2: 2 samples; 0x4: 4 samples; 0x8: 8 samples; 0x10: 16 samples; 0x20: 32 samples.
[31:6]	Reserved

Input Rise Time

This register defines the time constant of the derivative component of the PHA fast discriminator filter.
In case of RC-CR2 this value must be equal (or 50% more) to the input rising edge, in such a way the RC-CR2 peak value corresponds to the height of the input signal.

Address   0x1n58, 0x8058
Mode   R/W
Attribute   I

Bit	Description
[11:0]	Rise Time expressed in sampling clock units (10 ns).
[31:12]	Reserved.

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Trapezoid Rise Time

Sets the Trapezoid Rise Time, i.e. the Shaping Time of the energy filter.
Note: the sum of Trapezoid Rise Time and Trapezoid Flat Top (see register 0x1n60) should not exceed 40 us.

Address   0x1n5C, 0x805C
Mode   R/W
Attribute   I

Bit	Description
[11:0]	Trapezoid Rise Time value expressed in sampling clock unit (10 ns).
[31:12]	Reserved

Trapezoid Flat Top

Sets the Trapezoid Flat Top width. Note: the sum of the Trapezoid Rise Time (see register 0x1n5C) and Trapezoid Flat Top should not exceed 40 us.

Address   0x1n60, 0x8060
Mode   R/W
Attribute   I

Bit	Description
[11:0]	Trapezoid Flat Top duration expressed in sampling clock unit (10 ns).
[31:12]	Reserved

Peaking Time

Position in the flat top region where the samples are used for the calculation of the peak height. The peaking time is referred to the trigger position or to the trigger validation signal according to the trigger mode. Check the User Manual for further details.

Address   0x1n64, 0x8064
Mode   R/W
Attribute   I

Bit	Description
[11:0]	Peaking time expressed in sampling clock unit (10 ns).
[31:12]	Reserved

Decay Time

This register corresponds to the trapezoid pole-zero cancellation. The user must set this register equal to the decay time of the pre-amplifier.

Address   0x1n68, 0x8068
Mode   R/W
Attribute   I

Bit	Description
[15:0]	Decay time expressed in sampling clock unit (10 ns).
[31:16]	Reserved

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Trigger Threshold

Threshold of the Trigger and Timing filter of the DPP-PHA algorithm.

Address   0x1n6C, 0x806C
Mode   R/W
Attribute   I

Bit	Description
[13:0]	Trigger Threshold value expressed in LSB unit. The threshold arms the RC-CR2 signal and the event is identified (trigger) on the RC-CR2 zero crossing.
[31:14]	Reserved

Trigger Hold-Off Width

The Trigger Hold-Off is a logic signal of programmable width generated by the trigger logic in correspondence of the fast discriminator output. Other triggers are inhibited for the overall Trigger Hold-Off duration.

Address	0x1n74, 0x8074
Mode	R/W
Attribute	I

Bit	Description
[15:0]	Trigger Hold-Off width expressed in steps of 10 ns.
[31:16]	Reserved

Peak Hold-Off

The Peak Hold-off starts at the end of the trapezoid flat top and defines how close must be two trapezoids to be considered piled-up. Zero is the case where the flat top of one trapezoid starts exactly at the end of the flat top of the previous one.

Address   0x1n78, 0x8078
Mode   R/W
Attribute   I

Bit	Description
[9:0]	Peak hold-off expressed in steps of 80 ns.
[31:10]	Reserved

Baseline Hold-Off

The Baseline Hold-off defines how long the baseline is kept frozen beyond the end of the trapezoid; after that time, the baseline starts to be calculated again. Depending on the baseline mean value, the baseline itself might take some time to recover after the hold-off.

Address	0x1n7C, 0x807C
Mode	R/W
Attribute	I

Bit	Description
[9:0]	Baseline Hold-Off expressed in steps of the sampling clock unit (10 ns).
[31:10]	Reserved

DPP Algorithm Control

Management of the DPP algorithm features

Address	0x1n80, 0x8080
Mode	R/W
Attribute	I

Bit	Description
[5:0]	Trapezoid Rescaling: the trapezoid generated by the energy filter in the FPGA is k*M times higher than the input pulse, where k is the trapezoid rise time and M is the input signal decay time. This value is internally represented over 48 bits and must be rescaled to 15 bit (i.e. 32K channels) before it is used to calculate the energy value (=pulse height). The trapezoid rescaling SHF defines how many bits are right shifted (i.e. division by 2^{SHF}) before applying the mask with 0x3FFF and extract the 15 bit value of the pulse height. Use a value for SHF such that $2^{SHF} <= M*k < 2^{(SHF+1)}$. The parameter SHF in conjunction with the fine gain (see register 0x1nC4) acts as a digital gain for the energy scale.
[11:6]	Reserved
[13:12]	Peak Mean: corresponds to the number of samples for the averaging window of the trapezoid height calculation. Note: for a correct energy calculation the Peak Mean should be contained in the flat region of the Trapezoid Flat Top. Options are: 00: 1 sample; 01: 4 samples; 10: 16 samples; 11: 64 samples.
[14]	Reserved
[15]	Enable Spike Rejection. When this bit is enabled triggers are inhibited until the "Input Rise Time" duration is reached (register 0x1n58). In case of noisy signals this feature is quite useful to avoid triggering on spikes on the rise time of the RC- CR2 signal, which do not corresponds to real signals. This feature allows also the user to set lower values of the trigger threshold. Options are: 0: disabled; 1: enabled.
[16]	Invert Input: Individual setting for the input signal inversion. The DPP-PHA algorithm is designed to work with positive signals. In case of negative polarity the signal is inverted in the FPGA to make it positive. Options are: 0: positive polarity; 1: negative polarity.
[17]	Pulse Identification on RC-CR or RC-CR2 signal. Events are usually identified on the zero crossing of the RC-CR2 signal. For fast input signals it is possible to trigger on the zero crossing of the RC-CR signal (which becomes bipolar for fast signals). Options are: 0: Trigger on RC-CR2; 1: Trigger on RC-CR.
[19:18]	Trigger Mode. Options are: 00: Normal mode. Each channel self-triggers independently from the other channels; 01: Neighbour mode. The channel self-trigger is not used for the acquisition, it is propagated to mother board for processing or outside through GPO/LVDS. Each channel triggers according to the individual trigger logic (refer to register 0x8180 + 4n). Note: the user must take care of the proper trapezoid peaking, which is referred to the individual trigger logic; 10: Coincidence mode. Each channel can self-trigger independently from the other channels and it saves the event only when a validation signal occurs within its coincidence window (register 0x1n84); 11: Anti-coincidence mode. Each channel can self-trigger independently from the other channels and it saves the event only when no validation signal occurs within its coincidence window (register 0x1n84).

[22:20]	Baseline averaging window: number of samples for the baseline average calculation. Options are: 000: the baseline is not evaluated, and the energy values are not subtracted by the baseline; 001: 16 samples; 010: 64 samples; 011: 256 samples; 100: 1024 samples; 101: 4096 samples; 110: 16384 samples; 111: 32768 samples;
[23]	Reserved.
[24]	Disable Self-Trigger, the self-trigger is not used for the acquisition, nor for the propagation to the motherboard. Options are: 0 = self-trigger enabled; 1 = self-trigger disabled.
[25]	Reserved
[26]	Enable Roll-Over flag. When enabled, the algorithm creates a fake event with Time Stamp = 0, Energy = 0, PU = 1, bit[3] and bit[1] of EXTRAS = 1. See the Channel Aggregate data format in the User Manual for more details. Options are: 0: disabled; 1: enabled.
[27]	Reserved.
[28]	Enable energy skim. When enabled it allows the selection of the waveform within the LLD (register 0x1nC8) and ULD (register 0x1nCC). Options are: 0: disabled 1: enabled
[29]	Enable baseline restore clipping. When enabled it allows to disable the baseline calculation in case of events whose profile is not well defined and so not triggered by the fast timing filter. Options are: 0: disabled 1: enabled
[30]	TAC Mode: when enabled, the trapezoid is replaced by the input delayed signal and it is possible to acquire external signals having a flat top (e.g. TAC output). Options are: 0: disabled 1: enabled
[31]	Reserved.

Shaped Trigger Width

The Shaped Trigger (i.e. Fast Discriminator Output) is a logic signal generated by a channel in correspondence with its local self- trigger. It is used to propagate the trigger to the other channels of the board and to other external boards, as well as to feed the coincidence trigger logic.

Address   0x1n84, 0x8084
Mode   R/W
Attribute   I

Bit	Description
[9:0]	Shaped Trigger (Fast Discriminator Output) width in steps of 10 ns.
[31:8]	Reserved

Channel n Status

This register contains the status information of channel n.

Address   0x1n88
Mode   R
Attribute   I

Bit	Description
[1:0]	Reserved.
[2]	If 1, the SPI bus is busy.
[31:3]	Reserved.

AMC Firmware Revision

Returns the DPP firmware revision (mezzanine level).
To control the mother board firmware revision see register 0x8124.
For example: if the register value is 0xC3218303:
- Firmware Code and Firmware Revision are 131.3;
- Build Day is 21;
- Build Month is March;
- Build Year is 2012.
NOTE: since 2016 the build year started again from 0.

Address	0x1n8C
Mode	R
Attribute	I

Bit	Description
[7:0]	Firmware revision number.
[15:8]	Firmware DPP code. Each DPP firmware has a unique code.
[19:16]	Build Day (lower digit).
[23:20]	Build Day (upper digit).
[27:24]	Build Month. For example: 3 means March, 12 is December.
[31:28]	Build Year. For example: 0 means 2000, 12 means 2012. NOTE: since 2016 the build year started again from 0.

DC Offset

This register allows to adjust the baseline position (i.e. the 0 Volt) of the input signal on the ADC scale. The ADC scale ranges from 0 to 2^{NBit} - 1, where NBit is the number of bits of the on-board ADC. The DAC controlling the DC Offset has 16 bits, i.e. it goes from 0 to 65535 independently from the NBit value and the board type.

Typically a DC Offset value of 32K (DAC mid-scale) corresponds to about the ADC mid-scale. Increasing values of DC Offset make the baseline decrease. The range of the DAC is about 5% (typ.) larger than the ADC range, hence DAC settings close to 0 and 64K correspond to ADC respectively over and under range.

WARNING: before writing this register, it is necessary to check that bit[2] = 0 at 0x1n88, otherwise the writing process will not run properly!

Address	0x1n98, 0x8098
Mode	R/W
Attribute	I

Bit	Description
[15:0]	DC Offset value in DAC LSB unit.
[31:16]	Reserved.

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DPP Algorithm Control 2

This register controls the DPP features such as the source for the VETO mode, the TRG-OUT mode and the frequency of the flags counting for total and lost triggers.

Address   0x1nA0, 0x80A0
Mode   R/W
Attribute   I

Bit	Description
[5:0]	Set the source for the VETO mode. The veto duration can be defined through register 0x1nD4. Options are: 000000: None; 000001: Global Trigger from register 0x810C generates the veto. Note: coincidence mode (bit[19:18] = 0b10 @ 0x1n80) must be enabled to identify the global trigger as veto; 000010: Individual Trigger from register 0x8180 +4n generates the veto. Note: coincidence mode (bit[19:18] = 0b10 @ 0x1n80) must be enabled to identify the individual trigger as veto; 000100: Over saturation generates the veto; 001000: Under saturation generates the veto; 010000: Channel Trigger generates the veto i.e. any possible source of the channel trigger (Global Trigger, Individual Trigger, Software Trigger, Self Trigger) generates the veto. 100000: Global busy (OR of channel busy lines) generates the veto. This option is mainly suggested for neighbour trigger mode (bit[19:18] = 0b01 @ 0x1n80), when the trigger logic is the OR of the channels.
[7:6]	Reserved
[9:8]	Sets the channel probes to be propagated through the TRG-OUT front panel connector. The channel signal can be enabled through register 0x8110. Options are: 00: Normal mode, it is propagated the trigger (output of the timing filter); 01: Single Channel Analyzer (LLD set at 0x1nC8, ULD set at 0x1nCC registers); 10: Digital Probe: the TRG-OUT signal is generated as soon as the probe is generated, e.g. if the digital probe is set to be the PEAKING signal (see bit[23:20]@0x8000), as soon as the PEAKING signal comes, the TRG-OUT signal is generated. This mode is mainly intended for debugging purposes; 11: Channel Self-Trigger.
[10]	Reserved.
[11]	Inhibit the global trigger coming from TRG-IN and use it for counting only. The pulses coming to the TRG-IN connector are counted in the 0x1nF0 register. Options are: 0: Global trigger from TRG-IN not inhibited 1: Global trigger from TRG-IN inhibited
[15:12]	Reserved
[17:16]	Set the frequency of the flags to count total and lost triggers (flag at bit 22 of energy word). Options are: 00: Tag every 1024 triggers; 01: Tag every 128 triggers; 10: Tag every 8K triggers.
[31:18]	Reserved

Input Dynamic Range

The analog input stage of 780 series has 4 programmable gains. This register modifies the analog gains of channel n and therefore its input dynamics.

Address	0x1nB4, 0x80B4
Mode	W
Attribute	I

Bit	Description
[3:0]	Selects the channel input range of 780 series. Options are: 0x5: 0.6 Vpp; 0x6: 1.4 Vpp; 0x9: 3.7 Vpp; 0xA: 9.5 Vpp.
[31:4]	Reserved

Trapezoid Baseline Offset

This register adds a fixed value to the baseline of the trapezoid.

Address   0x1nB8, 0x80B8
Mode   R/W
Attribute   I

Bit	Description
[14:0]	Trapezoid baseline offset value.
[31:15]	Reserved

Individual Software Trigger

Sends the Software Trigger to the individual channel n. This is not affected by the Trigger Validation, i.e. the Individual Software Trigger can be issued also when coincidences are enabled without being affected.

Address	0x1nC0, 0x80C0
Mode	W
Attribute	I

Bit	Description
[31:0]	A write access to this register enables a software trigger for channel n.

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Fine Gain

The trapezoidal filter mathematically produces a signal whose amplitude is proportional to the input signal, with multiplicative factors depending on k (Trap. Rise Time) and M (Decay Time). In the DPP-PHA algorithm, the user must set two parameters: the Trapezoid Rescaling (SHF) (bits[5:0] of register 0x1n80) and the Fine Gain (f). Given a desired Fine Gain (fg), the user must write in the register: $f = 64K*fg*2^{SHF}/(k*M)$, where SHF is the closest power of 2 to k*M (refer to bits[5:0] of register 0x1n80), and 64K is the normalization over 16 bits.

Address   0x1nC4, 0x80C4
Mode   R/W
Attribute   I

Bit	Description
[15:0]	Fine Gain value.
[31:16]	Reserved

Energy skimming LLD

The Energy Skim allows the user to select a region in the (not calibrated) energy spectrum and to inspect the waveforms that provides the energy values falling into the selected interval defined by a Lower Level Discriminator (LLD) and an Upper Level Discriminator (ULD).

Address   0x1nC8, 0c80C8
Mode   R/W
Attribute   I

Bit	Description
[13:0]	Value of the energy skimming Lower Level Discriminator (LLD).
[31:14]	Reserved

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Energy skimming ULD

The Energy Skim allows the user to select a region in the (not calibrated) energy spectrum and to inspect the waveforms that provides the energy values falling into the selected interval defined by a Lower Level Discriminator (LLD) and an Upper Level Discriminator (ULD).

Address	0x1nCC, 0x8nCC
Mode	R/W
Attribute	I

Bit	Description
[13:0]	Value of the energy skimming Upper Level Discriminator (ULD).
[31:14]	Reserved

Derivative Zero Compensation

This register allows to Pole Zero compensate the Trigger and Timing filter summing a fraction of the input signal. The RC-CR2 fast discriminator acts taking the input signal, delaying it by a fixed quantity, and subtract this delayed signal from the input one (first derivative). This operation is done twice. This register acts after the first subtraction operation. In more details it comes in play as:

$Vb[n] = Vin[n] - Vin[n-b] + A*Vin[n-b]/65536$ where "b" is the delay value and A is the value written in this register.

Since the register is 16 bit, the A maximum value is 65535. It means that it is possible to sum a fraction of the input signal after the first subtraction operation. This allows to minimize the overshoot after the first derivative operation due to the subtraction involving exponential signals.

Address	0x1nD0, 0x80D0
Mode	R/W
Attribute	I

Bit	Description
[15:0]	Value of the fraction coefficient A in the compensation formula described in the register description.
[31:16]	Reserved

Veto Width

When a veto is enabled through register 0x1nA0, this register sets the veto duration.
Note: A Veto Width equal to 0 means that the veto lasts for the duration of the signal that generated it. A Veto Width different from 0 sets the veto duration by the amount of time written in the register.

Address	0x1nD4, 0x80D4
Mode	R/W
Attribute	I

Bit	Description
[23:0]	Value of the VETO width in steps of 10 ns.
[31:24]	Reserved

TRG-IN Counter

This register can be used to count external pulses connected to TRG-IN front panel connector: the counter is reset at start of run or by S-IN. It is an individual register although all channels count the same value. Set bit[11]=1@0x1nA0 to inhibit the global trigger coming from TRG-IN and use it for counting only.

Address   0x1nF0
Mode   R
Attribute   I

Bit	Description
[31:0]	Counter value.

Board Configuration

This register contains general settings for the board configuration.

Address   0x8000, 0x8004 (BitSet), 0x8008 (BitClear)
Mode   R/W
Attribute   C

Bit	Description
[0]	Enable Automatic Data Flush: in case of very slow rate, this command forces the automatic data readout in a time window of 16-32 ms, even if the buffer is not completed. Options are: 0: disabled (default value); 1: enabled.
[1]	Reserved: must be 0
[2]	Trigger Propagation: enables the propagation of the individual trigger from mother board individual trigger logic to the mezzanine. This is required in case of coincidence trigger mode
[3]	Reserved: must be 0
[4]	Reserved: must be 1.
[7:5]	Reserved: must be 0
[8]	Individual trigger: must be 1
[9]	Reserved. Must be 0.
[10]	Reserved: must be 0
[11]	Dual Trace: in oscilloscope or mixed mode, it is possible to plot two different waveforms. When the dual trace is enabled, the samples of the two signals are interleaved, thus each waveform is recorded at half of the ADC frequency. The two analog probes can be selected from bits[13:12] and bits[15:14] respectively.
[13:12]	Analog Probe 1: Selects which signal is associated to the Analog trace 1 in the readout data. Options are: 00: Input; 01: RC-CR (input 1st derivative); 10: RC-CR2 (input 2nd derivative); 11: Trapezoid (output of the trapezoid filter).
[15:14]	Analog Probe 2: Selects which signal is associated to the Analog trace 2 in the readout data. Options are: 00: Input; 01: Threshold, which is referred to the RC-CR2 signal; 10: Trapezoid - Baseline; 11: Baseline (of the trapezoid).
[16]	Waveform Recording: enables the data recording of the waveform. The user must define the number of samples to be saved in the Record Length (register 0x1n20). According to the Analog Probe option one or two waveforms are saved. Options are: 0: disabled; 1: enabled.
[17]	Energy Mode: When enabled, the height of the trapezoid (which corresponds to the peak amplitude of the pulses) is saved into the event data (last word of the event). Options are: 0: Energy Mode disabled. 1: Energy Mode enabled.
[18]	Time Stamp Recording: When enabled, the time stamp of the event (which corresponds to the zero crossing in the timing filter) is saved into the event data (first word of the event). 0: Time Stamp recording disabled. 1: Time Stamp recording enabled.
[19]	Reserved: must be 0

[23:20]	Digital Virtual Probe 1: when the mixed (or oscilloscope) mode is enabled, the following digital virtual probes can be selected. Check the User Manual for further details. 0000: "Peaking", shows where the energy is calculated; 0001: "Armed", digital input showing where the Timing Filter crosses the Threshold; 0010: "Peak Run", starts with the trigger and last for the whole event; 0011: "Pile-up", shows where a pile-up event occurred; 0100: "Peaking", shows where the energy is calculated; 0101: "Trg Validation Win", digital input showing the trigger validation acceptance window TVAW; 0110: "Baseline freeze", shows where the algorithm stops calculating the baseline and its value is frozen; 0111: "TRG Holdoff", shows the trigger hold-off parameter; 1000: "Trg Validation", shows the trigger validation signal TRG_VAL ; 1001: "Acq Busy", this is 1 when the board is busy (saturated input signal or full memory board) or there is a veto; 1010: "Zero Cross. Win.", shows the Zero Crossing Acceptance Windows width; 1011: "Ext TRG", shows the external trigger, when available; 1100: "Busy", shows when the memory board is full; 1101: "Peak Ready", shows after the Peak Mean time. See for reference bit[13:12] of the DPP Control Algorithm (0x1n80) register.
[24]	Enable the FORMAT Word in the aggregate data. It must be 1.
[25]	Reserved
[28:26]	Digital Virtual Probe 2. Options are: 000 = Trigger; Other options are reserved.
[31:29]	Reserved

Aggregate Organization

The internal memory of the digitizer can be divided into a programmable number of aggregates, where each aggregate contains a specific number of events. This register defines how many aggregates can be contained in the memory. Note: this register must not be modified while the acquisition is running.

Address	0x800C
Mode	R/W
Attribute	C

Bit	Description
[3:0]	Aggregate Organization Nb: the number of aggregates is equal to $N\_aggr = 2^{Nb}$. The corresponding values of Nb and N_aggr are: Nb: N_aggr 0x0 - 0x1: Not used 0x2 : 4 0x3 : 8 0x4 : 16 0x5 : 32 0x6 : 64 0x7 : 128 0x8 : 256 0x9 : 512 0xA : 1024
[31:4]	Reserved: must be 0

Record Length

Sets the record length for the waveform acquisition

Address	0x8020
Mode	R/W
Attribute	C

Bit	Description
[15:0]	Number of samples in the waveform according to the formula Ns = N * 2, where Ns is the record length and N is the register value. For example, write N = 10 to acquire 20 samples. Each sample corresponds to 10 ns.
[31:16]	Reserved

Acquisition Control

This register manages the acquisition settings.

Address   0x8100
Mode   R/W
Attribute   C

Bit	Description
[1:0]	Start/Stop Mode Selection (default value is 00). Options are: 00 = SW CONTROLLED. Start/stop of the run takes place on software command by setting/resetting bit[2] of this register; 01 = S-IN/GPI CONTROLLED (S-IN for VME, GPI for Desktop/NIM). Acquisition must be armed by setting bit[2] = 1, then the run can optionally START/STOP ON LEVEL or START ON EDGE according to bit[11] (NOTE: the START ON EDGE option is implemented from ROC FPGA fw revision 4.22 on); 10 = FIRST TRIGGER CONTROLLED. If the acquisition is armed (i.e. bit[2] = 1), then the run starts on the first trigger pulse (rising edge on TRG-IN); this pulse is not used as input trigger, while actual triggers start from the second pulse. The stop of Run must be SW controlled (i.e. bit[2] = 0); 11 = LVDS CONTROLLED (VME only). It is like option 01 but using LVDS (RUN) instead of S-IN. The LVDS can be set using registers 0x811C and 0x81A0.
[2]	Acquisition Start/Arm (default value is 0). When bits[1:0] = 00, this bit acts as a Run Start/Stop. When bits[1:0] = 01, 10, 11, this bit arms the acquisition and the actual Start/Stop is controlled by an external signal. Options are: 0 = Acquisition STOP (if bits[1:0]=00); Acquisition DISARMED (others); 1 = Acquisition RUN (if bits[1:0]=00); Acquisition ARMED (others).
[3]	Reserved
[5:4]	Reserved
[6]	PLL Reference Clock Source (Desktop/NIM only). Default value is 0. Options are: 0 = internal oscillator (50 MHz); 1 = external clock from front panel CLK-IN connector. NOTE: this bit is reserved in case of VME boards.
[31:7]	Reserved

Acquisition Status

This register monitors a set of conditions related to the acquisition status.

Address   0x8104
Mode   R
Attribute   C

Bit	Description
[1:0]	Reserved.
[2]	Acquisition Status. It reflects the status of the acquisition and drivers the front panel 'RUN' LED. Options are: 0 = acquisition is stopped ('RUN' is off); 1 = acquisition is running ('RUN' lits).
[3]	Event Ready. Indicates if any events are available for readout. Options are: 0 = no event is available for readout; 1 = at least one event is available for readout. NOTE: the status of this bit must be considered when managing the readout from the digitizer.
[4]	Event Full. Indicates if at least one channel has reached the FULL condition. Options are: 0 = no channel has reached the FULL condition; 1 = the maximum number of events to be read is reached.
[5]	Clock Source. Indicates the clock source status. Options are: 0 = internal (PLL uses the internal 50 MHz oscillator as reference); 1 = external (PLL uses the external clock on CLK-IN connector as reference).
[6]	Reserved
[7]	PLL Unlock Detect. This bit flags a PLL unlock condition. Options are: 0 = PLL has had an unlock condition since the last register read access; 1 = PLL has not had any unlock condition since the last register read access. NOTE: flag can be restored to 1 via read access to register 0xEF04.
[8]	Board Ready. This flag indicates if the board is ready for acquisition (PLL and ADCs are correctly synchronized). Options are: 0 = board is not ready to start the acquisition; 1 = board is ready to start the acquisition. NOTE: this bit should be checked after software reset to ensure that the board will enter immediately in run mode after the RUN mode setting; otherwise, a latency between RUN mode setting and Acquisition start might occur.
[14:9]	Reserved.
[15]	S-IN (VME boards) or GPI (DT/NIM boards) Status. Reads the logical level on S-IN (GPI) front panel connector.
[16]	TRG-IN Status. Reads the logical level on TRG-IN front panel connector.
[31:17]	Reserved.

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Software Trigger

Writing this register causes a software trigger generation which is propagated to all the enabled channels of the board.

Address   0x8108
Mode   W
Attribute   C

Bit	Description
[31:0]	Write whatever value to generate a software trigger.

Global Trigger Mask

This register sets which signal can contribute to the global trigger generation.

Address   0x810C
Mode   R/W
Attribute   C

Bit	Description
[0]	Enables the trigger request from channel 0 to participate to the global trigger logic. Options are: 0 = disabled; 1 = enabled.
[1]	Enables the trigger request from channel 1 to participate to the global trigger logic. Options are: 0 = disabled; 1 = enabled.
[19:2]	Reserved
[23:20]	Majority Coincidence Window. Sets the time window (10 ns steps) for the majority coincidence. Majority level must be set different from 0 through bits[26:24].
[26:24]	Majority Level. Sets the majority level for the global trigger generation. Allowed level values are 0 and 1. For a level m, the trigger fires when at least m+1 of the trigger requests are generated by the enabled channels (bits [1:0]) .
[29:27]	Reserved
[30]	External Trigger. When enabled, the external trigger on TRG-IN participates to the global trigger generation in logic OR with the other enabled signals (bit[31] and bits[1:0]). Options are: 0 = disabled; 1 = enabled.
[31]	Software Trigger. When enabled, the software trigger participates to the global trigger signal generation in logic OR with the other enabled signals (bit[30] and bits[1:0]). Options are: 0 = disabled; 1 = enabled.

Front Panel TRG-OUT (GPO) Enable Mask

This register sets which signal can contribute to generate the signal on the front panel TRG-OUT LEMO connector (GPO in case of DT and NIM boards).

Address   0x8110
Mode   R/W
Attribute   C

Bit	Description
[0]	Enables the trigger request from channel 0 to participate to the TRG-OUT logic. Options are: 0 = disabled; 1 = enabled.
[1]	Enables the trigger request from channel 1 to participate to the TRG-OUT logic. Options are: 0 = disabled; 1 = enabled.
[3:2]	Reserved
[7:4]	Reserved
[9:8]	TRG-OUT (GPO) Generation Logic. The enabled trigger requests can be combined to generate the TRG-OUT (GPO) signal. Options are: 00 = OR; 01 = AND; 10 = Majority; 11 = Reserved.
[12:10]	Majority Level. Sets the majority level for the TRG-OUT (GPO) signal generation. Allowed level values are 0 and 1. For a level m, the trigger fires when at least m+1 of the trigger requests are generated by the enabled channels (bits [1:0]) .
[29:13]	Reserved
[30]	External Trigger. When enabled, the external trigger on TRG-IN can participate in the TRG-OUT (GPO) signal generation in logic OR with the other enabled signals (bit[31] and bits[1:0]). Options are: 0 = disabled; 1 = enabled.
[31]	Software Trigger. When enabled, the software trigger can participate in the TRG-OUT (GPO) signal generation in logic OR with the other enabled signals (bit[30] and bits[1:0]). Options are: 0 = disabled; 1 = enabled.

Front Panel I/O Control

This register manages the front panel I/O connectors. Default value is 0x000000.

Address   0x811C
Mode   R/W
Attribute   C

Bit	Description
[0]	LEMO I/Os Electrical Level. This bit sets the electrical level of the front panel LEMO connectors: TRG-IN, TRG-OUT (GPO in case of DT and NIM boards), S-IN (GPI in case of DT and NIM boards). Options are: 0 = NIM I/O levels; 1 = TTL I/O levels.
[9:1]	Reserved
[10]	TRG-IN control. The board trigger logic can be synchronized either with the edge of the TRG-IN signal, or with its whole duration. Note: this bit must be used in conjunction with bit[11] = 0. Options are: 0 = trigger is synchronized with the edge of the TRG-IN signal; 1 = trigger is synchronized with the whole duration of the TRG-IN signal.
[11]	TRG-IN to Mezzanines (channels). Options are: 0 = TRG-IN signal is processed by the motherboard and sent to mezzanine (default). The trigger logic is then synchronized with TRG-IN; 1 = TRG-IN is directly sent to the mezzanines with no mother board processing nor delay. This option can be useful when TRG-IN is used to veto the acquisition. NOTE: if this bit is set to 1, then bit[10] is ignored.
[13:12]	Reserved.
[14]	Force TRG-OUT (GPO). This bit can force TRG-OUT (GPO in case of DT and NIM boards) test logical level if bit[15] = 1. Options are: 0 = Force TRG-OUT (GPO) to 0; 1 = Force TRG-OUT (GPO) to 1.
[15]	TRG-OUT (GPO) Mode. Options are: 0 = TRG-OUT (GPO) is an internal signal (according to bits[17:16]); 1= TRG-OUT (GPO) is a test logic level set via bit[14].
[17:16]	TRG-OUT (GPO) Mode Selection. Options are: 00 = Trigger: TRG-OUT/GPO propagates the internal trigger sources according to register 0x8110; 01 = Motherboard Probes: TRG-OUT/GPO is used to propagate signals of the motherboards according to bits[19:18]; 10 = Channel Probes: TRG-OUT/GPO is used to propagate signals of the mezzanines (Channel Signal Virtual Probe); 11 = S-IN (GPI) propagation.
[19:18]	Motherboard Virtual Probe Selection (to be propagated on TRG- OUT/GPO). Options are: 00 = RUN/delayedRUN: this is the RUN in case of ROC FPGA firmware rel. less than 4.12. This probe can be selected according to bit[20]. 01 = CLKOUT: this clock is synchronous with the sampling clock of the ADC and this option can be used to align the phase of the clocks in different boards; 10 = CLK Phase; 11 = BUSY/UNLOCK: this is the board BUSY in case of ROC FPGA firmware rel. 4.5 or lower. This probe can be selected according to bit[20].

[20]	According to bits[19:18], this bit selects the probe to be propagated on TRG- OUT . If bits[19:18] = 00, then bit[20] options are: 0 = RUN, the signal is active when the acquisition is running and it is synchronized with the start run. This option must be used to synchronize the start/stop of the acquisition through the TRG-OUT->TR-IN or TRG-OUT->S-IN (GPI) daisy chain. 1 = delayedRUN. This option can be used to debug the synchronization when the start/stop is propagated through the LVDS I/O (VME boards). If bits[19:18] = 11, then bit[20] options are: 0 = Board BUSY; 1 = PLL Lock Loss. NOTE: this bit is reserved in case of ROC FPGA firmware rel. 4.5 or lower. NOTE: this bit corresponds to BUSY/UNLOCK for ROC FPGA firmware rel. less than 4.12.
[22:21]	Reserved
[31:23]	Reserved.

Channel Enable Mask

This register enables/disables selected channels to participate in the event readout. Disabled channels are not operative.

WARNING: this register must not be modified while the acquisition is running.

Address   0x8120
Mode   R/W
Attribute   C

Bit	Description
[1:0]	Bit n can enable/disable selected channel n to participate to the event readout. Options are: 0: disabled; 1: enabled.
[31:2]	Reserved

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ROC FPGA Firmware Revision

This register contains the motherboard FPGA (ROC) firmware revision information.
The complete format is:
Firmware Revision = X.Y (16 lower bits)
Firmware Revision Date = Y/M/DD (16 higher bits)
EXAMPLE 1: revision 3.08, November 12th, 2007 is 0x7B120308.
EXAMPLE 2: revision 4.09, March 7th, 2016 is 0x03070409.
NOTE: the nibble code for the year makes this information to roll over each 16 years.

Address	0x8124
Mode	R
Attribute	C

Bit	Description
[7:0]	ROC Firmware Minor Revision Number (Y).
[15:8]	ROC Firmware Major Revision Number (X).
[31:16]	ROC Firmware Revision Date (Y/M/DD).

Board Info

This register contains the specific information of the board, such as the digitizer family, the channel memory size and the channel density.

Address   0x8140
Mode   R
Attribute   C

Bit	Description
[7:0]	Digitizer Family Code: 0x7: 780 digitizer family.
[15:8]	Channel Memory Size Code. Options are: 1: each channel is equipped with 512 kS acquisition memory; 8: each channel is equipped with 4 MS acquisition memory. For 780, 781, and 782 this is always 1.
[23:16]	Equipped Channels Number, i.e. 2.
[31:24]	Reserved.

CAEN **Electronic Instrumentation**

Event Size

This register contains the current available event size in 32-bit words. The value is updated after a complete readout of each event.

Address   0x814C
Mode   R
Attribute   C

Bit	Description
[31:0]	Event Size (32-bit words).

Fan Speed Control

This register manages the on-board fan speed in order to guarantee an appropriate cooling according to the internal temperature variations.

NOTE: from revision 4 of the motherboard PCB (see register 0xF04C of the Configuration ROM), the automatic fan speed control has been implemented, and it is supported by ROC FPGA firmware revision greater than 4.4 (see register 0x8124).

Independently of the revision, the user can set the fan speed high by setting bit[3] = 1. Setting bit[3] = 0 will restore the automatic control for revision 4 or higher, or the low fan speed in case of revisions lower than 4.

NOTE: this register is supported by Desktop (DT) boards only.

Address	0x8168
Mode	R/W
Attribute	C

Bit	Description
[2:0]	Reserved: Must be 0.
[3]	Fan Speed Mode. Options are: 0 = slow speed or automatic speed tuning; 1 = high speed.
[5:4]	Reserved: Must be 1.
[31:6]	Reserved: Must be 0.

Run/Start/Stop Delay

When the start of Run is given synchronously to several boards connected in Daisy chain, it is necessary to compensate for the delay in the propagation of the Start (or Stop) signal through the chain. This register sets the delay between the arrival of the Start signal at the input of the board (either on S-IN/GPI or TRG- IN) and the actual start of Run. The delay is usually zero for the last board in the chain and rises going backwards along the chain.

Address   0x8170
Mode   R/W
Attribute   C

Bit	Description
[7:0]	Delay value in steps of 20 ns.
[31:8]	Reserved.

Board Failure Status

This register monitors a set of board errors. In case of a failure, bit[26] in the second word of the event format header is set to 1 during data readout (refer to the digitizer User Manual for event structure description). Reading at this register checks which kind of error occurred.

NOTE: in case of problems with the board, the user is recommended to contact CAEN for support.

Address   0x8178
Mode   R
Attribute   C

Bit	Description
[3:0]	Reserved.
[4]	PLL Lock Loss. Options are: 0 = no error; 1 = PLL Lock Loss occurred.
[31:5]	Reserved.

CAEN ⬡ Electronic Instrumentation

Disable External Trigger

The External Trigger on TRG-IN connector can be disabled through this register. Any functionality related to TRG-IN is disabled as well.

Address	0x817C
Mode	R/W
Attribute	C

Bit	Description
[0]	Options are: 0: external trigger enabled; 1: external trigger disabled.
[31:1]	Reserved

Trigger Validation Mask

Sets the trigger validation logic

Address	0x8188 (ch0), 0x818C (ch1)
Mode	R/W
Attribute	I

Bit	Description
[3:0]	Sets the trigger request that participates to the generation of the trigger validation signal. Options are: 0000: reserved; 0010: reserved; 0100: channel 0; 1000: channel 1.
[7:4]	Reserved
[9:8]	Operation Mask. Sets the logic operation among the enabled trigger request signals. Options are: 00: OR; 01: AND; 10: majority; 11: reserved.
[12:10]	Majority Level. Allowed level values are 0 and 1. For a level m, the trigger fires when at least m+1 of the trigger requests are generated by the enabled channels (bits [3:0]) .
[29:13]	Reserved
[30]	External Trigger: when enabled the external trigger from TRG-IN front panel connector participates to the trigger validation generation (in logic OR). Options are: 0: disabled; 1: enabled.
[31]	Software Trigger: when enabled the software trigger participates to the trigger validation generation (in logic OR). Options are: 0: disabled; 1: enabled.

Readout Control

This register is mainly intended for VME boards, anyway some bits are applicable also for DT and NIM boards.

Address   0xEF00
Mode   R/W
Attribute   C

Bit	Description
[2:0]	Reserved
[3]	Optical Link Interrupt Enable. Options are: 0 = Optical Link interrupts are disabled; 1 = Optical Link interrupts are enabled.
[31:4]	Reserved

Readout Status

This register contains information related to the readout.

Address   0xEF04
Mode   R
Attribute   C

Bit	Description
[0]	Event Ready. Indicates if there are events stored ready for readout. Options are: 0 = no data ready; 1 = event ready.
[1]	Reserved.
[2]	Bus Error (VME boards) / Slave-Terminated (DT/NIM boards) Flag. Options are: 0 = no Bus Error occurred (VME boards) or no terminated transfer (DT/NIM boards); 1 = a Bus Error occurred (VME boards) or one transfer has been terminated by the digitizer in consequence of an unsupported register access or block transfer prematurely terminated in event aligned readout (DT/NIM). NOTE: this bit is reset after register readout at 0xEF04.
[3]	Reserved.
[31:4]	Reserved.

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Aggregate Number per BLT

This register sets the maximum number of complete aggregates which has to be transferred for each block transfer (via VME BLT/CBLT cycles or block readout through Optical Link).

Address   0xEF1C
Mode   R/W
Attribute   C

Bit	Description
[9:0]	Number of complete aggregates to be transferred for each block transfer (BLT).
[31:10]	Reserved.

Scratch

This register can be used to write/read words for test purposes.

Address   0xEF20
Mode   R/W
Attribute   C

Bit	Description
[31:0]	SCRATCH.

Software Reset

All the digitizer registers can be set back to their default values on software reset command by writing any value at this register, or by system reset from backplane in case of VME boards.

Address   0xEF24
Mode   W
Attribute   C

Bit	Description
[31:0]	Whatever value written at this location issues a software reset. All registers are set to their default values (actual settings are lost).

Software Clear

All the digitizer internal memories are cleared:
- automatically by the firmware at the start of each run;
- on software command by writing at this register;
- by hardware (VME boards only) through the LVDS interface properly configured.
A clear command does not change the registers actual value, except for resetting the following registers:
- Event Stored;
- Event Size;
- Channel / Group n Buffer Occupancy.
This register resets also the trigger time stamp.

Address	0xEF28
Mode	W
Attribute	C

Bit	Description
[31:0]	Whatever value written at this location generates a software clear.

Configuration Reload

A write access of any value at this location causes a software reset, a reload of Configuration ROM parameters and a PLL reconfiguration.

Address   0xEF34
Mode   W
Attribute   C

Bit	Description
[31:0]	Write whatever value to perform a software reset, a reload of Configuration ROM parameters and a PLL reconfiguration.

Configuration ROM Checksum

This register contains information on 8-bit checksum of Configuration ROM space.

Address   0xF000
Mode   R
Attribute   C

Bit	Description
[7:0]	Checksum.
[31:8]	Reserved.

Configuration ROM Checksum Length BYTE 2

This register contains information on the third byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address   0xF004
Mode   R
Attribute   C

Bit	Description
[7:0]	Checksum Length: bits[23:16].
[31:8]	Reserved.

Configuration ROM Checksum Length BYTE 1

This register contains information on the second byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address   0xF008
Mode   R
Attribute   C

Bit	Description
[7:0]	Checksum Length: bits[15:8].
[31:8]	Reserved.

Configuration ROM Checksum Length BYTE 0

This register contains information on the first byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address   0xF00C
Mode   R
Attribute   C

Bit	Description
[7:0]	Checksum Length: bits[7:0].
[31:8]	Reserved.

Configuration ROM Constant BYTE 2

This register contains the third byte of the 3-byte constant.

Address   0xF010
Mode   R
Attribute   C

Bit	Description
[7:0]	Constant: bits[23:16] = 0x83.
[31:8]	Reserved.

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Configuration ROM Constant BYTE 1

This register contains the second byte of the 3-byte constant.

Address   0xF014
Mode   R
Attribute   C

Bit	Description
[7:0]	Constant: bits[15:8] = 0x84.
[31:8]	Reserved.

Configuration ROM Constant BYTE 0

This register contains the first byte of the 3-byte constant.

Address   0xF018
Mode   R
Attribute C

Bit	Description
[7:0]	Constant: bits[7:0] = 0x01.
[31:8]	Reserved.

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Configuration ROM C Code

This register contains the ASCII C character code (identifies this as CR space).

Address   0xF01C
Mode   R
Attribute   C

Bit	Description
[7:0]	ASCII 'C' Character Code.
[31:8]	Reserved.

Configuration ROM R Code

This register contains the ASCII R character code (identifies this as CR space).

Address   0xF020
Mode   R
Attribute   C

Bit	Description
[7:0]	ASCII 'R' Character Code.
[31:8]	Reserved.

Configuration ROM IEEE OUI BYTE 2

This register contains information on the third byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Address   0xF024
Mode   R
Attribute   C

Bit	Description
[7:0]	IEEE OUI: bits[23:16].
[31:8]	Reserved.

Configuration ROM IEEE OUI BYTE 1

This register contains information on the second byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Address   0xF028
Mode   R
Attribute   C

Bit	Description
[7:0]	IEEE OUI: bits[15:8].
[31:8]	Reserved.

Configuration ROM IEEE OUI BYTE 0

This register contains information on the first byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Address   0xF02C
Mode   R
Attribute   C

Bit	Description
[7:0]	IEEE OUI: bits[7:0].
[31:8]	Reserved.

Configuration ROM Board Version

This register contains the board version information.

Address   0xF030
Mode   R
Attribute   C

Bit	Description
[7:0]	Board Version Code. Options for 780 digitizer family are: x780M: 0x90; x780N: 0x91; x780P: 0x92.
[31:8]	Reserved.

CAEN Electronic Instrumentation

Configuration ROM Board Form Factor

This register contains the information of the board form factor.

Address   0xF034
Mode   R
Attribute   C

Bit	Description
[7:0]	Board Form Factor CAEN Code. Options are: 0x00 = VME64; 0x01 = VME64X; 0x02 = Desktop; 0x03 = NIM.
[31:8]	Reserved.

Configuration ROM Board ID BYTE 1

This register contains the MSB of the 2-byte board identifier.

Address   0xF038
Mode   R
Attribute   C

Bit	Description
[7:0]	Board Number ID: bits[15:8].
[31:8]	Reserved.

CAEN Electronic Instrumentation

Configuration ROM Board ID BYTE 0

This register contains the LSB information of the 2-byte board identifier.

Address   0xF03C
Mode   R
Attribute   C

Bit	Description
[7:0]	Board Number ID: bits[7:0].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 3

This register contains information on the fourth byte of the 4-byte hardware revision.

Address   0xF040
Mode   R
Attribute   C

Bit	Description
[7:0]	PCB Revision: bits[31:24].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 2

This register contains information on the third byte of the 4-byte hardware revision.

Address	0xF044
Mode	R
Attribute	C

Bit	Description
[7:0]	PCB Revision: bits[23:16].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 1

This register contains information on the second byte of the 4-byte hardware revision.

Address   0xF048
Mode   R
Attribute   C

Bit	Description
[7:0]	PCB Revision: bits[15:8].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 0

This register contains information on the first byte of the 4-byte hardware revision.

Address   0xF04C
Mode   R
Attribute   C

Bit	Description
[7:0]	PCB Revision: bits[7:0].
[31:8]	Reserved.

Configuration ROM FLASH Type

This register contains information on which FLASH type (storing the FPGA firmware) is present on-board.

Address   0xF050
Mode   R
Attribute   C

Bit	Description
[7:0]	FLASH Type. Options are: 0x00 = 8 Mb FLASH; 0x01 = 32 Mb FLASH.
[31:8]	Reserved.

Configuration ROM Board Serial Number BYTE 1

This register contains information on the MSB of the board serial number.

Address   0xF080
Mode   R
Attribute   C

Bit	Description
[7:0]	Board Serial Number: bits[15:8].
[31:8]	Reserved.

Configuration ROM Board Serial Number BYTE 0

This register contains information on the LSB of the board serial number.

Address   0xF084
Mode   R
Attribute   C

Bit	Description
[7:0]	Board Serial Number: bits[7:0].
[31:8]	Reserved.

Configuration ROM VCXO Type

This register contains information on which type of VCXO is present on-board.

Address   0xF088
Mode   R
Attribute   C

Bit	Description
[31:0]	VCXO Type Code. Options for VME Digitizers are: 0 = AD9510 with 1 GHz; 1 = AD9510 with 500 MHz (not programmable); 2 = AD9510 with 500 MHz (programmable). Options for Desktop/NIM Digitizers are: Reserved (value = 0).

2 DPP-PHA Memory Organization

Memory Organization

Each channel has a fixed amount of RAM memory to save the events. The memory is divided into a programmable number of buffers (also called "aggregates"), where each buffer contains a programmable number of events. The event format is programmable as well. The board registers involved are the following:

- "Aggregate Organization" (*Nb*), address 0x800C: defines how many aggregates can be contained in the memory ($n_{aggr} = 2^{Nb}$).
- "Number of Events per Aggregate" (*Ne*), address 0x1n34: defines the number of events contained in one aggregate. The maximum allowed value is 1023.
- "Record Length" (*Ns*), address 0x8020: defines the number of samples for the waveform acquisition, when enabled (*rec_len = Ns * 2* for 724, 781 and 782 series).
- "Board Configuration", address 0x8000: defines the acquisition mode and the event data format.

Note: Those who need to write their own DAQ software, must take care to choose the Ne value according to the event and buffer size, as explained in the examples in the next section.

Information about the use of these parameters in the CAENDigitizer library can be found in **[RD1]**. According to the programmed event format, an event can contain a certain number of samples of the waveform, one trigger time stamp, the energy, and the Extras information.

780 series

The following section describes the structure of the memory organization of 724, 781, and 782 series. The physical memory of a board is made of memory locations, each of 32-bit (4B) In terms of location occupancy:

> FORMAT + SIZE = 1 location.
>
> Trigger Time Stamp = 1 location;
>
> Waveform (if enabled) = 1 location every 2 samples;
>
> Energy/EXTRAS = 1 location;

Therefore, the events size can be easily calculated. Fig. **2.1** shows how the data are saved into the physical memory.

Note: Fig. **2.1** refers to the event storage into the physical memory of the board. Data are then organized in a different format for the event readout. The event readout format is shown in the **Event Data Format** section.

As previously said, the "Record Length" and the "Board Configuration" settings determine the event size; the user must calculate the number of event per buffer (*Ne*) and the number of buffers (2^{Nb}) accordingly. When the board runs in List Mode, the event memory contains only three locations, one for the FORMAT+SIZE, on for the Trigger Time Tag, and one for the Energy and EXTRAS. Therefore it is very small and it is suggested to use a big value for Ne to make the buffer size as big as at least a few KB. Small buffer size results in low readout bandwidth. The only drawback of setting high values for *Ne* is that the events are not available for the readout until the buffer is complete; hence there is some latency between the arrival of a trigger and the readout of the relevant event data. Conversely, when the board runs in Oscilloscope Mode, especially when the record length is large, it is more convenient to keep *Ne* low (typically 1).
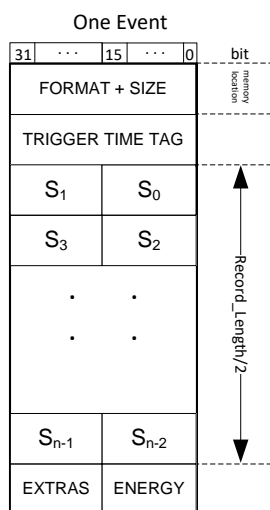

One Event

Fig. 2.1: Data organization into the Internal Memory of 780 series.

Event Data Format

The data format provided by the firmware is grouped into aggregates of events. Each aggregate of channels is then grouped into the board aggregate, and finally into block transfer. Those who need to write their own acquisition software must take care of the following sections.

Channel Aggregate Data Format for 780 series

The Channel Aggregate is composed by the set of Ne events, where Ne is the programmable number of events contained in one aggregate (see the previous section). The structure of the Channel Aggregate of two events (EVENT 0 and EVENT 1) is shown in Fig. **2.2**, where:

"CHANNEL AGGREGATE" DATA FORMAT
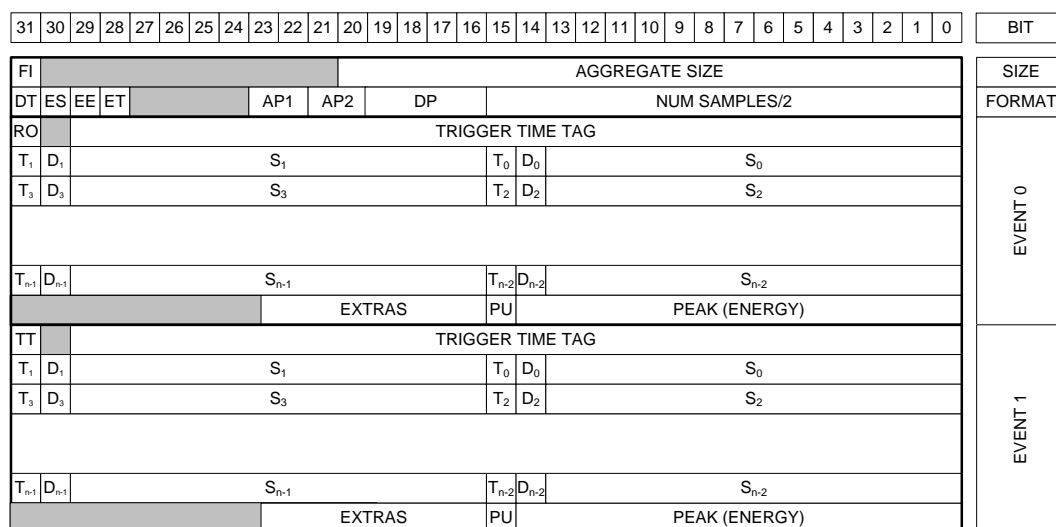
Fig. 2.2: Channel Aggregate Data Format scheme.

FI: when 1, the second word is the Format Info

DT: Dual trace enabled flag (0 = disabled, 1 = enabled)

ES: Waveform (samples) enabled flag

EE: Energy enabled flag

ET: Trigger Time Stamp enabled flag

AP1: Analog Probe 1 Selection. AP1 can be selected among:

> 00 = "Input": the input signal from pre-amplified detectors
> 01 = "RC-CR": first step of the trigger and timing filter
> 10 = "Fast Filter": second step of the trigger and timing filter
> 11 = "Trapezoid": trapezoid resulting from the energy filter

AP2: Analog Probe 2 Selection. AP2 can be selected among:

> 00 = "Input": the input signal from pre-amplified detectors
> 01 = "Threshold": the RC-CR2 threshold value
> 10 = "Trapezoid-BL": the trapezoid shape minus its baseline
> 11 = "Baseline": displays the trapezoid baseline

DP: Digital Virtual Probe Selection. DP can be selected among:

> 0000 = "Peaking": shows where the energy is calculated
> 0001 = "Armed": digital input showing where the RC-CR2 crosses the Threshold
> 0010 = "Peak Run": starts with the trigger and last for the whole event (see **[RD2]**)
> 0011 = "Pile-Up": shows when there is a pile-up event and corresponds to the time interval when the energy calculation is disabled due to the pile-up event
> 0100 = "Peaking": shows where the energy is calculated
> 0101 = "Trg Validation Win": digital input showing the trigger validation acceptance window TVAW (refer to **[RD3]**)
> 0110 = "BSL Freeze" : shows the time interval in which the baseline evaluation is freezed
> 0111 = "TRG Holdoff": shows the trigger hold-off parameter
> 1000 = "Trg Validation": shows the trigger validation signal TRG_VAL (refer to **[RD3]**)
> 1001 = "Over Range Protection Time", this is 1 when the input stage is saturated
> 1010 = "TRG Window": not used
> 1011 = "Ext TRG", shows the external trigger, when available
> 1100 = "Busy", shows when the memory board is full.
> 1101 = "Peak Ready", shows after the Peak Mean time.

RO: Timestamp roll-over (1 if roll-over event, 0 elsewhere)

S_m (m = 0, 2, 4n − 2): Even Samples of AP1 at time t = m

$S_{m'}$ (m' = 1, 3, 4n − 1): if DT=0, then $S_{m'}$ corresponds to the odd Samples of AP1 at time t = m'. Otherwise, if DT=1, they correspond to the even Samples of AP2 at time t = $m' − 1$

T_n: bit identifying in which sample the Trigger occurred

D_n: Digital Virtual Probe for each sample. The Probe type can be read from the "DP" field in the header

PU: This bit is set when the energy of the event is not correctly calculated, i.e. in case of pile-up, saturation, roll-over, fake event, etc. When this bit is found equal to 1, the user must discard the event. EXTRAS details which kind of event is.

EXTRAS:

> bit[0] = DEAD_TIME. This bit is set to 1 when a dead time due to board full memory status occurs before this event. Check Fig. **2.3** for more details.
> bit[1] = ROLL_OVER. Identify a trigger time stamp roll-over that occurred before this event.
> bit[2] = TT_RESET. Identify a trigger time stamp reset forced from external signals in S-IN (GPI for Desktop).
> bit[3] = FAKE_EVENT. This is a fake event (which does not correspond to any physical event) that identifies a time stamp roll-over. The roll-over can be due to an external or internal reset. The user can set bit[25] = 1 of register 0x1n80 to enable the fake-event saving in case of reset from S-IN, and bit[26] = 1 of register 0x1n80 to enable the fake-event saving in case of internal roll-over. In the first case the event will have both bit[3] and bit[2] set to 1, while in the second case the event will have both bit[3] and bit[1] set to 1.

bit[4] = INPUT SATURATION: identifies where the input saturates the ADC over/under range. The event reports Energy = 0x7FFFF, where the PU flag is set to 1 as well.

bit[5] = LOST_TRG: every N lost events this flag is high, where N is set from bits[17:16] of register 0x1nA0 (default value 1024).

bit[6] = TOT_TRG: every N total events this flag is high, where N is set from bits[17:16] of register 0x1nA0 (default value 1024).

bit[7] = reserved.

bit[10] = PILE_UP: identifies that the event is in pile-up. The PU flag is set to 1 as well.

bit[11] = SATURATION PROTECTION TIME: after an ADC saturation, there is a protection time equal to τ, i.e. the programmed decay time, where the events are tagged by this bit. This can be used to discard events too close to the saturation.

Note: DEAD_TIME in case of FULL board memory (see Fig. **2.3**). When the memory of the board is full (which is usually due to a write event), the board is not able any more to transfer the event data. When the board is ready again, the first event after the FULL will have the bit[1] of EXTRAS (bit[16] of the ENERGY word) set to 1, and the energy value as read from the algorithm. The dead-time is equal to the time difference between the last trigger occurred and the trigger after the FULL status.
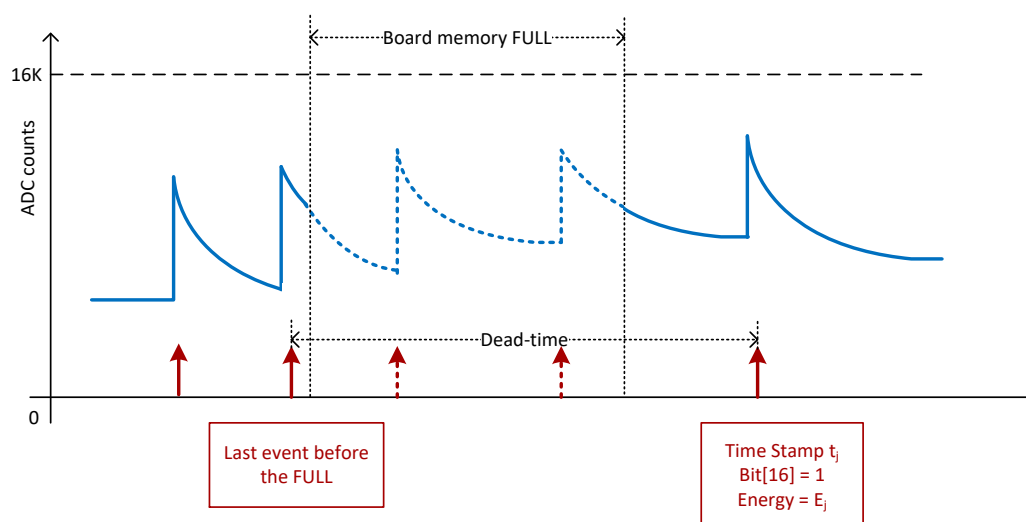

Fig. 2.3: Dead-time in case of FULL memory status. Events in the FULL are identified but not saved.

Board Aggregate Data Format

For each readout request (occurring when at least one channel has available data to be read) the "interface FPGA (ROC)" reads one aggregate from each enabled channel memory. No more than one aggregate per channel is read each time. The set of Channel Aggregates is the Board Aggregate. If one channel has no data, that channel does not come into the Board Aggregate. The data format when all 8 channels of a VME have available data is as shown in Fig. **2.4**, where:

"BOARD AGGREGATE" DATA FORMAT for 780 series
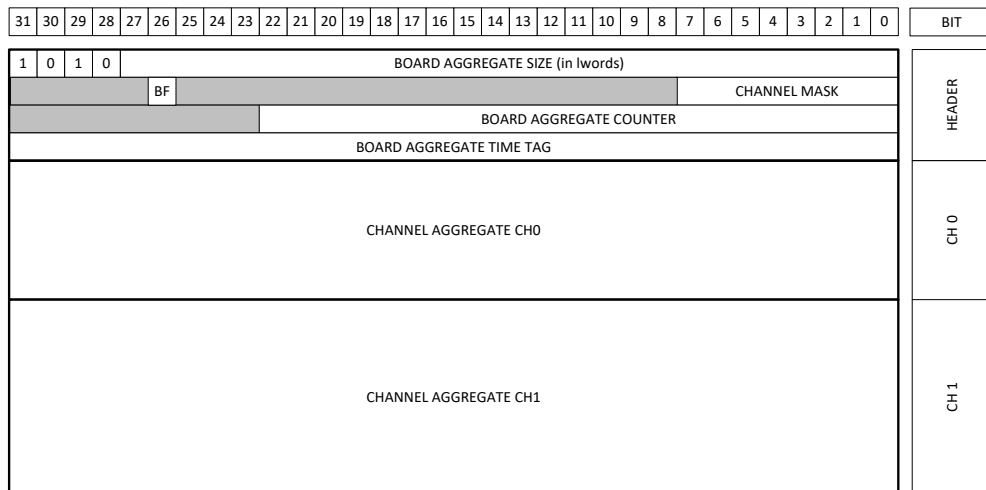
Fig. 2.4: Board Aggregate Data Format scheme.

BOARD AGGREGATE SIZE: total size of the aggregate

BF: Board Fail flag. This bit is set to "1" after a hardware problem, as for example the PLL unlocking, or over-temperature condition. The user can investigate the problem checking the error monitor register 0x8178, or contacting CAEN support (refer to **3).**

✎ **Note**: BF bit is meaningful only for ROC FPGA firmware revision greater than 4.5. It is reserved for previous releases.

CHANNEL MASK: corresponds to those channels participating to the Board Aggregate;

BOARD AGGREGATE COUNTER: counts the board aggregate. It increases with the increase of board aggregates;

BOARD AGGREGATE TIME TAG: is the time of creation of the aggregate (this does not correspond to any physical quantity);

Data Block

The readout of the digitizer is done using the Block Transfer (BLT, refer to **[RD1]**); for each transfer, the board gives a certain number of Board Aggregates, consisting in the Data Block. The maximum number of aggregates that can be transferred in a BLT is defined by the READOUT_BTL_AGGREGATE_NUMBER. In the final readout each Board Aggregate comes successively. In case of n Board Aggregates, the Data Block is as in Fig. **2.5**

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DATA BLOCK

BOARD AGGREGATE 0
BOARD AGGREGATE 1
…
BOARD AGGREGATE n-1

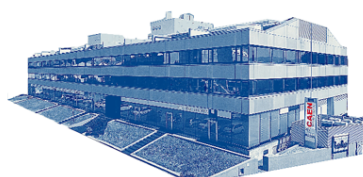**Fig. 2.5:** Data Block scheme.

3 Technical Support

CAEN makes available the technical support of its specialists for requests concerning the software and hardware. Use the support form available at the following link:

https://www.caen.it/support-services/support-form/

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