CAEN
Tools for Discovery

Electronic Instrumentation

PRELIMINARY

User Manual UM6698

A55PETx

PETIROC Piggyback Board for DT5550W

Rev. 5 - March 2nd, 2022

Purpose of this User Manual

This User Manual contains the full description of the A55PETx Piggyback Boards family for DT5550W.

Change Document Record

Date	Revision	Changes
November 6th, 2018	00	Initial release
March 6th, 2019	01	Modified **SiPM connection and biasing** with additional information on the pitch adapter. Modified **Technical Support**
July 18th, 2019	02	Modified **DT5550W Readout Software.** Revised **SiPM connection and biasing**
February 21st, 2020	03	Revised **DT5550W Readout Software.** Added **Multiboard readout script**
July 2nd, 2021	04	Revised **Time Measurements**
March 2nd, 2022	05	General revision

Symbols, abbreviated terms and notation

ADC	Analog to Digital Converter
FPGA	Field Programmable Gate Array
OEM	Original Equipment Manufacturer
OS	Operating system
PHA	Pulse Height Analysis

Reference Document

[RD1] PETIROC 2A Datasheet (available on WeeROC website)

[RD2] UM6697 - DT5550W User Manual

[RD3] UM6377 – A7585 DT5485 User Manual

[RD4] DS8241 – Remotization kit datasheet

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Limitation of responsibility

If the warnings contained in this manual are not followed, CAEN will not be responsible for damage caused by improper use of the device. The manufacturer declines all responsibility for damage resulting from failure to comply with the instructions for use of the product. The equipment must be used as described in the user manual, with particular regard to the intended use, using only accessories as specified by the manufacturer. No modification or repair can be performed.

Disclaimer

The information contained herein has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies. CAEN spa reserves the right to modify its products specifications without giving any notice; for up to date information please visit www.caen.it.

MADE IN ITALY: We remark that all our boards have been designed and assembled in Italy. In a challenging environment where a competitive edge is often obtained at the cost of lower wages and declining working conditions, we proudly acknowledge that all those who participated in the production and distribution process of our devices were reasonably paid and worked in a safe environment (this is true for the boards marked "MADE IN ITALY", while we cannot guarantee for third-party manufactures).

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1 Introduction

The A55PETx board is the Piggyback Board for DT5550W, hosting up to four PETIROC 2A WeeROC (*) ASICs. It can be used in conjunction with DT5550W motherboard to perform **energy and high-resolution time measurements with SiPMs and SiPM matrixes.**

The device is designed to operate in laboratory environment under the supervision of skilled technicians.

The PETIROC 2A ASIC is the ideal solution for high density channel systems, aiming to readout SiPM sensors extracting energy, time and positional information. In fact, the PETIROC chip, besides the classical readout chain made of preamp, fast and slow shaper, it also integrates a trigger with a timing resolution better than 35 ps, a TDC, a Sample&Hold circuit and an internal ADC which can convert onboard the charge cumulated on each sensor. Each PETIROC 2A integrates 32 readout channels.
The A55PETx piggyback is equipped with CAEN module A7585D to be used for SiPM biasing. The A7585D power supply is directly soldered on the PCB.

The PETIROC 2A integrates in a chip an entire readout system, requiring externally only few passive components, two clock lines and a FPGA connected with few lines, which can manage up one hundred ASICs. Therefore, a system exploiting this chip is the best solution for experiments in which the high number of channels requires the reduction of the hardware components, because of geometrical reasons and costs.

The A55PETx Piggyback can be easily plugged onto the DT5550W motherboard to arrange a **complete Data Acquisition System for SiPM with up to 128 channels**. The PETIROCs readout is completely managed by the firmware preloaded on the FPGA hosted by the DT5550W motherboard.

The **DT5550W Readout Software** is the free and open source Windows-based software developed to perform acquisitions with the DT5550W. It works in conjunction with the DT5550W default firmware and it can be modified by the user according to the custom functions implemented in the firmware and for any other need. It allows to perform:

- List event readout (energy, time)
- Energy Spectrum measurements
- Time spectrum measurements
- Imaging with configurable detector shape
- System and ASIC configuration
- ASIC monitor signal probing

For more detailed information, see **[RD2]**.

Available board models and accessories are listed below.

Motherboard	Description	Product Code
DT5550W	DT5550W - WeeROC ASICs Evaluation and DAQ System	WDT5550WXAAA
Piggyback Board Models	**Description**	**Product Code**
A55PET1	A55PET1 - Piggyback Board with 1 PETIROC chip	WW55PETI2AA1
A55PET2	A55PET2 - Piggyback Board with 2 PETIROC chip	WW55PETI2AA2
A55PET4	A55PET4 - Piggyback Board with 4 PETIROC chip	WW55PETI2AA4
Accessories	**Description**	**Product Code**
REMOT5550W	Remotization kit with 2-meters cable for DT5550W	WKREMOT5550W

Table 1.1: table of available board models and accessories

(*) https://www.weeroc.com

2 Safety Notices

N.B. Read carefully the "Precautions for Handling, Storage and Installation" document provided with the product before starting any operation.

The following HAZARD SYMBOLS may be reported on the unit:

	Caution, refer to product manual
	Caution, risk of electrical shock
	Protective conductor terminal
	Earth (Ground) Terminal
	Alternating Current
	Three-Phase Alternating Current

The following symbol may be reported in the present manual:

	General warning statement

The symbol could be followed by the following terms:

- **DANGER**: indicates a hazardous situation which, if not avoided, will result in serious injury or death.
- **WARNING**: indicates a hazardous situation which, if not avoided, could result in death or serious injury.
- **CAUTION**: indicates a situation or condition that, if not avoided, could cause physical injury or damage the product and / or its environment.

To avoid potential hazards, use the product only as specified. Only qualified personnel should perform service procedures.
Avoid Electric Overload. To avoid electric shock or fire hazard, do not power a load outside of its specified range.
Avoid Electric Shock. To avoid injury or loss of life, do not connect or disconnect cables while they are connected to a voltage source.

Do Not Operate without Covers. To avoid electric shock or fire hazard, do not operate this product with covers or panels removed.
Do Not Operate in Wet/Damp Conditions. To avoid electric shock, do not operate this product in wet or damp conditions.
Do Not Operate in an Explosive Atmosphere. To avoid injury or fire hazard, do not operate this product in an explosive atmosphere.
Do Not Operate with Suspected Failures. If you suspect this product to be damaged, please contact Technical Support.

The mezzanine connector carries more than 250 I/O lines that can be grouped as:

- Digital 3.3V single ended I/O
- Digital 2.5V single ended I/O
- Digital differential 2.5V LVDS
- Analog differential Input
- Analog Common Mode Output
- I2C
- Power Supply
- Clock output

The following operating limits must be respected:

Net class	Connector	Unit	Min	Max
Digital lines	Mezzanine connector			
	Digital 3.3V	Voltage	0 V	3.5V
		Current		10 mA
	Digital 2.5V	Voltage	0 V	2.7 V
		Current		10 mA
	LVDS	Voltage	0.5 V	2.1 V
		Current		10 mA
		Common Mode		1.25 V
	I2C	Voltage	0	3.5 V
	Analog Differential Input	Voltage	0.45 V	1.55 V
		Common Mode	0.95 V	0.95 V
	Analog Common Mode Output	Current		6 mA
	Power 5V	Current		2 A
	Power 3.3V	Current		2 A
	Power 1.8V	Current		1 A
	Power 4V A	Current		600 mA
	Power -1V A	Current		600 mA
	Clock Output	Differential Impedance	80 Ω	120 Ω

Table 2.1: operating limits for A55PETx mezzanine connector.

WARNING: the piggyback connector lines are directly connected to the FPGA I/O. Violation in maximum absolute rating given in this document will likely destroy the FPGA.

THIS DEVICE SHOULD BE INSTALLED AND USED BY SKILLED TECHNICIAN ONLY OR UNDER HIS SUPERVISION

3 Block Diagram

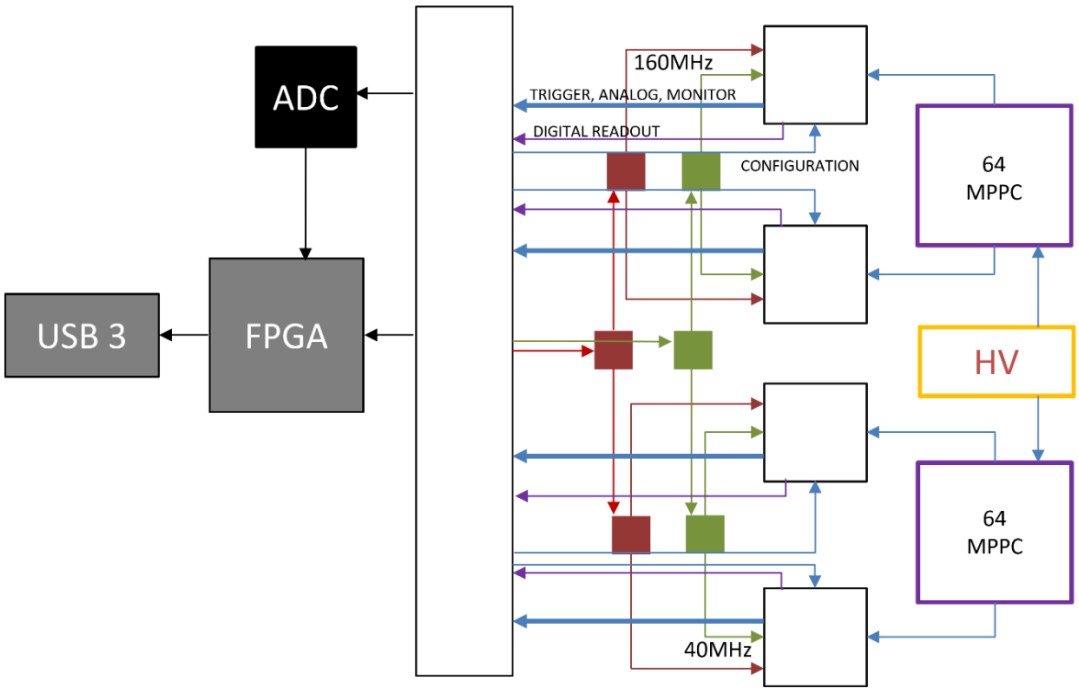


Figure 3.1: A55PET4 Piggyback Board block diagram with A7585D High Voltage Power Supply for SiPM. On the left, the connections to the DT5550W motherboard components, through the mezzanine connector (big white rectangle), are shown.

4 Technical Specifications

TECHNICAL	
POWER CONSUMPTION	DT5550W + A55PET4 piggyback - 0.9A @ 12V (Typ.)
ANALOG INPUT	**Channels** 32, 64 or 128 (=1, 2 or 4 Petiroc-2A) **Connector** Compatible with 64-channel Hamamatsu matrix S13361-3050AE-08 INCLUDED **strip adapter with 2.54 mm pitch**
SIGNAL POLARITY	Positive or Negative
SENSITIVITY	High bandwidth (GBW>1GHz) inverting voltage preamplifier with fixed gain (=40)
DYNAMIC RANGE	The Petiroc-2A preamplifiers ensure a dynamic range from 160 fC to 400 pC (i.e. from 1 to 2500 photo-electrons with 10^6 SiPM gain)
SHAPING TIME	**CRRC** 4 options from 25 ns to 100 ns (25 ns step) for each RC filter
SELF-TRIGGERS	- Programmable 10-bit DAC for common threshold - Separate trigger line per channel - Programmable 6-bit DAC for channel-by-channel threshold fine adjustment V_{th} = 0.89V + (10-bit DAC * 0.92 mV) – (6-bit DAC * 1.5mV) - Logic combination (AND, OR) of triggers for start of A/D conversion and time reference -**Custom combinations** through open FPGA and **SCI-Compiler**
EXTERNAL TRIGGER	From LEMO 5 of the DT5550W motherboard programmable I/Os
HIGH VOLTAGE POWER SUPPLY	Single channel PCB mounted A7585D High Voltage Power Supply: - Common SiPM bias voltage: 20 ÷ 85 V -Vset vs. Vout Accuracy: ±0.2% ±50mV - Individual channel adjustment: 8-bit (2.5V or 4.5V dynamic range) - Max. output bias current: 10 mA - Programmable temperature compensation
ACQUISITION MODE	**Digital Readout (PHA + timestamp)** -Simultaneous acquisition of all channels – energy and timestamp - 10-bit A/D conversion - Systematic conversion time + serial data outing ~ 12.8 + 12 µs → Max. trigger rate ~ 40 kHz
TIME STAMP	Resolution below 40ps for fine timestamp
INTERCONNECTION	Mezzanine connector carrying more than 200 analog/digital lines, to connect the A55PETx onto the DT5550W motherboard
SOFTWARE	- **DT5550W Readout Software** to manage the default firmware - **SCI-Compiler** for custom firmware development on the DT5550W motherboard
MECHANICAL	
FORM FACTOR	Desktop bare PCB unit
DIMENSIONS (H/W/L)	Piggyback: 5/160/145 mm^3 (including connectors) Piggyback mounted on DT5550W: 24/152/260 mm^3 (including connectors)
ENVIRONMENTAL	
ENVIRONMENTAL	Indoor use
OPERATING TEMPERATURE	Operating Temperature -20 °C ÷ 50 °C
OPERATING HUMIDITY	25% ÷ 95% RH non condensing
STORAGE TEMPERATURE	-30 °C ÷ +80 °C
STORAGE HUMIDITY	5% ÷ 90% RH non condensing
ALTITUDE	≤2000 m
POLLUTION DEGREE	2
OVERVOLTAGE CATEGORY	II
EMC ENVIRONMENT	Commercial and light industrial
IP DEGREE	IPX0 enclosure, not for wet location
REGULATORY	
COMPLIANCE	• EMC: CE 2014/30/EU Electromagnetic compatibility Directive • Safety: CE 2014/35/EU Low Voltage Directive

Table 4.1: technical specifications of the A55PETx

5 Packaging and compliancy

The A55PETx is a bare piggyback PCB – 5/160/145 mm^3 (including connectors) H/W/L – intended to be mounted on the DT5550W motherboard. The system is provided as OEM device without any enclosure in order to be easily integrated in the final experimental setup. If the A55PETx is purchased together with the DT5550W motherboard, the system is provided already assembled, as shown in **Figure 5.1**

Figure 5.1: general view of the DT5550W system, where the piggyback is the upper board.

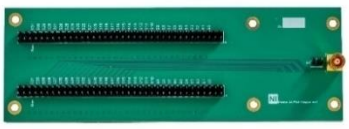
The unit is inspected by CAEN before the shipment, and it is guaranteed to leave the factory free of mechanical or electrical defects.

When receiving the unit, the user is strictly recommended to inspect for any damage which may have occurred during transportation. Particularly, inspect for exterior damages like broken connectors and check that the panel is not scratched or cracked.

All packing material should be held on until the inspection has been completed. If damage is detected, the user must file a claim with the carrier immediately and notify CAEN.

Before installing the unit, make sure to read thoroughly the safety rules and installation requirements (Sec. **Safety Notices** and **Installing the device**), then place the package content onto your bench.

The content of the delivered package standardly consists of the part list shown in the table below (**Table 5.1**). All the official documentation, firmware updates, software tools, and accessories are available on *www.caen.it* at the product web page.

	Part	Description	Qty
	A55PETx piggyback	Weeroc ASICs evaluation and DAQ system	x1
	Dark box	3D-printed dark box with connector for optical fiber, compatible with CAEN SP5601/SP5605 LED Driver kit. It can be used to operate the SiPMs in a light-tight environment and illuminate them with an external light source.	x1 or x2
	2.54 mm pitch adapter	2.54 mm pitch adapter to convert the Ultra Fine Pitch Socket for SiPM connection into a double 2.54 mm strip connector	x1 or x2

	Fixing kit	Nuts and bolts to secure the dark box or pitch adapter to the A55PETx – by default it is already mounted to secure the dark boxes	
	User guide	UM7028 – A55PETx User Manual	x1

Table 5.1: delivered kit.

CAUTION: to manage the product, consult the operating instructions provided.

A55PETx is an ESD sensitive item. Handling without ESD protective covering shall be performed only into approved ESD Protected Area (EPAs)

A55PETx complies with EMC directive only if installed in a CE marked system

It is recommended to:

- Inspect containers for damage during shipment. Report any damage to the freight carrier for possible insurance claims.
- Check that all the components received match those listed on the enclosed packing list. (CAEN cannot accept responsibility for missing items unless we are notified promptly of any discrepancies.)
- Open shipping containers; be careful not to damage contents.
- Inspect contents and report any damage. The inspection should confirm that there is no exterior damage to the unit such as broken knobs or connectors and that the front panel and display face are not scratched or cracked. Keep all packing material until the inspection has been completed.
- If damage is detected, file a claim with carrier immediately and notify CAEN service.
- If equipment must be returned for any reason, carefully repack equipment in the original shipping container with original packing materials if possible. Please contact CAEN service.
- If equipment is to be installed later, place equipment in original shipping container and store in a safe place until ready to install

DO NOT SUBJECT THE ITEM TO UNDUE SHOCK OF VIBRATIONS

DO NOT BUMP, DROP OR SLIDE SHIPPING CONTAINERS

DO NOT LEAVE ITEMS OR SHIPPING CONTAINERS UNSUPERVISED IN AREAS WHERE UNTRAINED PERSONNEL MAY MISHANDLE THE ITEMS

USE ONLY ACCESSORIES WICH MEET THE MANUFACTURER SPECIFICATIONS

6 PID (Product Identifier)

PID is the CAEN product identifier, an incremental number greater than 10000 that is unique for each product. The PID is on a label affixed to the product (**Fig. 6.1**).

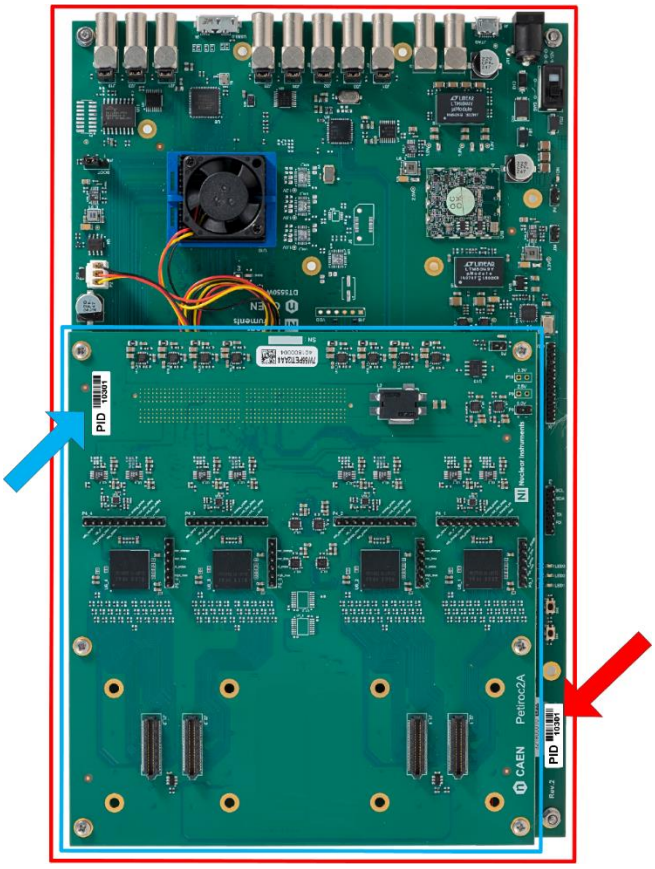


Fig. 6.1: PID location. The blue arrow points to the piggyback board PID.

7 Power Requirements

The A55PETx is powered by the DT5550W motherboard. The motherboard is powered by an external 220-110 V to 12V, 60W AC/DC stabilized power supply provided with the board and included in the delivered kit, together with a standard wall IEC C13 power chord.

Note: using a different power supply source, like battery or linear type, it is recommended the source to provide +12 V and 2A; the power jack is a 2.1 mm type, a suitable cable is the RS 656-3816 type (or similar)

The maximum operating voltage is 12.8V while the minimum is 9V

8 Cooling Management

The A55PETx piggyback board can operate in the temperature range -20 + 50 °C.

The following paragraph refers to the piggyback mounted onto the DT5550W board.

An air flow fan is installed onboard, onto the FPGA of the DT5550W. The user must take in care to provide a proper cooling to the board with external fan if the board is used in an enclosure or if the board is installed in a setup with poor air flow.
Excessive temperature will, in first instance, reduce the performance and the quality of the measurements and can also damage the board.

Please do not stop fan operation to avoid FPGA overheating. If in a single rack tower, multiple units are installed, please consider external fans or rack mounted air conditioning system.

If the board is stored in cold environmental, please check for water condensation before power on.

The board has not been tested for radiation hardness. High energy particle can be source of soft error and can damage the FPGA. If used in strong proton or neutron beams, arrange proper shielding or remote the sensor with a custom cable.

9 Installing the device

- Connect the A55PETx piggyback onto the mezzanine connector of the DT5550W motherboard
- Power on the DT5550W as described in **[RD2]**

If the A55PETx is purchased together with the DT5550W motherboard, the system is provided already assembled, as shown in **Figure 5.1.**

ONLY QUALIFIED PERSONNEL SHOULD PERFORM INSTALLATION, OPERATIONS

DO NOT INSTALL THE EQUIPMENT SO THAT IT IS DIFFICULT TO OPERATE THE ON/OFF SWITCH ONBOARD

IT IS RECOMMENDED THAT THE SWITCH OR CIRCUIT-BREAKER IS NEAR THE EQUIPMENT

THE SAFETY OF ANY SYSTEM THAT INCORPORATES THE DEVICE IS UNDER THE RESPONSIBILITY OF THE ASSEMBLER OF THE SYSTEM

A55PETx is an ESD sensitive item. Handling without ESD protective covering shall be performed only into approved ESD Protected Area (EPAs)

A55PETx complies with EMC directive only if installed in a CE marked system

Do not use the device and contact technical support if one of these situations is verified:

- Enclosure integrity is compromised
- Insulation of HV chord is damaged (if present)
- The indication led or display is not performing as required (e.g. led not working, display with incorrect graphic)
- Fans are not working (if present)

10 Hardware Description

The A55PETx piggyback boards are designed to be plugged onto DT5550W motherboard to build a complete readout system for SiPM (32, 64 or 128 channels).

In the following picture the most important components and connectors on the front and rear side of the A55PET2 (taken as example for the A55PETx family) are highlighted.

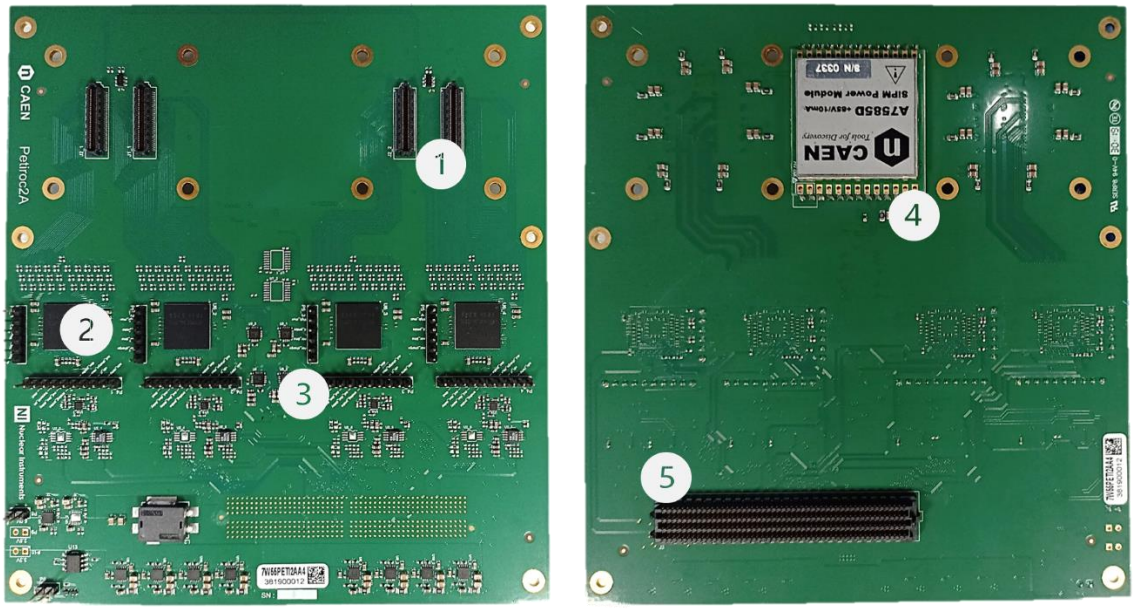


Figure 10.1: general view (left front side, right: rear side) of the A55PET4 piggyback, shown as example.

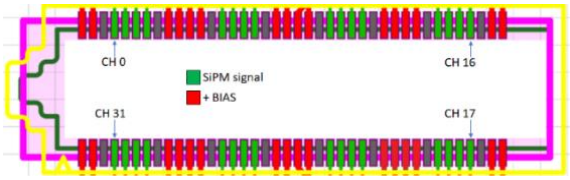
Number	Description
1	**Input connectors** SAMTEC SS4-40-3.00-L-D-K-TR, compatible with 64-channel Hamamatsu matrix S13361-3050AE-08. Each couple of connectors can host a SiPM matrix each. The pinout is the following: 
2	PETIROC ASIC in BGA packaging
3	**Test Pins** – 2.54 mm strip – refer to Par. **Test Pins** for more details
4	**A7585D 20-85 V Power Supply** for SiPM biasing
5	**Mezzanine connector** – SAMTEC SEAM-50-02.0-S-08-2-A-K-TR, 8 column, 64 rows, BGA array connector used to plug the piggyback onto the DT5550W motherboard

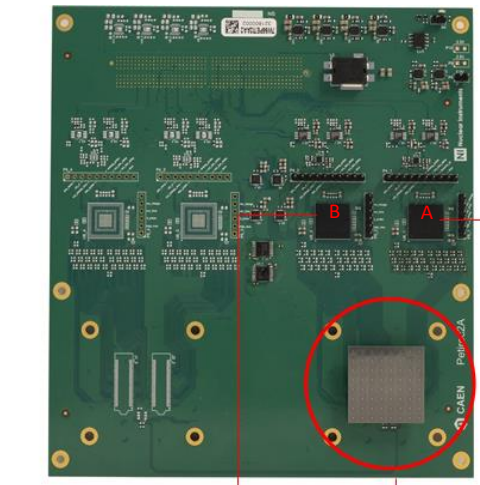
Table 10.1: description of the main components and connectors of the A55PETx board

SiPM connection and biasing

It is possible to connect SiPMs to the A55PETx board in three ways:

- use Hamamatsu S13361-3050AE-08 matrix to be connected directly on the onboard Samtec SS4-40-3.0-L-D-K-TR connectors.
- plug the PCB pitch adapter on the board connectors and use the exposed 2.54 mm pitch strip to easily solder any kind of SiPM matrix or array (refer to **Pitch Adapter Kit**). SiPM cathodes must be connected to *Bias* pins, while anodes to S_x pins.
- use a compatible remoting cable to be plugged on the board connectors and design a custom PCB hosting SiPMs – for example CAEN 64-channels Remotization kit **[RD3]**

If connecting a S13361-3050AE-08 Hamamatsu 64-channels matrix directly onboard, the resulting correspondence with the board readout channels is the following:



A-1 ch14	B-1 ch15	C-1 ch16	D-1 ch17	E-1 ch14	F-1 ch15	G-1 ch16	H-1 ch17
A-2 ch13	B-2 ch12	C-2 ch19	D-2 ch18	E-2 ch13	F-2 ch12	G-2 ch19	H-2 ch18
A-3 ch10	B-3 ch11	C-3 ch20	D-3 ch21	E-3 ch10	F-3 ch11	G-3 ch20	H-3 ch21
A-4 ch9	B-4 ch8	C-4 ch23	D-4 ch22	E-4 ch9	F-4 ch8	G-4 ch23	H-4 ch22
A-5 ch6	B-5 ch7	C-5 ch24	D-5 ch25	E-5 ch6	F-5 ch7	G-5 ch24	H-5 ch25
A-6 ch5	B-6 ch4	C-6 ch27	D-6 ch26	E-6 ch5	F-6 ch4	G-6 ch27	H-6 ch26
A-7 ch2	B-7 ch3	C-7 ch28	D-7 ch29	E-7 ch2	F-7 ch3	G-7 ch28	H-7 ch29
A-8 ch1	B-8 ch0	C-8 ch31	D-8 ch30	E-8 ch1	F-8 ch0	G-8 ch31	H-8 ch30

Figure 10.2: the Hamamatsu S13361-3050AE-08 connected onboard. The grid reports the association between the matrix pixels (A-1 …. H-8) and the ASIC channels (ch0 … ch31). The green-coloured pixels are connected to ASIC A while yellow-coloured pixels are connected to ASIC B.

The SiPM bias is provided onboard by the CAEN A7585D Power Supply module, which is extremely low noise (no additional filters needed). The bias lines for SiPMs are grouped eight by eight and connected to the A7585D through a 50 Ω resistance in series, as shown in **Figure 10.3**. The provided PCB adapter, instead, is equipped with independent filters for each bias line to be fed into the SiPMs.

Since the A7585D feeds the SiPM with positive high voltage, the anode of SiPMs are independently connected to the ASIC input lines, while cathodes are connected to the bias voltage (see **Figure 10.3**). On the A55PETx, before feeding the ASIC input channel, the SiPM signal passes through two components. By default, a short circuit configuration is mounted, with a series 0 Ω resistance and no component mounted towards ground. In this configuration, the SiPM generates a positive pulse which is processed by the ASIC.

At the ASIC input stage, an 8-bit DAC allows to perform a fine tuning of the bias, individually for each SiPM channel. The voltage can be adjusted in the range 0-1 V. This is important in particular to tune the gain of each element, especially when connecting single SiPMs, which can have a spread on the breakdown voltage up to 400 mV. In default SiPM configuration (as in **Figure 10.3**) , increasing the DAC value has the effect of lowering the effective bias voltage on the SiPM.

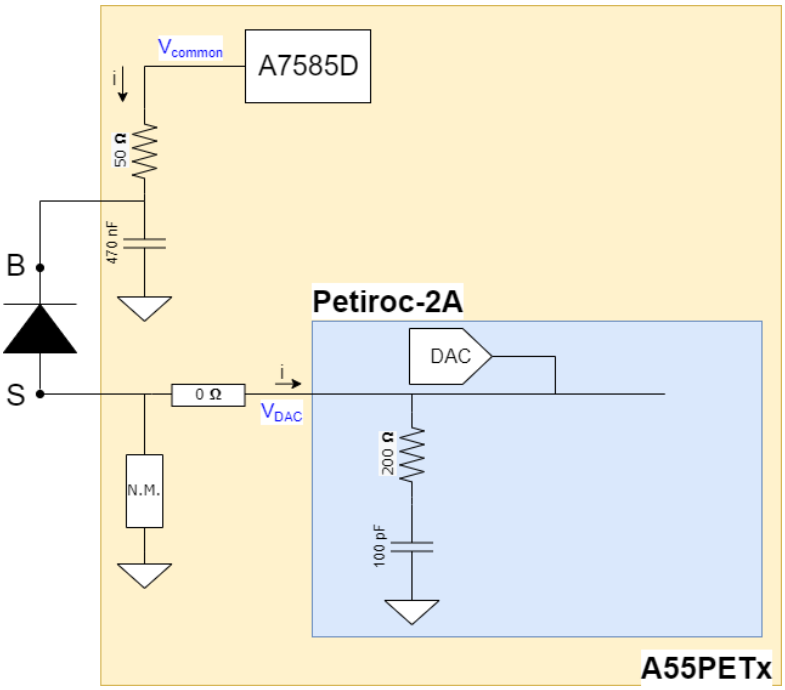


Figure 10.3: SiPM connection scheme to the ASIC input lines in standard configuration. N.M. means Not Mounted component.

Note: in case the user wants to use negative bias SiPMs, an external power supply is needed and the board components must be modified to achieve the correct coupling of the SiPMs to the ASIC. Refer to **Connecting a matrix in negative-bias configuration** for more details.

Pitch Adapter Kit

CAEN provides with the A55PETx board, an adapter kit composed by one or two 64-ch PCB boards, to allow the user to easily connect any kind of single SiPM, matrix or array to the board.

The PCB is designed to be pressure-pluggable onto the input connectors available onboard and converts a couple of SAMTEC SS4-40-3.00-L-D-K-TR to a **double 2.54 mm strip connector** (see **Figure 10.4**)**.** In this way, the user can easily mount through-holes 2.54 mm headers on the adapter PCB to connect SiPMs anode/cathode lines. Using two of these PCBs allows to exploit the 128 readout channels of the A55PETx board, exposed on the 2.54 mm pitch strips.

The adapter provides 64 signal readout lines (S_x) and 64 sensor bias (B) lines. Each adapter has two 2.54mm-pitch strip connectors, each one exposing 32 bias/signal couples. Once the adapters are plugged in, the bias can be provided by the A7585D on the A55PETx board itself or externally through the LEMO HV connector available on the adapter. The jumper P2, if inserted, connects the bias pins to the DT5550W High Voltage generator while the LEMO connector is always connected to the Bias pins. The adapter is designed to optimize connections to SiPMs. Each detector has independent bias lines filtered with 1kΩ resistor and 100nF capacitor, as shown in Figure 10.6

In order to operate with external bias generator, the jumper P2 should be removed from the pitch adapter, in order to avoid damaging the A55PETx board. External high voltage should not exceed 100V.

Note: the channels pinout indicated on the PCB silkscreen is merely indicative. The effective correspondence with the ASIC channels is defined in the *Mapping* section of the DT5550W Readout Software.

Note: Refer to Figure 10.7 for instructions to correctly plug the pitch adapter onto the A55PETx.

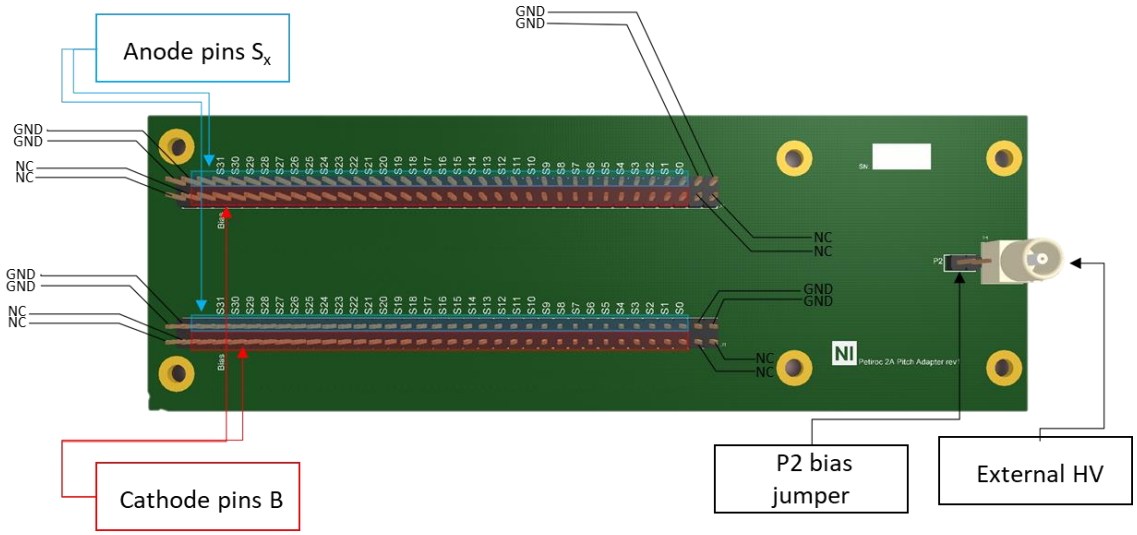


Figure 10.4: view of the 64-ch pitch adapters. The strip connectors (each for 32 channels), the External HV LEMO and the P2 jumper are clearly visible.

Name	Description
Anode pins S_x	**2.54 mm strip – 32 pins.** Connection to ASIC input lines, to wire SiPM anodes. GND = ground
Cathode pins B	**2.54 mm strip – 32 pins.** Connection to High Voltage lines, to wire SiPM cathodes for biasing. NC = not connected
External HV	**LEMO HV.** External High Voltage input for SiPM biasing. Connection to SiPMs cathodes as shown in **Figure 10.6**. The external HV connector is always connected to the Cathode pins B
P2 Jumper	If inserted, connects the Cathode pins B to the DT5550W High Voltage generator

Table 10.2: description of the pitch adapter connectors.

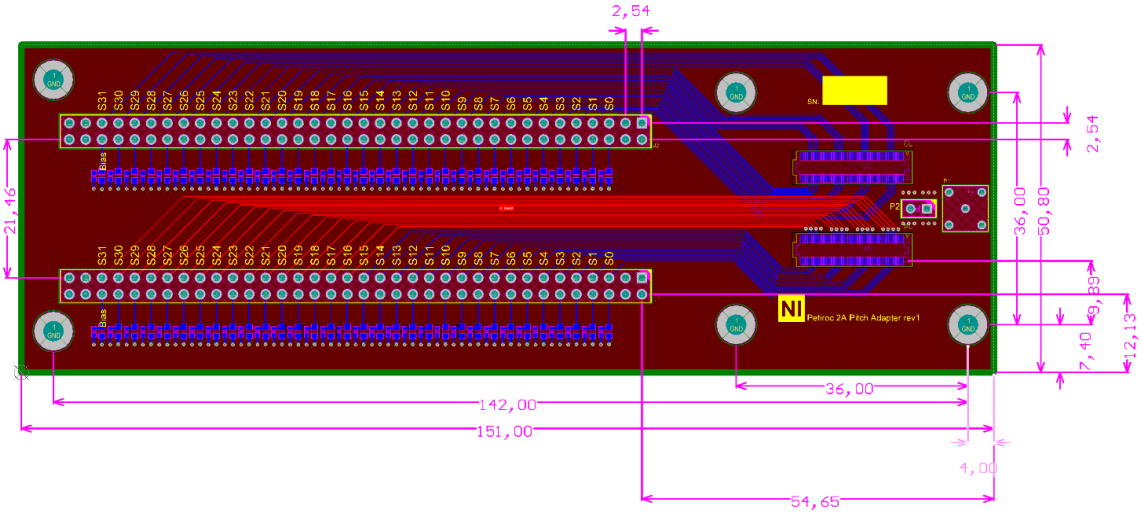


Figure 10.5: dimensions of the pitch adapter.

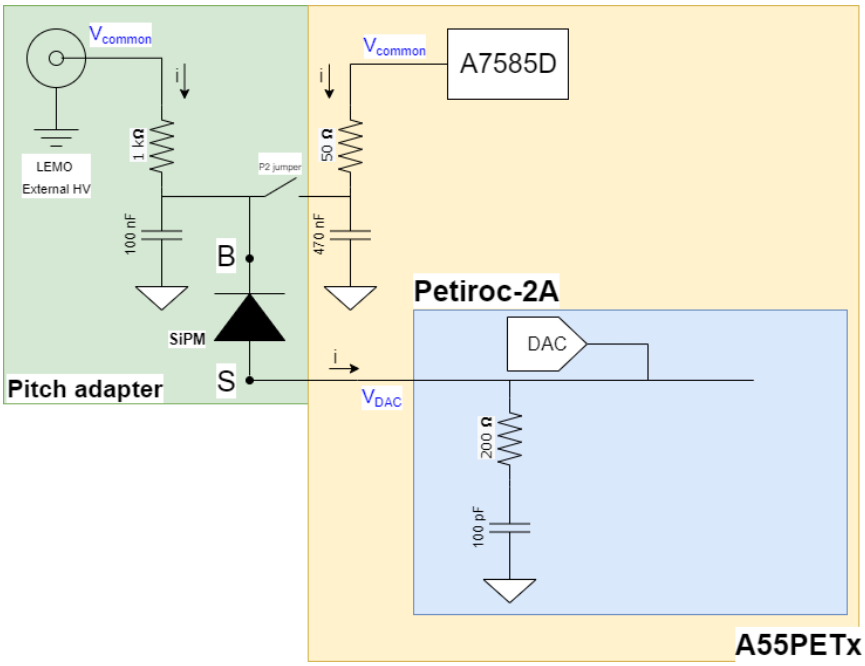


Figure 10.6: SiPM connection scheme to the ASIC and biasing lines when using the pitch adapter kit

Figure 10.7: Top: how to plug the pitch adapter on the board's SiPM connector. The connectors are pressure-pluggable. Bottom: general view of a DT5550W with A55PET4 piggyback and two pitch adapters plugged in. In this configuration, all 128 channels of the DT5550W board are exposed on the strip connectors.

Connecting a matrix in negative-bias configuration

The A55PETx piggyback is designed to provide positive bias voltage to the SiPM. In this standard configuration, suitable for a wide range of SiPM matrices, the A7585D feeds the SiPM with positive high voltage, the anode of SiPMs are independently connected to the ASIC input lines, while cathodes are connected to the bias voltage line (see **Figure 10.3**).

However, exploiting the features of the pitch adapter, it is possible to read out SiPMs also in negative-bias configuration, for instance the one suggested for SensL ARRAYJ−60035−64P with common cathode. In order to do that, an external high

voltage source can be connected to the LEMO of the pitch adapter and the board needs a component modifications in order to correctly couple the sensor to the ASIC. A typical connection of a negative bias SiPM is shown in **Figure 10.8.**

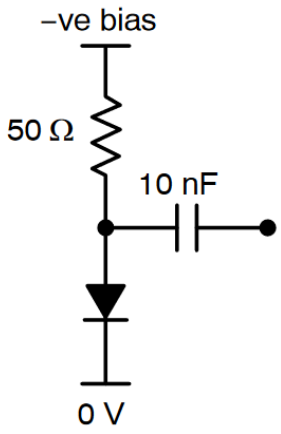


Figure 10.8: typical connection of a cells of a SiPM matrix with common cathode using negative bias.

In order to AC couple the sensor, the user needs to mount a series 10 nF capacitance replacing the 0 Ω resistance (mounted by default), as shown in **Figure 10.9.** The component to ground can be left not mounted. Using the AC coupled configuration, the ASIC internal DAC is useless.

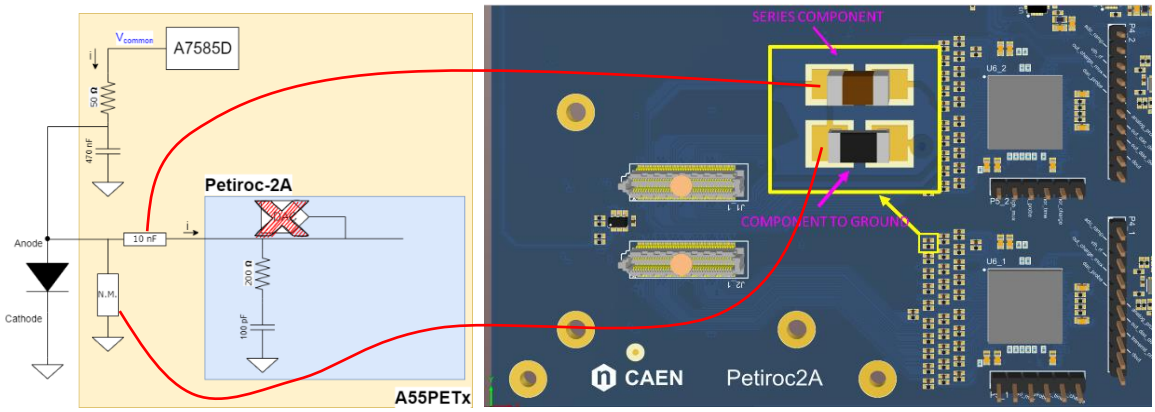


Figure 10.9: connections of the SiPM to the ASIC input stage, to obtain AC coupling with negative bias voltage. All *series components* (by default 0 Ω resistance) must be dismounted and replaced with a 10 nF capacitance. The *component to ground* can be left not mounted. The hardware components for each input channels, are shown on the right.

Temperature Feedback

Near each SiPM connector hosted on the A55PETx board, a temperature sensor is soldered. This sensor is read by the FPGA and the information is used by the DT5550W Readout Software for SiPM bias active compensation during temperature changes.

In case of using SiPMs mounted on an external PCB, it is recommended exploiting the USER I2C bus, available on the motherboard, to read out an external sensor (pinout of I2C on the PCB serigraphy). In this case, in order to use the active bias compensation as defined in the DT5550W Readout Software, the user needs a Texas Instruments TMP100 external sensor, configuring its address at 0x50, bit A0 = GND and A1 = 3.3V.

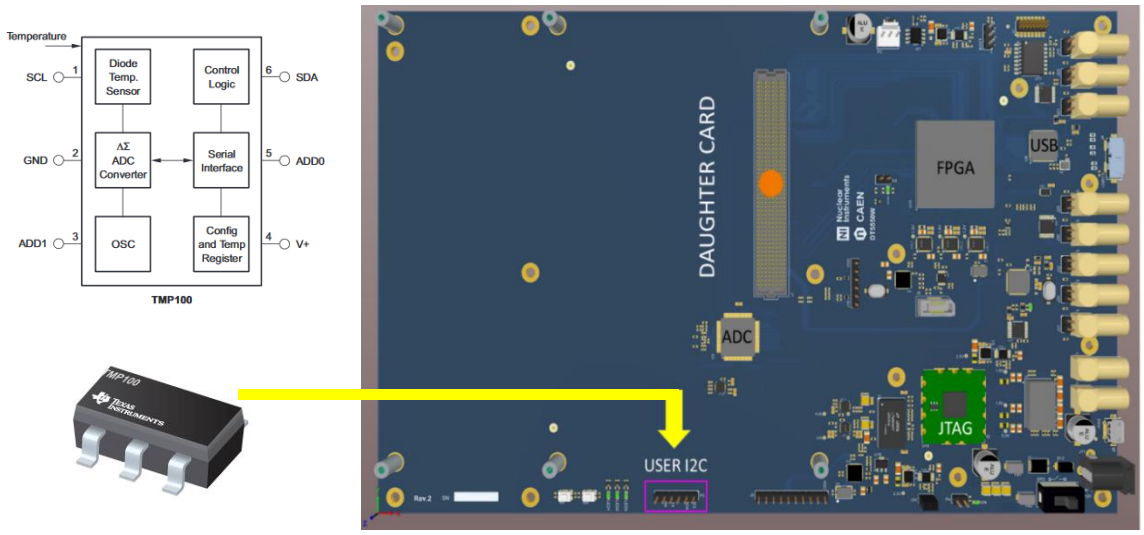


Figure 10.10: the user I2C interface on the motherboard, to be used for external temperature sensor connection.

In general, there are several methods to perform the active SiPM bias compensation, using:

- The average temperature read out by the two sensors soldered on the piggyback PCB, near the matrix connectors. This method is directly supported by DT5550W Readout Software.
- The temperature read by an external sensor. If using a Texas Instruments TMP100 with address 0x50, this method is directly supported by DT5550W Readout Software.
- A temperature read out with any other method (like thermocouples or similar sensors readout). The provided temperature can be passed to the SDK libraries for active bias compensation.

Test Pins

On the sides of each ASIC hosted on the A55PETx board, some test pins are available, to allow the user to debug the internal operation of the chip itself. The name of each pin is reported on the PCB serigraphy (see **Table 10.3** for more details)

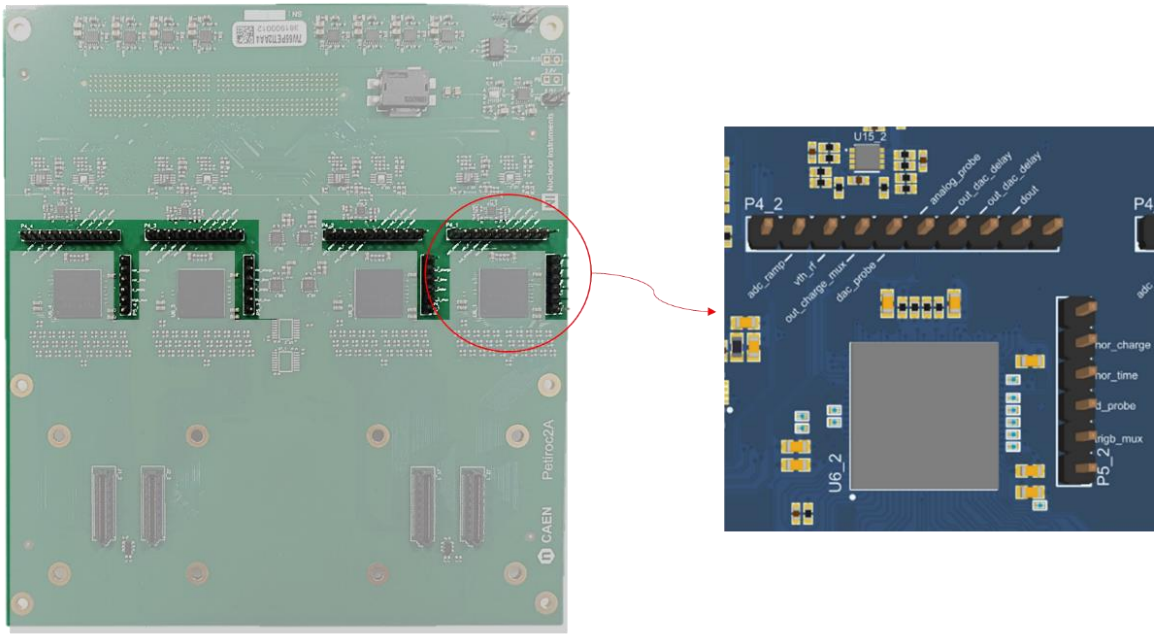


Figure 10.11: the test pins for A55PETx piggyback boards.

Pin name	Description
trigb_mux	**Charge triggers multiplexed output**, available during analog readout.
d_probe	Internal probe managed by the software. For the selected channel it shows one of the following: • **charge trigger**

	• **ADC ramp start** • **hold signal** for the slow shaper, i.e. the delayed time trigger.
nor_time	**NOR32 of the time triggers** (disabled by default, to reduce the noise during the readout)
nor_charge	**NOR32 of the charge triggers**
dout	**Serial output of the converted bitstream**, available during digital readout
out_dac_delay	Signal verifying the correct operation of the **delay setting for the hold signal**.
analog_probe	Internal probe managed by the software. For the selected channel it shows one of the following: • **the voltage on the input DAC** • **the preamplifier output** • **preamplifier output of the dummy channel** • **the time threshold** with fine adjustment • **TAC ramp** • **charge shaper output**
dac_probe	**Input DAC output**
out_charge_mux	**Charge multiplexed output**, available during analog readout
vth_rf	**Reference voltage for the threshold settings**
adc_ramp	**Ramp of the Wilkinson ADC**

Table 10.3: A55PETx test pins description.

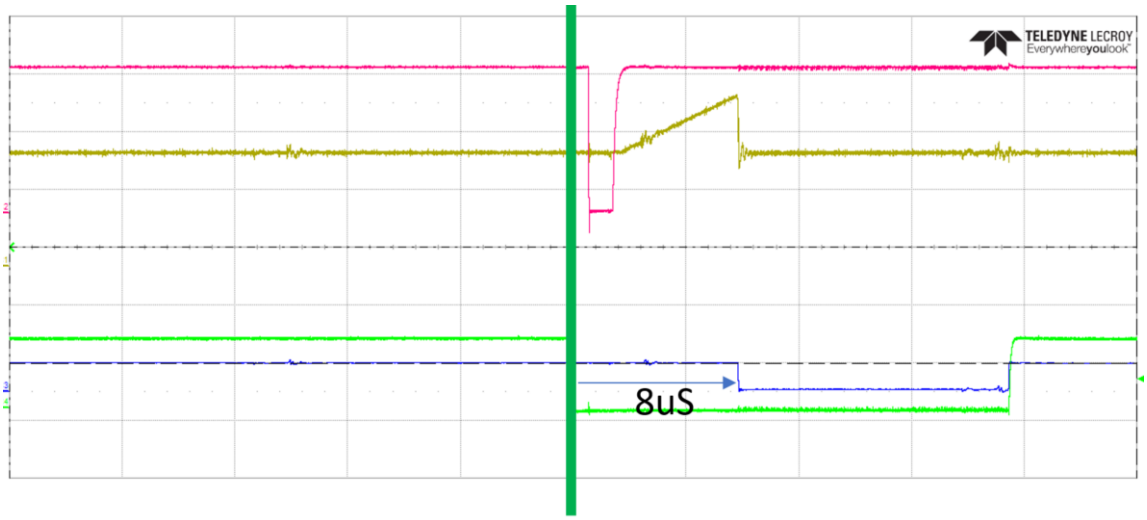


Figure 10.12: a typical debugging acquisition made at the oscilloscope using test pins. Yellow: the ADC ramp. Magenta: the NOR32 charge trigger. Blue: the Transmit_on signal. Green: The NOR32 time trigger. The charge trigger starts the ADC ramp. When the digital conversion is finished, the ADC ramp falls and the transmit_on signal is set and the ASIC begins to transfer digital data to the FPGA. This happens 8 µs after the time trigger, which must be considered as the conversion time.

Motherboard I/Os

When the A55PETx is mounted onto the DT5550W motherboard running the default firmware to manage the Petiroc-2A chips, the assignment of the 8 programmable LEMO I/Os on the DT5550W motherboard is also defined as shown in the following scheme.

Figure 10.13: the programmable LEMO digital I/Os of the DT5550W

LEMO	Description
A	**CLK IN** - accepts a 25MHz, 3.3V signal, 50 Ω input impedance.
B	**CLK OUT** - provides a 25MHz, 3.3V signal (can be used to drive a 50Ω coaxial cable).
0	T0 OUT
1	RUN OUT
2	TRG OUT
3	BUSY
4	VETO IN
5	TRG EXT
6	T0 IN
7	RUN IN

Table 10.4: assignment of the programmable LEMO digital I/Os in the default firmware for A55PETx management.

11 Functional Description

The A55PETx is based on the functions and readout chains of the PETIROC 2A WeeROC ASIC. A scheme of the chip is given below.

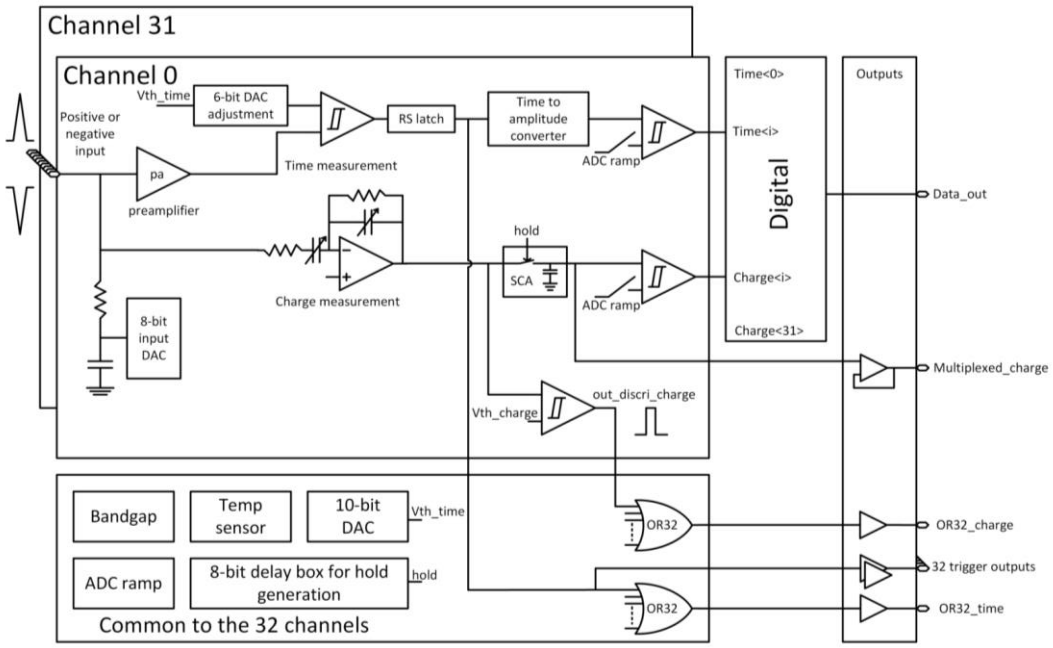


Figure 11.1: scheme of the PETIROC 2A ASIC.

Each of the 32 readout channels available in the chip integrates a classical readout chain made of preamp, fast and slow shaper, a trigger line with a timing resolution better than 35 ps, a TDC, a Sample&Hold circuit and an internal ADC. Moreover, for each channel, a block for the fine bias regulation is available (0 …1 V).

ASIC Trigger Operation

The ASIC operation relies upon two trigger lines:

- A time trigger, which allows to sample the shaper output and perform precise time measurements
- A charge trigger, which selects events basing on a charge threshold and is used to validate the time trigger.

The time trigger, internally delayed, is used to sample the peak of the slow shaper signal. The shape of the slow shaper signal is configurable, to maximize the energy resolution.
The time trigger is also used to perform an accurate timestamp measurement on each channel. Each channel integrates a TAC (time to amplitude converter) which is used to calculate the temporal distance between the reference clock and the event causing the trigger.
The trigger signals are given as output on 32 independent lines and the trigger information are stored in a register, called HIT, which can be read after each recorded event to know which channels effectively caused the trigger.
The time trigger can operate in latched or non-latched mode. In latched mode (as set in the default firmware) the trigger signal is stored in a flip-flop until the reset event. The reset can be performed manually through a dedicated reset line (RazChn) or automatically at the end of the acquisition (this latter option is set in the default firmware). In non-latched mode, the comparator output is directly connected to the output pin. This is useful to count the exact number of trigger hits on each channel.

The PETIROC ASIC uses two clock signals in phase for its operation, at 40 MHz and 160 MHz. The 40 MHz clock is used as coarse clock for the TDC. Being available a fine time (with resolution 37 ps and full scale 20 ns) and a coarse time (with resolution 20 ns and full scale 20 µs), it is easy to correlate the measurements of multiple ASICs in clusters.

The slow shaper output sampled by the trigger it is digitized by the internal 10-bit ADC. Besides this, the slow shaper output is also provided to the charge trigger, which operates on the filtered signal, so that it less affected by the noise even if it has a very poor timing resolution. Therefore, the charge trigger can be used as validation of the time trigger.

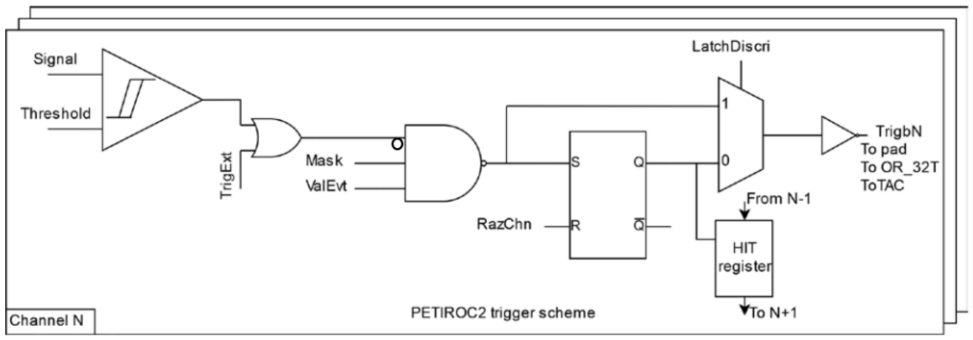


Figure 11.2: the PETIROC 2A trigger scheme

Many trigger signals are available at the ASIC outputs and are sent to the DT5550W FPGA, to select some events and reject other ones, basing on a trigger logic. The available triggers are:

- **32 independent time triggers**, one for each channel of the ASIC. The trigger is high when the inverted signal coming from the preamplifier exceed the set trigger threshold. Basing on the input signal polarity, the trigger operates on the rising or falling edge. The time trigger threshold is composed of a coarse part, common to all channels, and a fine part which is adjustable independently for each channel. The time trigger can be vetoed for each channel. In this case the trigger signal for the specific channel is not sent in output and it does not participate to the OR32 logic among the channels. It is possible to disable the trigger outputs on the ASIC pins to reduce the noise but to let them participate to the OR32 logic.
- **NOR32 time trigger.** It is the OR32 of time triggers in inverted logic. It is available as output of the ASIC and it is used internally to generate the "hold" signal to extract the charge information
- **NOR32 charge trigger.** It is the OR32 of charge triggers in inverted logic. The individual charge triggers are not available as output at the ASIC pins. Only the OR32 is available.
- **Charge Trigger MUX.** It is not a real trigger but a shift register, which contains the independent charge trigger of each channel for the last acquired event. In output, the 32 bits indicating the channels causing the charge triggers are available.

External Trigger

The PETIROC 2A can be fed with an external trigger, which is in logic OR with the time trigger. The external trigger can be used for three main purposes:

- verify the ASIC operation without any signal
- pedestal measurements
- imaging trigger for multiple ASICs and boards

The pedestal measurement is fundamental for the ASIC channels equalization. The ASIC can be triggered by an internal generator with programmable frequency (1 kHz by default). At this point, the transferred data are useful to measure the baseline in absence of any input signal.

The imaging trigger is important to tune energy measurements on multiple pixels. For example, we can consider a SiPM matrix connected to two ASICs. If the light on a pixel of the matrix is very low but enough to cause a trigger, for instance, on ASIC A, also the adjacent pixels will count some charge even if the signal is too low to cause a trigger. Some of these pixels could be connected to ASIC A and will be readout since the channel trigger cause the entire ASIC to be readout, while pixels connected to ASIC B will not be readout and, therefore, some information are lost.
The imaging trigger, when enabled via software, propagates the trigger generated by an ASIC to all the other ASICs and to other boards, allowing the readout of the entire sensor connected.

Note: the external trigger operates on the time trigger. If the readout based on the charge trigger is enabled, the external trigger cannot start the readout process.

Charge Measurements

The charge measurement involves both the charge and time lines of the PETIROC.
Basically, the charge of the input signal is measured through a Track&Hold system, where the peak of the slow shaper output is sampled by the time trigger signal. Since the PETIROC has not an internal peak sense holder, the temporal information on the position of the peak must be resolved through the information on the time trigger. In practice, the

OR32 of the time triggers is delayed and used to perform the "hold" of the slow shaper output (see **Figure 11.3**). Therefore, having a time trigger is mandatory to start the sampling of the shaper and obtain a charge measurement. In case all time triggers are vetoed, even in presence of a charge trigger, it is not possible to acquire the correct analog signal. On the other side the time trigger needs to be correlated to the charge trigger to avoid the sampling of the shaper in a casual position, resulting in big fluctuations on the measured charge.
This way of operating is quite immune from the random walk since the charge preamplifier is so fast and the time trigger threshold so low, that the amplitude of the signal is not relevant to decide the exact moment to sample the flat top of the shaper, which much longer than the time jitter due to the time walk.

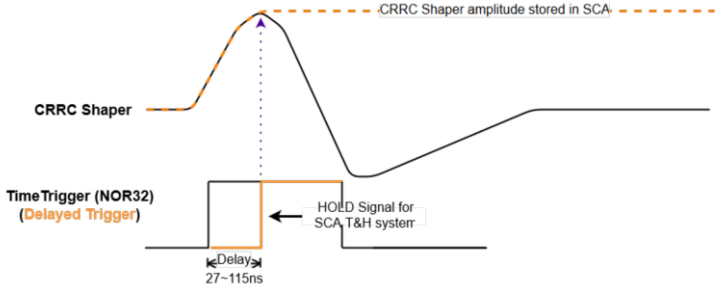
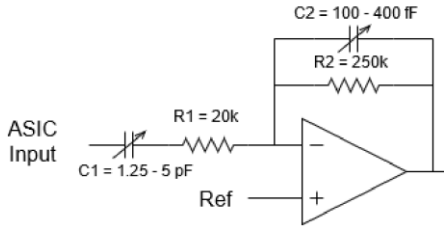


Figure 11.3: the charge measurement mechanism in PETIROC ASIC.

Since the shape of the slow shaper is adjustable, varying the shapes of the input signals and the trigger threshold, the delay between the time OR32 and the sampling instant must be programmable. To find the correct delay, it is needed to pulse the SiPM with light and identify the point of maximum in the measured charge amplitude. This scan can be easily performed manually thanks to the DT5550W Readout Software.

The shaper is adjustable by varying the input and feedback capacitance of the RC-CR circuit, as shown below. See **[RD1]** for more details.



C1 (pF)	R1 (kΩ)	τ 1 (ns)	C2 (pF)	R2 (kΩ)	τ 2 (ns)
1.25	20	25	100	250	25
2.5	20	50	200	250	50
3.75	20	75	300	250	75
5	20	100	400	250	100

Figure 11.4: the RC-CR shaper with adjustable capacitance to change the shape of the output signal.

Time Measurements

The time measurement with PETIROC can be performed in two ways:

- Using external TDCs connected to the 32 time triggers output. This operating mode allows to maximize the timing resolution of the ASIC, but it requires developing an accurate 32 channels TDC in the FPGA.
- Using the internal TDC, which has a bin resolution of 37ps.

The DT5550W equipped with its default firmware exploits this latter method.

The internal TDC is realized through two circuits:

- a "coarse" circuit, which counts uninterruptedly the clock cycles starting from a reset signal (rstb). When an event is detected by the time trigger, the value of the coarse counter is stored in a register. The coarse counter has 10 bits and operates at 40 MHz, with a full scale of 20 µs. This implies that it is not possible to use the coarse counter to perform measurements between different events, since the deadtime of the ASIC to perform

a digital readout is more than 20 µs. Therefore, the main function of the coarse circuit is to allow an easy implementation of clusters within the same ASIC, between different ASICs and between different boards. For example, if all the considered ASICs have the same clock and are reset by the same signal, in case an event involves multiple channels, it is possible to open an "acceptance window" which groups in the same event all the channels (cluster) which detected the event itself within the "acceptance window". This is useful when performing imaging, in order not to separate events which only ran across different distances.

- a "fine" circuit, composed by a TAC, to perform a fine time measurement. The TAC measures the time between the event and the subsequent clock cycle. The fine time conversion is about 37 ps/ADC unit.

The **absolute timestamp** is given by the following formula:

$$absolute\ timestamp = (\text{coarse time} + 1) * (25\ ns) - (\text{fine time}_{\text{ns}})$$

In order to calculate the fine time, an offline analysis on the dataset is needed. Infact, the fine time TDC has an offset and LSB changing channel-to-channel and ASIC-to-ASIC. Therefore, the offset (*$fine_0$*) and ps/LSB (*alfa*) parameters need to be extracted from the dataset in the following way:

$$fine_0 = \text{MIN. VALUE (dataset)}$$

$$alfa = \frac{25ns}{MAX.VALUE\ (dataset) - MIN.VALUE\ (dataset)}$$

The fine time in ns can be then calculated as

$$fine\ time_{ns} = (fine\ time - fine_0) * \text{alfa}$$

The **ToF (Time of Flight)** between two channels is performed using the following formula

$$ToF = (\text{coarse time\_1} + \text{fine time\_1}) - (\text{coarse time \_2} + \text{fine time\_2})$$

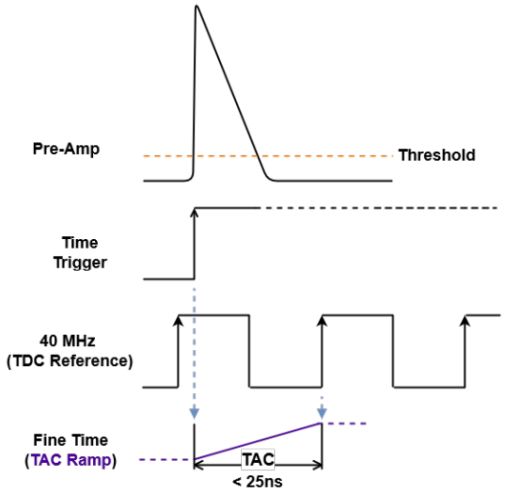


Figure 11.5: time measurements scheme for PETIROC 2A, using the internal TDC.

Besides the internal TDC, the DT5550W hosts an external timestamping unit for each ASIC, which generates a timestamp at 30 bits with LSB of 6.25 ns. This timestamp is captured at the arrival of the trigger which causes the starting of the readout process into an ASIC. Since this timestamp has a full scale of 6.7 s, it can be used to perform time measurements between subsequent events. Since the ASIC readout is always performed at the entire chip level (not at level of a single channel), this timestamp is correlated to the event and not to the channel.

The DT5550W provides a T0 time reference signal. The T0 can be configured via the DT5550W Readout Software to operate only on the 30-bits timestamp or also on the internal ASIC TDC. Therefore, the T0 signals allows to synchronize multiple ASICs and multiple boards. When an acquisition is started, the DT5550W motherboard generates a T0 signal towards all the ASICs hosted on the piggyback board. The T0 signal resets first the 160 MHz counter and then, through

the *rstb* signal, the coarse counter. In this way all the ASICs are synchronous, and it is possible to correlate time measurements between different ASICs.

Also, in case of multiple boards, the T0 signal, together with the CLK IN/OUT daisy chain, allows the different boards to count with the same clock and the same time reference. Therefore, it is possible to easily scale the DT5550W system to readout many channels and maintain each board independent.

Note: the T0 signal is sampled by the FPGA with 160 MHz clock and by the ASIC with 40 MHz clock. Consequently, the DT5550W timestamping unit and the ASIC coarse counter begin to count starting from the clock cycle after the T0 arrival. This introduces an uncertainty on the T0 measurement (25 ns for the ASIC and 6.25 ns for the FPGA) and therefore it is not possible to perform accurate time of flight measurements between a start signal (for example a trigger from a laser pulse) and the signal generated by the arrival of photons on the SiPM. **The timing resolution of 37 ps can be reached only for ToF measurements performed between the ASIC channels or channels of different ASICs**.

Note: a way to perform accurate ToF measurements between T0 and the ASIC channels, is to synchronize the clock of the DT5550W with the clock of the light source illuminating the SiPM.

Readout Modes

The PETIROC 2A readout can be performed in three ways:

- **Photon Counting**: only the trigger lines are used, in non-latched mode, to count the number of trigger transitions (i.e. the number of events) on each ASIC channel. When using this readout mode, the ASIC clocks are switched off.
  This allows to count events with a frequency of more than 10 MHz

- **Analog Multiplexed Readout**: the time trigger lines can be used to implement in the FPGA a trigger logic which is able to select some events. In alternative, if the accurate the time measurement is not important, the time trigger lines can be disabled and only the NOR32 charge trigger can be used to analogically readout the ASIC. This latter way of operation, together with the clocks disabling, minimize the noise and maximize the energy resolution. When using the analog readout, only some dedicated analog lines of the ASIC are used and the charge measurement is performed using the external ADC hosted on the DT5550W motherboard.
  This allows to read out up to 500k events/s.

- **Fully Digital Readout** (*fully managed by the DT5550W default firmware and DT5550W Readout Software*): the time triggers are used to know when an event has been captured by the ASIC. After a trigger, the ASIC internal ADC is started, and the energy and time information are digitized. At the end of the conversion, the ASIC send to the FPGA a serial stream at 80 MHz which is decoded by the FPGA and then sent to the PC through USB bus. For each channel, the transferred data are:

  - **Charge:** value converted by the ADC
  - **Fine time:** time between the event and the clock (37 ps resolution)
  - **Coarse time:** time between the T0 (ASIC signal *rstb*) and the event (20 ns resolution)
  - **Hit:** a flag indicating if the channel has generated a time trigger

  Using digital readout, the maximum readout frequency is 40 kHz.

Photon Counting

If the charge information is not required, it is possible to work in photon counting mode.

In this mode the firmware just counts the transitions of the channels trigger output pins: the ASIC works in fully asynchronous mode and no internal ADC/TDC is enabled. Only the ASIC fast shaper and comparator are used.

It is possible to implement a photon counting firmware, to read out the number of photons per channel from the beginning of the run and extract a list (energy of a series of events) in a specific integration window opened by a start signal. The start signal could be generated by an internal periodic signal or by an external signal provided on one of the programmable LEMO available on the DT5550W motherboard. Our suggestion is to set this window width between 100ns and 4s. The internal start signal frequency could be set between 1Hz and 1MHz.

The readout scheme in photon counting mode is shown below.

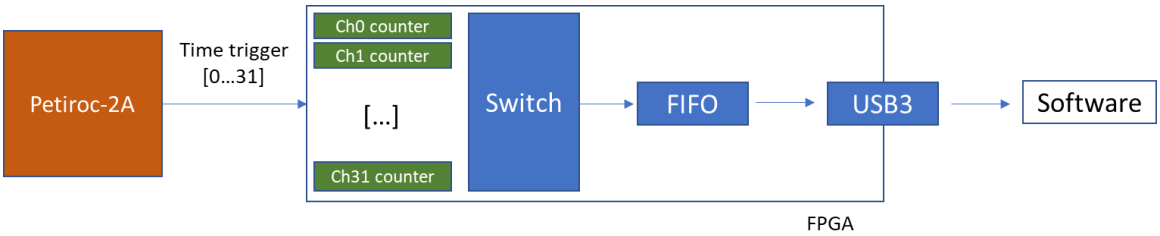


Figure 11.6: readout scheme of DT5550W and ASIC operating in photon counting mode.

Analog Multiplexed Readout

The PETIROC 2A can be read out using its analog multiplexed output through the external 80 MS/s, 14-bit ADC, which is mounted on the DT5550W motherboard. This ADC has 8 channels but only the odd channels (1,3,5,7) are connected to the "*out_charge_mux*" output of the ASICs.

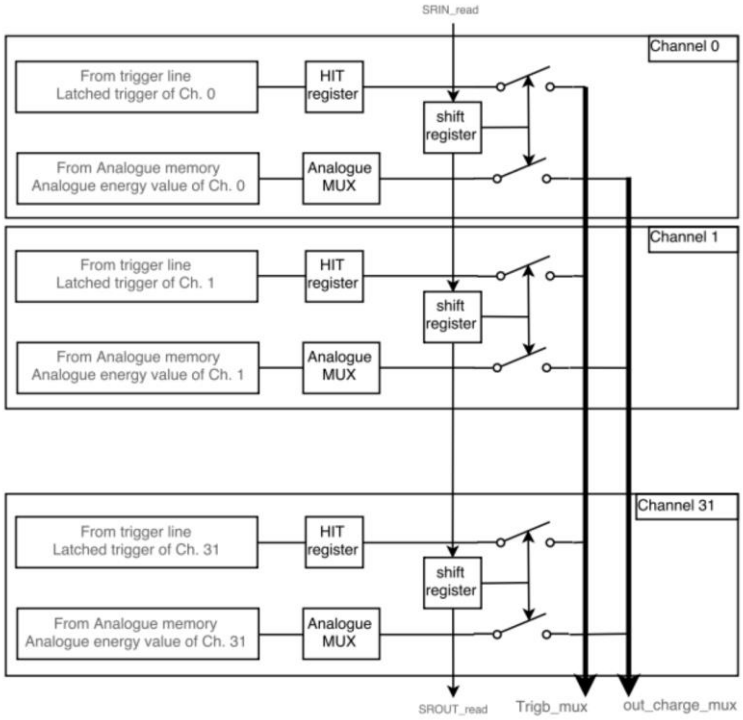


Figure 11.7: the analog readout scheme of PETIROC 2A, where analog multiplexed data are available as outputs.

On the "*out_charge_mux*" and "*Trigb_mux*" outputs are available, for all channels, the charge and trigger values stored by the ASIC for the latest event. These data are read out thanks to a shift register which selects a channel at each subsequent clock cycle. There are two digital lines to control the analog shift register:

- *SRIN_read*: user must load a '1' at the beginning of the read procedure to select the first channel
- *Ck_read*: user must generate a few clock cycles equal to the number of channels plus one to shift out the analog information.

The charge analog information is provided on the *out_charge_mux* output. At the same time, on the *Trigb_mux* output, the multiplexed triggers are available, providing a coarse timestamp for the correspondent charge events.

In analog readout mode, the FPGA timestamps the events with a resolution of 12.5 ns.

The analog data conversion is done on the DT5550W motherboard by mean of the 80 MS/s, 14-bit ADC. The charge data are correlated to the channel knowing the number of clock cycles generated from the beginning of the readout process.

Note: the analog multiplexed readout mode is not fully implemented in the default firmware preloaded on the DT5550W. However, using the default firmware, it is possible to visualize the involved analog signals on a monitor, which can be used as debugger for the analog section of the ASIC. This means that the readout process is completely performed but the data are not stored in the FIFO to be transferred to the PC, so that they are only shown on a virtual oscilloscope internal to the board and transferred to the software for the graphical visualization.

Fully Digital Readout

The PETIROC 2A has an integrated ADC/TDC and can provide the result of the measurement as a binary serialized stream. *The serial bit-stream contains for each channel the trigger information, the time of arrival and the charge information*. The stream is read out by a serial link at 80 MHz between the ASIC and the FPGA. The transmitted data packet is organized as follows:

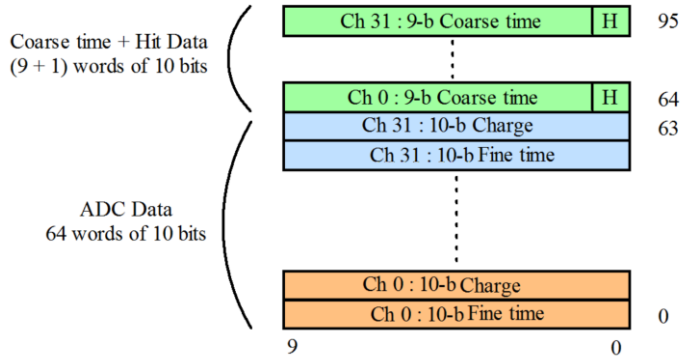


Figure 11.8: structure of the data packets transferred during digital readout

A total of 96x10 = 960 bits is sent for each event to the serial link. The effective readout time is 12 µs for each event. The ASIC does not perform any zero suppression, therefore also channels without any trigger are always transferred.
All the transmitted numerical values are decoding in gray code. For the fine time and charge, the value 4 flags an underflow of the ADC, while 1020 flags an overflow.

The digital readout process is coordinated by the FPGA firmware. It is possible to choose if the readout starts because of a charge or a time trigger. At that point, if the FPGA detects a trigger, it can accept it and proceed as described in the following, or it can reject it and generate a 100 ns pulse on the "RazChn" line to reset the ASIC. If the event is accepted, the FPGA starts the ASIC ADC converter using that "Start_Conv" signal. When the conversion is completed the ASIC automatically sets the "TransmitOn" signal and the ASIC is rearmed to capture a new event. In the meantime, the FPGA starts to sample the 80 MHz data stream and deserializes it. The deserialized data contains the energy/time/position for all the cannels of the ASIC and generate an event. Events from all channels are pushed in a common FIFO buffer and are directly read out by the DT5550W Readout Software using the USB 3.0 communication port of the DT5550W board.

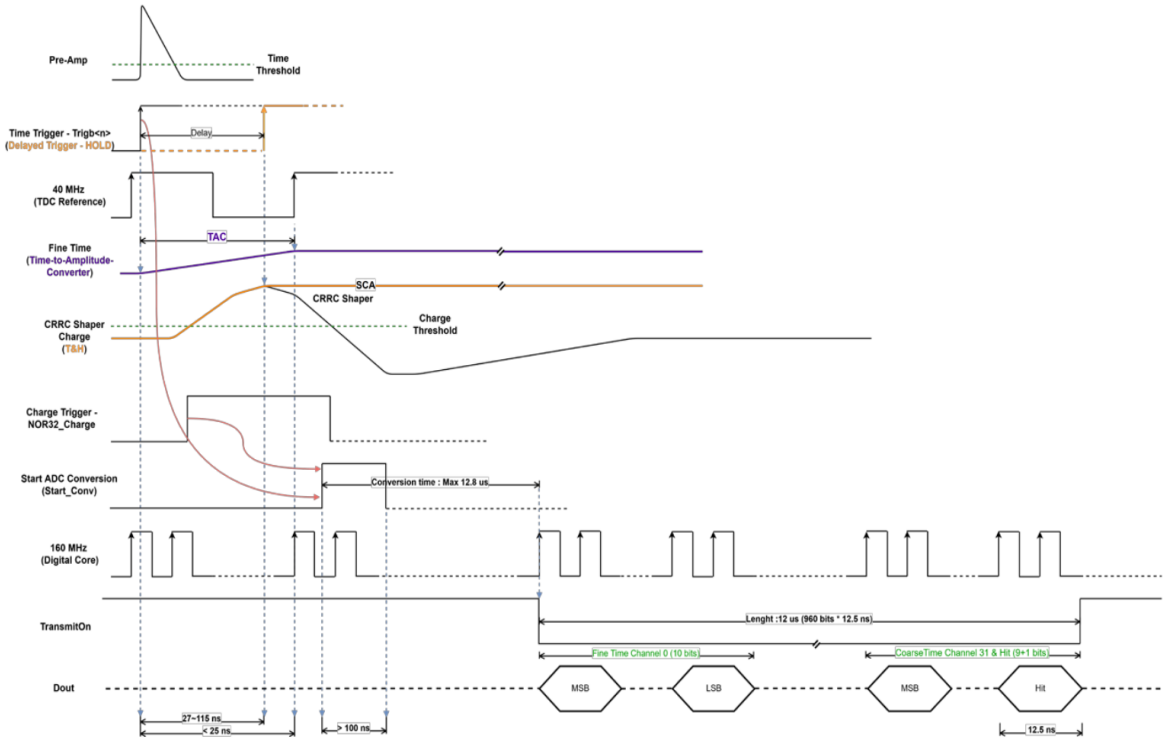


Figure 11.9: the digital readout scheme of PETIROC 2A, where data serialization process is shown.

Note: the PETIROC 2A digital readout mode is fully supported and managed by the default firmware preloaded on the DT5550W and by the DT5550W readout software, since this is the most powerful readout mode, which maximizes the amount of information that can be extract from the ASIC.

Default trigger logic

The default trigger logic is implemented in the FPGA firmware of the DT5550W, as shown in **Figure 11.10**. It is possible to set each ASIC to trigger independently using the time triggers, or use a global board trigger that is the OR of all the possible triggers (internal, software, external , etc.).

The external trigger can be fed at LEMO4 of the DT5550W motherboard. It can be used for three main purposes:

- verify the ASIC operation without any signal
- pedestal measurements
- imaging trigger for multiple ASICs and boards

The pedestal measurement is fundamental for the ASIC channels equalization. The ASIC can be triggered by an internal generator with programmable frequency (1 kHz by default). At this point, the transferred data are useful to measure the baseline in absence of any input signal.
The imaging trigger is important to tune energy measurements on multiple pixels. For example, we can consider a SiPM matrix connected to two ASICs. If the light on a pixel of the matrix is very low but enough to cause a trigger, for instance, on ASIC 1, also the adjacent pixels will count some charge even if the signal is too low to cause a trigger. Some of these pixels could be connected to ASIC 2 and will be readout since the channel trigger cause the entire ASIC to be readout, while pixels connected to ASIC 2 will not be readout and, therefore, some information are lost.
The imaging trigger, when enabled via software, propagates the trigger generated by an ASIC to all the other ASICs and to other boards, allowing the readout of the entire sensor connected.

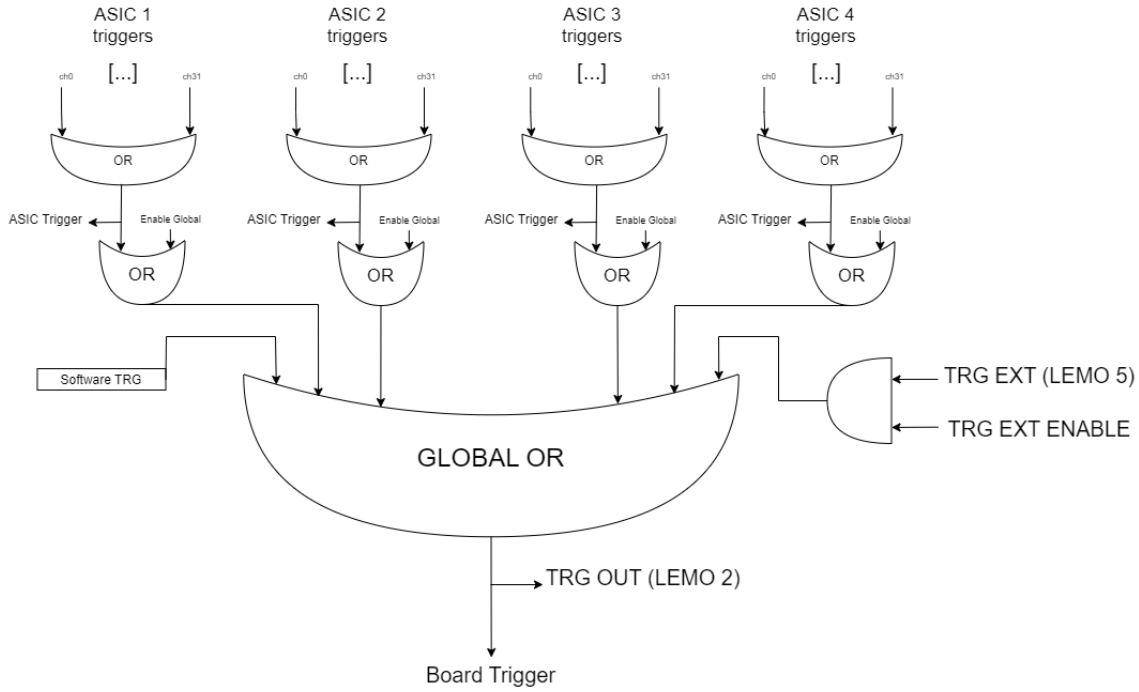


Figure 11.10: scheme of the triggering logic set in the default firmware loaded on DT5550W for A55PETx management.

ASICs configuration

The configuration of all the ASICs hosted on the piggyback board is managed by the DT5550W Readout Software, which allows the user to easily set some of the ASICs parameters.
The ASIC is configured via a shift register with more than 600 bits. Some parameters are preconfigured, to make the board working correctly in digital readout mode. In any case the Readout Software is distributed as open source code and the used can modify it to access the configuration bits which are not accessible from the software GUI (refer to **[RD1]** for a detailed description of each bit).

The configuration is generated directly by the Readout Software, as a bitstream representing the sequence to be loaded in the ASIC. The bitstream is transferred via USB bus from the PC to the FPGA, which stores it in 32-bit registers; at the beginning of the programming sequence, the FPGA sends the stream to the ASIC to configure it. The FPGA and the Readout Software allows to manage independently the configuration of each ASIC.

12 Firmware and data format

The default firmware version preloaded on DT5550W for A55PETx piggyback allows to perform the following operations:

- Petiroc-2A parameters configuration
- Configuration of the triggering logic as per the scheme in Figure 11.10:
  - ASICs trigger signals (by default OR32)
  - External Trigger
  - Veto, to inhibit all trigger signals
- Receive digital data from Petiroc-2A, i.e. energy and time for each channel
- T0/Veto management
- Read out data from multiple Petiroc chips
- Readout of the analog data from Petiroc (as monitor mode)
- Multiple ASICs and multiple boards synchronization
- Channel rate measurements
- Data transmission through USB 3.0

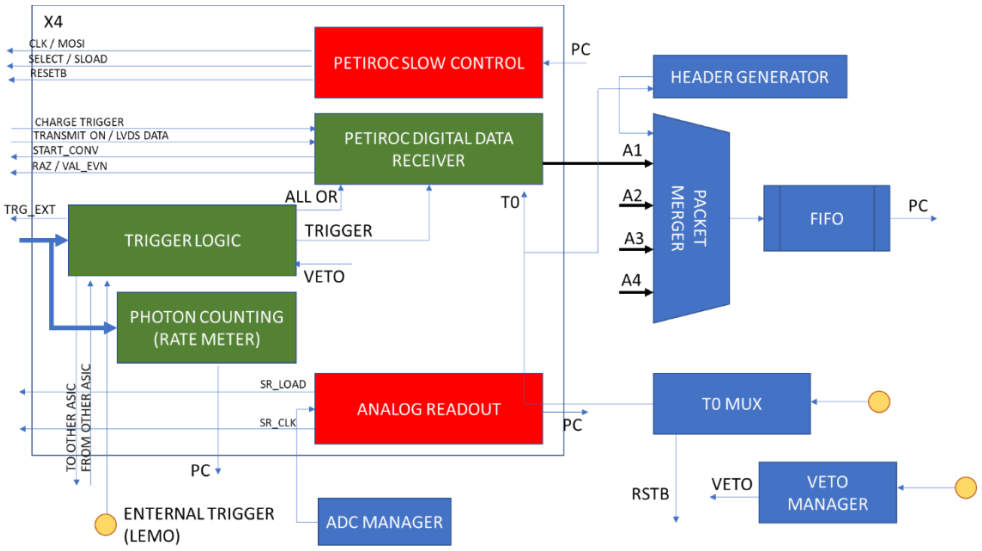


Figure 12.1: scheme of the default firmware loaded on DT5550W for A55PETx management. Refer to PETIROC 2A datasheet [RD1] for the meaning of each line of the ASIC involved in the block diagram.

Data are transmitted in packets coming from each ASIC. Each packet from each ASIC has the following structure:

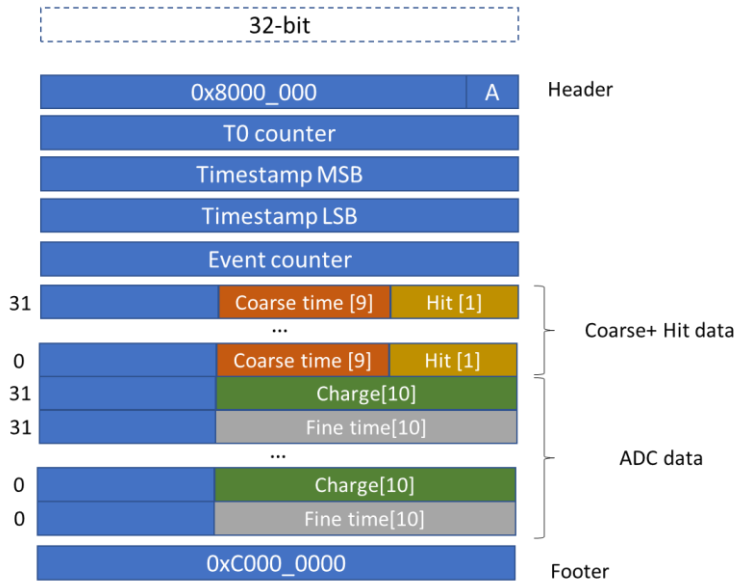


Figure 12.2: structure of the data packet sent to the PC using the default firmware.

- The *header* is used to validate the packet: in absence of the header 0x8000_000, the packet must be discarded. The letter *A* is identifying the ASIC from which the data are coming [A,B,C,D]
- *T0 counter* is the number of T0 cycles
- the *Timestamp* is the time code from the last T0
- *Event counter* is a common counter to all ASICs and indicates the number of packets sent from the beginning of the run
- The body contains data coming from the ASIC, including Charge, Coarse timestamp and Fine timestamp for each channel of the ASIC
- The *footer* is used to validate the packet: in absence of the footer 0xC000_0000, the packet must be discarded.

Note: the firmware is provided as open source VHDL project. The user can modify this firmware or write his own code, with the help of SCI-Compiler. The upgrade of the firmware on DT5550W FPGA, can be performed via SCI-Compiler or through the OpenHardwareProgrammer tool. Refer to **[RD2]** for more details.

13 DT5550W Readout Software

DT5550W Readout Software is a **free and open-source** software developed for **Windows OS** to operate **in conjunction with the default firmware** of the DT5550W, in order to provide a ready-to-use solution. The software is common for all A55xxxx piggyback models.

Note: The software is distributed both as compiled application on the CAEN website and as source code. The source code is available at https://github.com/NuclearInstruments/DT5550W. It is written in VB.NET and C# and it can be easily customized by the user to adapt to a custom firmware and for any other need. In order to recompile the DT5550W Readout Software, a free version of Visual Studio .NET 2015 or later must be installed on the user's PC.

Note: the general functionalities of the software are described in DT5550W User Manual **[RD2]**. In this Chapter we recall them briefly and go into more details with the specific functionalities for A55PETx piggyback

The DT5550W Readout Software allows for:

- Simultaneous readout of up to 4 Petiroc-2A ASICs
- Triggering scheme setting
- Energy measurements
- Time of flight measurements
- Online Cluster reconstruction between multiple ASICs, based on timestamp
- Imaging
- Energy and time spectra plot
- Event list mode readout (energy, time, position)
- Monitor of the analog signals
- High Voltage management
- Data saving in binary and ASCII format

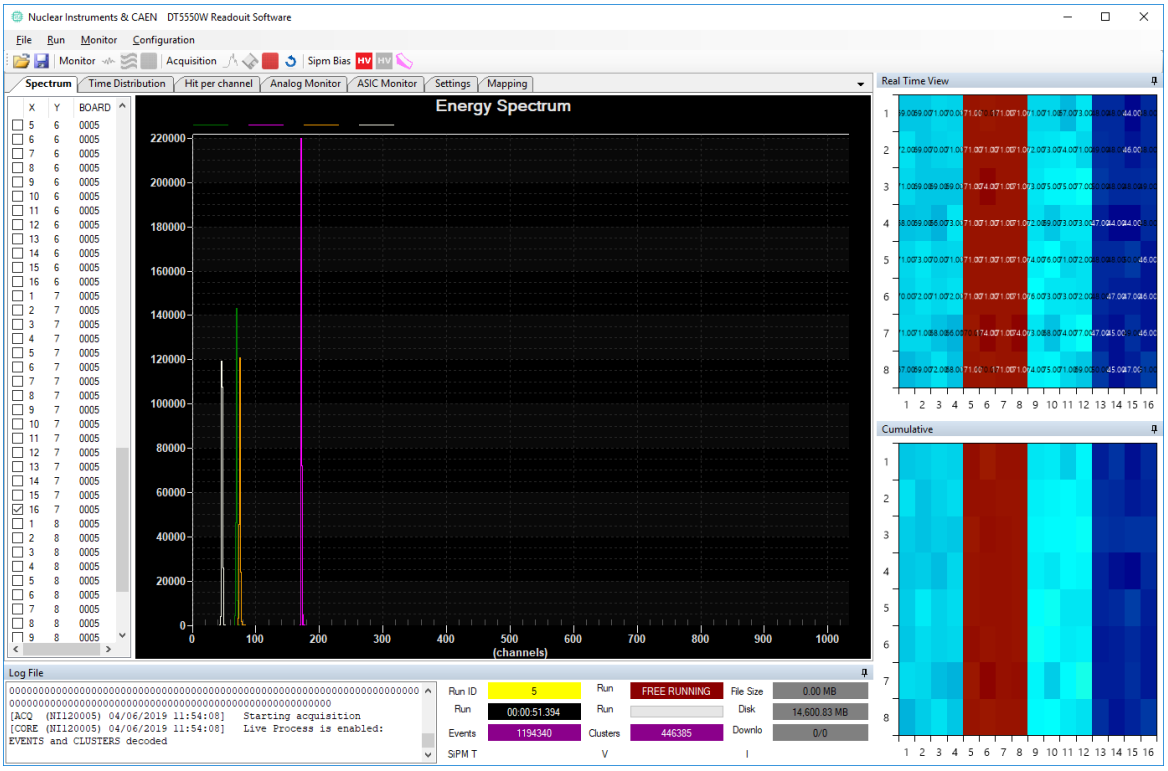


Figure 13.1: general view of the DT5550W Readout Software. In this example, a pedestal acquisition is being performed with A55PET4 board, using two 64-channel SiPM matrix.

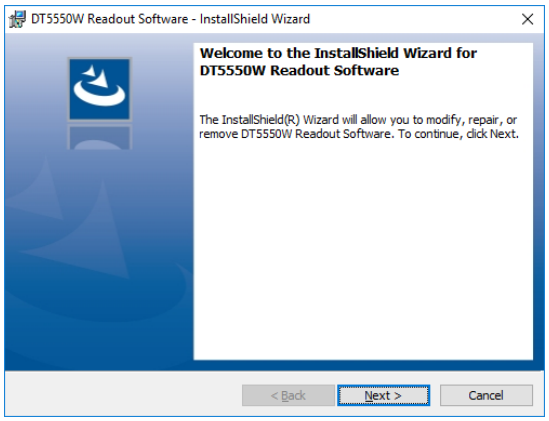
Software installation

DT5550W Readout Software is compliant with Windows 10-64bit

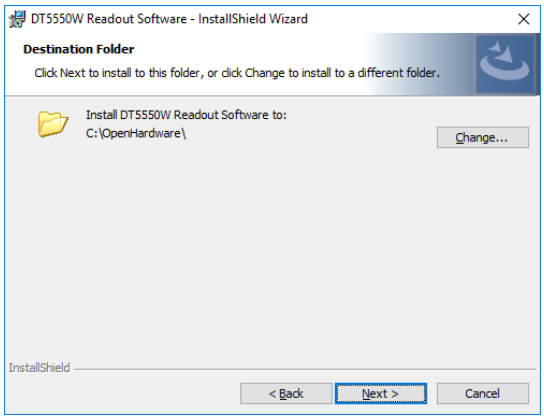
Note: The software is standalone and does not require the prior installation of any library

In order to install the DT5550W Readout Software, follow the steps below:

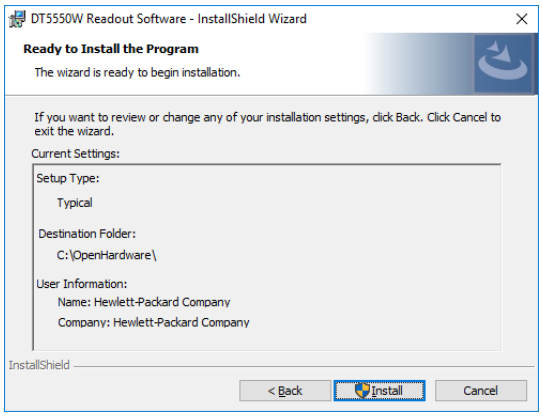
- Download the software package from the DT5550W product page on the CAEN website (**login required**)
- Unzip and run the executable as administrator.
- A setup wizard will start. **Press "Next" to continue.**



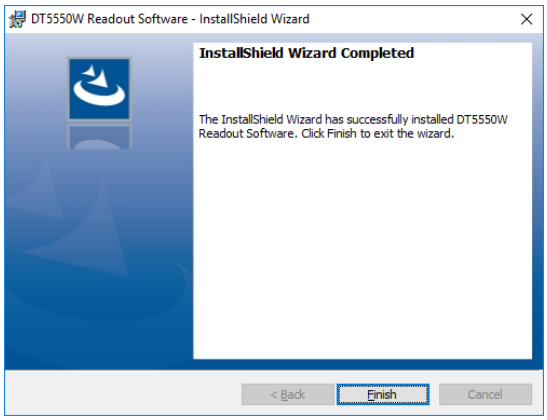
- Choose the destination folder and **press "Next".**



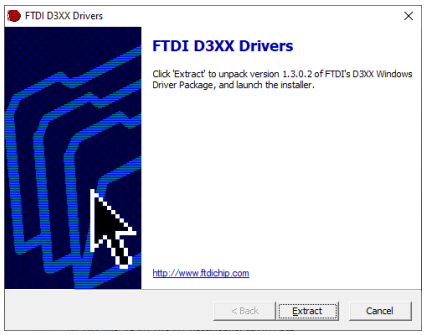
- **Click "Install"** to complete software installation.

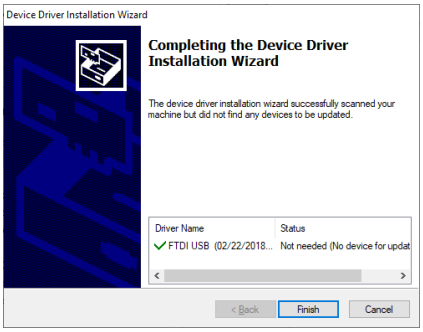


- Wait until installation is completed and press "**Finish**" to complete the setup.



- Follow the instruction to install the FTDI USB drivers





- Now it is possible to launch the DT5550W Readout software from the Windows programs menu.

Board Connection

After launching the software, the “Connection” window will open, and the user is asked to connect a board specifying the connection parameters:

- *Device*: select the PID/Serial Number of the DT5550W to be connected
- *ASIC model*: select Citiroc. In *Auto* mode, the software automatically detects the ASIC type
- *ASIC count:* specify the number of ASICs on your A55PETx. In *Auto* mode, the software automatically detects the number of ASICs mounted on the piggyback board.

Note: the software does not support connection to multiple boards: multiple instances of the software must be opened to manage acquisitions on each board.

Press *Connect* to establish a connection with the specified parameters and *Refresh* to update the list of devices listed in the Combo box.

Figure 13.2: the "Connection" window at start-up of the DT5550W Readout Software

Software GUI Description

Menu and Control Toolbar

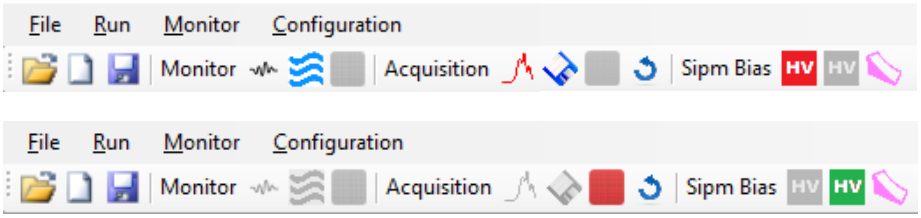


Figure 13.3: the Menu and Control Toolbar of the DT5550W Readout Software, before (top) and during (bottom) acquisition.

The *Menu and Control Toolbar* contains the following buttons:

- Open: open a configuration file
- Save: save a configuration file

Monitor (Oscilloscope acquisition configuration)

- Single Shot: acquire a single waveform in the oscilloscope
- Wave: start continuous acquisition of waveforms on the oscilloscope
- Stop: stop the oscilloscope acquisition

Acquisition

- *Spectrum*: start acquisition according to the ASIC settings (no data saving)
- Save: start energy/time or photon counting acquisition according to the ASIC settings and dump data on file.
- Stop: stop current acquisition
- Reset: reset the online spectra

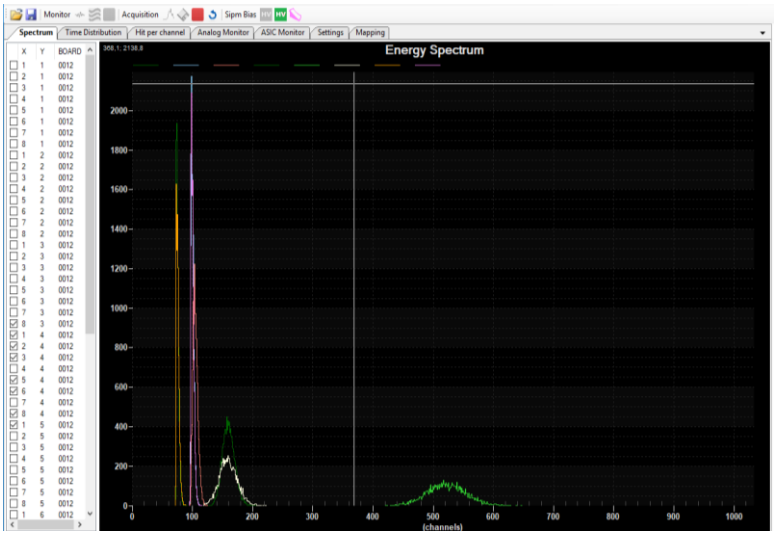
SiPM Bias

- Turns ON/OFF the SiPM Power Supply. The Voltage is selected in the *Settings* tab. It is not possible to change the Voltage status during acquisition.
- *Ramp icon*: open the channel counts monitor

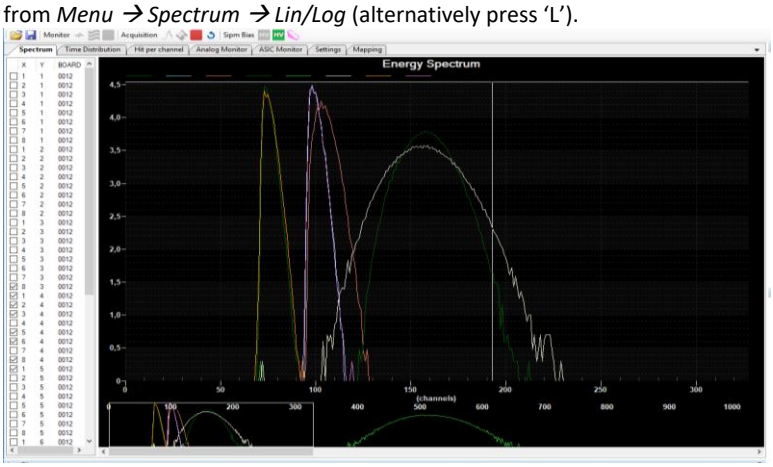
Main plots

The main working area hosts all the tabs related to the ASICs settings, configuration of the acquisition and online plots (spectra, oscilloscope, …). The main available plots are:

- ***Energy*** shows the energy spectrum for each board channel. The spectrum of multiple channels can be displayed on the same plot, by checking the relative checkboxes in the channels list on the left of the tab. The channels are listed as element of a matrix (X-Y coordinates) reproducing the detector shape. Also the sum spectrum, realized summing all energy values of all channels. It is possible to set a scaling factor in the *Settings* for this spectrum.

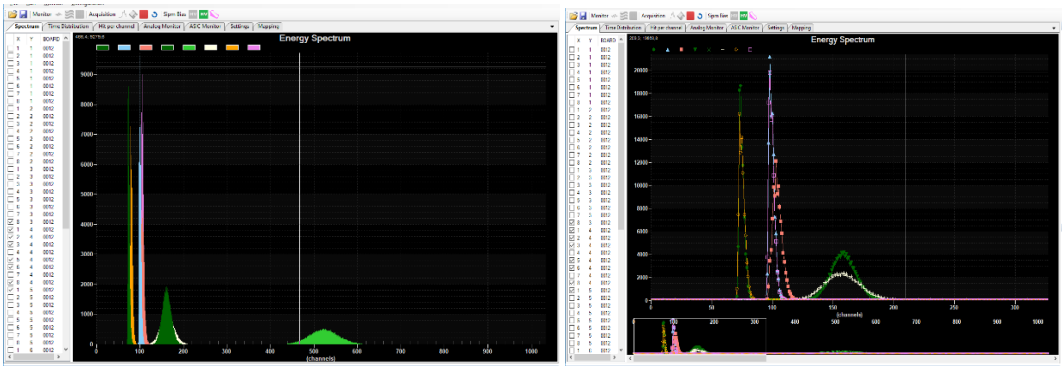


It is possible to zoom in the spectrum with keyboard command and then the mouse to drag on the interested area: rectangular zoom (press 'Z'), horizontal zoom (press 'H'), vertical zoom (press 'V'), unzoom (press 'U'). The spectrum can be displayed in bot linear and semi-log scale. It is possible to switch between the two modes from *Menu* → *Spectrum* → *Lin/Log* (alternatively press 'L').

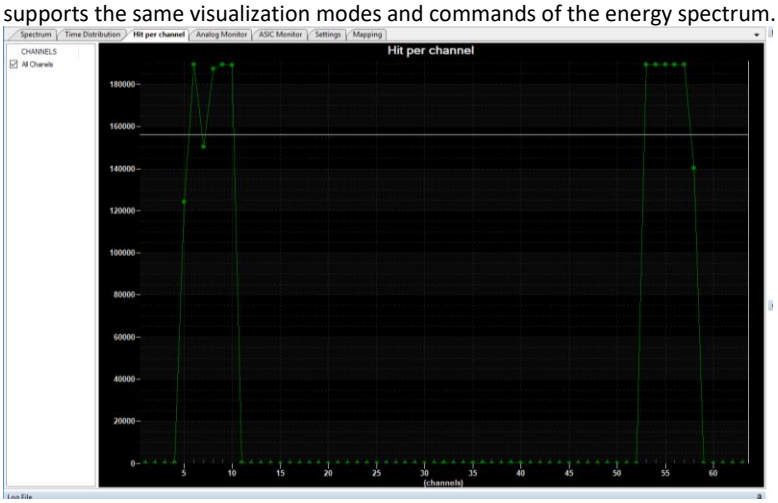


It is also possible to change the plot type: press 'O' to cycle between plot modes. Available plot modes are:

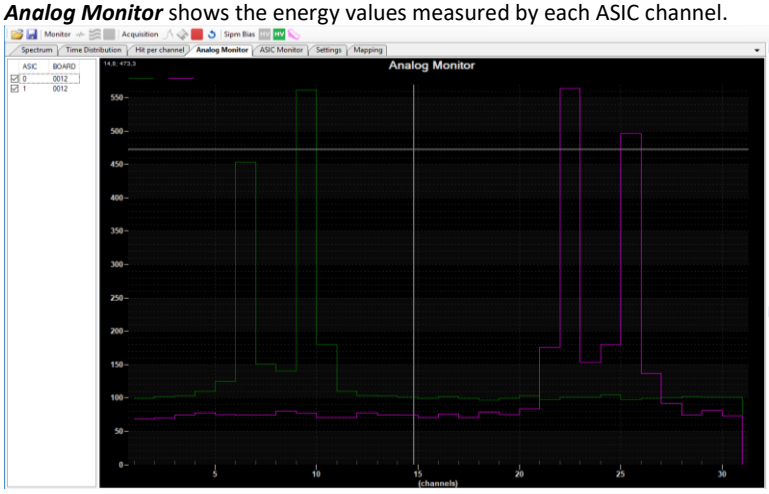
- Step
- Line
- Line with interpolation
- Bar
- Area
- Area with interpolation
- Dot
- Dot with Line
- Dot with interpolation

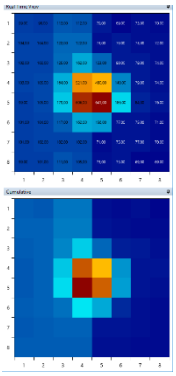


- ***Hit per channel,*** to visualize the number of triggers detected on each channel from the acquisition start. It supports the same visualization modes and commands of the energy spectrum.



- ***Analog Monitor*** shows the energy values measured by each ASIC channel.





- In the ***Imaging*** area, the results of energy acquisition are shown as real-time and cumulative image. The real-time image shows the energy acquired on each channel event by event, while the cumulative image shows the sum of the energy channel by channel, acquired during the entire run. It is possible to ZOOM in the image using the mouse wheel. Press 'a' on the keyboard to perform a zoom to fit.

The ASIC Monitor Tab

For A55PETx piggyback, the *ASIC Monitor* Tab shows on oscilloscope the *charge_mux* output signal of the selected ASIC, i.e. the charge multiplexed analog output. The signal is synchronous to the following ASIC signals (refer to **[RD1]** for more details), shown in the plot:

- Digital Probe
- Time Trigger
- Analog Readout Clock
- Data In (srin_read)
- LEMO Trigger
- Global Trigger
- Charge trigger multiplexed output

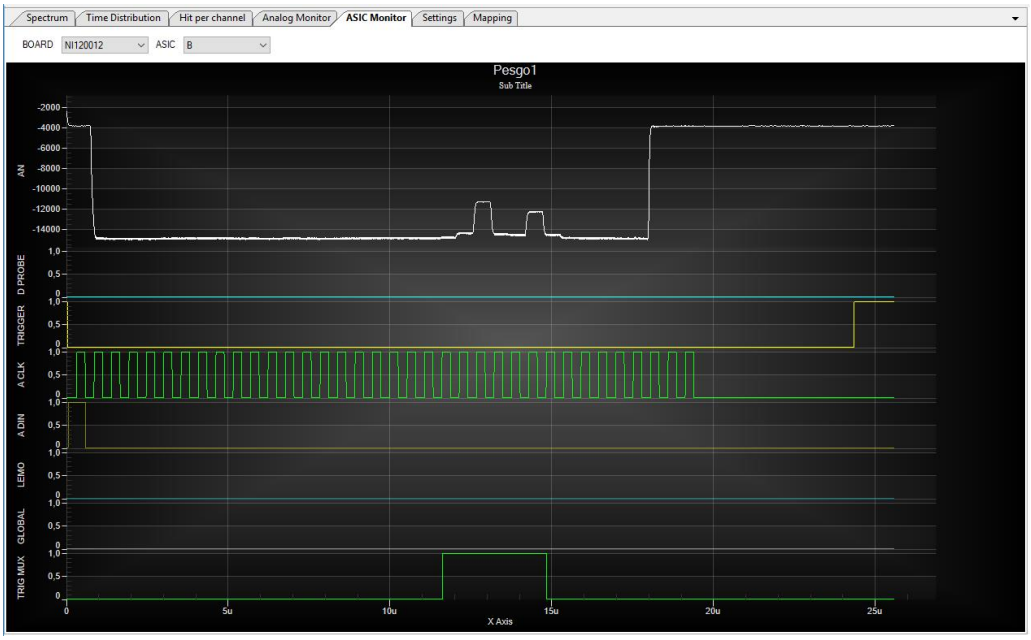


Figure 13.4: the *ASIC Monitor* Tab for A55PETx Piggyback. The white plot shows the charge multiplexed output.

The Settings Tab

The *Settings* Tab allows to configure the ASICs and the acquisition parameters.
It is divided in two areas:

- the top area contains the global settings, common to all ASICs, and the DAQ parameters
- the bottom area contains the settings relative to a specific ASIC or channel

The *Apply Settings* button allows to effectively apply the given settings. No parameters can be changed during acquisition.

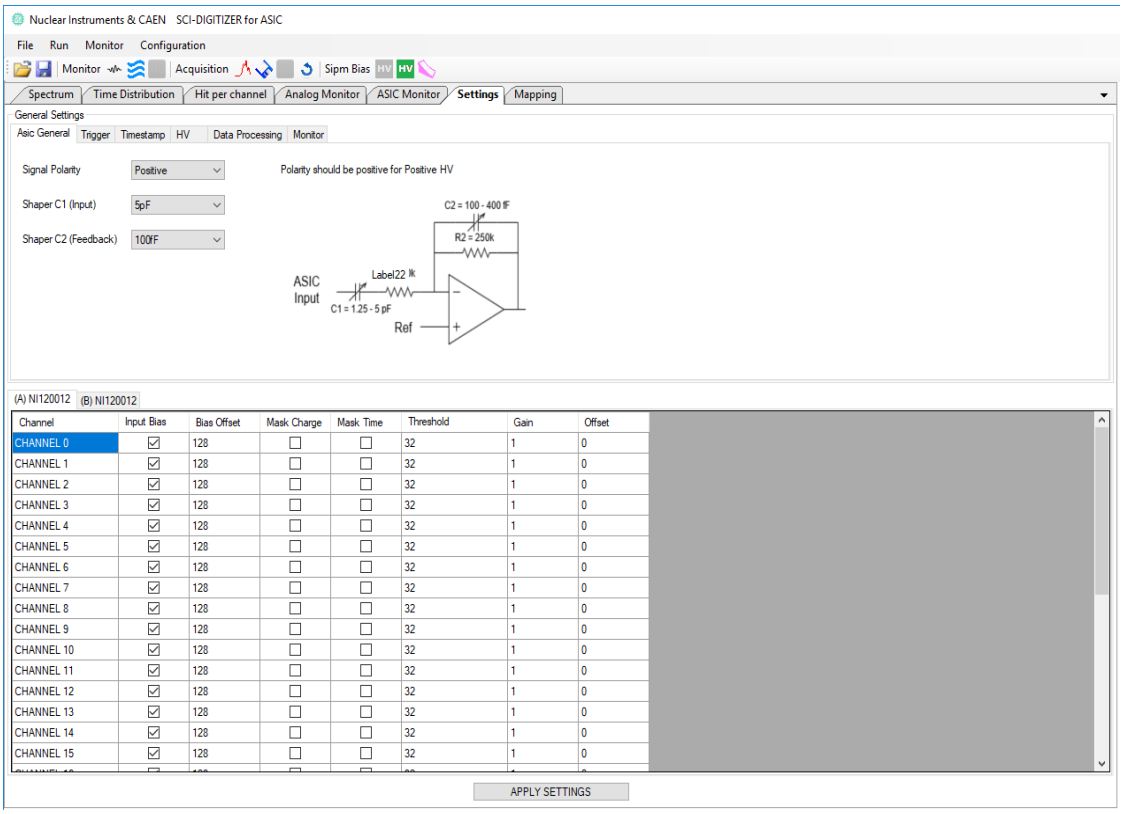


Figure 13.5: the *Settings* tab for A55PETx piggyback. The top and bottom area are clearly visible. The top area has different tabs for general configuration and the bottom area has a tab for each ASIC.

The *top area* is divided in different subtabs:

- ***Asic General***, which allows to configure the ASIC analog input stage
- ***Trigger,*** for ASIC and board trigger management
- ***Timestamp,*** for online time data processing management
- ***HV,*** to set parameters for A7585D soldered on the board
- ***Data Processing,*** for data processing management
- ***Monitor,*** to set parameters related to the analog readout and probe signals

The *bottom area* has a tab for each ASIC hosted on the board. Each tab can be used to set the specific settings of each channel, like the offset for fine bias regulation and the trigger threshold.

Asic General

This tab contains the settings for the configuration of the analog input stage of the ASIC.

- ***Signal Polarity*** defines the signal polarity (positive/negative) of the input signal. With positive bias voltage (as given by A7585D onboard) the user must use positive polarity.
- ***Shaper C1/C2*** define the feedback capacitance for the charge shaper, so setting the shaping time. Refer to [RD1] for more details.

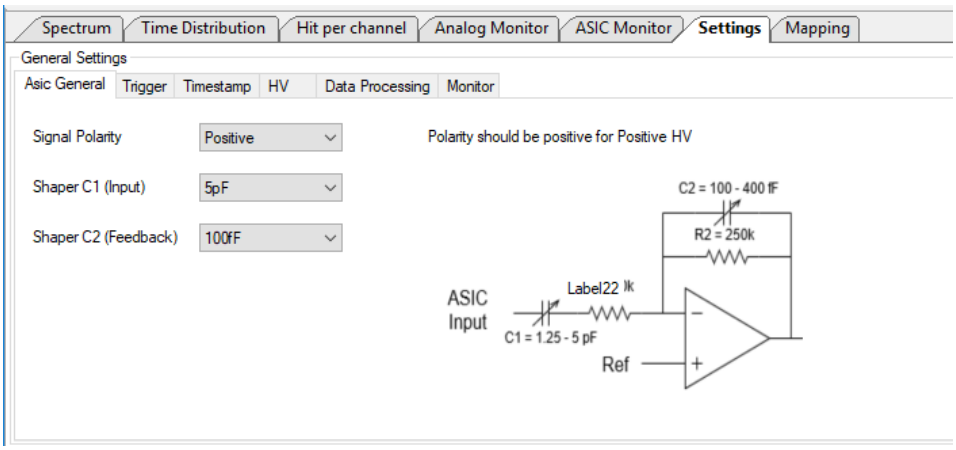


Figure 13.6: the *Asic General* subtab of the *Settings* tab.

Trigger

This tab contains the settings for the configuration of ASIC and board trigger.

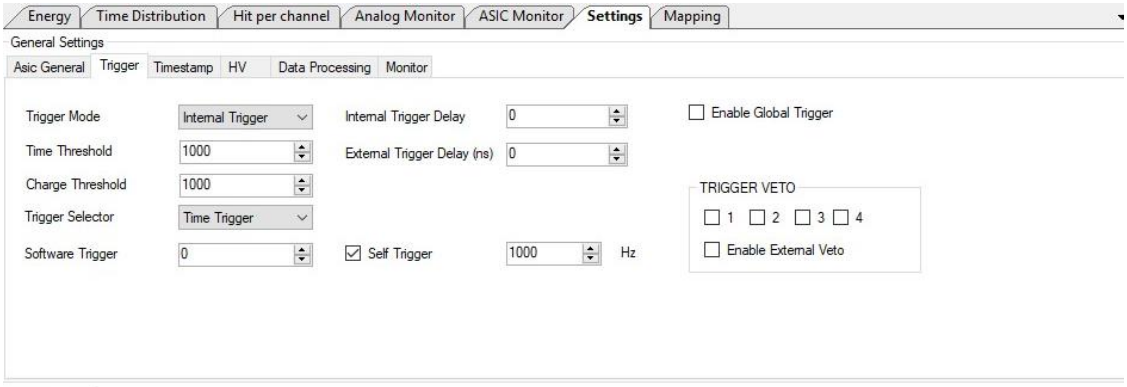


Figure 13.7: the *Trigger* subtab of the *Settings* tab.

- ***Trigger Mode*** sets the triggering source to Internal, Int/Ext (OR of the two triggers), External. External trigger signal is a TTL to be fed to LEMO 5 (if using the default firmware).
- ***Time Threshold*** sets the threshold for the time trigger. The value is set in LSB and the correspondent value in photoelectrons varies from ASIC to ASIC. With a Hamamatsu matrix S13361-3050AE-08 and bias voltage 54 V, Time Threshold = 900 results in zero counts in dark environment.
- ***Charge Threshold*** sets the threshold for the charge trigger.
- ***Trigger Selector*** can be used to select between time and charge trigger. The charge trigger cannot be used in conjunction with software trigger or global trigger.
- ***Software Trigger*** sets the threshold for zero suppression.
- ***Self-Trigger*** allows to enable the software trigger and set the triggering rate.
- ***Internal Trigger Delay*** sets the delay used by the ASIC to sample the shaped signal peak.
- ***External Trigger Delay*** sets the delay applied on the external trigger to sample the shaped signal peak.
- ***Trigger Veto*** enables/disables on or more ASICs (named as 1,2,3,4) and allows to use an external veto (on LEMO 4 for the default firmware) .
- ***Enable Global Trigger*** allows to propagate the trigger signal among different ASICs, to capture all board channels even when only an ASIC is triggering. The effect of the global trigger is shown below.

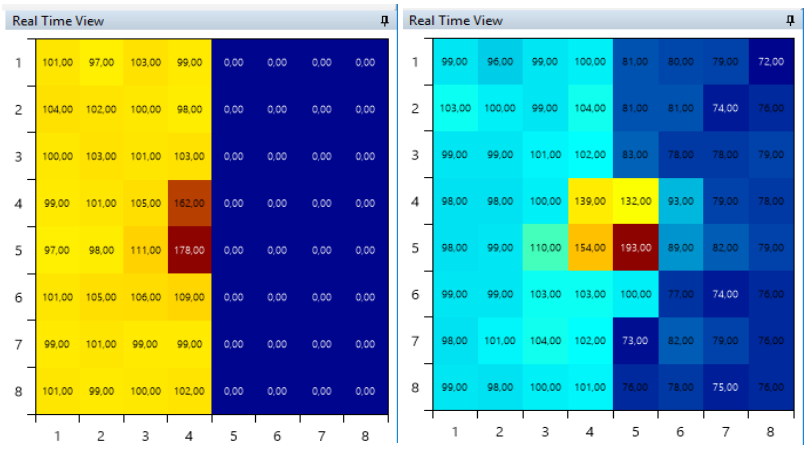


Figure 13.8: the effect of the global trigger on imaging acquisition. On the left, with the global trigger disabled and a more intense light on ASIC A, this latter is triggering while ASIC B is not triggering. On the right, the global trigger is enabled and both ASICs are acquiring.

Timestamp

This tab allows to manage the time data online processing.

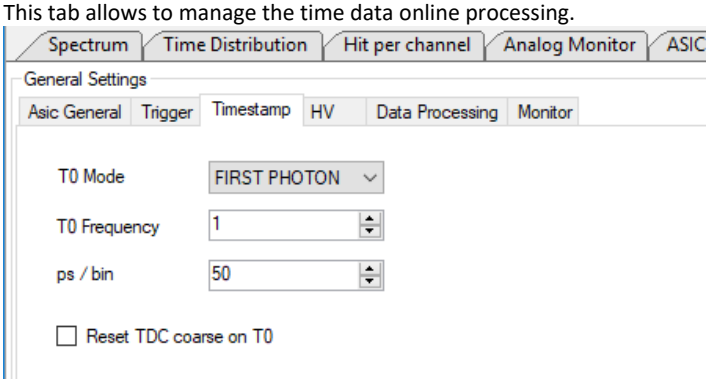


Figure 13.9: the *Timestamp* subtab of the *Settings* tab.

- ***T0 mode*** allows to manage the reference for time measurements. The possible options are:
  - FIRST PHOTON: T0 is given by the first triggering channel of the board
  - FIRST PHOTON ASIC: T0 is different for each ASIC and is given by the first triggering channel on that ASIC
  - RUN START: T0 is given at the beginning of the run
  - INTERNAL-PERIODIC: T0 is generated by the software with the frequency specified in *T0 Frequency*
  - EXTERNAL-LEMO6: T0 is given by an external signal (on LEMO 6 for the default firmware)
  - SOFTWARE: T0 is generated by the software with the frequency specified in *T0 Frequency*
- ***T0 Frequency*** sets the frequency of the software T0, if used.
- ***ps/bin*** sets the converting factor for the time axis of the *Time Distribution* spectrum.
- ***Reset TDC coarse on T0****:* when using external T0, allows to reset on T0 signal, not only the internal timestamp counter, but also the coarse counter of the ASIC TDC.

High Voltage (HV)

This tab allows to adjust the parameters of the A7585D module, mounted on the A55PETx board. The module can supply a voltage between 20 and 85 V with maximum current of 10 mA.

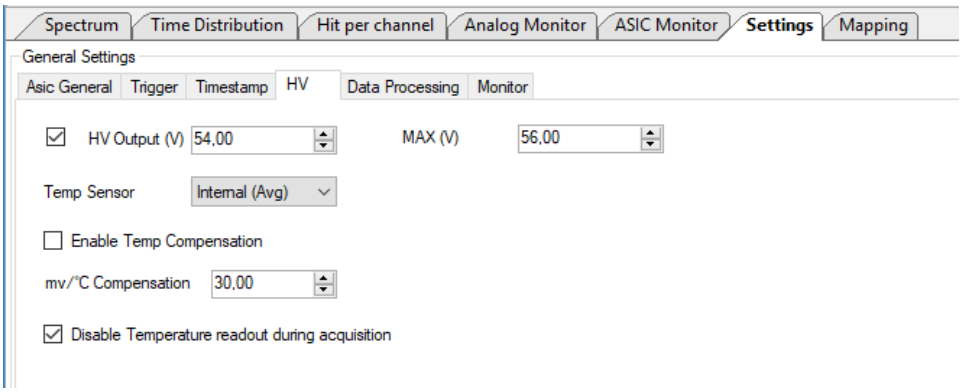


Figure 13.10: the *HV* subtab of the *Settings* tab.

- ***HV Output (V)*** allows to set the voltage value and enable the power supply, by checking the checkbox. When enabling temperature compensation, this is considered the voltage at 25° C.
- ***MAX (V)*** allows to limit the output voltage at the set value (protection against failure or error)
- ***Temp Sensor*** allows to choose the temperature sensor on which the temperature compensation is based. It is possible to choose the average of the two onboard sensors (Internal) or an external sensor.
- ***Enable Temp Compensation****:* if checked, the A7585D output voltage is adjusted depending on the measured temperature. It is needed to specify the *mV/°C compensation* factor.
- ***Disable Temperature readout during acquisition****:* if checked, the temperature sensors are not read out. This is useful since the application of temperature compensation could require 10 ms every 5 s, being the board unable to transmit data during this interval. If the rate is very high the board could enter in busy state. With this option the temperature is read out only with the board not acquiring, to avoid as much as possible the busy state.

Data Processing

This tab allows to set the parameters for the software data processing.

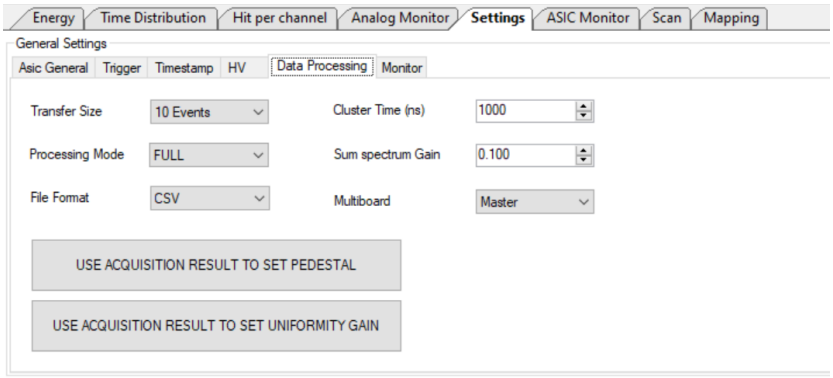


Figure 13.11: the *Data Processing* subtab of the *Settings* tab.

- ***Transfer Size*** is used to set the number of events to be included in each data transmission. The plot on the software are updated at each transmission, therefore the transfer size should be minimal to obtain a nearly real-time update of the plots. On the other hand, small transmissions packets do not exploit efficiently the USB3.0 bandwidth and are suggested only in case of low rate.
- ***Processing Mode*** is used to select the data processing:
  - FULL: events coming from different ASICs are considered correlated a reconstructed in a single cluster.
  - DECODE EVENTS: events coming from different ASICs are considered uncorrelated. Only the cluster of events on the channels of the same ASIC are reconstructed.
  - NONE: no online processing is done. The data must be saved in binary format and processed offline.
- ***Cluster Time***: maximum time distance between two events in order that they can be considered in the same cluster
- ***Sum Spectrum Gain*** sets the multiplying factor to be applied to the energy sum spectrum shown in the Spectrum tab.
- ***File Format*** allows to choose the file format saved by the software:
  - *CSV:* data are decodified as CSV standard and saved in .data format

- *BINARY:* data are not decodified and saved in binary format. The data are the binary which comes along the USB 3.0 bus. The user must implement a script to decode the data, but the raw data saving requires less space on disk.

- ***Multiboard*** can be used when synchronizing multiple boards to decide if the one correspondent to the current software instance is *Master* or *Slave*. It is possible to open a software instance for each board. A script to readout all boards at once is available in the installation folder under the name MultiboardDAQDT5550W_PETIROC.exe
- ***Use Acquisition Result to set Pedestal***: this button allows the user to easily perform the pedestal calculation (refer to **How to perform pedestal calculation**)
- ***Use Acquisition Result to set Uniformity Gain***: this button automatically performs the regulation of the channels gain to uniform the response of sensor's pixels (refer to **How to set uniformity gain**)

Monitor

This tab allows to set the parameters related to the analog readout and probe signals. The settings in this tab can be changed without reprogramming the entire ASIC pressing the general *Apply Settings* button. It is sufficient to press the *Set* button available in this tab.

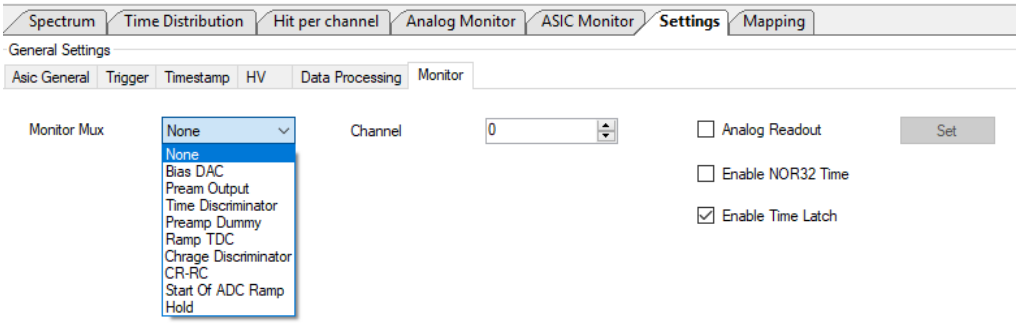


Figure 13.12: the *Monitor* subtab of the *Settings* tab.

- ***Monitor Mux*** selects which ASIC internal signal to be sent on the Analog/Digital Probe pin (see **Test Pins**)
- ***Channel*** selects the ASIC channel for which the signal specified in *Monitor Mux* is shown
- ***Analog Readout*** enables the analog readout mode. If enabled, this option corrupts data coming from the digital readout.
- ***Enable NOR32 Time*** enables the NOR32 trigger output of the ASIC. This option introduces noise in the ASIC itself.
- ***Enable Time Latch*** enables the time trigger latching for charge measurements. If not latched, the charge trigger cannot work correctly.

Channel specific settings

The bottom area of the *Settings Tab* contains a table to set the ASIC channels specific parameters. Each tab of this area is related to an ASIC hosted on the board and can be used to set parameters like the offset for fine bias regulation and the trigger threshold.

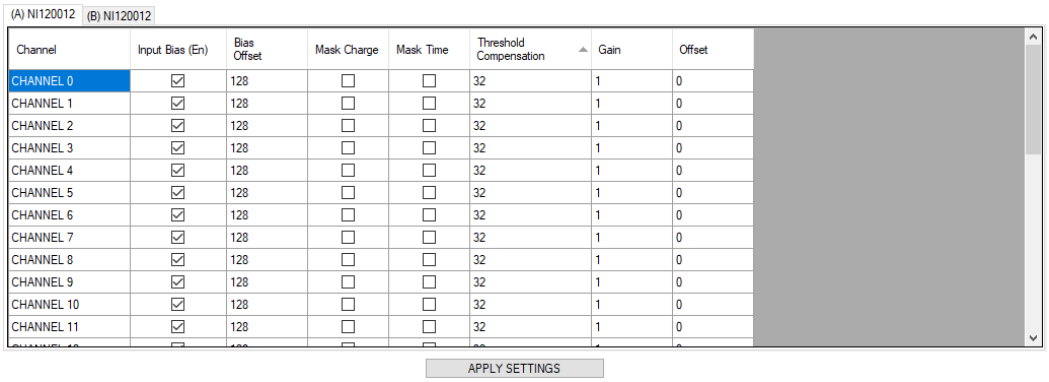


Figure 13.13: the bottom area of the *Settings* tab, containing the table for ASIC channels specific settings. In this case two ASICs (called A and B) are hosted on the board (NI120012).

The parameters configurable from the channel specific settings tabs are:

- *Input Bias*, to enable/disable the ASIC's channel input DAC for fine bias regulation

- *Bias Offset,* to set the 8-bit input DAC value for fine bias regulation. In case of a positive bias given by A7585D module, an higher offset results in a lower bias voltage. The bias can be adjusted in the range ±1 V. The value 128 corresponds to a zero offset and so the bias is not adjusted.
- *Mask Charge,* to disable the charge trigger of the specific channel
- *Mask Time,* to disable the time trigger of the specific channel
- *Threshold Compensation,* to set the individual channel time trigger threshold adjustment. The values of this threshold and the general time threshold are not linearly correlated.
- *Gain,* to set the energy gain
- *Offset,* to set the pedestal value

How to perform an acquisition

Before starting an acquisition, the user should set all the relevant parameters in the *Settings* tab.
The acquisition is started pressing the correspondent button in the *Menu and Control Toolbar (Acquisition section)*. The Spectrum icon starts an acquisition without data saving, while the Floppy Disk icon starts an acquisition with data saving in the specified file format.
After pressing the Floppy Disk icon, the *Start Run* window automatically opens. In this menu it is possible to specify the data saving folder and compile the logbook, with the relevant acquisition parameters, the date and other annotations. It is also possible to set the Target mode for the acquisition: in *Free running* the acquisition must be stop manually, in *Run Time* the user must specify a target time at which the acquisition is stopped, in *Cluster Number* the user must specify the target number of events in a cluster (this latter is available only in *Processing Mode* = FULL).

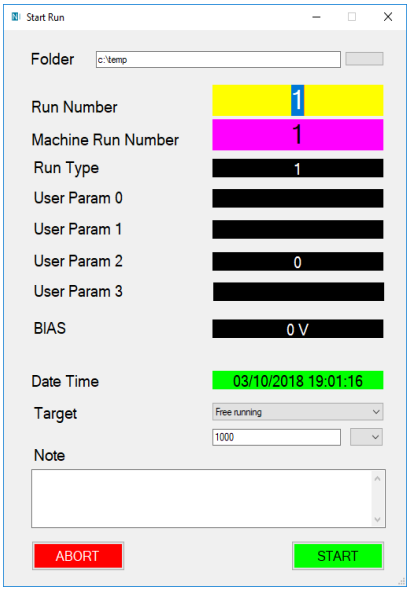


Figure 13.14: the *Start Run* window which opens after the acquisition with data saving is started.

After setting the fields in the *Start Run* window, press 'Start' to effectively start the board acquisition with specified parameters, press 'Abort' to return to the main software window.

After the acquisition is started, the user can visualize on plots the results of the acquisition, using the tabs described in **[RD2]**.

Data Saving Format

For each run, two files with the same name and different format are saved:

- a .JSON file, which contains the run information and the entire ASIC configuration. It can be easily decodified via a json parser (available in all modern programming languages) or via strings elaboration.

- a .data or binary file containing the data, depending on the format chosen in the *Data Processing* tab.

The binary file is a direct dump of the data transmitted on USB3.0 bus, without any elaboration. For PETIROC, the packet is made of 1216 bits per event. It is possible to write a function, for example in C language, to decode the binary data (see **Appendix**)

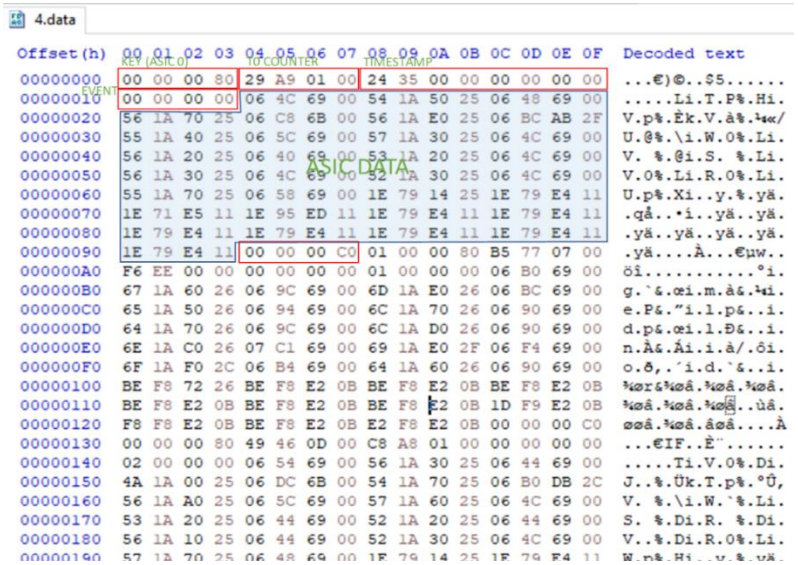


Figure 13.15: data saved in binary format for A55PETx board

The .data file is a textual CSV format. Each line represents an event and each column a decodified field (timestamp, hits, energy, time, ….). Column are separated by ; separator.
The data format is different depending on the Processing Mode. In decoded events mode, each line contains only the data relative to one ASIC; multiple ASIC on the board are processed and saved as completely independent. In full processing mode, the software reconstructs clusters using the event timecode as reference to merge multiple events.

With *Processing Mode* = DECODE EVENTS, the structure of the data file is as follows (the fields are placed in columns in the file and a first header row explains the column field):

Field	Size (Columns)	Description
ID	1	Progressive number (increment by 1 for each row by the software)
ASIC	1	ID of the ASIC on the board (0,1, 2 …)
EventCounter	1	Progressive number in hardware for each acquisition (acquisition=trigger that can be enqueued in the output FIFO)
RUN_EventTimeCodeLSB	1	Timecode of the event from the start of the acquisition in clock cycles
RUN_EventTimecode_ns	1	Timecode of the event from the start of the acquisition in clock ns
T0_to_Event_Timecode	1	Timecode of the event from the last T0 in clock cycles
T0_to_Event_Timecode_ns	1	Timecode of the event from the last T0 in ns
HIT	32	1/0 vector containing the ASIC hit flag for each channel
CHARGE	32	integer vector containing the ASIC decoded charge information for each channel
COARSE	32	integer vector containing the ASIC time coarse counter information for each channel
FINE	32	integer vector containing the ASIC time fine counter information for each channel

Table 13.1: saved data format in *Processing Mode* = DECODE EVENTS

With *Processing Mode* = FULL, the size of the packet (each row) depends on how many ASICs are merged in a cluster. For example, if an events interact with just one part of the sensor and only one of four ASIC triggers the cluster will contain information relative to just one ASIC and the number of columns will be less than the maximum .The structure of the .csv file is as follows (the fields are placed in columns in the file and a first header row explains the column field):

Field	Size (Columns)	Description
ID_CLUSTER	1	Progressive number (increment by 1 for each row by the software)

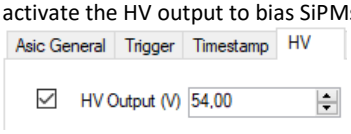
CLUSTER_RUN_Timecode_ns	1	Timecode of the cluster from the start of the acquisition in clock ns (the timecode of the cluster is the timecode of the first event of the cluster)
CLUSTER_Timecode_ns	1	Timecode of the event from the last T0 in ns (the timecode of the cluster is the timecode of the first event of the cluster)
NEventsInCluster	1	Number of events (ASICs) present in the cluster
THE FOLLOWING PART IS REPEATED FOR EACH EVENT IN THE CLUSTER		
RUN_EventTimeCodeLSB	1	Timecode of the event from the start of the acquisition in clock cycles
RUN_EventTimecode_ns	1	Timecode of the event from the start of the acquisition in clock ns
T0_to_Event_Timecode	1	Timecode of the event from the last T0 in clock cycles
T0_to_Event_Timecode_ns	1	Timecode of the event from the last T0 in ns
HIT	32	1/0 vector containing the ASIC hit flag for each channel
CHARGE	32	integer vector containing the ASIC decoded charge information for each channel
COARSE	32	integer vector containing the ASIC time coarse counter information for each channel
FINE	32	integer vector containing the ASIC time fine counter information for each channel

Table 13.2: saved data format in *Processing Mode* = FULL

How to perform pedestal calculation

The DT5550W Readout Software allows to easily manage the pedestal calculation automatically.
In order to exploit this functionality, the user should :

- remove any light source from the sensors
- activate the HV output to bias SiPMs



- enable the Software Trigger at 1 kHz frequency

At this point, the user can reset the plots view, start the acquisition and acquire for nearly 10 seconds. The acquired image will be extremely non-uniform, with great differences of energy detected by different channels, as shown in **Figure 13.16.**
At this point the user can:

- stop the acquisition
- press the '*Use Acquisition Result to set Pedestal*' button in the *Data Processing* tab and the software will automatically adjust the *Offset* of each channel to uniform at best the pedestal
- press 'Apply Settings'
- start again the acquisition

The result after pedestal calculation is shown in **Figure 13.16,** where the image on the right is detecting, in absence of light, much more uniform energies with respect to the image on the left.

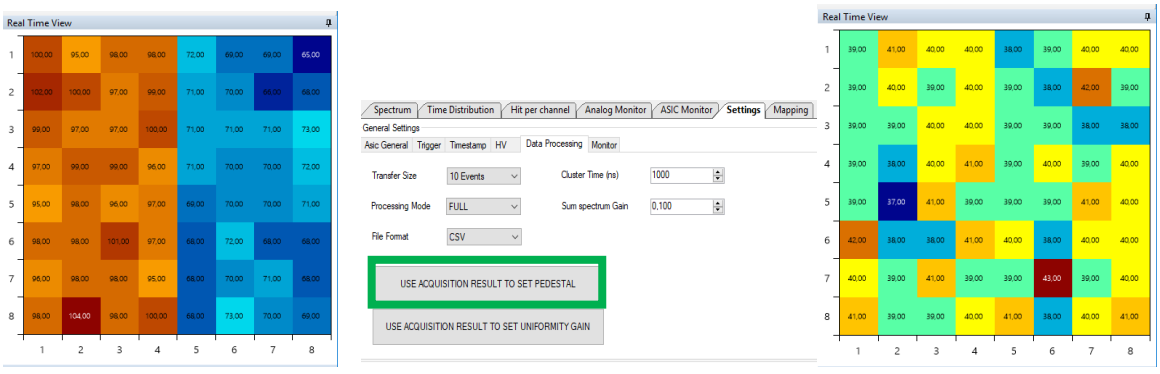
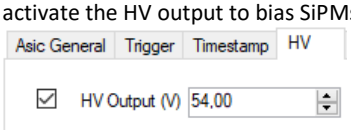


Figure 13.16: an image of a 64-channel SiPM matrix acquired before (left) and after (right) the pedestal calculation.

How to set uniformity gain

The DT5550W Readout Software allows to easily manage the channels gain regulation automatically.
In order to exploit this functionality, the user should :

- illuminate the SiPM with pulsed light in the more uniform possible way, so that each pixel receive the same amount of light
- activate the HV output to bias SiPMs



- operate with the internal ASIC trigger

At this point, the user can reset the plots view, start the acquisition and acquire the time needed to collect a sufficient amount of data.
At this point the user can

- stop the acquisition
- press the '*Use Acquisition Result to set Uniformity Gain*' button in the *Data Processing* tab and the software will automatically adjust the *Gain* coefficient of each channel to uniform at best the energies detected by the matrix pixels
- press 'Apply Settings'
- reset real-time results
- start again the acquisition

In **Figure 13.17,** the results of gain and pedestal compensation are shown, taking as example a 64-channel matrix.

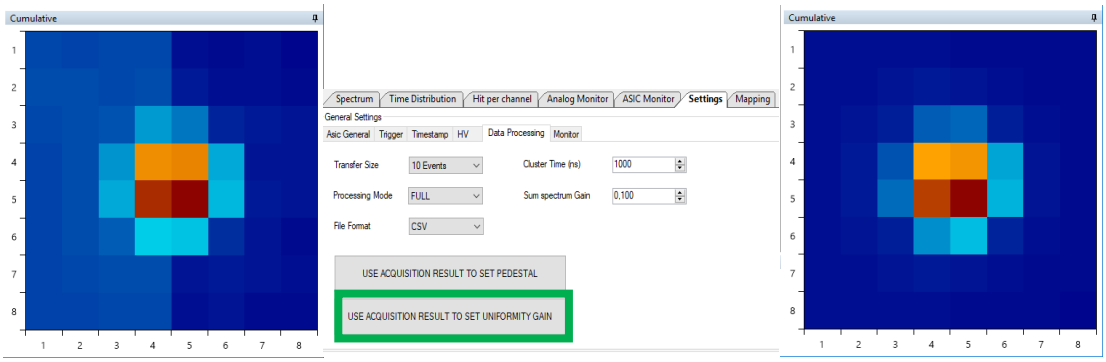


Figure 13.17: the results of pedestal calculation and gain regulation. The image on the right (after compensation of offset and gain) has a more uniform background (deep blue pixels) and small energy differences in neighbouring pixels with respect to the image on the left.

14 Appendix

C function to decode binary data coming from A55PETx board

```
public int DecodePetirocRowEvents(ref UInt32[] bufferA, UInt32 valid_wordA, ref Queue<t_DataPETIROC>
pC, int ThresholdSoftware, int Polarity)
        {
            int DecodedPackets = 0;
            double Time=0;
            double minTime=0;
            UInt32 i, j, t, s;
            uint[] datarow = new uint[97];

            t_DataPETIROC DataPETIROCA = null;
            t = 0;
            s = 0;
            while (t < valid_wordA)
            {
                switch (s)
                {
                    case 0:
                        if (((bufferA[t] >> 4) & 0xc000000) == 0x8000000)
                        {
                            s = 1;
                            DataPETIROCA = new t_DataPETIROC();
                            DataPETIROCA.AsicID = (UInt16) (bufferA[t] & 0xF);
                            DataPETIROCA.EventTimecode = ((UInt64)bufferA[t +
                                      1]);
                            DataPETIROCA.RunEventTimecode = (((UInt64)bufferA[t
                                       + 2]) ) + (((UInt64)bufferA[t + 3]) << 32);
                            DataPETIROCA.EventCounter = ((UInt64)bufferA[t + 4]);

                            DataPETIROCA.EventTimecode_ns =
                                      DataPETIROCA.EventTimecode * 25;
                            DataPETIROCA.RunEventTimecode_ns =
                                      DataPETIROCA.RunEventTimecode * 25;

                            t = t + 5;
                            minTime = 100000000000000;
                        }
                        else
                            t++;
                        break;

                    case 1:
                        for (i = 0; i < 32; i++)
                        {

                            datarow[i * 3 + 2] = (bufferA[t] >> 0) & 0x3FF;
                            datarow[i * 3 + 1] = (bufferA[t] >> 10) & 0x3FF;
                            datarow[i * 3 + 0] = (bufferA[t] >> 20) & 0x3FF;
                            t++;
                        }
                        for (i = 0; i < 32; i++)
                        {
                            DataPETIROCA.hit[i] = (bool)((datarow[64 + i] & 0x1)
                                                == 1 ? true : false);
```

```
                        DataPETIROCA.FineTime[i] =
                                  (ushort)gray_to_bin(datarow[(i * 2) + 0], 10);
                        int data = (int)gray_to_bin(datarow[(i * 2) + 1], 10);
                        if (Polarity==0)
                            data = 1024 - data;


                        if (data > ThresholdSoftware)
                         DataPETIROCA.charge[i] = (ushort)data;
                        else
                            DataPETIROCA.charge[i] = 0;

                           DataPETIROCA.CoarseTime[i] =
                                   (ushort)gray_to_bin(datarow[64 + i] >> 1, 9);

                        Time = (((double)DataPETIROCA.CoarseTime[i] + 1) *
                                  25) - (((double)(DataPETIROCA.FineTime[i])) *
                                               .037);
                        if (DataPETIROCA.hit[i])
                            minTime = Time < minTime ? Time : minTime;
                        DataPETIROCA.relative_time[i] = Time;
                        DataPETIROCA.Time[i] = Time;
                    }
                    s = 2;
                    break;

                case 2:
                    if ((bufferA[t] & 0xc0000000) == 0xc0000000)
                    {
                        if (minTime == 100000000000000) minTime = 0;
                        for (i = 0; i < 32; i++)
                        {
                            DataPETIROCA.relative_time[i] -= minTime;
                        }

                        pC.Enqueue(DataPETIROCA);
                        DecodedPackets++;
                    }
                    t++;
                    s = 0;
                    break;
            }
        }
            return DecodedPackets;
    }


public class t_DataPETIROC
    {
        public UInt64 EventTimecode;
        public UInt64 RunEventTimecode;
        public UInt64 EventCounter;
        public UInt16 AsicID;

        public double EventTimecode_ns;
        public double RunEventTimecode_ns;

        public ushort[] CoarseTime;
```

```
    public ushort[] FineTime;
    public ushort[] charge;
    public double[] Time;
    public double[] relative_time;
    public bool[] hit;
    public t_DataPETIROC()
    {
        CoarseTime = new ushort[32];
        FineTime = new ushort[32];
        charge = new ushort[32];
        hit = new bool[32];
        relative_time = new double[32];
        Time = new double[32];
    }

}
```

Multiboard readout script

A Multi Board Acquisition Script to run acquisition from multiple DT5550W hosting PETIROC ASICs is available. This script is available as **compiled executable** in the DT5550W Readout Software installation folder (C:\OpenHardware\DT5550W\Readout Software\ MultiboardDAQDT5550W_PETIROC.exe) or the **source code** can be downloaded at the following link:

https://github.com/NuclearInstruments/SCI_Digitizer_Asic/tree/development_citiroc

One or more DT5550W acquisition system is required in order to run this script. The minimum compatible firmware version is 2020.01. Older firmware will not work properly.

One master board provides the trigger and sync signals to all other slave boards. The master board could either work with internal trigger or externally triggered. The Master and slave board must be properly connected in order to acquire synchronously the data, as shown below. Termination jumper on output LEMO must be removed.

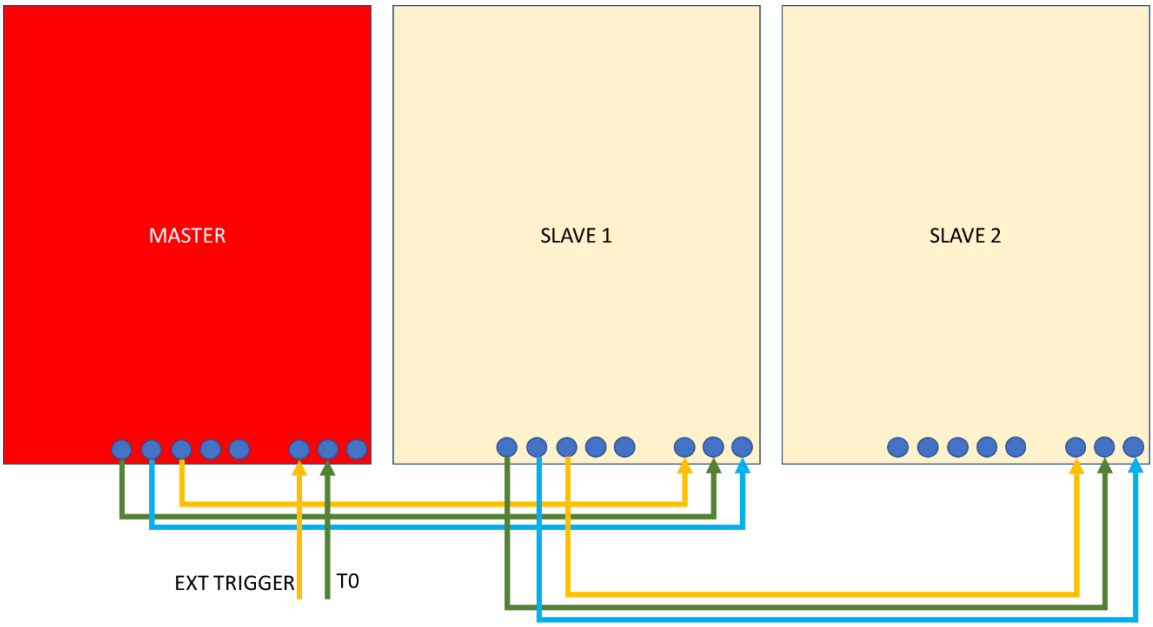


Figure 14.1: connection of multiple DT5550W+A55PETx boards. The yellow, green and cyan lines are distributing trigger, timing reference and run signal respectively.

The application must be called by command line MultiboardDAQDT5550W_PETIROC.exe. By default it loads the file config.json as configuration source. This file must contain a valid configuration in order to run the acquisition. The acquisition process is divided in four parts:

- Board enumeration. All board listened in the configuration file are enumerated on the USB chain.

```
Loading configuration file: config.json
Successfully loaded

-------------------------------------------------------------------------------
|   ID    |       SN       |      MODEL      |  CHANNELS  |     BUILD      |  MASTER  |
|---------|----------------|-----------------|------------|----------------|----------|
| 0       | NI120027       | PET             | 128        | 18100201       | *        |
| 1       | NI120010       | PET             | 64         | 18100201       |          |
-------------------------------------------------------------------------------

2/2 connected. Master board is: 0
```

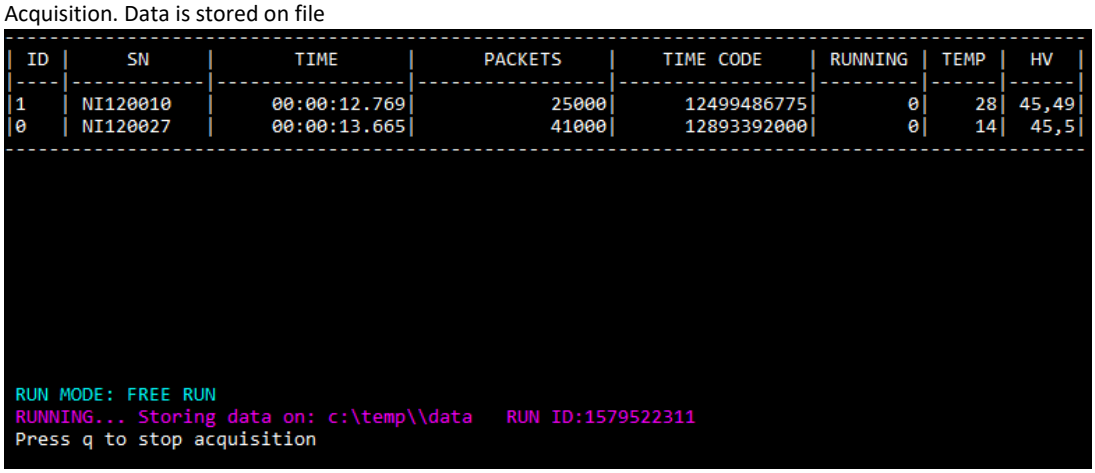
- Board and Asic configuration

```
-------------------------------------------------------------------------------
|   ID    |       SN       |      MODEL      |  CHANNELS  |     BUILD      |  MASTER  |
|---------|----------------|-----------------|------------|----------------|----------|
| 0       | NI120027       | PET             | 128        | 18100201       | *        |
| 1       | NI120010       | PET             | 64         | 18100201       |          |
-------------------------------------------------------------------------------
 Waiting HV on selected board...
2/2 connected. Master board is: 0ip waiting HV


Configuring ASIC...
Configuring BOARD 0...
    Generating bitstream ASIC 0 OK
    Configuring ASIC 0 OK
    Generating bitstream ASIC 1 OK
    Configuring ASIC 1 OK
    Generating bitstream ASIC 2 OK
    Configuring ASIC 2 OK
    Generating bitstream ASIC 3 OK
    Configuring ASIC 3 OK
Configuring BOARD 1...
    Generating bitstream ASIC 0 OK
    Configuring ASIC 0 OK
    Generating bitstream ASIC 1 OK
```

- HV waiting. The acquisition is paused waiting that all board HVs reach the target value

```
-------------------------------------------------------------------------------
|   ID    |       SN       |    SET POINT    |        V        | WAIT |    mA    |
|---------|----------------|-----------------|-----------------|------|----------|
|0        |NI120027        |            45,5|           36,054|  **  |         0|
|1        |NI120010        |            45,5|           29,164|  **  |         0|
-------------------------------------------------------------------------------









 Waiting HV on selected board...
 Press q to exit or press s to skip waiting HV
```

- Acquisition. Data is stored on file



Configuration File

The configuration file must be a valid json. Verify it online (https://jsonformatter.curiousconcept.com/). The parameters are named as in the DT5550W Readout Software GUI and are self-explicative.
Below we report a configuration file example.

```
{
    "ListOfDevices": [
        "NI120027",
        "NI120010"
    ],
    "MasterSN": "NI120027",
    "DataStorageFolder": "c:\\temp\\",
    "FileName": "data",
    "GeneralSettings": {
        "RunTarget": "FREE",
        "TargetValue": 5.5
    },
    "BoardsSettings": [
        {
            "SN": "NI120027",
            "HV_VOLT": 45.5,
            "HV_MAX": 57.2,
            "wait_hv": true,
            "switch_off_hv_on_end": true,
            "ReadTemperatureAndHV": true,
            "EnableHVCompensation": false,
            "HVCompensationCoefficent": 0.05,
            "TriggerSource": "INTERNAL",
            "EnableFrameTrigger": false,
            "ExtHoldDelay": 0,
            "UseChangeTrigger": false,
            "EnableExternalVeto": false,
            "SelfTrigger": {
                "enable": true,
                "rate": 1000
            },
            "Polarity": "POSITIVE",
            "configuration_mode": "ASIC_CONFIGURATION",
            "asic_configuration": {
                "global_settings": {
                    "SHAPER_C1": "5pF",
                    "SHAPER_C2": "100fF",
                    "CHARGE_TRIGGER": 1000,
                    "TIME_TRIGGER": 1000,
                    "INTERNAL_TRIGGER_DELAY": 0
```

```
                },
                "asic_settings": [
                    {
                        "channel_specific": [
                            {
                                "ID": 0,
                                "BIAS": true,
                                "BIAS_OFFSET": 128,
                                "MASK_CHARGE": false,
                                "MASK_TIME": false,
                                "THRESHOLD_ADJ": 32
                            }
                        ]
                    }
                ]
            },
            "bitstreams": [

"000000000000000000000000000000000000000110000000110000000110000000110000
000011000000011000000011000000011000000011000000011000000011000000011000
000011000000011000000011000000011000000011000000011000000011000000011000
000011000000011000000011000000011000000011000000011000000011000000011000
000011000000011000000011000000011000000000000000000000000000000000000000
000000100000100000100000100000100000100000100000100000100000100000100000
100000100000100000100000100000100000100000100000100000100000100000100000
100000100000100000100000100000100000100000100000111000001100000000110001
10011110000000011111111111111111001111111111001111111111111001001",

"000000000000000000000000000000000000000110000000110000000110000000110000
000011000000011000000011000000011000000011000000011000000011000000011000
000011000000011000000011000000011000000011000000011000000011000000011000
000011000000011000000011000000011000000011000000011000000011000000011000
000011000000011000000011000000011000000000000000000000000000000000000000
000000100000100000100000100000100000100000100000100000100000100000100000
100000100000100000100000100000100000100000100000100000100000100000100000
100000100000100000100000100000100000100000100000111000001100000000110001
10011110000000011111111111111111001111111111001111111111111001001",

"000000000000000000000000000000000000000110000000110000000110000000110000
000011000000011000000011000000011000000011000000011000000011000000011000
000011000000011000000011000000011000000011000000011000000011000000011000
000011000000011000000011000000011000000011000000011000000011000000011000
000011000000011000000011000000011000000000000000000000000000000000000000
000000100000100000100000100000100000100000100000100000100000100000100000
100000100000100000100000100000100000100000100000100000100000100000100000
100000100000100000100000100000100000100000100000111000001100000000110001
10011110000000011111111111111111001111111111001111111111111001001",

"000000000000000000000000000000000000000110000000110000000110000000110000
000011000000011000000011000000011000000011000000011000000011000000011000
000011000000011000000011000000011000000011000000011000000011000000011000
000011000000011000000011000000011000000011000000011000000011000000011000
000011000000011000000011000000011000000000000000000000000000000000000000
000000100000100000100000100000100000100000100000100000100000100000100000
100000100000100000100000100000100000100000100000100000100000100000100000
100000100000100000100000100000100000100000100000111000001100000000110001
10011110000000011111111111111111001111111111001111111111111001001"
            ]
        },
        {
            "SN": "NI120010",
            "HV_VOLT": 45.5,
```

```
            "HV_MAX": 57.2,
            "wait_hv": true,
            "switch_off_hv_on_end": true,
            "ReadTemperatureAndHV": true,
            "EnableHVCompensation": false,
            "HVCompensationCoefficent": 0.05,
            "TriggerSource": "EXTERNAL",
            "EnableFrameTrigger": false,
            "ExtHoldDelay": 0,
            "UseChangeTrigger": false,
            "EnableExternalVeto": false,
            "SelfTrigger": {
                "enable": true,
                "rate": 1000
            },
            "Polarity": "POSITIVE",
            "configuration_mode": "ASIC_CONFIGURATION",
            "asic_configuration": {
                "global_settings": {
                    "SHAPER_C1": "5pF",
                    "SHAPER_C2": "100fF",
                    "CHARGE_TRIGGER": 1000,
                    "TIME_TRIGGER": 1000,
                    "INTERNAL_TRIGGER_DELAY": 0
                },
                "asic_settings": [
                    {
                        "channel_specific": [
                            {
                                "ID": 0,
                                "BIAS": true,
                                "BIAS_OFFSET": 128,
                                "MASK_CHARGE": false,
                                "MASK_TIME": false,
                                "THRESHOLD_ADJ": 32
                            }
                        ]
                    }
                ]
            },
            "bitstreams": [

"11111111111111111111111111111110000000110000000110000000110000000110000
00001100000001100000001100000001100000001100000001100000001100000001100000
00001100000001100000001100000001100000001100000001100000001100000001100000
00001100000001100000001100000001100000001100000001100000001100000001100000
00001100000001100000001100000001100000001100000001100000001100000001100000
00001100000001100000001100000001111111111111111111111111111111111111111111
10000010000010000010000010000010000010000010000010000010000010000010000100000
10000010000010000010000010000010000010000010000010000010000010000010000100000
10000010000010000010000010000010000010000010000011100000110000000011000100
10011000000000000111100111100111001111111111001111111111111001001",

"11111111111111111111111111111110000000110000000110000000110000000110000
00001100000001100000001100000001100000001100000001100000001100000001100000
00001100000001100000001100000001100000001100000001100000001100000001100000
00001100000001100000001100000001100000001100000001100000001100000001100000
00001100000001100000001100000001100000001100000001100000001100000001100000
00001100000001100000001100000001111111111111111111111111111111111111111111
10000010000010000010000010000010000010000010000010000010000010000010000100000
10000010000010000010000010000010000010000010000010000010000010000010000100000
10000010000010000010000010000010000010000010000011100000110000000011000100
10011000000000000111100111100111001111111111001111111111111001001"
            ]
```

```
        }
    ]
}
```

The possible values of enumerative parameters are:

```
RunTarget: FREE:       Unlimited acquisition
           TIME:       Number of seconds
           COUNTS:     Number of events

TriggerSource:  INTERNAL:   Trigger source is internal
                INT/EXT:    Trigger source is internal and external
                EXTERNAL:   Trigger source is external

Polarity:       POSITIVE
                NEGATIVE

configuration_mode:   ASIC_CONFIGURATION: Use parametricconfiguration
                      BITSTREAM: Use ASIC bitstream as string

SHAPER_C1       1.25pF
                2.5pF
                3.75pF
                5pF

SHAPER_C2       100fF
                200fF
                300fF
                400fF
```

In order to operate Petiroc chip must be properly configured. The configuration can be performed in two ways:

- ASIC_CONFIGURATION mode uses the structure **"asic_configuration"** to internally generate the bitstream to be uploaded on the ASIC. This configuration mode is the suggested way to configure ASICs because all parameters are correctly generated according to master/slave.
- BITSTREAM mode uses offline generated bitstream listened in the bitstreams array. In this mode the asic_configuration structure is ignored.

In order to select the configuration mode, the **"configuration_mode"** parameter must be set accordingly

When ASIC_CONFIGURATION is used, it is possible to specify different settings channel by channels or set common parameters for all the channels, as shown in the example below.

```
"asic_settings": [
        {
            "channel_specific": [
                {
                    "ID": 0,
                    "BIAS": true,
                    "BIAS_OFFSET": 128,
                    "MASK_CHARGE": false,
                    "MASK_TIME": false,
                    "THRESHOLD_ADJ": 32
                }
            ]
        }
    ]
```

Command line parameters

`/config=<file_name>`	specify the path of configuration file
`/skipconfig`	skip reconfiguration of the board

Data Format

The script produces, for each run, a separate data file for each connected board. The data format in the file is the following:

ID	Id of the event
ASIC	Asic ID
EventCounter	Event counter for start of run
RUN_EventTimeCodeLSB	Time code from start of run (LSB = 20ns)
T0_to_Event_Timecode	Time code from T0 (LSB = 20ns)
HIT_x	Petiroc channel x-th hit
CHARGE_x	Petiroc channel x-th charge
COARSE_x	Petiroc channel x-th time coarse TDC
FINE_x	Petiroc channel x-th time fine TDC
HV	HV value
mA	mA drown form HV
TEMPERATURE	Temperature in °C

15 Technical Support

CAEN makes available the technical support of its specialists for request concerning the software and the hardware. Use the support form available at the following link:

https://www.caen.it/support-services/support-form/

CAEN SpA is acknowledged as the only company in the world providing a complete range of High/Low Voltage Power Supply systems and Front-End/Data Acquisition modules which meet IEEE Defaults for Nuclear and Particle Physics. Extensive Research and Development capabilities have allowed CAEN SpA to play an important, long term role in this field. Our activities have always been at the forefront of technology, thanks to years of intensive collaborations with the most important Research Centres of the world. Our products appeal to a wide range of customers including engineers, scientists and technical professionals who all trust them to help achieve their goals faster and more effectively.

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