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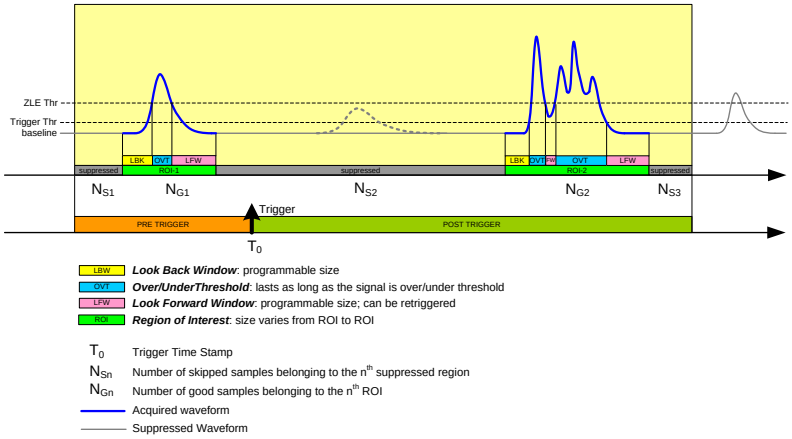

User Manual UM6065

730-725 DPP-ZLE*plus* Registers

Register Description for 725 and 730 DPP-ZLE*plus*

Rev. 2 - July 8th 2020

Purpose of this Manual

The Register Manual contains the full description of the DPP-ZLE*plus* firmware registers for 725 and 730 family series and 725S and 730S family series. The description is compliant with the DPP-ZLE*plus* firmware revision **4.17_140.04** for 725 and 730 series and **4.22_140.04** for 725S and 730S series. For future release compatibility check in the firmware history files.

Change Document Record

Date	Revision	Changes
June 9th 2019	00	Initial release
May 15th 2020	01	Added support to x725S and x730S series
July 8th 2020	02	Modified register ZLE Baseline

Symbols, abbreviated terms and notation

ADC	Analog-to-Digital Converter
AMC	ADC & Memory Controller
DAQ	Data Acquisition
DAC	Digital-to-Analog Converter
DC	Direct Current
DPP	Digital Pulse Processing
DPP-ZLE	DPP for Zero Length Encoding
LVDS	Low-Voltage Differential Signal
ROC	ReadOut Controller
USB	Universal Serial Bus

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1 Registers and Data Format

All registers described in the User Manual are 32-bit wide. In case of VME access, **A24** and **A32** addressing mode can be used.

Reset and Clear

The module's registers can be set back to their default values on software reset command by writing in the Software Reset register or by system reset from backplane, in case of VME boards. In particular, the registers or buffers listed below

- Event Readout Buffer
- Buffer Occupancy
- Event Stored
- Event Size

are also be set back to their default values (registers) or emptied (buffers) by a clear issued:

- automatically by the firmware at the start of each run;
- on software command by writing in the Software Clear register
- by hardware (VME boards only), through the LVDS interface properly configured (see the section "Front Panel LVDS I/Os" of the digitizer User Manual).

Register Address Map

The table below reports the complete list of registers that can be accessed by the user. The register names in the first column can be clicked to be redirected to the relevant register description. The register address is reported on the second column as a hex value. The third column indicates the allowed register access mode, where:

R	**Read only**. The register can be accessed in read only mode.
W	**Write only**. The register can be accessed in write only mode.
R/W	**Read and write**. The register can be accessed both in read and write mode.

According to the attribute reported in the fourth column, the following choices are available:

I	**Individual register**. This kind of register has N instances, where N is the total number of channels in the board. Individual registers can be written either in single mode (individual setting) or broadcast (simultaneous write access to all channels). Read command must be individual. Single access can be performed at address 0x1nXY, where n is the channel number, while broadcast write can be performed at the address 0x80XY. For example: • access to address 0x1570 to read/write register 0x1n70 for channel 5 of the board; • to write the same value for all channels in the board, access to 0x8070 (broadcast write). To read the corresponding value, access to the individual address 0x1n70.
C	**Common register**. Register with this attribute has a single instance, therefore read and write access can be performed at address 0x80XY only.

Register Name	Address	Mode	Attribute
Input Dynamic Range	0x1n28, 0x8028	R/W	I
ZLE Baseline	0x1n34, 0x8034	R/W	I
Pre Trigger	0x1n38, 0x8038	R/W	I
Samples Look Back	0x1n54, 0x8054	R/W	I
Samples Look Forward	0x1n58, 0x8058	R/W	I
ZLE Threshold	0x1n5C, 0x805C	R/W	I
Trigger Threshold	0x1n60, 0x8060	R/W	I
Input Control	0x1n64, 0x8064	R/W	I
Couple Trigger Logic	0x1n68, 0x8068	R/W	I
Channel n Status	0x1n88	R	I
AMC Firmware Revision	0x1n8C	R	I
DC Offset	0x1n98, 0x8098	R/W	I
Channel n ADC Temperature	0x1nA8	R	I
Board Configuration	0x8000, 0x8004 (BitSet), 0x8008 (BitClear)	R/W	C
Record Length	0x8020	R/W	C
Couple Self-Trigger Logic	0x8068	R/W	C
Channel ADC Calibration	0x809C	W	C
Acquisition Control	0x8100	R/W	C
Acquisition Status	0x8104	R	C
Software Trigger	0x8108	W	C
Global Trigger Mask	0x810C	R/W	C
Front Panel TRG-OUT (GPO) Enable Mask	0x8110	R/W	C
LVDS I/O Data	0x8118	R/W	C
Front Panel I/O Control	0x811C	R/W	C
Channel Enable Mask	0x8120	R/W	C
ROC FPGA Firmware Revision	0x8124	R	C
Event Stored	0x812C	R	C
Voltage Level Mode Configuration	0x8138	R/W	C
Software Clock Sync	0x813C	W	C
Board Info	0x8140	R	C
Analog Monitor Mode	0x8144	R/W	C
Event Size	0x814C	R	C
Fan Speed Control	0x8168	R/W	C
Run/Start/Stop Delay	0x8170	R/W	C
Board Failure Status	0x8178	R	C
Front Panel LVDS I/O New Features	0x81A0	R/W	C
Buffer Occupancy Gain	0x81B4	R/W	C
Extended Veto Delay	0x81C4	R/W	C
Readout Control	0xEF00	R/W	C
Readout Status	0xEF04	R	C
Board ID	0xEF08	R/W	C
MCST Base Address and Control	0xEF0C	R/W	C
Relocation Address	0xEF10	R/W	C
Interrupt Status/ID	0xEF14	R/W	C
Interrupt Event Number	0xEF18	R/W	C
Max Number of Events per BLT	0xEF1C	R/W	C
Scratch	0xEF20	R/W	C
Software Reset	0xEF24	W	C
Software Clear	0xEF28	W	C
Configuration Reload	0xEF34	W	C
Configuration ROM Checksum	0xF000	R	C
Configuration ROM Checksum Length BYTE 2	0xF004	R	C
Configuration ROM Checksum Length BYTE 1	0xF008	R	C
Configuration ROM Checksum Length BYTE 0	0xF00C	R	C
Configuration ROM Constant BYTE 2	0xF010	R	C

Configuration ROM Constant BYTE 1	0xF014	R	C
Configuration ROM Constant BYTE 0	0xF018	R	C
Configuration ROM C Code	0xF01C	R	C
Configuration ROM R Code	0xF020	R	C
Configuration ROM IEEE OUI BYTE 2	0xF024	R	C
Configuration ROM IEEE OUI BYTE 1	0xF028	R	C
Configuration ROM IEEE OUI BYTE 0	0xF02C	R	C
Configuration ROM Board Version	0xF030	R	C
Configuration ROM Board Form Factor	0xF034	R	C
Configuration ROM Board ID BYTE 1	0xF038	R	C
Configuration ROM Board ID BYTE 0	0xF03C	R	C
Configuration ROM PCB Revision BYTE 3	0xF040	R	C
Configuration ROM PCB Revision BYTE 2	0xF044	R	C
Configuration ROM PCB Revision BYTE 1	0xF048	R	C
Configuration ROM PCB Revision BYTE 0	0xF04C	R	C
Configuration ROM FLASH Type	0xF050	R	C
Configuration ROM Board Serial Number BYTE 1	0xF080	R	C
Configuration ROM Board Serial Number BYTE 0	0xF084	R	C
Configuration ROM VCXO Type	0xF088	R	C

Input Dynamic Range

This register sets the input dynamic range of each channel individually.

Address	0x1n28, 0x8028
Mode	R/W
Attribute	I

Bit	Description
[0]	Input Dynamic Range. Options are: 0 = 2 Vpp (default); 1 = 0.5 Vpp.
[31:1]	Reserved.

ZLE Baseline

This register manages the baseline calculation for the ZLE. The user can define a fixed value of baseline, which remains constant for the whole acquisition, or let the board calculate it dynamically. In the second case it is required to define the level of the baseline noise in ADC counts. The baseline is then iteratively evaluated as the mean value over 16 samples. When the value does not exceeds the noise level for at least four iterations, then it is frozen. The algorithm then looks for the signal threshold crossing.

WARNING: in case of fixed baseline, if, in any of the channels taking part to the trigger generation, the difference between the signal and the set baseline is always larger than the trigger threshold (as set in register 0x1n60), that channel, or any other channel, will not be able to generate a trigger.

Address	0x1n34, 0x8034
Mode	R/W
Attribute	I

Bit	Description
[13:0]	Value of fixed baseline in ADC counts.
[15:14]	Reserved.
[23:16]	Baseline noise level in ADC counts.
[24]	Enable/Disable baseline calculation. Options are: 0 = the baseline is calculated by the algorithm; 1 = the baseline is fixed at the value written in bits[13:0].
[31:25]	Reserved.

Pre Trigger

The Pre Trigger defines the number of samples before the trigger in the waveform saved into memory.

Address	0x1n38, 0x8038
Mode	R/W
Attribute	I

Bit	Description
[7:0]	Number of pre trigger samples according to the formula Ns = N * 4, where Ns is the pre trigger and N is the register value. For example, write N = 5 to set 20 samples of pre trigger. Each sample corresponds to 4 ns for 725 series and 2 ns for 730 series. NOTE: maximum value is 240. NOTE: A fixed latency should be added to the pre trigger value, equal to 16 ns in case of trigger generated by over-threshold channels; 186 and 132 ns in case of external trigger from TRG IN connector for 725 and 730 series respectively.
[31:8]	Reserved.

Samples Look Back

Samples to be acquired before the ZLE over/under threshold (N_LBK). The polarity can be defined through bit[11] of register 0x1n64.

Address	0x1n54, 0x8054
Mode	R/W
Attribute	I

Bit	Description
[7:0]	Number of samples according to the formula N_LBCK = N * 2, where N is the register value. For example, write N = 12 to acquire 24 samples. Each sample corresponds to 4 ns in case of x725, and 2 ns in case of x730.
[31:8]	Reserved.

Samples Look Forward

Number of samples to be acquired after the ZLE over/under threshold (N_LFW). The polarity can be defined through bit[11] of register 0x1n64.

Address	0x1n58, 0x8058
Mode	R/W
Attribute	I

Bit	Description
[7:0]	Number of samples according to the formula N_LFW = N * 2, where N is the register value. For example, write N = 12 to acquire 24 samples. Each sample corresponds to 4 ns in case of x725, and 2 ns in case of x730.
[31:8]	Reserved.

ZLE Threshold

This register defines the threshold for the zero length encoding. The ZLE threshold is compared with the height of each sample in the event minus the baseline, and according to the polarity (bit[11] of register 0x1n64), samples over/under threshold are defined as ”good” samples and included in the data packet. The other samples are flagged as ”skipped” and discarded; in the data it is reported the number of skipped samples only. It is also possible to define the number of samples to be acquired before and after the over/under threshold through registers 0x1n54 and 0x1n58.

Address	0x1n5C, 0x805C
Mode	R/W
Attribute	I

Bit	Description
[13:0]	Number of LSB counts for the ZLE Threshold, where 1 LSB = 0.12 mV for 725 and 730 series with 2 Vpp input range, and 1 LSB = 0.03 mV for 725 and 730 series with 0.5 Vpp input range. The threshold is referred to the baseline level.
[31:14]	Reserved.

Trigger Threshold

Sets the threshold of the trigger (leading edge discriminator) to identify an event inside the ZLE acquisition window. For those events, the ZLE algorithm is then applied.

Address	0x1n60, 0x8060
Mode	R/W
Attribute	I

Bit	Description
[13:0]	Sets the number of LSB counts for the Trigger Threshold, where 1 LSB = 0.12 mV for 725 and 730 series with 2 Vpp input range, and 1 LSB = 0.03 mV for 725 and 730 series with 0.5 Vpp input range. The threshold is referred to the baseline level.
[31:14]	Reserved.

Input Control

This register defines the properties of the input and enables an internal pulse emulator for debug purposes.

Address	0x1n64, 0x8064
Mode	R/W
Attribute	I

Bit	Description
[0]	Test Pulse Enable. When enabled an internal exponential pulse is generated. The pulse replaces the input and it can be used for testing and debugging. Options are: 0 = disabled; 1 = enabled.
[3:1]	Test Pulse Rate. Options are: 0 = 1 Hz for 730, 0.5 Hz for 725; 1 = 10 Hz for 730, 5 Hz for 725; 2 = 100 Hz for 730, 50 Hz for 725; 3 = 1 kHz for 730, 500 Hz for 725; 4 = 10 kHz for 730, 5 kHz for 725; 5 = 100 kHz for 730, 50 kHz for 725; 6 = 1 MHz for 730, 500 kHz for 725; 7 = 10 MHz for 730, 5 MHz for 725.
[5:4]	Test Pulse Amplitude. Options are: 00 = x1 (peak height of 2000 ADC counts, baseline at mid-scale); 01 = x2 (peak height of 4000 ADC counts, baseline at mid-scale); 10 = x3 (peak height of 6000 ADC counts, baseline at mid-scale); 11 = x4 (peak height of 8000 ADC counts, baseline at mid-scale).
[6]	Test Pulse Polarity. Options are: 0 = negative polarity; 1 = positive polarity.
[7]	No ZLE Threshold (default value is 0). When enabled, the ZLE threshold is not applied and the event is completely acquired in the acquisition window. Options are: 0 = disabled; 1 = enabled.
[8]	Input Polarity. Options are: 0 = negative polarity, the input crosses the threshold when BSL - Si < Thr, where BSL is the baseline value, Si is the i^{th} sample, and Thr is the threshold value; 1 = positive polarity, the input crosses the threshold when Si - BSL > Thr, where BSL is the baseline value, Si is the i^{th} sample, and Thr is the threshold value.
[31:9]	Reserved.

Couple Trigger Logic

The register defines the logic with which a channel pair contributes to the global trigger generation.

Address	0x1n68, 0x8068
Mode	R/W
Attribute	I

Bit	Description
[1:0]	Defines the logic with which a channel pair contributes to the global trigger generation. Options are: 00: The trigger request is the logical AND of the channels self trigger 01: The trigger request is the even channel self trigger 10: The trigger request is the odd channel self trigger 11: The trigger request is the logical OR of the channels self trigger
[31:2]	Reserved

Channel n Status

This register contains the status information of channel n.

Address	0x1n88
Mode	R
Attribute	I

Bit	Description
[0]	Channel memory full (TRUNCATE condition)
[1]	Channel memory empty
[2]	If 1, the SPI bus is busy.
[3]	ADC Calibration Status. Options are: 0 = Calibration not done; 1 = Calibration done. NOTE: this bit is meaningless in case on 725S and 730S.
[4]	ADC Power Down. When set to 1, it means that the ADC of channel n has been shut down due to an over-temperature condition.
[31:5]	Reserved

AMC Firmware Revision

Returns the DPP firmware revision (mezzanine level).
To control the mother board firmware revision see register 0x8124.
For example: if the register value is 0xC3218303:
- Firmware Code and Firmware Revision are 131.3;
- Build Day is 21;
- Build Month is March;
- Build Year is 2012.

NOTE: since 2016 the build year started again from 0.

Address	0x1n8C
Mode	R
Attribute	I

Bit	Description
[7:0]	Firmware revision number.
[15:8]	Firmware DPP code. Each DPP firmware has a unique code.
[19:16]	Build Day (lower digit).
[23:20]	Build Day (upper digit).
[27:24]	Build Month. For example: 3 means March, 12 is December.
[31:28]	Build Year. For example: 0 means 2000, 12 means 2012. NOTE: since 2016 the build year started again from 0.

DC Offset

This register allows to adjust the baseline position (i.e. the 0 Volt) of the input signal on the ADC scale. The ADC scale ranges from 0 to 2^{NBit} - 1, where NBit is the number of bits of the on-board ADC. The DAC controlling the DC Offset has 16 bits, i.e. it goes from 0 to 65535 independently from the NBit value and the board type.
Typically a DC Offset value of 32K (DAC mid-scale) corresponds to about the ADC mid-scale. Increasing values of DC Offset make the baseline decrease. The range of the DAC is about 5% (typ.) larger than the ADC range, hence DAC settings close to 0 and 64K correspond to ADC respectively over and under range.
WARNING: before writing this register, it is necessary to check that bit[2] = 0 at 0x1n88, otherwise the writing process will not run properly! After writing, the user is recommended to wait for few seconds before a new RUN to let the DAC output (i.e. the new programmed DC offset) get stabilized.

Address	0x1n98, 0x8098
Mode	R/W
Attribute	I

Bit	Description
[15:0]	DC Offset value in DAC LSB unit
[31:16]	Reserved

Channel n ADC Temperature

This register monitors the temperature of the ADC chips.
NOTE: if the temperature varies significantly during the digitizer operation, the user is recommended to perform a new channel calibration procedure (see register 0x809C) to restore the board performance. This is not true in case of 725S and 730S as these models do not require any calibration.

Address	0x1nA8
Mode	R
Attribute	I

Bit	Description
[7:0]	ADC Chip Temperature (expressed in °C). Values are signed, ranging from - 64°C to 127°C.
[31:8]	Reserved.

Board Configuration

This register contains general settings for the board configuration.

Address	0x8000, 0x8004 (BitSet), 0x8008 (BitClear)
Mode	R/W
Attribute	C

Bit	Description
[0]	Reserved: must be 0.
[1]	Reserved: must be 0
[2]	Reserved: must be 0.
[3]	Test Mode (default value is 0). When the test pattern is enabled, the input samples are replaced by a sawtooth test signal. Options are: 0 = Test Mode disabled; 1 = Test Mode enabled.
[4]	Reserved: must be 1.
[31:5]	Reserved: must be 0.

Record Length

Sets the record length for the waveform acquisition. The record length is defined by the time of arrival of the global trigger and by the pre trigger (register 0x1n38). Other triggers are inhibited during the whole record length.
Note: only a maximum of 2000 "good" samples can be saved despite the record length value. If an event exceeds 2000 samples, it is truncated and flagged.

Address	0x8020
Mode	R/W
Attribute	C

Bit	Description
[19:0]	Number of samples in the waveform according to the formula Ns = N * 4, where Ns is the record length and N is the register value. For example, write N = 6 to acquire 24 samples. Each sample corresponds to 4 ns in case of x725, and 2 ns in case of x730.
[31:20]	Reserved.

Couple Self-Trigger Logic

This register sets the logic of the self-trigger signal from couples of adjacent channels. The signal is propagated from mezzanine to mother board for further processing, as for the global trigger generation, or TRG-OUT.
NOTE: this register must be read at address 0x1n68, where n is the channel number.

Address	0x8068
Mode	R/W
Attribute	C

Bit	Description
[15:0]	Each couple of bits ([1:0], [3:2], etc.]) sets the self-trigger logic for the i^{th} couple (couple 0 = channel 0 and channel 1, couple 1 = channel 2 and channel 3). Options are: 00 = AND; 01 = even channel of the couple; 10 = odd channel of the couple; 11 = OR (default). For example 0xFF sets the OR for the first four couples of the digitizer. NOTE: in case of DT, NIM and 8-channel VME boards, only bits[7:0] are meaningful, while bits[15:8] are reserved.
[31:16]	Reserved.

Channel ADC Calibration

This register is meaningless for x725S and x730S digitizers as they do not require channel calibration; writing to this register does not generate any error (BERR) but simply has no effect.

Other x725 and x730 digitizers require a channel calibration to achieve the best performances. A calibration of the ADCs is automatically performed by the firmware at the power-on, but the user is recommended to manually execute the calibration after the ADCs have stabilized their operating temperature (see register 0x1nA8). The calibration will not need to be repeated at each acquisition run, unless the operating temperature varies significantly, or clock settings are modified (e.g. switching from internal to external clock).
WARNING: before writing this register, it is necessary to check that bit[2] = 0 of register 0x1n88, otherwise the writing process cannot run properly.
WARNING: It is normally not required to calibrate after a board reset but, if a Reset command is intentionally issued to the digitizer (write access at 0xEF24) to be directly followed by a calibration procedure, it is recommended to wait for the board to reach stable conditions (indicatively 100 ms) before to start the calibration.
WARNING: at power-on, a Sync command is issued by the firmware to the ADCs to synchronize all of them to the board's clock. In the standard operating, this command is not required to be repeated by the user. If a Sync command is intentionally issued (see register 0x813C), the user must consider that a new calibration procedure is needed for a correct board operating.

Address	0x809C
Mode	W
Attribute	C

Bit	Description
[31:0]	Write any value to start the automatic simultaneous calibration of the ADC for all channels of the board. Bit[3] of register 0x1n88 will be set to 0. Poll this bit until it returns to 1.

Acquisition Control

This register manages the acquisition settings.

Address	0x8100
Mode	R/W
Attribute	C

Bit	Description
[1:0]	Start/Stop Mode Selection (default value is 00). Options are: 00 = SW CONTROLLED. Start/stop of the run takes place on software command by setting/resetting bit[2] of this register; 01 = S-IN/GPI CONTROLLED (S-IN for VME, GPI for Desktop/NIM). Acquisition must be armed by setting bit[2] = 1, then the run can optionally START/STOP ON LEVEL or START ON EDGE according to bit[11] (NOTE: the START ON EDGE option is implemented from ROC FPGA fw revision 4.22 on); 10 = FIRST TRIGGER CONTROLLED. If the acquisition is armed (i.e. bit[2] = 1), then the run starts on the first trigger pulse (rising edge on TRG-IN); this pulse is not used as input trigger, while actual triggers start from the second pulse. The stop of Run must be SW controlled (i.e. bit[2] = 0); 11 = LVDS CONTROLLED (VME only). It is like option 01 but using LVDS (RUN) instead of S-IN. The LVDS can be set using registers 0x811C and 0x81A0.
[2]	Acquisition Start/Arm (default value is 0). When bits[1:0] = 00, this bit acts as a Run Start/Stop. When bits[1:0] = 01, 10, 11, this bit arms the acquisition and the actual Start/Stop is controlled by an external signal. Options are: 0 = Acquisition STOP (if bits[1:0]=00); Acquisition DISARMED (others); 1 = Acquisition RUN (if bits[1:0]=00); Acquisition ARMED (others).
[3]	Reserved.
[5:4]	Reserved
[6]	PLL Reference Clock Source (Desktop/NIM only). Default value is 0. Options are: 0 = internal oscillator (50 MHz); 1 = external clock from front panel CLK-IN connector. NOTE: this bit is reserved in case of VME boards.
[7]	Reserved.
[8]	LVDS I/O Busy Enable (VME only). Default value is 0. The LVDS I/Os can be programmed to accept a Busy signal as input, or to propagate it as output. Options are: 0 = disabled; 1 = enabled. NOTE: this bit is supported only by VME boards and meaningful only if the LVDS new features are enabled (bit[8]=1 of register 0x811C). Register 0x81A0 should also be configured for nBusy/nVeto.
[9]	LVDS I/O Veto Enable (VME only). Default value is 0. The LVDS I/Os can be programmed to accept a Veto signal as input, or to transfer it as output. Options are: 0 = disabled (default); 1 = enabled. NOTE: this bit is supported only by VME boards and meaningful only if the LVDS new features are enabled (bit[8]=1 of register 0x811C). Register 0x81A0 should also be configured for nBusy/nVeto.
[10]	Reserved.

[11]	LVDS I/O RunIn Enable Mode (VME only) and START ON EDGE Enable for S-IN/GPI CONTROLLED Mode. - If LVDS CONTROLLED MODE is set (bit[1:0] = 0b11) and acquisition is armed (bit[2] = 1), the LVDS I/Os can be programmed to accept a RunIn signal as input, or to transfer it as output: 0 = starts on RunIn level (default); 1 = starts on RunIn rising edge. NOTE: this bit is meaningful only if the LVDS new features are enabled (bit[8]=1 of register 0x811C). Register 0x81A0 must also be configured for nBusy/nVeto. NOTE: this register is valid from ROC FPGA fw revision 4.16 on. - If S-IN/GPI CONTROLLED Mode is set (bit[1:0] = 0b01) and acquisition is armed (bit[2] = 1): 0 = Start/Stop run on S-IN/GPI level (default); 1 = Start run on S-IN/GPI rising edge (stop must be by software command: bit[2] = 0). NOTE: options bit[11] = 1 is valid from ROC FPGA fw revision 4.22 on.
[12]	VetoIn as veto for TRG-OUT (VME boards only). When the LVDS VetoIn signal is enabled (bit[9] = 1 in the 0x8100 register), this bit permits to use VetoIn to inhibit the triggers on TRG-OUT connector. The duration of the veto signal on TRG- OUT can be optionally extended by a time value set in the 0x81C4 register. Such function is useful in particular cases of synchronization of a multi-board system. Options are: 0 = VetoIn not used (default) 1 = VetoIn used for TRG-OUT inhibit NOTE: this bit is reserved in case of Desktop and NIM digitizers or ROC FPGA firmware rel. <= 4.16 .
[31:13]	Reserved.

Acquisition Status

This register monitors a set of conditions related to the acquisition status.

Address	0x8104
Mode	R
Attribute	C

Bit	Description
[1:0]	Reserved.
[2]	Acquisition Status. It reflects the status of the acquisition and drivers the front panel 'RUN' LED. Options are: 0 = acquisition is stopped ('RUN' is off); 1 = acquisition is running ('RUN' lits).
[3]	Event Ready. Indicates if any events are available for readout. Options are: 0 = no event is available for readout; 1 = at least one event is available for readout. NOTE: the status of this bit must be considered when managing the readout from the digitizer.
[4]	Event Full. Indicates if at least one channel has reached the FULL condition. Options are: 0 = no channel has reached the FULL condition; 1 = the maximum number of events to be read is reached.
[5]	Clock Source. Indicates the clock source status. Options are: 0 = internal (PLL uses the internal 50 MHz oscillator as reference); 1 = external (PLL uses the external clock on CLK-IN connector as reference).
[6]	Reserved.
[7]	PLL Unlock Detect. This bit flags a PLL unlock condition. Options are: 0 = PLL has had an unlock condition since the last register read access; 1 = PLL has not had any unlock condition since the last register read access. NOTE: flag can be restored to 1 via read access to register 0xEF04.
[8]	Board Ready. This flag indicates if the board is ready for acquisition (PLL and ADCs are correctly synchronized). Options are: 0 = board is not ready to start the acquisition; 1 = board is ready to start the acquisition. NOTE: this bit should be checked after software reset to ensure that the board will enter immediately in run mode after the RUN mode setting; otherwise, a latency between RUN mode setting and Acquisition start might occur.
[14:9]	Reserved.
[15]	S-IN (VME boards) or GPI (DT/NIM boards) Status. Reads the logical level on S-IN (GPI) front panel connector.
[16]	TRG-IN Status. Reads the logical level on TRG-IN front panel connector.
[18:17]	Reserved.
[19]	Channels Shutdown Status. This bit monitors the shutdown of the channels according to bit[8] of register 0x1n88 and the procedure described at 0x81C0 register. Options are: 0 = channels are ON; 1 = channels are in shutdown.

[23:20]	Bits[23:20] (bits[21:20] in case of DT, NIM and 8-channel VME versions) monitor the temperature status of the board channels. Each bit refers to a 4- channel mezzanine, i.e. bit[20] refers to channels 3-0, bit[21] to channels 7-4, and so on. When at least one of the channels in the mezzanine exceeds the 70°C limit (85°C in case of x725S/x730S models), the relevant bit is set automatically to 1. As soon as at least one of these bits becomes 1, the board enters the temperature protection condition which causes the automatic channel turn-off and the acquisition RUN stop (if it was on): 1. Bit[19] becomes 1. 2. Bit[2] of register 0x8100 is automatically set to 0. Data possibly stored at the moment can be readout in any case. When all the bits[23:20] (bits[21:20]) become 0, the board exits the temperature protection condition. This means that the channel temperature reached at least 61°C (74°C in case of x725S/x730S models). The user has then to turn on the board channels and the acquisition RUN (if necessary): 1. Bit[0] of register 0x81C0 must be set to 0 (bit[19] of register 0x8104 becomes 0). 2. Bit[2] of register 0x8100 must be set to 1.
[31:24]	Reserved. NOTE: in case of DT, NIM and 8-channel VME boards, bits[31:22] are reserved.

Software Trigger

Writing this register causes a software trigger generation which is propagated to all the enabled channels of the board.

Address	0x8108
Mode	W
Attribute	C

Bit	Description
[31:0]	Write whatever value to generate a software trigger.

Global Trigger Mask

This register sets which signal can contribute to the global trigger generation.

Address	0x810C
Mode	R/W
Attribute	C

Bit	Description
[7:0]	Bit n corresponds to the trigger request from couple n that participates to the global trigger generation (n = 0,...,3 for DT, NIM and 8-channel VME boards; n = 0,...,7 for 16-channel VME boards). Options are: 0 = trigger request does not participate to the global trigger generation; 1 = trigger request participates to the global trigger generation. Couple n corresponds to the two consecutive channels 2n and 2n+1: couple 0 is channel 0 and channel 1, couple 1 is channel 2 and channel 3, and so on. The trigger request from the couple can be programmed through register 0x1n84 to be the AND/OR/one of the channels. NOTE: in case of DT, NIM and 8-channel VME boards, only bits[3:0] are meaningful, while bits[7:4] are reserved.
[19:8]	Reserved. NOTE: in case of DT, NIM and 8-channel VME Boards, bits[19:4] are reserved.
[23:20]	Majority Coincidence Window. Sets the time window for the majority coincidence in units of the Trigger Clock (8 ns for 730 and 16 ns for 725). Majority level must be set different from 0 through bits[26:24].
[26:24]	Majority Level. Sets the majority level for the global trigger generation. For a level m, the trigger fires when at least m+1 of the enabled trigger requests (bits[7:0] or [3:0]) are over-threshold inside the majority coincidence window (bits[23:20]). NOTE: The majority level must be smaller than the number of channel enabled via bits[7:0] mask (or [3:0]).
[28:27]	Reserved.
[29]	LVDS Trigger (VME boards only). When enabled, the trigger from LVDS I/O participates to the global trigger generation (in logic OR). Options are: 0 = disabled; 1 = enabled.
[30]	External Trigger (default value is 1). When enabled, the external trigger on TRG-IN participates to the global trigger generation in logic OR with the other enabled signals. Options are: 0 = disabled; 1 = enabled.
[31]	Software Trigger (default value is 1). When enabled, the software trigger participates to the global trigger signal generation in logic OR with the other enabled signals. Options are: 0 = disabled; 1 = enabled.

Front Panel TRG-OUT (GPO) Enable Mask

This register sets which signal can contribute to generate the signal on the front panel TRG-OUT LEMO connector (GPO in case of DT and NIM boards).

Address	0x8110
Mode	R/W
Attribute	C

Bit	Description
[7:0]	This mask sets the trigger requests participating in the TRG-OUT (GPO) signal. Bit n corresponds to the trigger request from couple n (n=0,...,3 in case of DT, NIM and 8-channel VME boards; n = 0,..., 7 in case of 16-channel VME boards). Options are: 0 = Trigger request does not participate to the TRG-OUT (GPO) signal; 1 = Trigger request participates to the TRG-OUT (GPO) signal. Couple n corresponds to the two consecutive channels 2n and 2n+1: couple 0 is channel 0 and channel 1, couple 1 is channel 2 and channel 3, and so on. The trigger request from the couple can be programmed through register 0x1n84 to be the AND/OR/one of the two channels. NOTE: In case of DT, NIM and 8-channels VME boards, only bits[3:0] are meaningful while bis[7:4] are reserved.
[9:8]	TRG-OUT (GPO) Generation Logic. The enabled trigger requests (bits [7:0] or [3:0]) can be combined to generate the TRG-OUT (GPO) signal. Options are: 00 = OR; 01 = AND; 10 = Majority; 11 = Reserved.
[12:10]	Majority Level. Sets the majority level for the TRG-OUT (GPO) signal generation. Allowed level values are between 0 and 7 for VME boards, while between 0 and 3 for DT, NIM and 8-channel VME boards. For a level m, the trigger fires when at least m+1 of the trigger requests are generated by the enabled couples of channels (bits [7:0] or [3:0]) .
[28:13]	Reserved.
[29]	LVDS Trigger Enable (VME boards only). LVDS connectors programmed as inputs (according to registers 0x811C and 0x81A0) can participate in the TRG- OUT (GPO) signal generation, in logic OR with the other enabled signals. Options are: 0 = disabled; 1 = enabled.
[30]	External Trigger (default value is 1). When enabled, the external trigger on TRG-IN can participate in the TRG-OUT (GPO) signal generation in logic OR with the other enabled signals. Options are: 0 = disabled; 1 = enabled.
[31]	Software Trigger (default value is 1). When enabled, the software trigger can participate in the TRG-OUT (GPO) signal generation in logic OR with the other enabled signals. Options are: 0 = disabled; 1 = enabled.

LVDS I/O Data

This register allows to read out the logic level of the LVDS I/Os if the LVDS pins are configured as outputs, and to set the logic level of the LVDS I/Os if the pins are configured as inputs.
NOTE: this register is supported by VME boards only.

Address	0x8118
Mode	R/W
Attribute	C

Bit	Description
[15:0]	LVDS I/O Data (VME boards only). It is the logic level of the corresponding nth LVDS I/O to read out or write, according to its direction (0x811C, bit[5:2]). A write operation sets the corresponding pin logic state if configured as output, while a read operation returns the logic state of the corresponding pin if configured as input. In case of Old LVDS I/O Features (0x811C, bit[8] = 0), the general purpose I/O option must be set (0x811C, bit[7:6] = 00). In case of New LVDS I/O Features (0x811C, bit[8] = 1), REGISTER mode must be set (0000 option in the 0x81A0 register).
[31:16]	Reserved.

Front Panel I/O Control

This register manages the front panel I/O connectors. Default value is 0x000000.

Address	0x811C
Mode	R/W
Attribute	C

Bit	Description
[0]	LEMO I/Os Electrical Level. This bit sets the electrical level of the front panel LEMO connectors: TRG-IN, TRG-OUT (GPO in case of DT and NIM boards), S-IN (GPI in case of DT and NIM boards). Options are: 0 = NIM I/O levels; 1 = TTL I/O levels.
[1]	TRG-OUT Enable (VME boards only). Enables the TRG-OUT LEMO front panel connector. Options are: 0 = enabled (default); 1 = high impedance. NOTE: this bit is reserved in case of DT and NIM boards.
[2]	LVDS I/O [3:0] Direction (VME boards only). Sets the direction of the signals on the first 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. NOTE: this bit is reserved in case of DT and NIM boards.
[3]	LVDS I/O [7:4] Direction (VME boards only). Sets the direction of the second 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. NOTE: this bit is reserved in case of DT and NIM boards.
[4]	LVDS I/O [11:8] Direction (VME boards only). Sets the direction of the third 4- pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. NOTE: this bit is reserved in case of DT and NIM boards.
[5]	LVDS I/O [15:12] Direction (VME boards only). Sets the direction of the fourth 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. NOTE: this bit is reserved in case of DT and NIM boards.
[7:6]	LVDS I/O Signal Configuration (VME boards only). Valid for old LVDS I/O features only (0x811C, bit[8] = 0). Options are: 00 = general purpose I/Os: LVDS I/Os work as register; I/O direction is configured through bit[5:2]; the logic level is read out or set in the 0x8118 register. 01 = programmed I/Os: direction and function of the LVDS signals are fixed (see the tabled signal pinout in the digitizer User Manual). 10 = pattern mode: LVDS signals are inputs and their value is written into the header PATTERN field of the event (see the digitizer User Manual); 11 = reserved. NOTE: these bits are reserved in case of DT and NIM boards.

[8]	LVDS I/O New Features Selection (VME boards only). Options are: 0 = LVDS old features; 1 = LVDS new features. The new features options can be configured through register 0x81A0. Please, refer to the User Manual for all details. NOTE: LVDS I/O New Features option is valid from motherboard firmware revision 3.8 on. NOTE: this bit is reserved in case of DT and NIM boards.
[9]	LVDS I/Os Pattern Latch Mode (VME boards only). Options are: 0 = Pattern (i.e. 16-pin LVDS status) is latched when the (internal) global trigger is sent to channels, in consequence of an external trigger. It accounts for post-trigger settings and input latching delays; 1 = Pattern (i.e. 16-pin LVDS status) is latched when an external trigger arrives. NOTE: this bit is reserved in case of DT and NIM boards.
[10]	TRG-IN control. The board trigger logic can be synchronized either with the edge of the TRG-IN signal, or with its whole duration. Note: this bit must be used in conjunction with bit[11] = 0. Options are: 0 = trigger is synchronized with the edge of the TRG-IN signal; 1 = trigger is synchronized with the whole duration of the TRG-IN signal.
[11]	TRG-IN to Mezzanines (channels). Options are: 0 = the TRG-IN signal is processed by the motherboard and sent to mezzanine (default). The trigger logic is then synchronized with TRG-IN; 1 = TRG-IN is directly sent to the mezzanines with no mother board processing nor delay. NOTE: if this bit is set to 1, then bit[10] is ignored.
[13:12]	Reserved.
[14]	Force TRG-OUT (GPO). This bit can force TRG-OUT (GPO in case of DT and NIM boards) test logical level if bit[15] = 1. Options are: 0 = Force TRG-OUT (GPO) to 0; 1 = Force TRG-OUT (GPO) to 1.
[15]	TRG-OUT (GPO) Mode. Options are: 0 = TRG-OUT (GPO) is an internal signal (according to bits[17:16]); 1= TRG-OUT (GPO) is a test logic level set via bit[14].
[17:16]	TRG-OUT (GPO) Mode Selection. Options are: 00 = Trigger: TRG-OUT/GPO propagates the internal trigger sources according to register 0x8110; 01 = Motherboard Probes: TRG-OUT/GPO is used to propagate signals of the motherboards according to bits[19:18]; 10 = Channel Probes: TRG-OUT/GPO is used to propagate signals of the mezzanines (Channel Signal Virtual Probe); 11 = S-IN (GPI) propagation.
[19:18]	Motherboard Virtual Probe Selection (to be propagated on TRG- OUT/GPO). Options are: 00 = RUN/delayedRUN: this is the RUN in case of ROC FPGA firmware rel. less than 4.12. This probe can be selected according to bit[20]. 01 = CLKOUT: this clock is synchronous with the sampling clock of the ADC and this option can be used to align the phase of the clocks in different boards; 10 = CLK Phase; 11 = BUSY/UNLOCK: this is the board BUSY in case of ROC FPGA firmware rel. 4.5 or lower. This probe can be selected according to bit[20].

[20]	According to bits[19:18], this bit selects the probe to be propagated on TRG- OUT . If bits[19:18] = 00, then bit[20] options are: 0 = RUN, the signal is active when the acquisition is running and it is synchronized with the start run. This option must be used to synchronize the start/stop of the acquisition through the TRG-OUT->TR-IN or TRG-OUT->S-IN (GPI) daisy chain. 1 = delayedRUN. This option can be used to debug the synchronization when the start/stop is propagated through the LVDS I/O (VME boards). If bits[19:18] = 11, then bit[20] options are: 0 = Board BUSY; 1 = PLL Lock Loss. NOTE: this bit is reserved in case of ROC FPGA firmware rel. 4.5 or lower. NOTE: this bit corresponds to BUSY/UNLOCK for ROC FPGA firmware rel. less than 4.12.
[22:21]	Pattern Configuration. Configures the information given by the 16-bit PATTERN field in the header of the event format (VME only). Option are: 00 = PATTERN: 16-bit pattern latched on the 16 LVDS signals as one trigger arrives (default); Other options are reserved.
[31:23]	Reserved.

Channel Enable Mask

This register enables/disables selected channels to participate in the event readout. Disabled channels are not operative.
WARNING: this register must not be modified while the acquisition is running.

Address	0x8120
Mode	R/W
Attribute	C

Bit	Description
[15:0]	Channel Enable Mask. Bit n can enable/disable channel n to participate in the event readout. Options are: 0 = disabled; 1 = enabled. NOTE: bits[15:8] are reserved in case of DT, NIM and 8-channel VME boards.
[31:16]	Reserved.

ROC FPGA Firmware Revision

This register contains the motherboard FPGA (ROC) firmware revision information.
The complete format is:
Firmware Revision = X.Y (16 lower bits)
Firmware Revision Date = Y/M/DD (16 higher bits)
EXAMPLE 1: revision 3.08, November 12th, 2007 is 0x7B120308.
EXAMPLE 2: revision 4.09, March 7th, 2016 is 0x03070409.
NOTE: the nibble code for the year makes this information to roll over each 16 years.

Address	0x8124
Mode	R
Attribute	C

Bit	Description
[7:0]	ROC Firmware Minor Revision Number (Y).
[15:8]	ROC Firmware Major Revision Number (X).
[31:16]	ROC Firmware Revision Date (Y/M/DD).

Event Stored

This register contains the number of events currently stored in the Output Buffer.
NOTE: the value of this register cannot exceed the maximum number of available buffers according to the register address 0x800C.

Address	0x812C
Mode	R
Attribute	C

Bit	Description
[31:0]	Number of the current events stored in the Output Buffer.

Voltage Level Mode Configuration

When the Voltage Level Mode is enabled (bit[2:0] = 100 (bin) of register 0x8144), this register sets the DAC value to be provided on the front panel MON/Sigma output LEMO connector: 1 LSB = 0.244 mV, terminated on 50 Ohm.
NOTE: this register is supported by VME boards only.

Address	0x8138
Mode	R/W
Attribute	C

Bit	Description
[11:0]	DAC Voltage Setting (VME boards only). The corresponding output value is multiplied by 0.244 mV.
[31:12]	Reserved

Software Clock Sync

At power-on, a Sync command is issued by the firmware to the ADCs to synchronize all of them to the clock of the board. In the standard operating, this command is not required to be repeated by the user.
A write access to this register (any value) forces the PLL to re-align all the clock outputs with the reference clock.
EXAMPLE: in case of Daisy chain clock distribution among VME boards, during the initialization and configuration, the reference clocks along the Daisy chain can be unstable and a temporary loss of lock may occur in the PLLs; although the lock is automatically recovered once the reference clocks return stable, it is not guaranteed that the phase shift returns to a known state. This command allows the board to restore the correct phase shift between the CLK-IN and the internal clocks.
NOTE: this register is supported by VME boards only.
NOTE: the command must be issued starting from the first to the last board in the clock chain.
NOTE: if a Sync command is intentionally issued, the user must consider that a new channels calibration procedure is needed for a correct board operating (see 0x809C).

Address	0x813C
Mode	W
Attribute	C

Bit	Description
[31:0]	Write whatever value to generate a Sync command.

Board Info

This register contains the specific information of the board, such as the digitizer family, the channel memory size and the channel density.

Address	0x8140
Mode	R
Attribute	C

Bit	Description
[7:0]	Digitizer Family Code. Options are: 0x0E = 725 digitizer family; 0x0B = 730 digitizer family.
[15:8]	Channel Memory Size Code. Options are: 0x01 = 640 kS acquisition memory per channel; 0x08 = 5.12 MS acquisition memory per channel.
[23:16]	Equipped Channels Number. Options are: 0x10 = 16 channels (VME boards); 0x08 = 8 channels (DT, NIM and 8-channel VME boards). NOTE: if this number is lower than the physical channels number, there could be a communication problem with some of the mezzanines.
[31:24]	Reserved.

Analog Monitor Mode

This register selects which output mode is provided on the MON/Sigma front panel LEMO connector.
NOTE: this register is supported by VME boards only.

Address	0x8144
Mode	R/W
Attribute	C

Bit	Description
[2:0]	Analog Monitor Mode (VME boards only). Options are: 000 = Trigger Majority mode; 001 = Test mode; 010 = reserved; 011 = Buffer Occupancy mode; 100 = Voltage Level mode; Others = reserved. Please, refer to the digitizer User Manual for a detailed description.
[31:3]	Reserved.

Event Size

This register contains the current available event size in 32-bit words. The value is updated after a complete readout of each event.

Address	0x814C
Mode	R
Attribute	C

Bit	Description
[31:0]	Event Size (32-bit words).

Fan Speed Control

This register manages the on-board fan speed in order to guarantee an appropriate cooling according to the internal temperature variations.
NOTE: from revision 4 of the motherboard PCB (see register 0xF04C of the Configuration ROM), the automatic fan speed control has been implemented, and it is supported by ROC FPGA firmware revision greater than 4.4 (see register 0x8124).
Independently of the revision, the user can set the fan speed high by setting bit[3] = 1. Setting bit[3] = 0 will restore the automatic control for revision 4 or higher, or the low fan speed in case of revisions lower than 4.
NOTE: this register is supported by Desktop (DT) boards only.

Address	0x8168
Mode	R/W
Attribute	C

Bit	Description
[2:0]	Reserved: Must be 0.
[3]	Fan Speed Mode. Options are: 0 = slow speed or automatic speed tuning; 1 = high speed.
[5:4]	Reserved: Must be 1.
[31:6]	Reserved: Must be 0.

Run/Start/Stop Delay

When the start of Run is given synchronously to several boards connected in Daisy chain, it is necessary to compensate for the delay in the propagation of the Start (or Stop) signal through the chain. This register sets the delay between the arrival of the Start signal at the input of the board (either on S-IN/GPI or TRG- IN) and the actual start of Run. The delay is usually zero for the last board in the chain and rises going backwards along the chain.

Address	0x8170
Mode	R/W
Attribute	C

Bit	Description
[7:0]	Delay value in steps of 16 ns for 730 and 32 ns for 725.
[31:8]	Reserved.

Board Failure Status

This register monitors a set of board errors. In case of a failure, bit[26] in the second word of the event format header is set to 1 during data readout (refer to the digitizer User Manual for event structure description). Reading at this register checks which kind of error occurred.
NOTE: in case of problems with the board, the user is recommended to contact CAEN for support.

Address	0x8178
Mode	R
Attribute	C

Bit	Description
[3:0]	Reserved.
[4]	PLL Lock Loss. Options are: 0 = no error; 1 = PLL Lock Loss occurred.
[5]	Temperature Failure. Options are: 0 = no error; 1 = Temperature Failure occurred (i.e. at least one channel is in over-temperature condition).
[6]	ADC Power Down. Options are: 0 = no error; 1 =ADC Power Down occurred (i.e. at least one channel is in power down mode due to an automatic over-temperature protection).
[31:7]	Reserved.

Front Panel LVDS I/O New Features

If the LVDS I/O new features are enabled (bit[8] = 1 of 0x811C), this register programs the functions of the front panel LVDS I/O 16-pin connector. It is possible to configure the LVDS I/O pins by group of four (4).
Options are:
1) 0000 = REGISTER, where the four LVDS I/O pins act as register (read/write according to the configured input/output option);
2) 0001 = TRIGGER, where each group of four LVDS I/O pins can be configured to receive an input trigger for each channel (DPP Firmware only), or to propagate out the trigger request;
3) 0010 = nBUSY/nVETO, where each group of four LVDS I/O pins can be configured as inputs (0 = nBusyIn, 1 = nVetoIn, 2 = nTrigger In, 3 = nRun In) or as outputs (0 = nBusy, 1 = nVeto, 2 = nTrigger Out, 3 = nRun);
4) 0011 = LEGACY, that is to say according to the old LVDS I/O configuration (i.e. ROC FPGA firmware revisions lower than 3.8), where the LVDS can be configured as 0 = nclear TTT, and 1 = 2 = 3 = reserved in case of input LVDS setting, while they can be configured as 0 = Busy, 1 = Data ready, 2 = Trigger, 3 = Run in case of output LVDS setting.
Please refer to the Front Panel LVDS I/Os section of the digitizer User Manual for detailed description.
NOTE: LVDS I/O new features are supported from ROC FPGA firmware revision 3.8 on.
NOTE: this register is supported by VME boards only.

Address	0x81A0
Mode	R/W
Attribute	C

Bit	Description
[3:0]	LVDS I/O pins[3:0] Configuration.
[7:4]	LVDS I/O pins[7:4] Configuration.
[11:8]	LVDS I/O pins[11:8] Configuration
[15:12]	LVDS I/O pins[15:12] Configuration.
[16]	This bit permits selecting whether the nTrigger signal, when configured as output (in nBusy/nVeto LVDS I/O mode), is a copy of the signal sent on the TRG- OUT connector or a copy of the acquisition common trigger. Options are: 0 = nTrigger output is a copy of TRG-OUT signal 1 = nTrigger output is a copy of the acquisition common trigger. NOTE: this bit is reserved for ROC FPGA firmware revisions less than 4.9.
[31:17]	Reserved.

Buffer Occupancy Gain

If the Buffer Occupancy Mode is selected (bit[2:0] = 011 of 0x8144), the LEMO MON/Sigma output connector provides a voltage level whose amplitude increases in fixed steps exactly with the number of events in the event buffer. Each step of the output voltage level is 0.976 mV. A gain can be applied to the step by this register. Allowed values are in the range [0:A]. The default value, 0, means no gain applied while writing 0xn means that the fixed step is $0.976*2^n$ mV.
NOTE: this register is supported from ROC FPGA firmware revision 4.9 on.
NOTE: this register is supported by VME boards only.

Address	0x81B4
Mode	R/W
Attribute	C

Bit	Description
[3:0]	Buffer Occupancy Gain.
[31:4]	Reserved.

Extended Veto Delay

This register is valid for VME boards only and set the duration of the Extended VetoIn signal for trigger inhibit on TRG-OUT when bit[12]=1 of 0x8100 register. Such function is useful in particular cases of synchronization of a multi-board system.
NOTE: This register is valid from ROC FPGA fw revision 4.16 on.

Address	0x81C4
Mode	R/W
Attribute	C

Bit	Description
[15:0]	Extended VetoIn duration value in units of Trigger Clock (8 ns for 730 and 16 ns for 725).
[31:16]	Reserved.

Readout Control

This register is mainly intended for VME boards, anyway some bits are applicable also for DT and NIM boards.

Address	0xEF00
Mode	R/W
Attribute	C

Bit	Description
[2:0]	VME Interrupt Level (VME boards only). Options are: 0 = VME interrupts are disabled; 1,..,7 = sets the VME interrupt level. NOTE: these bits are reserved in case of DT and NIM boards.
[3]	Optical Link Interrupt Enable. Options are: 0 = Optical Link interrupts are disabled; 1 = Optical Link interrupts are enabled.
[4]	VME Bus Error / Event Aligned Readout Enable (VME boards only). Options are: 0 = VME Bus Error / Event Aligned Readout disabled (the module sends a DTACK signal until the CPU inquires the module); 1 = VME Bus Error / Event Aligned Readout enabled (the module is enabled either to generate a Bus Error to finish a block transfer or during the empty buffer readout in D32). NOTE: this bit is reserved (must be 1) in case of DT and NIM boards.
[5]	VME Align64 Mode (VME boards only). Options are: 0 = 64-bit aligned readout mode disabled; 1 = 64-bit aligned readout mode enabled. NOTE: this bit is reserved (must be 0) in case of DT and NIM boards.
[6]	VME Base Address Relocation (VME boards only). Options are: 0 = Address Relocation disabled (VME Base Address is set by the on-board rotary switches); 1 = Address Relocation enabled (VME Base Address is set by register 0xEF0C). NOTE: this bit is reserved (must be 0) in case of DT and NIM boards.
[7]	Interrupt Release mode (VME boards only). Options are: 0 = Release On Register Access (RORA): this is the default mode, where interrupts are removed by disabling them either by setting VME Interrupt Level to 0 (VME Interrupts) or by setting Optical Link Interrupt Enable to 0; 1 = Release On Acknowledge (ROAK). Interrupts are automatically disabled at the end of a VME interrupt acknowledge cycle (INTACK cycle). NOTE: ROAK mode is supported only for VME interrupts. ROAK mode is not supported on interrupts generated over Optical Link. NOTE: this bit is reserved (must be 0) in case of DT and NIM boards.
[8]	Extended Block Transfer Enable (VME boards only). Selects the memory interval allocated for block transfers. Options are: 0 = Extended Block Transfer Space is disabled, and the block transfer region is a 4kB in the 0x0000 - 0x0FFC interval; 1 = Extended Block Transfer Space is enabled, and the block transfer is a 16 MB in the 0x00000000 - 0xFFFFFFFC interval. NOTE: in Extended mode, the board VME Base Address is only set via the on- board [31:28] rotary switches or bits[31:28] of register 0xEF10. NOTE: this register is reserved in case of DT and NIM boards.
[31:9]	Reserved.

Readout Status

This register contains information related to the readout.

Address	0xEF04
Mode	R
Attribute	C

Bit	Description
[0]	Event Ready. Indicates if there are events stored ready for readout. Options are: 0 = no data ready; 1 = event ready.
[1]	Reserved.
[2]	Bus Error (VME boards) / Slave-Terminated (DT/NIM boards) Flag. Options are: 0 = no Bus Error occurred (VME boards) or no terminated transfer (DT/NIM boards); 1 = a Bus Error occurred (VME boards) or one transfer has been terminated by the digitizer in consequence of an unsupported register access or block transfer prematurely terminated in event aligned readout (DT/NIM). NOTE: this bit is reset after register readout at 0xEF04.
[3]	VME FIFO Flag. Options are: 0 = VME FIFO not empty; 1 = VME FIFO is emplty.
[31:4]	Reserved.

Board ID

The meaning of this register depends on which VME crate it is inserted in.
In case of VME64X crate versions, this register can be accessed in read mode only and it contains the GEO address of the module picked from the backplane connectors; when CBLT is performed, the GEO address will be contained in the Board ID field of the Event header (see the User Manual for further details).
In case of other crate versions, this register can be accessed both in read and write mode, and it allows to write the correct GEO address (default setting = 0) of the module before CBLT operation. GEO address will be contained in the Board ID field of the Event header (see the User Manual for further details).
NOTE: this register is supported by VME boards only.

Address	0xEF08
Mode	R/W
Attribute	C

Bit	Description
[4:0]	GEO Address (VME boards only).
[31:5]	Reserved.

MCST Base Address and Control

This register configures the board for the VME Multicast Cycles.
NOTE: this register is supported by VME boards only.

Address	0xEF0C
Mode	R/W
Attribute	C

Bit	Description
[7:0]	These bits contain the most significant bits of the MCST/CBLT address of the module set via VME, that is the address used in MCST/CBLT operations.
[9:8]	Board Position in Daisy chain. Options are: 00 = board disabled; 01 = last board; 10 = first board; 11 = intermediate board.
[31:10]	Reserved.

Relocation Address

If address relocation is enabled through register 0xEF00 (bit[6] = 1), this register sets the VME Base Address of the module.
NOTE: this register is supported by VME boards only.

Address	0xEF10
Mode	R/W
Attribute	C

Bit	Description
[15:0]	These bits contain the A31...A16 bits of the address of the module. If bit[6] = 1 of 0xEF00, they set the VME Base Address of the module.
[31:16]	Reserved.

Interrupt Status/ID

This register contains the STATUS/ID that the module places on the VME data bus during the Interrupt Acknowledge cycle.
NOTE: this register is supported by VME boards only.

Address	0xEF14
Mode	R/W
Attribute	C

Bit	Description
[31:0]	STATUS/ID (VME boards only).

Interrupt Event Number

This register sets the number of events that causes an interrupt request. If interrupts are enabled, the module generates a request whenever it has stored in memory a Number of Events > INTERRUPT EVENT NUMBER.

Address	0xEF18
Mode	R/W
Attribute	C

Bit	Description
[9:0]	INTERRUPT EVENT NUMBER.
[31:10]	Reserved.

Max Number of Events per BLT

This register sets the maximum number of complete events which has to be transferred for each block transfer (via VME BLT/CBLT cycles, or block readout through USB or Optical Link).

Address	0xEF1C
Mode	R/W
Attribute	C

Bit	Description
[9:0]	MAX NUM EVENT PER BLT.
[31:10]	Reserved.

Scratch

This register can be used to write/read words for test purposes.

Address	0xEF20
Mode	R/W
Attribute	C

Bit	Description
[31:0]	SCRATCH.

Software Reset

All the digitizer registers can be set back to their default values on software reset command by writing any value at this register, or by system reset from backplane in case of VME boards.

Address	0xEF24
Mode	W
Attribute	C

Bit	Description
[31:0]	Whatever value written at this location issues a software reset. All registers are set to their default values (actual settings are lost).

Software Clear

All the digitizer internal memories are cleared:
- automatically by the firmware at the start of each run;
- on software command by writing at this register;
- by hardware (VME boards only) through the LVDS interface properly configured.

A clear command does not change the registers actual value, except for resetting the following registers:
- Event Stored;
- Event Size;
- Channel / Group n Buffer Occupancy.

This register resets also the trigger time stamp.

Address	0xEF28
Mode	W
Attribute	C

Bit	Description
[31:0]	Whatever value written at this location generates a software clear.

Configuration Reload

A write access of any value at this location causes a software reset, a reload of Configuration ROM parameters and a PLL reconfiguration.

Address	0xEF34
Mode	W
Attribute	C

Bit	Description
[31:0]	Write whatever value to perform a software reset, a reload of Configuration ROM parameters and a PLL reconfiguration.

Configuration ROM Checksum

This register contains information on 8-bit checksum of Configuration ROM space.

Address	0xF000
Mode	R
Attribute	C

Bit	Description
[7:0]	Checksum.
[31:8]	Reserved.

Configuration ROM Checksum Length BYTE 2

This register contains information on the third byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address	0xF004
Mode	R
Attribute	C

Bit	Description
[7:0]	Checksum Length: bits[23:16].
[31:8]	Reserved.

Configuration ROM Checksum Length BYTE 1

This register contains information on the second byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address	0xF008
Mode	R
Attribute	C

Bit	Description
[7:0]	Checksum Length: bits[15:8].
[31:8]	Reserved.

Configuration ROM Checksum Length BYTE 0

This register contains information on the first byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address	0xF00C
Mode	R
Attribute	C

Bit	Description
[7:0]	Checksum Length: bits[7:0].
[31:8]	Reserved.

Configuration ROM Constant BYTE 2

This register contains the third byte of the 3-byte constant.

Address	0xF010
Mode	R
Attribute	C

Bit	Description
[7:0]	Constant: bits[23:16] = 0x83.
[31:8]	Reserved.

Configuration ROM Constant BYTE 1

This register contains the second byte of the 3-byte constant.

Address	0xF014
Mode	R
Attribute	C

Bit	Description
[7:0]	Constant: bits[15:8] = 0x84.
[31:8]	Reserved.

Configuration ROM Constant BYTE 0

This register contains the first byte of the 3-byte constant.

Address	0xF018
Mode	R
Attribute	C

Bit	Description
[7:0]	Constant: bits[7:0] = 0x01.
[31:8]	Reserved.

Configuration ROM C Code

This register contains the ASCII C character code (identifies this as CR space).

Address	0xF01C
Mode	R
Attribute	C

Bit	Description
[7:0]	ASCII 'C' Character Code.
[31:8]	Reserved.

Configuration ROM R Code

This register contains the ASCII R character code (identifies this as CR space).

Address	0xF020
Mode	R
Attribute	C

Bit	Description
[7:0]	ASCII 'R' Character Code.
[31:8]	Reserved.

Configuration ROM IEEE OUI BYTE 2

This register contains information on the third byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Address	0xF024
Mode	R
Attribute	C

Bit	Description
[7:0]	IEEE OUI: bits[23:16].
[31:8]	Reserved.

Configuration ROM IEEE OUI BYTE 1

This register contains information on the second byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Address	0xF028
Mode	R
Attribute	C

Bit	Description
[7:0]	IEEE OUI: bits[15:8].
[31:8]	Reserved.

Configuration ROM IEEE OUI BYTE 0

This register contains information on the first byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Address	0xF02C
Mode	R
Attribute	C

Bit	Description
[7:0]	IEEE OUI: bits[7:0].
[31:8]	Reserved.

Configuration ROM Board Version

This register contains the board version information.

Address	0xF030
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Version Code. Options are: 0xF0 = V1725/VX1725/DT5725/N6725; 0xF1 = V1725B/VX1725B/DT5725B/N6725B; 0xF2 = V1725C/VX1725C; 0xF3 = V1725D/VX1725D; 0xF4 = V1725S/VX1725S/DT5725S/N6725S; 0xF5 = V1725BS/VX1725BS/DT5725BS/N6725BS; 0xF6 = V1725CS/VX1725CS; 0xF7 = V1725DS/VX1725DS; 0xC0 = V1730/VX1730/DT5730/N6730; 0xC1 = V1730B/VX1730B/DT5730B/N6730B; 0xC2 = V1730C/VX1730C; 0xC3 = V1730D/VX1730D; 0xC4 = V1730S/VX1730S/DT5730S/N6730S; 0xC5 = V1730BS/VX1730BS/DT5730BS/N6730BS; 0xC6 = V1730CS/VX1730CS; 0xC7 = V1730DS/VX1730DS.
[31:8]	Reserved.

Configuration ROM Board Form Factor

This register contains the information of the board form factor.

Address	0xF034
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Form Factor CAEN Code. Options are: 0x00 = VME64; 0x01 = VME64X; 0x02 = Desktop; 0x03 = NIM.
[31:8]	Reserved.

Configuration ROM Board ID BYTE 1

This register contains the MSB of the 2-byte board identifier.

Address	0xF038
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Number ID: bits[15:8].
[31:8]	Reserved.

Configuration ROM Board ID BYTE 0

This register contains the LSB information of the 2-byte board identifier.

Address	0xF03C
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Number ID: bits[7:0].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 3

This register contains information on the fourth byte of the 4-byte hardware revision.

Address	0xF040
Mode	R
Attribute	C

Bit	Description
[7:0]	PCB Revision: bits[31:24].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 2

This register contains information on the third byte of the 4-byte hardware revision.

Address	0xF044
Mode	R
Attribute	C

Bit	Description
[7:0]	PCB Revision: bits[23:16].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 1

This register contains information on the second byte of the 4-byte hardware revision.

Address	0xF048
Mode	R
Attribute	C

Bit	Description
[7:0]	PCB Revision: bits[15:8].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 0

This register contains information on the first byte of the 4-byte hardware revision.

Address	0xF04C
Mode	R
Attribute	C

Bit	Description
[7:0]	PCB Revision: bits[7:0].
[31:8]	Reserved.

Configuration ROM FLASH Type

This register contains information on which FLASH type (storing the FPGA firmware) is present on-board.

Address	0xF050
Mode	R
Attribute	C

Bit	Description
[7:0]	FLASH Type. Options are: 0x00 = 8 Mb FLASH; 0x01 = 32 Mb FLASH.
[31:8]	Reserved.

Configuration ROM Board Serial Number BYTE 1

This register contains information on the MSB of the board serial number.

Address	0xF080
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Serial Number: bits[15:8].
[31:8]	Reserved.

Configuration ROM Board Serial Number BYTE 0

This register contains information on the LSB of the board serial number.

Address	0xF084
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Serial Number: bits[7:0].
[31:8]	Reserved.

Configuration ROM VCXO Type

This register contains information on which type of VCXO is present on-board.

Address	0xF088
Mode	R
Attribute	C

Bit	Description
[31:0]	VCXO Type Code. Options for VME Digitizers are: 0 = AD9510 with 1 GHz; 1 = AD9510 with 500 MHz (not programmable); 2 = AD9510 with 500 MHz (programmable). Options for Desktop/NIM Digitizers are: Reserved (value = 0).

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