CAEN
Tools for Discovery

Electronic Instrumentation

User Manual UM5416

DT5790 DPP-PSD

Register Description and Data Format

Rev. 1 - May 5th, 2020

Purpose of this Manual

The User Manual contains the full description of the DPP-PSD firmware registers for 720 family series. The description is compliant with the DPP-PSD firmware revision **4.17_131.11**. For future release compatibility check in the firmware history files.

Change Document Record

Date	Revision	Changes
September 21st, 2016	00	Initial Release
May 5th, 2020	01	Added register Trigger Latency. Modified registers: Acquisition Control, Acquisition Status, Run/Start/Stop Delay, Board Failure Status, Readout Status, Aggregate Number per BLT. Added Chap. DPP-PSD Memory Organization

Symbols, abbreviated terms and notation

ADC	Analog-to-Digital Converter
AMC	ADC & Memory Controller
DAQ	Data Acquisition
DAC	Digital-to-Analog Converter
DC	Direct Current
DPP	Digital Pulse Processing
DPP-QDC	DPP for Charge to Digital Converter
DPP-PHA	DPP for Pulse Height Analysis
DPP-PSD	DPP for Pulse Shape Discrimination
LVDS	Low-Voltage Differential Signal
ROC	ReadOut Controller
USB	Universal Serial Bus

Reference Documents

[RD1] UM1935 - CAENDigitizer User & Reference Manual.

[RD2] GD2827 - How to make coincidences with CAEN digitizers.

[RD3] UM5960 - CoMPASS User Manual.

All CAEN documents can be downloaded at:
`www.caen.it/support-services/documentation-area`

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1 Registers and Data Format

All registers described in the User Manual are 32-bit wide. In case of VME access, **A24** and **A32** addressing mode can be used.

Register Address Map

The table below reports the complete list of registers that can be accessed by the user. The register names in the first column can be clicked to be redirected to the relevant register description. The register address is reported on the second column as a hex value. The third column indicates the allowed register access mode, where:

R	**Read only**. The register can be accessed in read only mode.
W	**Write only**. The register can be accessed in write only mode.
R/W	**Read and write**. The register can be accessed both in read and write mode.

According to the attribute reported in the fourth column, the following choices are available:

I **Individual register**. This kind of register has N instances, where N is the total number of channels in the board. Individual registers can be written either in single mode (individual setting) or broadcast (simultaneous write access to all channels). Read command must be individual.
Single access can be performed at address 0x1nXY, where n is the channel number, while broadcast write can be performed at the address 0x80XY. For example:

- access to address 0x1570 to read/write register 0x1n70 for channel 5 of the board;
- to write the same value for all channels in the board, access to 0x8070 (broadcast write). To read the corresponding value, access to the individual address 0x1n70.

C **Common register**. Register with this attribute has a single instance, therefore read and write access can be performed at address 0x80XY only.

H **HV register**. In case of 780 series and DT5790 some registers manage the HV channels of the boards. Read and write access can be performed at address 0x1nXY only, where n=2 corresponds to the HV channel 0 and n=3 corresponds to the HV channel 1.

Register Name	Address	Mode	Attribute
High Voltage VSet	0x1n20 (n=2 for HV-ch0, n=3 for HV-ch1)	R/W	H
High Voltage ISet	0x1n24 (n=2 for HV-ch0, n=3 for HV-ch1)	R/W	H
High Voltage Ramp Up	0x1n28 (n=2 for HV-ch0, n=3 for HV-ch1)	R/W	H
High Voltage Ramp Down	0x1n2C (n=2 for HV-ch0, n=3 for HV- ch1)	R/W	H
High Voltage VMax	0x1n30 (n=2 for HV-ch0, n=3 for HV-ch1)	R/W	H
High Voltage Control	0x1n34 (n=2 for HV-ch0, n=3 for HV-ch1)	R/W	H
High Voltage Status/A639 Firmware Release	0x1n38 (n=2 for HV- ch0, n=3 for HV-ch1)	R	H
High Voltage VMon/Analog In	0x1n40 (n=2 for HV-ch0, n=3 for HV-ch1)	R	H
High Voltage IMon/Temperature In	0x1n44 (n=2 for HV-ch0, n=3 for HV-ch1)	R	H
Short Gate Width	0x1n54, 0x8054	R/W	I
Long Gate Width	0x1n58, 0x8058	R/W	I
Gate Offset	0x1n5C, 0x805C	R/W	I
Trigger Threshold	0x1n60, 0x8060	R/W	I
Fixed Baseline	0x1n64, 0x8064	R/W	I
Trigger Latency	0x1n6C, 0x8n6C	R/W	I
Shaped Trigger Width	0x1n70, 0x8070	R/W	I
Threshold for the PSD cut	0x1n78, 0x8078	R/W	I
PUR-GAP Threshold	0x1n7C, 0x807C	R/W	I
DPP Algorithm Control	0x1n80, 0x8080	R/W	I
Channel n Status	0x1n88	R	I
AMC Firmware Revision	0x1n8C	R	I
DC Offset	0x1n98, 0x8098	R/W	I
Board Configuration	0x8000, 0x8004 (BitSet), 0x8008 (BitClear)	R/W	C
Aggregate Organization	0x800C	R/W	C
Record Length	0x8020	R/W	C
Number of Events per Aggregate	0x8034	R/W	C
Pre Trigger	0x8038	R/W	C
Trigger Hold-Off Width	0x8074	R/W	C
Acquisition Control	0x8100	R/W	C
Acquisition Status	0x8104	R	C
Software Trigger	0x8108	W	C
Global Trigger Mask	0x810C	R/W	C
Front Panel TRG-OUT (GPO) Enable Mask	0x8110	R/W	C
Front Panel I/O Control	0x811C	R/W	C
Channel Enable Mask	0x8120	R/W	C
ROC FPGA Firmware Revision	0x8124	R	C
Board Info	0x8140	R	C
Event Size	0x814C	R	C
Fan Speed Control	0x8168	R/W	C
Run/Start/Stop Delay	0x8170	R/W	C
Board Failure Status	0x8178	R	C
Disable External Trigger	0x817C	R/W	C
Trigger Validation Mask	0x8188 (ch0), 0x818C (ch1)	R/W	I
Readout Control	0xEF00	R/W	C
Readout Status	0xEF04	R	C
Aggregate Number per BLT	0xEF1C	R/W	C

Scratch	0xEF20	R/W	C
Software Reset	0xEF24	W	C
Software Clear	0xEF28	W	C
Configuration Reload	0xEF34	W	C
Configuration ROM Checksum	0xF000	R	C
Configuration ROM Checksum Length BYTE 2	0xF004	R	C
Configuration ROM Checksum Length BYTE 1	0xF008	R	C
Configuration ROM Checksum Length BYTE 0	0xF00C	R	C
Configuration ROM Constant BYTE 2	0xF010	R	C
Configuration ROM Constant BYTE 1	0xF014	R	C
Configuration ROM Constant BYTE 0	0xF018	R	C
Configuration ROM C Code	0xF01C	R	C
Configuration ROM R Code	0xF020	R	C
Configuration ROM IEEE OUI BYTE 2	0xF024	R	C
Configuration ROM IEEE OUI BYTE 1	0xF028	R	C
Configuration ROM IEEE OUI BYTE 0	0xF02C	R	C
Configuration ROM Board Version	0xF030	R	C
Configuration ROM Board Form Factor	0xF034	R	C
Configuration ROM Board ID BYTE 1	0xF038	R	C
Configuration ROM Board ID BYTE 0	0xF03C	R	C
Configuration ROM PCB Revision BYTE 3	0xF040	R	C
Configuration ROM PCB Revision BYTE 2	0xF044	R	C
Configuration ROM PCB Revision BYTE 1	0xF048	R	C
Configuration ROM PCB Revision BYTE 0	0xF04C	R	C
Configuration ROM FLASH Type	0xF050	R	C
Configuration ROM Board Serial Number BYTE 1	0xF080	R	C
Configuration ROM Board Serial Number BYTE 0	0xF084	R	C
Configuration ROM VCXO Type	0xF088	R	C

High Voltage VSet

Set the channel voltage value (V)

Address	0x1n20 (n=2 for HV-ch0, n=3 for HV-ch1)
Mode	R/W
Attribute	H

Bit	Description
[15:0]	Channel voltage value in steps of 0.1 V. For example to set 2500 V write 25000.
[31:16]	Reserved

High Voltage ISet

Set the maximum current limit that can be supplied by a channel

Address	0x1n24 (n=2 for HV-ch0, n=3 for HV-ch1)
Mode	R/W
Attribute	H

Bit	Description
[15:0]	Set the maximum current in steps of 10 nA (780 series) and 50 nA (DT5790). For example to set 2000 uA, write 40000 for DT5790 and 200000 for 780 series.
[31:16]	Reserved

High Voltage Ramp Up

Set the ramp up voltage value in V/s

Address	0x1n28 (n=2 for HV-ch0, n=3 for HV-ch1)
Mode	R/W
Attribute	H

Bit	Description
[8:0]	Ramp up in V/s.
[31:9]	Reserved

High Voltage Ramp Down

Set the ramp down voltage value in V/s

Address	0x1n2C (n=2 for HV-ch0, n=3 for HV-ch1)
Mode	R/W
Attribute	H

Bit	Description
[8:0]	Ramp down in V/s.
[31:9]	Reserved

High Voltage VMax

VMax is the hardware value that can be programmed by the user to limit the maximum voltage of a channel. If a value VSet > VMax is erroneously programmed, the HV channels supplies up to VMax and marks bit[6] of register High Voltage Status 0x1n38.

Address	0x1n30 (n=2 for HV-ch0, n=3 for HV-ch1)
Mode	R/W
Attribute	H

Bit	Description
[7:0]	Maximum voltage value in steps of 20 V for 780 series and DT5790, and 2 V for 780SD boards. Note: the VMax resolution of 2 V is supported for HV firmware release greater than 2.2. For HV firmware release less than 2.2 the VMax resolution is 20 V.
[31:8]	Reserved

High Voltage Control

This register manages the high voltage power and monitor mode

Address	0x1n34 (n=2 for HV-ch0, n=3 for HV-ch1)
Mode	R/W
Attribute	H

Bit	Description
[0]	Manages the Power ON/OFF of the HV channel. Options are: 0: HV channel OFF; 1: HV channel ON.
[1]	Manages how the channel shuts down. This setting applies both when the user shuts the channel down and when the channel automatically shuts down due to an alarm (see register High Voltage Status 0x1n38). Options are: 0: kill mode, the HV channel shuts down instantaneously; 1: ramp mode, the HV channel shuts down with a rate of V/s as defined by the HV Ramp Down register, 0x1n2C.
[6:2]	Reserved
[7]	Manages the monitor mode of the HV channel. Options are: 0: Register 0x1n40 used to monitor the HV Channel VMon, register 0x1n44 used to monitor the HV Channel IMon, register 0x1n38 used to monitor the HV Channel Status; 1: Register 0x1n40 used to monitor the Analog In, register 0x1n44 used to monitor the Temperature In, register 0x1n38 used to monitor the A639 Firmware Release.
[31:8]	Reserved

High Voltage Status/A639 Firmware Release

According to the monitor mode value (bit[7] of register High Voltage Control 0x1n34) this register corresponds to:
1. monitor mode = 0, HV channel status (see the bit description for more details). NOTE: in case of bit[3], bit[9], bit[10] or bit[14] = 1 the HV channel is turned off according to Power Down Mode (see HV Channel Control register, 0x1n34);
2. monitor mode = 1, A639 firmware release. For example, for a firmware release 1.03, the register value is 0x103, where 1 corresponds to the register word high byte, and 3 corresponds to the register word low byte.

Address	0x1n38 (n=2 for HV-ch0, n=3 for HV-ch1)
Mode	R
Attribute	H

Bit	Description
[0]	1 = HV power ON
[1]	1 = HV channel rump up
[2]	1 = HV channel rump down
[3]	1 = HV channel is in Over Current (IMon > ISet)
[4]	1 = HV channel is in Over Voltage (VMon > VSet + 2%)
[5]	1 = HV channel is in Under Voltage (VMon < VSet - 2%)
[6]	1 = HV channel is over Maximum Voltage (Vout > VMax)
[7]	1 = HV channel is over Maximum Current (IMon > hardware maximum IOut)
[8]	1 = Temperature warning. The temperature of the HV channel is greater than 80°C.
[9]	1 = Over Temperature. The temperature of the HV channel is greater than 125°C.
[10]	1 = HV channel is disabled for an active external inhibit.
[11]	1 = Calibration error. There is a calibration error on the HV channel.
[12]	1 = Alarm Reset. The HV channel is resetting the alarms.
[13]	1 = HV channel is shutting down
[14]	1 = Maximum Power. The HV output power is greater than 4 W.
[15]	1 = Fan speed high
[31:16]	Reserved

High Voltage VMon/Analog In

According to the monitor mode value (bit[7] of register High Voltage Control 0x1n34) this register corresponds to:
1. monitor mode = 0, HV channel VMon;
2. monitor mode = 1, voltage between Pin 3 (EXT_ANALOG) and Pin 1 (GND) of the DB9 connector related to the selected channel.

Address	0x1n40 (n=2 for HV-ch0, n=3 for HV-ch1)
Mode	R
Attribute	H

Bit	Description
[15:0]	If monitor mode = 0, these bits read the HV channel VMon. VMon is equal to the content of the register multiplied by the resolution of 0.1 V. For example, if the register value is 10238, VMon = 1023.8 V. If monitor mode = 1, these bits read the voltage between Pin 3 (EXT_ANALOG) and Pin 1 (GND) of the DB9 connector related to the selected channel. The voltage value is equal to the content of the register multiplied by the inverse of the resolution of 0.001 V.
[31:16]	Reserved

High Voltage IMon/Temperature In

According to the monitor mode value (bit[7] of register High Voltage Control 0x1n34) this register corresponds to:
1. monitor mode = 0, this register provides the monitored current value;
2. monitor mode = 1, this register is used to read the value of the resistance between Pin 8 (EXT_TEMP) and Pin 1 (GND) of the DB9 connector related to the selected channel.

Address	0x1n44 (n=2 for HV-ch0, n=3 for HV-ch1)
Mode	R
Attribute	H

Bit	Description
[15:0]	If monitor mode = 0, these bits provide the monitored current value. The value of Imon is equal to the content of the register multiplied by the resolution (780 series: 10 nA; DT5790: 50 nA). For example, if Imon Reg = 10238 then IMon = 102.38 uA (DT5780). If Imon Reg = 10238 then IMon = 511.9 uA (DT5790). If Monitor Mode = 1, these bits are used to read the value of the resistance between Pin 8 (EXT_TEMP) and Pin 1 (GND) of the DB9 connector related to the selected channel. The resistance value is that of a temperature probe PT100 or PT1000. The resistance value is equal to the content of the register multiplied by the resolution of 0.1 Ohm. For example, if Reg value = 1234, then the resistance value = 123.4 Ohm.
[31:16]	Reserved

Short Gate Width

Sets the Short Gate width for the charge integration of the fast component in the Pulse Shape Discrimination

Address	0x1n54, 0x8054
Mode	R/W
Attribute	I

Bit	Description
[9:0]	Number of samples for the Short Gate width. Each sample corresponds to 4 ns.
[31:10]	Reserved

Long Gate Width

Sets the Long Gate width for the charge integration of the slow component in the Pulse Shape Discrimination. The Long integration Gate is also used for the energy spectra calculation

Address	0x1n58, 0x8058
Mode	R/W
Attribute	I

Bit	Description
[13:0]	Number of samples for the Long Gate width. Each sample corresponds to 4 ns.
[31:14]	Reserved

Gate Offset

To correctly integrate the input pulse, the integration Gate starts before the trigger position. The Gate Offset defines how many samples the Gate starts before the trigger.

Address	0x1n5C, 0x805C
Mode	R/W
Attribute	I

Bit	Description
[7:0]	Number of samples of the Gate Offset. Each sample corresponds to 4 ns.
[31:8]	Reserved

Trigger Threshold

Sets the Trigger Threshold value for the Leading Edge discrimination

Address	0x1n60, 0x8060
Mode	R/W
Attribute	I

Bit	Description
[11:0]	Set the number of LSB counts for the Trigger Threshold, where 1 LSB = 0.49 mV. The threshold is referred to the baseline level.
[31:12]	Reserved

Fixed Baseline

The baseline calculation can be performed either dynamically or statically. In the first case the user can set the samples of the moving average window through register 0x1n80. In the latter case the user must disable the automatic baseline calculation through bits[22:20] of register 0x1n80 and set the desired value of fixed baseline through this register. The baseline value then remains constant for the whole acquisition.
Note: This register is ignored in case of dynamic calculation.

Address	0x1n64, 0x8064
Mode	R/W
Attribute	I

Bit	Description
[11:0]	Value of Fixed Baseline in LSB counts
[31:12]	Reserved

Trigger Latency

This register allows the user to set a time window (latency) to be added to the Shaped Trigger Width (i.e. the lenght of the correlation window) required to take into account the latency in the trigger propagation from the piggyback to the motherboard when setting coincidence/anticoincidence between the digitizer channels.
Mandatory values are:
- 0x9 for the x720 (DT5790) and x751 series
- 0x2 for the x725 and x730 series when setting coincidence/anticoincidence within the same channel couple
- 0x9 for the x725 and x730 series when setting coincidence/anticoincidence between channels belonging to different couples.

Address	0x1n6C, 0x8n6C
Mode	R/W
Attribute	I

Bit	Description
[9:0]	Value of the latency in trigger clock cycles, 8 ns step.
[31:10]	Reserved

Shaped Trigger Width

The Shaped Trigger is a logic signal of programmable width generated by a channel in correspondence to its local self-trigger (that is the output of the leading edge discriminator). It is used to propagate the trigger to the other channels of the board and to other external boards, as well as to feed the coincidence trigger logic.

Address	0x1n70, 0x8070
Mode	R/W
Attribute	I

Bit	Description
[9:0]	Shaped Trigger width in steps of 8 ns.
[31:10]	Reserved

Threshold for the PSD cut

Sets the PSD threshold to online select events according to their PSD value. PSD ranges from 0 to 1.

Address	0x1n78, 0x8078
Mode	R/W
Attribute	I

Bit	Description
[9:0]	Set the PSD threshold value. The desired value has to be multiplied by 1024. For example for a PSD threshold of 0.12, write 122 (= 0.12 * 1024). Set bits[28:27] of register 0x1n80 to enable the cut on gamma or neutron respectively.
[31:10]	Reserved

PUR-GAP Threshold

A pile-up event is detected when there is a situation of ”peak-valley-peak” inside the same gate. The gap between the valley and the peak can be programmed through this register. Refer to the CoMPASS User Manual for additional details.

Address	0x1n7C, 0x807C
Mode	R/W
Attribute	I

Bit	Description
[11:0]	PUR-GAP value in LSB units, where 1 LSB = 0.49 mV.
[31:12]	Reserved

DPP Algorithm Control

Management of the DPP algorithm features

Address	0x1n80, 0x8080
Mode	R/W
Attribute	I

Bit	Description
[1:0]	Charge Sensitivity: defines how many fC of charge correspond to one channel of the energy spectrum. Options are: 00: 40 fC; 01: 160 fC; 10: 640 fC; 11: 2.56 pC.
[3:2]	Reserved
[4]	Charge Pedestal: when enabled a fixed value of 1024 is added to the charge. This feature is useful in case of energies close to zero.
[5]	Trigger Counting. Options are: 0 (default value): the shaped trigger used for TRG-OUT and coincidences reflects only the accepted self-triggers, i.e. the real events saved into memory; 1: the shaped trigger used for TRG-OUT and coincidences reflects all the self- triggers, even those of rejected events (for example consecutive events on the same gate, or events occurring during the board busy condition).
[6]	Reserved
[7]	Enable Extended Time Stamp. When this option is enabled, additional 15 bits of Time Stamp are recorded into the EXTRAS word of the Event Data format. Refer to the CoMPASS User Manual for additional details. Also bit[17] of register 0x8000 should be enabled. Options are: 0: disabled; 1: enabled.
[8]	Internal Test Pulse. It is possible to enable an internal test pulse for debugging purposes. The ADC counts are replaced with the built-in pulse emulator. Options are: 0: disabled. 1: enabled.
[10:9]	Test Pulse Rate. Set the rate of the built-in test pulse emulator. Options are: 00: 1 kHz; 01: 10 kHz; 10: 100 kHz; 11: 1 MHz.
[15:11]	Reserved
[16]	Pulse Polarity. Options are: 0: positive pulse; 1: negative pulse.
[17]	Reserved
[19:18]	Trigger Mode. Options are: 00: Normal mode. Each channel can self-trigger independently from the other channels. 01: Coincidence mode. Each channel saves the event only when a validation signal occurs inside the shaped trigger coincidence window. 10: Reserved. 11: Anti-coincidence mode. Each channel saves the event only when no validation signal occurs inside the shaped trigger coincidence window.
[22:20]	Baseline Mean. Sets the number of events for the baseline mean calculation. Options are: 000: Fixed: the baseline value is fixed to the value set in register 0x1n64; 001: 8 samples; 010: 32 samples; 011: 128 samples; other options are reserved.
[23]	Reserved.

[24]	Disable Self Trigger. When disabled, the self-trigger is still propagated to the mother board for coincidence logic and TRG-OUT front panel connector, though it is not used by the channel to acquire the event. Options are: 0: self-trigger used to acquire and propagated to the trigger logic; 1: self-trigger only propagated to the trigger logic.
[25]	Reserved
[26]	Pile-Up Rejection. Events flagged as pile-up are completely rejected and they are no more available for readout. See the CoMPASS User Manual for additional details. Options are: 0: disabled; 1: enabled.
[27]	Enable PSD cut below threshold (to cut on gammas)
[28]	Enable PSD cut above threshold (to cut on neutrons).
[31:29]	Reserved

Channel n Status

This register contains the status information of channel n.

Address	0x1n88
Mode	R
Attribute	I

Bit	Description
[1:0]	Reserved.
[2]	If 1, the SPI bus is busy.
[31:3]	Reserved.

AMC Firmware Revision

Returns the DPP firmware revision (mezzanine level).
To control the mother board firmware revision see register 0x8124.
For example: if the register value is 0xC3218303:
- Firmware Code and Firmware Revision are 131.3;
- Build Day is 21;
- Build Month is March;
- Build Year is 2012.

NOTE: since 2016 the build year started again from 0.

Address	0x1n8C
Mode	R
Attribute	I

Bit	Description
[7:0]	Firmware revision number.
[15:8]	Firmware DPP code. Each DPP firmware has a unique code.
[19:16]	Build Day (lower digit).
[23:20]	Build Day (upper digit).
[27:24]	Build Month. For example: 3 means March, 12 is December.
[31:28]	Build Year. For example: 0 means 2000, 12 means 2012. NOTE: since 2016 the build year started again from 0.

DC Offset

This register allows to adjust the baseline position (i.e. the 0 Volt) of the input signal on the ADC scale. The ADC scale ranges from 0 to 2^{NBit} - 1, where NBit is the number of bits of the on-board ADC. The DAC controlling the DC Offset has 16 bits, i.e. it goes from 0 to 65535 independently from the NBit value and the board type.
Typically a DC Offset value of 32K (DAC mid-scale) corresponds to about the ADC mid-scale. Increasing values of DC Offset make the baseline decrease. The range of the DAC is about 5% (typ.) larger than the ADC range, hence DAC settings close to 0 and 64K correspond to ADC respectively over and under range.
WARNING: before writing this register, it is necessary to check that bit[2] = 0 at 0x1n88, otherwise the writing process will not run properly!

Address	0x1n98, 0x8098
Mode	R/W
Attribute	I

Bit	Description
[15:0]	DC Offset value in DAC LSB unit.
[31:16]	Reserved.

Board Configuration

This register contains general settings for the board configuration.

Address 0x8000, 0x8004 (BitSet), 0x8008 (BitClear)
Mode R/W
Attribute C

Bit	Description
[0]	Reserved: must be 0.
[1]	Reserved: must be 0
[2]	Trigger Propagation: enables the propagation of the individual trigger from mother board individual trigger logic to the mezzanine. This is required in case of coincidence trigger mode
[3]	Reserved: must be 0
[4]	Reserved: must be 1.
[7:5]	Reserved: must be 0
[8]	Individual trigger: must be 1
[10:9]	Reserved: must be 0
[11]	Dual Trace: in oscilloscope or mixed mode, it is possible to plot two different waveforms, i.e. the Input and the Baseline. When the dual trace is enabled, the samples of the two signals are interleaved, thus each waveform is recorded at half of the ADC frequency. When disabled only the Input is recorded at the ADC frequency. Options are: 0: disabled; 1: enabled.
[15:12]	Reserved
[16]	Waveform Recording: enables the data recording of the waveform. The user must define the number of samples to be saved in the Record Length (register 0x1n20). According to the Analog Probe option one or two waveforms are saved. Options are: 0: disabled; 1: enabled.
[17]	Extras Recording: when enabled the EXTRAS word is saved into the event data. Refer to the "Channel Aggregate Data Format" chapter below for more details about the EXTRAS word. Options are: 0: disabled; 1: enabled.
[18]	Time Stamp Recording: enables the recording of the time stamp in the Channel Aggregate Data format. Options are: 0: disabled; 1: enabled.
[19]	Charge Recording: enables the recording of the charge in the Channel Aggregate Data format. Options are: 0: disabled; 1: enabled.
[22:20]	Reserved

[25:23]	Digital Virtual Probe 3: when the mixed or oscilloscope mode are enabled, the following digital virtual probes can be selected: 000 = "External Trigger"; 001 = "Over Threshold", digital signal that is 1 when the input signal is over the requested threshold; 010 = "Shaped TRG", logic signal of programmable width generated by a channel in correspondence with its local self- trigger. It is used to propagate the trigger to the other channels of the board and to other external boards, as well as to feed the coincidence trigger logic; 011 = "TRG Val. Acceptance Win.", logic signal corresponding to the time window where the coincidence validation is accepted. The validation enables the event dump into the memory; 100 = "Pile Up", logic pulse set to 1 when a pile-up event occurred; 101 = "Coincidence", logic pulse set to 1 when a coincidence occurred; 110 = Reserved; 111 = Reserved
[28:26]	Digital Virtual Probe 4: when the mixed or oscilloscope mode are enabled, the following digital virtual probes can be selected: 000 = "Short Gate"; 001 = "Over Threshold", digital signal that is 1 when the input signal is over the requested threshold; 010 = "TRG Validation", digital signal that is 1 when a coincidence validation signal comes from the mother board FPGA; 011 = "TRG HoldOff", logic signal of programmable width generated by a channel in correspondence with its local self- trigger. Other triggers are inhibited for the overall Trigger Hold-Off duration; 100 = "Pile Up", logic pulse set to 1 when a pile up event occurred; 101 = "Coincidence", logic pulse set to 1 when a coincidence occurred; 110 = Reserved; 111 = Reserved.
[31:29]	Reserved: must be 0

Aggregate Organization

The internal memory of the digitizer can be divided into a programmable number of aggregates, where each aggregate contains a specific number of events. This register defines how many aggregates can be contained in the memory. Note: this register must not be modified while the acquisition is running.

Address	0x800C
Mode	R/W
Attribute	C

Bit	Description
[3:0]	Aggregate Organization Nb: the number of aggregates is equal to N_aggr = 2^{Nb}. The corresponding values of Nb and N_aggr are: Nb: N_aggr 0x0 - 0x1: Not used 0x2 : 4 0x3 : 8 0x4 : 16 0x5 : 32 0x6 : 64 0x7 : 128 0x8 : 256 0x9 : 512 0xA : 1024
[31:4]	Reserved: must be 0

Record Length

Sets the record length for the waveform acquisition

Address	0x8020
Mode	R/W
Attribute	C

Bit	Description
[11:0]	Number of samples in the waveform according to the formula Ns = N * 8, where Ns is the record length and N is the register value. For example, write N = 3 to acquire 24 samples. Each sample corresponds to 4 ns.
[31:12]	Reserved

Number of Events per Aggregate

Each channel has a fixed amount of RAM memory to save the events. The memory is divided into a programmable number of buffer, called ”aggregates”, whose number of events can be programmed by this register.

Address	0x8034
Mode	R/W
Attribute	C

Bit	Description
[9:0]	Number of events per aggregate. Maximum value is 1023.
[31:10]	Reserved

Pre Trigger

The Pre Trigger defines the number of samples before the trigger in the waveform saved into memory.

Address	0x8038
Mode	R/W
Attribute	C

Bit	Description
[8:0]	Number of samples Ns of the Pre Trigger width. The value is expressed in steps of sampling frequency (4 ns). NOTE: the Pre Trigger value must be greater than the Gate Offset value by at least 32 ns.
[31:9]	Reserved

Trigger Hold-Off Width

The Trigger Hold-Off is a logic signal of programmable width generated by a channel in correspondence with its local self- trigger. Other triggers are inhibited for the overall Trigger Hold-Off duration

Address	0x8074
Mode	R/W
Attribute	C

Bit	Description
[9:0]	Set the Trigger Hold-Off width in steps of 8ns.
[31:10]	Reserved.

Acquisition Control

This register manages the acquisition settings.

Address 0x8100
Mode R/W
Attribute C

Bit	Description
[1:0]	Start/Stop Mode Selection (default value is 00). Options are: 00 = SW CONTROLLED. Start/stop of the run takes place on software command by setting/resetting bit[2] of this register; 01 = S-IN/GPI CONTROLLED (S-IN for VME, GPI for Desktop/NIM). If the acquisition is armed (i.e. bit[2] = 1), then the acquisition starts when S-IN/GPI is asserted and stops when S-IN/GPI returns inactive. If bit[2] = 0, the acquisition is always off; 10 = FIRST TRIGGER CONTROLLED. If the acquisition is armed (i.e. bit[2] = 1), then the run starts on the first trigger pulse (rising edge on TRG-IN); this pulse is not used as input trigger, while actual triggers start from the second pulse. The stop of Run must be SW controlled (i.e. bit[2] = 0); 11 = LVDS CONTROLLED (VME only). It is like option 01 but using LVDS (RUN) instead of S-IN. The LVDS can be set using registers 0x811C and 0x81A0.
[2]	Acquisition Start/Arm (default value is 0). When bits[1:0] = 00, this bit acts as a Run Start/Stop. When bits[1:0] = 01, 10, 11, this bit arms the acquisition and the actual Start/Stop is controlled by an external signal. Options are: 0 = Acquisition STOP (if bits[1:0]=00); Acquisition DISARMED (others); 1 = Acquisition RUN (if bits[1:0]=00); Acquisition ARMED (others).
[3]	Reserved.
[5:4]	Reserved
[6]	PLL Reference Clock Source (Desktop/NIM only). Default value is 0. Options are: 0 = internal oscillator (50 MHz); 1 = external clock from front panel CLK-IN connector. NOTE: this bit is reserved in case of VME boards.
[31:7]	Reserved

Acquisition Status

This register monitors a set of conditions related to the acquisition status.

Address 0x8104
Mode R
Attribute C

Bit	Description
[1:0]	Reserved.
[2]	Acquisition Status. It reflects the status of the acquisition and drivers the front panel 'RUN' LED. Options are: 0 = acquisition is stopped ('RUN' is off); 1 = acquisition is running ('RUN' lits).
[3]	Event Ready. Indicates if any events are available for readout. Options are: 0 = no event is available for readout; 1 = at least one event is available for readout. NOTE: the status of this bit must be considered when managing the readout from the digitizer.
[4]	Event Full. Indicates if at least one channel has reached the FULL condition. Options are: 0 = no channel has reached the FULL condition; 1 = the maximum number of events to be read is reached.
[5]	Clock Source. Indicates the clock source status. Options are: 0 = internal (PLL uses the internal 50 MHz oscillator as reference); 1 = external (PLL uses the external clock on CLK-IN connector as reference).
[6]	Reserved.
[7]	PLL Unlock Detect. This bit flags a PLL unlock condition. Options are: 0 = PLL has had an unlock condition since the last register read access; 1 = PLL has not had any unlock condition since the last register read access. NOTE: flag can be restored to 1 via read access to register 0xEF04.
[8]	Board Ready. This flag indicates if the board is ready for acquisition (PLL and ADCs are correctly synchronized). Options are: 0 = board is not ready to start the acquisition; 1 = board is ready to start the acquisition. NOTE: this bit should be checked after software reset to ensure that the board will enter immediately in run mode after the RUN mode setting; otherwise, a latency between RUN mode setting and Acquisition start might occur.
[14:9]	Reserved.
[15]	S-IN (VME boards) or GPI (DT/NIM boards) Status. Reads the current logical level on S-IN (GPI) front panel connector.
[16]	TRG-IN Status. Reads the current logical level on TRG-IN front panel connector.
[31:17]	Reserved.

Software Trigger

Writing this register causes a software trigger generation which is propagated to all the enabled channels of the board.

Address	0x8108
Mode	W
Attribute	C

Bit	Description
[31:0]	Write whatever value to generate a software trigger.

Global Trigger Mask

This register sets which signal can contribute to the global trigger generation.

Address	0x810C
Mode	R/W
Attribute	C

Bit	Description
[0]	Enables the trigger request from channel 0 to participate to the global trigger logic. Options are: 0 = disabled; 1 = enabled.
[1]	Enables the trigger request from channel 1 to participate to the global trigger logic. Options are: 0 = disabled; 1 = enabled.
[19:2]	Reserved
[23:20]	Majority Coincidence Window. Sets the time window for the majority coincidence in units of the Trigger Clock (8 ns). Majority level must be set different from 0 through bits[26:24].
[26:24]	Majority Level. Sets the majority level for the global trigger generation. Allowed level values are 0 and 1. For a level m, the trigger fires when at least m+1 of the trigger requests are generated by the enabled channels (bits [1:0]) .
[29:27]	Reserved
[30]	External Trigger. When enabled, the external trigger on TRG-IN participates to the global trigger generation in logic OR with the other enabled signals (bit[31] and bits[1:0]). Options are: 0 = disabled; 1 = enabled.
[31]	Software Trigger. When enabled, the software trigger participates to the global trigger signal generation in logic OR with the other enabled signals (bit[30] and bits[1:0]). Options are: 0 = disabled; 1 = enabled.

Front Panel TRG-OUT (GPO) Enable Mask

This register sets which signal can contribute to generate the signal on the front panel TRG-OUT LEMO connector (GPO in case of DT and NIM boards).

Address	0x8110
Mode	R/W
Attribute	C

Bit	Description
[0]	Enables the trigger request from channel 0 to participate to the TRG-OUT logic. Options are: 0 = disabled; 1 = enabled.
[1]	Enables the trigger request from channel 1 to participate to the TRG-OUT logic. Options are: 0 = disabled; 1 = enabled.
[3:2]	Reserved
[7:4]	Reserved
[9:8]	TRG-OUT (GPO) Generation Logic. The enabled trigger requests can be combined to generate the TRG-OUT (GPO) signal. Options are: 00 = OR; 01 = AND; 10 = Majority; 11 = Reserved.
[12:10]	Majority Level. Sets the majority level for the TRG-OUT (GPO) signal generation. Allowed level values are 0 and 1. For a level m, the trigger fires when at least m+1 of the trigger requests are generated by the enabled channels (bits [1:0]) .
[29:13]	Reserved
[30]	External Trigger. When enabled, the external trigger on TRG-IN can participate in the TRG-OUT (GPO) signal generation in logic OR with the other enabled signals (bit[31] and bits[1:0]). Options are: 0 = disabled; 1 = enabled.
[31]	Software Trigger. When enabled, the software trigger can participate in the TRG-OUT (GPO) signal generation in logic OR with the other enabled signals (bit[30] and bits[1:0]). Options are: 0 = disabled; 1 = enabled.

Front Panel I/O Control

This register manages the front panel I/O connectors. Default value is 0x000000.

Address	0x811C
Mode	R/W
Attribute	C

Bit	Description
[0]	LEMO I/Os Electrical Level. This bit sets the electrical level of the front panel LEMO connectors: TRG-IN, TRG-OUT (GPO in case of DT and NIM boards), S-IN (GPI in case of DT and NIM boards). Options are: 0 = NIM I/O levels; 1 = TTL I/O levels.
[9:1]	Reserved
[10]	TRG-IN control. The board trigger logic can be synchronized either with the edge of the TRG-IN signal, or with its whole duration. Note: this bit must be used in conjunction with bit[11] = 0. Options are: 0 = trigger is synchronized with the edge of the TRG-IN signal; 1 = trigger is synchronized with the whole duration of the TRG-IN signal.
[11]	TRG-IN to Mezzanines (channels). Options are: 0 = TRG-IN signal is processed by the motherboard and sent to mezzanine (default). The trigger logic is then synchronized with TRG-IN; 1 = TRG-IN is directly sent to the mezzanines with no mother board processing nor delay. This option can be useful when TRG-IN is used to veto the acquisition. NOTE: if this bit is set to 1, then bit[10] is ignored.
[13:12]	Reserved.
[14]	Force TRG-OUT (GPO). This bit can force TRG-OUT (GPO in case of DT and NIM boards) test logical level if bit[15] = 1. Options are: 0 = Force TRG-OUT (GPO) to 0; 1 = Force TRG-OUT (GPO) to 1.
[15]	TRG-OUT (GPO) Mode. Options are: 0 = TRG-OUT (GPO) is an internal signal (according to bits[17:16]); 1= TRG-OUT (GPO) is a test logic level set via bit[14].
[17:16]	TRG-OUT (GPO) Mode Selection. Options are: 00 = Trigger: TRG-OUT/GPO propagates the internal trigger sources according to register 0x8110; 01 = Motherboard Probes: TRG-OUT/GPO is used to propagate signals of the motherboards according to bits[19:18]; 10 = Channel Probes: TRG-OUT/GPO is used to propagate signals of the mezzanines (Channel Signal Virtual Probe); 11 = S-IN (GPI) propagation.
[19:18]	Motherboard Virtual Probe Selection (to be propagated on TRG- OUT/GPO). Options are: 00 = RUN/delayedRUN: this is the RUN in case of ROC FPGA firmware rel. less than 4.12. This probe can be selected according to bit[20]. 01 = CLKOUT: this clock is synchronous with the sampling clock of the ADC and this option can be used to align the phase of the clocks in different boards; 10 = CLK Phase; 11 = BUSY/UNLOCK: this is the board BUSY in case of ROC FPGA firmware rel. 4.5 or lower. This probe can be selected according to bit[20].

[20]	According to bits[19:18], this bit selects the probe to be propagated on TRG- OUT . If bits[19:18] = 00, then bit[20] options are: 0 = RUN, the signal is active when the acquisition is running and it is synchronized with the start run. This option must be used to synchronize the start/stop of the acquisition through the TRG-OUT->TR-IN or TRG-OUT->S-IN (GPI) daisy chain. 1 = delayedRUN. This option can be used to debug the synchronization when the start/stop is propagated through the LVDS I/O (VME boards). If bits[19:18] = 11, then bit[20] options are: 0 = Board BUSY; 1 = PLL Lock Loss. NOTE: this bit is reserved in case of ROC FPGA firmware rel. 4.5 or lower. NOTE: this bit corresponds to BUSY/UNLOCK for ROC FPGA firmware rel. less than 4.12.
[22:21]	Pattern Configuration. Configures the information given by the 16-bit PATTERN field in the header of the event format (VME only). Option are: 00 = PATTERN: 16-bit pattern latched on the 16 LVDS signals as one trigger arrives (default); Other options are reserved.
[31:23]	Reserved.

Channel Enable Mask

This register enables/disables selected channels to participate in the event readout. Disabled channels are not operative.
WARNING: this register must not be modified while the acquisition is running.

Address	0x8120
Mode	R/W
Attribute	C

Bit	Description
[1:0]	Bit n can enable/disable selected channel n to participate to the event readout. Options are: 0: disabled; 1: enabled.
[31:2]	Reserved

ROC FPGA Firmware Revision

This register contains the motherboard FPGA (ROC) firmware revision information.
The complete format is:
Firmware Revision = X.Y (16 lower bits)
Firmware Revision Date = Y/M/DD (16 higher bits)
EXAMPLE 1: revision 3.08, November 12th, 2007 is 0x7B120308.
EXAMPLE 2: revision 4.09, March 7th, 2016 is 0x03070409.
NOTE: the nibble code for the year makes this information to roll over each 16 years.

Address	0x8124
Mode	R
Attribute	C

Bit	Description
[7:0]	ROC Firmware Minor Revision Number (Y).
[15:8]	ROC Firmware Major Revision Number (X).
[31:16]	ROC Firmware Revision Date (Y/M/DD).

Board Info

This register contains the specific information of the board, such as the digitizer family, the channel memory size and the channel density.

Address	0x8140
Mode	R
Attribute	C

Bit	Description
[23:16]	Equipped Channels Number, i.e. 2.
[31:24]	Reserved.

Event Size

This register contains the current available event size in 32-bit words. The value is updated after a complete readout of each event.

Address	0x814C
Mode	R
Attribute	C

Bit	Description
[31:0]	Event Size (32-bit words).

Fan Speed Control

This register manages the on-board fan speed in order to guarantee an appropriate cooling according to the internal temperature variations.
NOTE: from revision 4 of the motherboard PCB (see register 0xF04C of the Configuration ROM), the automatic fan speed control has been implemented, and it is supported by ROC FPGA firmware revision greater than 4.4 (see register 0x8124).
Independently of the revision, the user can set the fan speed high by setting bit[3] = 1. Setting bit[3] = 0 will restore the automatic control for revision 4 or higher, or the low fan speed in case of revisions lower than 4.
NOTE: this register is supported by Desktop (DT) boards only.

Address	0x8168
Mode	R/W
Attribute	C

Bit	Description
[2:0]	Reserved: Must be 0.
[3]	Fan Speed Mode. Options are: 0 = slow speed or automatic speed tuning; 1 = high speed.
[5:4]	Reserved: Must be 1.
[31:6]	Reserved: Must be 0.

Run/Start/Stop Delay

When the start of Run is given synchronously to several boards connected in Daisy chain, it is necessary to compensate for the delay in the propagation of the Start (or Stop) signal through the chain. This register sets the delay between the arrival of the Start signal at the input of the board (either on S-IN/GPI or TRG- IN) and the actual start of Run. The delay is usually zero for the last board in the chain and rises going backwards along the chain.

Address	0x8170
Mode	R/W
Attribute	C

Bit	Description
[7:0]	Delay value in steps of 16 ns.
[31:8]	Reserved.

Board Failure Status

This register monitors a set of board errors. In case of a failure, bit[26] in the second word of the event format header is set to 1 during data readout (refer to the digitizer User Manual for event structure description). Reading at this register checks which kind of error occurred.
NOTE: in case of problems with the board, the user is recommended to contact CAEN for support.

Address	0x8178
Mode	R
Attribute	C

Bit	Description
[3:0]	Reserved.
[4]	PLL Lock Loss. Options are: 0 = no error; 1 = PLL Lock Loss occurred.
[31:5]	Reserved.

Disable External Trigger

The External Trigger on TRG-IN connector can be disabled through this register. Any functionality related to TRG-IN is disabled as well.

Address	0x817C
Mode	R/W
Attribute	C

Bit	Description
[0]	Options are: 0: external trigger enabled; 1: external trigger disabled.
[31:1]	Reserved

Trigger Validation Mask

Sets the trigger validation logic

Address	0x8188 (ch0), 0x818C (ch1)
Mode	R/W
Attribute	I

Bit	Description
[3:0]	Sets the trigger request that participates to the generation of the trigger validation signal. Options are: 0000: reserved; 0010: reserved; 0100: channel 0; 1000: channel 1.
[7:4]	Reserved
[9:8]	Operation Mask. Sets the logic operation among the enabled trigger request signals. Options are: 00: OR; 01: AND; 10: majority; 11: reserved.
[12:10]	Majority Level. Allowed level values are 0 and 1. For a level m, the trigger fires when at least m+1 of the trigger requests are generated by the enabled channels (bits [3:0]) .
[29:13]	Reserved
[30]	External Trigger: when enabled the external trigger from TRG-IN front panel connector participates to the trigger validation generation (in logic OR). Options are: 0: disabled; 1: enabled.
[31]	Software Trigger: when enabled the software trigger participates to the trigger validation generation (in logic OR). Options are: 0: disabled; 1: enabled.

Readout Control

This register is mainly intended for VME boards, anyway some bits are applicable also for DT and NIM boards.

Address	0xEF00
Mode	R/W
Attribute	C

Bit	Description
[2:0]	Reserved
[3]	Optical Link Interrupt Enable. Options are: 0 = Optical Link interrupts are disabled; 1 = Optical Link interrupts are enabled.
[31:4]	Reserved

Readout Status

This register contains information related to the readout.

Address	0xEF04
Mode	R
Attribute	C

Bit	Description
[0]	Event Ready. Indicates if there are events stored ready for readout. Options are: 0 = no data ready; 1 = event ready.
[1]	Reserved.
[2]	Bus Error (VME boards) / Slave-Terminated (DT/NIM boards) Flag. Options are: 0 = no Bus Error occurred (VME boards) or no terminated transfer (DT/NIM boards); 1 = a Bus Error occurred (VME boards) or one transfer has been terminated by the digitizer in consequence of an unsupported register access or block transfer prematurely terminated in event aligned readout (DT/NIM). NOTE: this bit is reset after register readout at 0xEF04.
[3]	Reserved.
[31:4]	Reserved.

Aggregate Number per BLT

This register sets the maximum number of complete aggregates which has to be transferred for each block transfer (via VME BLT/CBLT cycles or block readout through Optical Link).

Address	0xEF1C
Mode	R/W
Attribute	C

Bit	Description
[9:0]	Number of complete aggregates to be transferred for each block transfer (BLT).
[31:10]	Reserved.

Scratch

This register can be used to write/read words for test purposes.

Address	0xEF20
Mode	R/W
Attribute	C

Bit	Description
[31:0]	SCRATCH.

Software Reset

All the digitizer registers can be set back to their default values on software reset command by writing any value at this register, or by system reset from backplane in case of VME boards.

Address	0xEF24
Mode	W
Attribute	C

Bit	Description
[31:0]	Whatever value written at this location issues a software reset. All registers are set to their default values (actual settings are lost).

Software Clear

All the digitizer internal memories are cleared:
- automatically by the firmware at the start of each run;
- on software command by writing at this register;
- by hardware (VME boards only) through the LVDS interface properly configured.

A clear command does not change the registers actual value, except for resetting the following registers:
- Event Stored;
- Event Size;
- Channel / Group n Buffer Occupancy.

This register resets also the trigger time stamp.

Address	0xEF28
Mode	W
Attribute	C

Bit	Description
[31:0]	Whatever value written at this location generates a software clear.

Configuration Reload

A write access of any value at this location causes a software reset, a reload of Configuration ROM parameters and a PLL reconfiguration.

Address	0xEF34
Mode	W
Attribute	C

Bit	Description
[31:0]	Write whatever value to perform a software reset, a reload of Configuration ROM parameters and a PLL reconfiguration.

Configuration ROM Checksum

This register contains information on 8-bit checksum of Configuration ROM space.

Address	0xF000
Mode	R
Attribute	C

Bit	Description
[7:0]	Checksum.
[31:8]	Reserved.

Configuration ROM Checksum Length BYTE 2

This register contains information on the third byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address	0xF004
Mode	R
Attribute	C

Bit	Description
[7:0]	Checksum Length: bits[23:16].
[31:8]	Reserved.

Configuration ROM Checksum Length BYTE 1

This register contains information on the second byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address	0xF008
Mode	R
Attribute	C

Bit	Description
[7:0]	Checksum Length: bits[15:8].
[31:8]	Reserved.

Configuration ROM Checksum Length BYTE 0

This register contains information on the first byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address	0xF00C
Mode	R
Attribute	C

Bit	Description
[7:0]	Checksum Length: bits[7:0].
[31:8]	Reserved.

Configuration ROM Constant BYTE 2

This register contains the third byte of the 3-byte constant.

Address	0xF010
Mode	R
Attribute	C

Bit	Description
[7:0]	Constant: bits[23:16] = 0x83.
[31:8]	Reserved.

Configuration ROM Constant BYTE 1

This register contains the second byte of the 3-byte constant.

Address	0xF014
Mode	R
Attribute	C

Bit	Description
[7:0]	Constant: bits[15:8] = 0x84.
[31:8]	Reserved.

Configuration ROM Constant BYTE 0

This register contains the first byte of the 3-byte constant.

Address	0xF018
Mode	R
Attribute	C

Bit	Description
[7:0]	Constant: bits[7:0] = 0x01.
[31:8]	Reserved.

Configuration ROM C Code

This register contains the ASCII C character code (identifies this as CR space).

Address	0xF01C
Mode	R
Attribute	C

Bit	Description
[7:0]	ASCII ’C’ Character Code.
[31:8]	Reserved.

Configuration ROM R Code

This register contains the ASCII R character code (identifies this as CR space).

Address	0xF020
Mode	R
Attribute	C

Bit	Description
[7:0]	ASCII 'R' Character Code.
[31:8]	Reserved.

Configuration ROM IEEE OUI BYTE 2

This register contains information on the third byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Address	0xF024
Mode	R
Attribute	C

Bit	Description
[7:0]	IEEE OUI: bits[23:16].
[31:8]	Reserved.

Configuration ROM IEEE OUI BYTE 1

This register contains information on the second byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Address	0xF028
Mode	R
Attribute	C

Bit	Description
[7:0]	IEEE OUI: bits[15:8].
[31:8]	Reserved.

Configuration ROM IEEE OUI BYTE 0

This register contains information on the first byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Address	0xF02C
Mode	R
Attribute	C

Bit	Description
[7:0]	IEEE OUI: bits[7:0].
[31:8]	Reserved.

Configuration ROM Board Version

This register contains the board version information.

Address	0xF030
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Version Code. Options for DT5790 are: DT5790N: 0xD0; DT5790P: 0xD1; DT5790M: 0xD2.
[31:8]	Reserved.

Configuration ROM Board Form Factor

This register contains the information of the board form factor.

Address	0xF034
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Form Factor CAEN Code. Options are: 0x00 = VME64; 0x01 = VME64X; 0x02 = Desktop; 0x03 = NIM.
[31:8]	Reserved.

Configuration ROM Board ID BYTE 1

This register contains the MSB of the 2-byte board identifier.

Address	0xF038
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Number ID: bits[15:8].
[31:8]	Reserved.

Configuration ROM Board ID BYTE 0

This register contains the LSB information of the 2-byte board identifier.

Address	0xF03C
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Number ID: bits[7:0].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 3

This register contains information on the fourth byte of the 4-byte hardware revision.

Address	0xF040
Mode	R
Attribute	C

Bit	Description
[7:0]	PCB Revision: bits[31:24].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 2

This register contains information on the third byte of the 4-byte hardware revision.

Address	0xF044
Mode	R
Attribute	C

Bit	Description
[7:0]	PCB Revision: bits[23:16].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 1

This register contains information on the second byte of the 4-byte hardware revision.

Address	0xF048
Mode	R
Attribute	C

Bit	Description
[7:0]	PCB Revision: bits[15:8].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 0

This register contains information on the first byte of the 4-byte hardware revision.

Address	0xF04C
Mode	R
Attribute	C

Bit	Description
[7:0]	PCB Revision: bits[7:0].
[31:8]	Reserved.

Configuration ROM FLASH Type

This register contains information on which FLASH type (storing the FPGA firmware) is present on-board.

Address	0xF050
Mode	R
Attribute	C

Bit	Description
[7:0]	FLASH Type. Options are: 0x00 = 8 Mb FLASH; 0x01 = 32 Mb FLASH.
[31:8]	Reserved.

Configuration ROM Board Serial Number BYTE 1

This register contains information on the MSB of the board serial number.

Address	0xF080
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Serial Number: bits[15:8].
[31:8]	Reserved.

Configuration ROM Board Serial Number BYTE 0

This register contains information on the LSB of the board serial number.

Address	0xF084
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Serial Number: bits[7:0].
[31:8]	Reserved.

Configuration ROM VCXO Type

This register contains information on which type of VCXO is present on-board.

Address	0xF088
Mode	R
Attribute	C

Bit	Description
[31:0]	VCXO Type Code. Options for VME Digitizers are: 0 = AD9510 with 1 GHz; 1 = AD9510 with 500 MHz (not programmable); 2 = AD9510 with 500 MHz (programmable). Options for Desktop/NIM Digitizers are: Reserved (value = 0).

2 DPP-PSD Memory Organization

Each channel has a fixed amount of RAM memory to save the events. The memory is divided into a programmable number of buffers (also called "aggregates"), where each buffer contains a programmable number of events. The event format is programmable as well. The board registers involved are the following:

- "Aggregate Organization" (*Nb*), address 0x800C: defines how many aggregates can be contained in the memory ($n_{aggr} = 2^{Nb}$).
- "Number of Events per Aggregate" (*Ne*), address 0x1n34: defines the number of events contained in one aggregate. The maximum allowed value is 1023.
- "Record Length" (*Ns*), address 0x1n20: defines the number of samples for the waveform acquisition, when enabled (*rec_len = Ns * 8*).
- "Board Configuration", address 0x8000: defines the acquisition mode and the event data format.

Note: Those who need to write their own DAQ software, must take care to choose the Ne value according to the event and buffer size, as explained in the examples in the next section.

Information about the use of these parameters in the CAENDigitizer library can be found in **[RD1]**. According to the programmed event format, an event can contain a certain number of samples of the waveform, one trigger time stamp, the two charges Q_{short} and Q_{long}, and the Baseline/Extras information.

DT5790 series

The following section describes the structure of the memory organization of DT5790. The physical memory inside the board is made of memory locations, each of 128-bit (16B). In terms of location occupancy:

Trigger Time Stamp = 1 location;

Waveform (if enabled) = 1 location every 8 samples;

Charges (QL and QS) and EXTRAS = 1 location.

Fig. **2.1** shows the data format as saved into the physical memory for DT5790 series.

Note: Fig. **2.1** refers to the event storage into the physical memory of the board. Data are then organized in a different format for the event readout. The event readout format is shown in the **Event Data Format** section.

As previously said, the "Record Length" and the "Board Configuration" settings determine the event size; the user must calculate the number of event per buffer (*Ne*) and the number of buffers (2^{Nb}) accordingly. When the board runs in List Mode, the event memory contains only two locations, one for the Trigger Time Tag and one for the Charge and Baseline. Therefore it is very small and it is suggested to use a big value for Ne to make the buffer size as big as at least a few KB. Small buffer size results in low readout bandwidth. The only drawback of setting high values for *Ne* is that the events are not available for the readout until the buffer is complete; hence there is some latency between the arrival of a trigger and the readout of the relevant event data. Conversely, when the board runs in Oscilloscope Mode, especially when the record length is large, it is more convenient to keep *Ne* low (typically 1).

Example1: suppose that the mixed mode is enabled and Ns is set to 400 samples:
Event size (in locations) = 1(Time_Stamp) + *Ns*/8(Waveform) + 1(Charge_EXTRA) = 52 loc. Suppose to set *Ne* = 60 (number of events per buffer), hence: buffer_size (in locations) = 52 * 60 = 3120 loc. Supposing that the memory board is made of 128k loc./ch, the number of buffers will be: 128k/3120 = 42 (buffers). This value corresponds to the maximum number of buffers that the memory can contain. However, since the programmable value must be a power of two, the user has to choose the closest number smaller than 42 which can be represented as a power of two, that is 2^5 = 32 (i.e. *Nb* = 5 has to be written in the "Aggregate Organization" register).

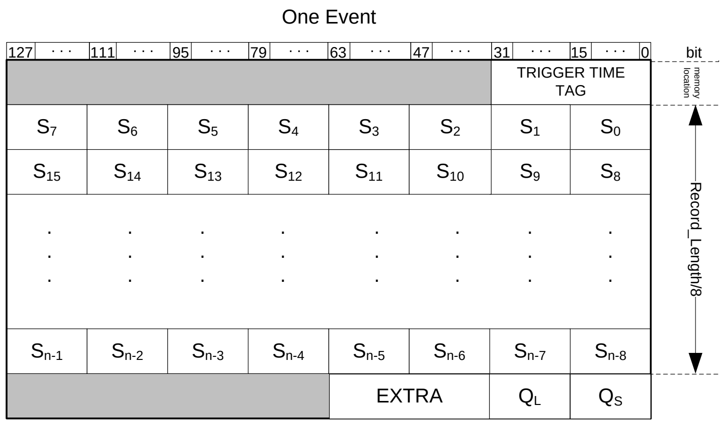


Fig. 2.1: Data organization into the Internal Memory of DT5790.

Example2: suppose that the mixed mode is enabled and *Ns* is set to 24 samples: Event size (in locations) = 1(Time_Stamp) + *Ns*/8(Waveform) + 1(Charge_EXTRAS) = 5 loc. Having a small event size, it is convenient to divide the memory into few buffers of bigger size to store a large number of events. Suppose to have set *Nb* = 3, so that the number of buffers is 8. Supposing that the board memory option is made of 64k locations, each buffer consists in 64k/8 = 8k locations and so the resulting number of event per aggregate should be: *Ne* = 8k/5 = 1639. **IMPORTANT**: in this case, the real number of events stored per aggregate is 1023, due to the register length constraint already mentioned.

Event Data Format

The data format provided by the firmware is grouped into aggregates of events. Each aggregate of channels is then grouped into the board aggregate, and finally into block transfer. Those who need to write their own acquisition software must take care of the following sections.

Channel Aggregate Data Format for DT5790 series

The Channel Aggregate is composed by the set of Ne events, where Ne is the programmable number of events contained in one aggregate (see the previous section). The structure of the Channel Aggregate of two events (EVENT 0 and EVENT 1) for 720 (DT5790) series is shown in Fig. **2.2**, where:

FI: if 1, the second word is the Format Info

DT: Dual trace enabled flag (1 = enabled, 0 = disabled)

EQ: Charge enabled flag

ET: Time Tag enabled flag

EE: Extras enabled flag.

ES: Waveform (samples) enabled flag

EP: Pedestal enabled flag

Trg Md: Trigger Mode enabled flag

EET: Enable Extended Time Stamp flag. When enabled the extended time stamp is written in the EXTRAS word, according to the options of the EE flag.

Note: to enable the Extended Time Stamp word set bit[7] of register 0x1n80..

DP3: Digital Virtual Probe 3 selection among:

"CHANNEL AGGREGATE" DATA FORMAT

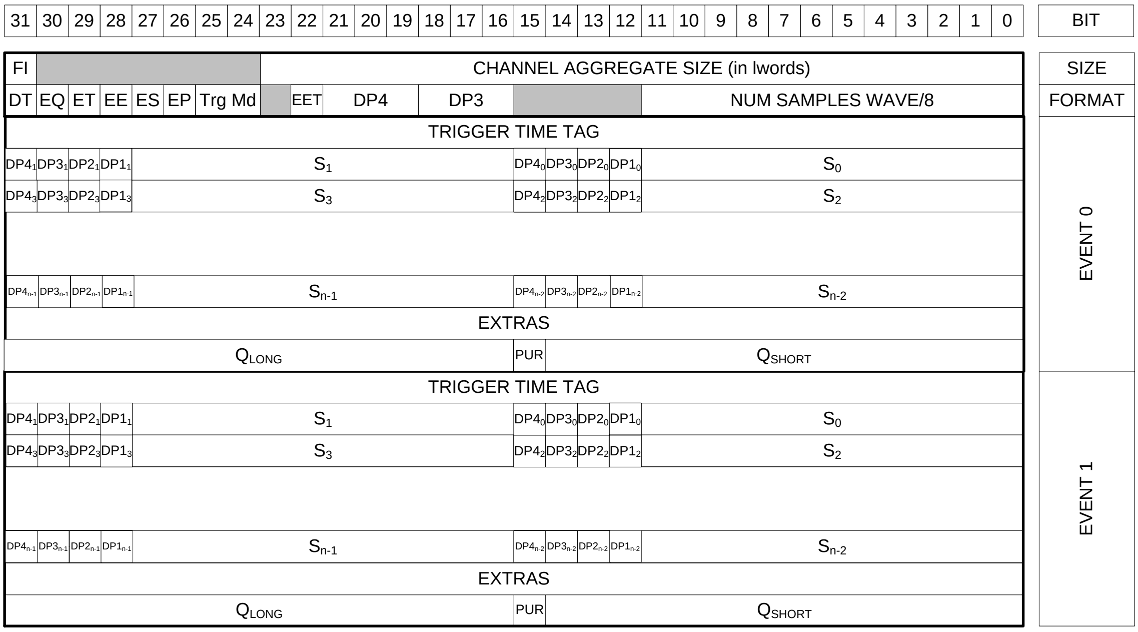


Fig. 2.2: Channel Aggregate Data Format scheme for DT5790 series.

000 = "External TRG", the external trigger signal when enabled;

001 = "Over Threshold", digital signal that is 1 when the input signal is over the requested threshold;

010 = "Shaped TRG", logic signal generated by a channel in correspondence with its local self- trigger. It is used to propagate the trigger to the other channels of the board and to other external boards, as well as to feed the coincidence trigger logic (refer to **[RD2]**);

011 = "TRG Val. Acceptance Win.", logic signal corresponding to the time window where the coincidence validation is accepted. The validation enables the event dump into the memory (see **[RD2]**);

100 = "Pile Up", logic pulse set to 1 when a pile up event occurred (to be implemented);

101 = "Coincidence", logic pulse set to 1 when a coincidence occurred (refer to **[RD2]**).

DP4: Digital Virtual Probe 4 selection among:

000 = "Short Gate";

001 = "Over Threshold", digital signal that is 1 when the input signal is over the requested threshold;

010 = "TRG Validation", digital signal that is 1 when a coincidence validation signal comes from the mother board FPGA(refer to **[RD2]**);

011 = "TRG HoldOff", logic signal generated by a channel in correspondence with its local self- trigger. Other triggers are inhibited for the overall Trigger Hold-Off duration;

100 = "Pile Up", logic pulse set to 1 when a pile up event occurred (to be implemented);

101 = "Coincidence", logic pulse set to 1 when a coincidence occurred (refer to **[RD2]**).

NUM SAMPLES WAVE/8 corresponds to the number of words to be read in the event related to the waveform / 4 (2 samples per word)

DPi_m (i=1, ...,4; m=0, 1, ...,n-1): Digital Virtual Probe value i for sample m

$DP1_m$ is always the "Trigger" probe value

$DP2_m$ is always the "Long Gate" probe value

$DP3_m$ is the value of the probe written in DP3 flag

$DP4_m$ is the value of the probe written in DP4 flag

$S_{m'}$ (m'=0, 2, 4, ..., n-2): Even Samples of input signal at time t=m'. If DT=1, $S_{m'}$ corresponds to the Baseline at time t=m'+1

$S_{m''}$ (m''=1, 3, 5, ..., n-1): Odd Samples of input signal at time t=m''s

EXTRAS: According to the value of EET, the EXTRAS word is read as follows:

Note: when the **"Dual Trace"** option is enabled half of the samples are used to store the baseline. Therefore only the remaining half samples are used for the input waveform. In the plot visualization each input sample is duplicated to keep the same granularity. Those who need to acquire waveforms with full resolution should disable the dual trace option. In CoMPASS select the "NONE" option for "Analog Probe 2" (refer to **[RD3]** for more details).

If EET = 0, EXTRAS[15] = memory full flag; EXTRAS[11:0] = Baseline.

If EET = 1, EXTRAS[15] = memory full flag; EXTRAS[14:0] = Extended Time Stamp, corresponding to the most significant bits of the Time stamp. The time stamp therefore becomes a 32 + 15 = 47 bit number.

Note: to enable the "EXTRAS" word set bit[17] of register 0x8000.

$Q_{short/long}$: integrated charge value in the short/long gate

Board Aggregate Data Format

For each readout request (occurring when at least one channel has available data to be read) the "interface FPGA (ROC)" reads one aggregate from each enabled channel memory. No more than one aggregate per channel is read each time. The sample of Channel Aggregates is the Board Aggregate. If one channel has no data, that channel does not come into the Board Aggregate. The data format when the two channels of DT5790 have available data is as shown in Fig. **2.3** for DT5790 series:

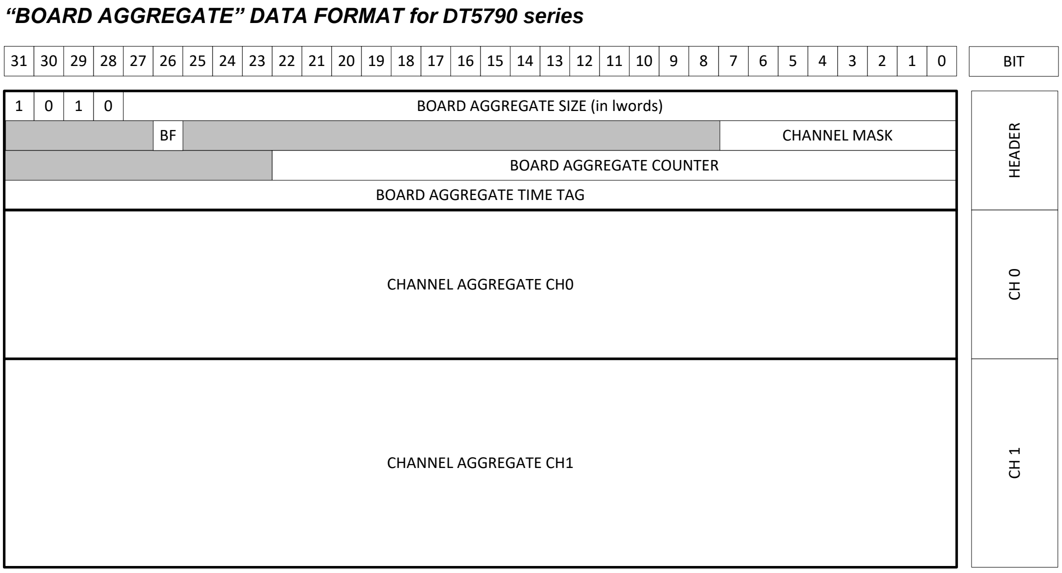


Fig. 2.3: Board Aggregate Data Format scheme for DT5790 series.

BOARD AGGREGATE SIZE: total size of the aggregate

BF: Board Fail flag. This bit is set to "1" because of a hardware problem, as for example the PLL unlock. The user can investigate the problem checking the Board Failure Status register 0x8178, or contacting CAEN support (refer to Chapter **Technical Support**).

Note: BF bit is meaningful only for ROC FPGA firmware revision greater than 4.5. It is reserved for previous releases.

CHANNEL MASK: corresponds to those channels participating to the Board Aggregate;

BOARD AGGREGATE COUNTER: counts the board aggregate. It increases with the increase of board aggregates;

BOARD AGGREGATE TIME TAG: is the time of creation of the aggregate (this does not correspond to any physical quantity).

Data Block

The readout of the digitizer is done using the Block Transfer (BLT, refer to **[RD1]**); for each transfer, the board gives a certain number of Board Aggregates, consisting in the Data Block. The maximum number of aggregates that can be transferred in a BLT is defined by the Aggregate Number per BLT. In the final readout each Board Aggregate comes successively. In case of n Board Aggregates, the Data Block is as in Fig. **2.4**

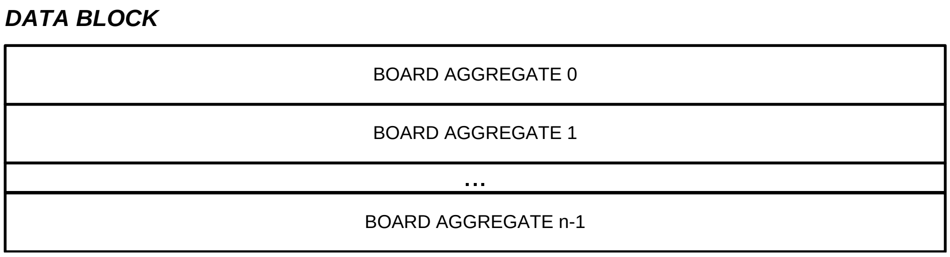


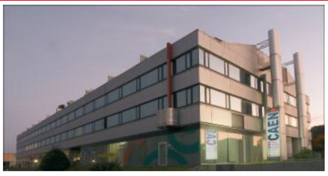
Fig. 2.4: Data Block scheme.

3 Technical Support

CAEN makes available the technical support of its specialists for requests concerning the software and hardware. Use the support form available at the following link:

https://www.caen.it/support-services/support-form/

Scan me



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