Rev. 12 - June 21st, 2023

N6742

16+1 Channel 12 bit 5 GS/s Switched Capacitor Digitizer

CAEN
Tools for Discovery

User Manual
UM4295

Purpose of the Document

This document contains the full hardware description of the N6742 CAEN digitizer and its principle of operating as Waveform Recording Digitizer (basing on the hereafter called *"waveform recording firmware"*). The reference firmware revision is: **4.25_1.06**.
For any reference to registers in this user manual, please refer to document [RD1] at the digitizer web page.

Change Document Record

Date	Revision	Changes
-	00-07	*n.a.*
Jan. 30th, 2017	08	Revised text layout. Improved text description to make it clearer.
Feb. 5th, 2020	09	Updated **Sec. 8.1**, **Sec. 9.5**, **Sec. 9.13**. Added **Sec. 9.9** and **Sec. 9.14**.
Apr. 4th, 2022	10	Updated text formatting and copyrights. Added **Safety Notices**, **Chap. 5**, **Chap. 7**, **Chap. 14**, **Chap. 15**, **Chap. 16**, Updated **Chap. 1** (**Tab. 1.1**), **Chap. 3**, **Chap. 4**, **Chap. 8**, **Chap. 9** (**Sec. 9.6.3**, **Sec. 9.7.2**, **Sec. 9.8.3**, **Sec. 9.8.4**, **Sec. 9.11**, **Sec. 9.13**), **Chap. 10**, **Chap. 12**.
January 31st, 2023	11	Added the extended 60-bit Trigger Timestamp specifications in **Chap. 3** and the description in **Sec. Event Structure**.
June 21st, 2023	12	Added information about the input range customization at 2 V_{pp} in **Chap. 1**, **Chap. 3**, **Chap. 8**, and **Chap. 9**.

Symbols, Abbreviated Terms, and Notations

ADC	Analog-to-Digital Converter
AMC	ADC & Memory Controller
CML	Current-Mode Logic
DAQ	Data Acquisition
DAC	Digital-to-Analog Converter
DC	Direct Current
DRS4	Domino Ring Sampler 4
ECL	Emitter Coupled Logic
FPGA	Field-Programmable Gate Array
GPI	General Purpose Input
GPO	General Purpose Output
LVDS	Low-Voltage Differential Signal
LVPECL	Low-Voltage Positive Emitter Coupled Logic
NIM	Nuclear Instrumentation Module
PECL	Positive Emitter Coupled Logic
PLL	Phase-Locked Loop
ROC	ReadOut Controller
SW	SoftWare
TTL	Transistor-Transistor Logic
TTT	Trigger Time Tag
USB	Universal Serial Bus

Reference Documents

[RD1] UM5698 - 742 Registers Description

[RD2] GD2512 - CAENUpgrader QuickStart Guide

[RD3] Precautions for Handling, Storage and Installation

[RD4] UM1935 - CAENDigitizer User & Reference Manual

[RD5] UM2091 - CAEN WaveDump User Manual

[RD6] UM7715 - CAENVMELib User & Reference Manual

[RD7] UM1934 - CAENComm User & Reference Manual

[RD8] GD5695 - 742 Quick Start Guide

[RD9] AN2472 - CONET1 to CONET2 Migration

[RD10] UM4413 - A2818 Technical Information Manual

[RD11] UM3121 - A3818 Technical Information Manual

[RD12] GD2783 - First Installation Guide to Desktop Digitizers & MCA

All CAEN documents can be downloaded at:
https://www.caen.it/support-services/documentation-area/ (**login required)**

Manufacturer Contacts

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Limitation of Responsibility

If the warnings contained in this manual are not followed, CAEN will not be responsible for damage caused by improper use of the device. The manufacturer declines all responsibility for damage resulting from failure to comply with the instructions for use of the product. The equipment must be used as described in the user manual, with particular regard to the intended use, using only accessories as specified by the manufacturer. No modification or repair can be performed.

Disclaimer

The information contained herein has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies. CAEN SpA reserves the right to modify its products specifications without giving any notice; for up to date information please visit www.caen.it.

Made in Italy

We remark that all our boards have been designed and assembled in Italy. In a challenging environment where a competitive edge is often obtained at the cost of lower wages and declining working conditions, we proudly acknowledge that all those who participated in the production and distribution process of our devices were reasonably paid and worked in a safe environment (while this is true for the boards marked ”MADE IN ITALY”, we cannot guarantee for third-party manufactures).

Index

List of Figures

List of Tables

Safety Notices

N.B. Read carefully the "Precautions for Handling, Storage and Installation document provided with the product before starting any operation.

The following HAZARD SYMBOLS may be reported on the unit:

	Caution, refer to product manual
	Caution, risk of electrical shock
	Protective conductor terminal
	Earth (Ground) Terminal
	Alternating Current
	Three-Phase Alternating Current

The following symbol may be reported in the present manual:

	General warning statement

The symbol could be accompanied by the following terms:

- **DANGER**: indicates a hazardous situation which, if not avoided, will result in serious injury or death.
- **WARNING**: indicates a hazardous situation which, if not avoided, could result in death or serious injury.
- **CAUTION**: indicates a situation or condition which, if not avoided, could cause physical injury or damage the product and / or the surrounding environment.

CAUTION: To avoid potential hazards

USE THE PRODUCT ONLY AS SPECIFIED.
ONLY QUALIFIED PERSONNEL SHOULD PERFORM SERVICE PROCEDURES

CAUTION: Avoid Electric Overload

TO AVOID ELECTRIC SHOCK OR FIRE HAZARD, DO NOT POWER A LOAD OUTSIDE OF ITS SPECIFIED RANGE

CAUTION: Avoid Electric Shock

TO AVOID INJURY OR LOSS OF LIFE, DO NOT CONNECT OR DISCONNECT CABLES WHILE THEY ARE CONNECTED TO A VOLTAGE SOURCE

CAUTION: Do Not Operate without Covers

TO AVOID ELECTRIC SHOCK OR FIRE HAZARD, DO NOT OPERATE THIS PRODUCT WITH COVERS OR PANELS REMOVED

CAUTION: Do Not Operate in Wet/Damp Conditions

TO AVOID ELECTRIC SHOCK, DO NOT OPERATE THIS PRODUCT IN WET OR DAMP CONDITIONS

CAUTION: Do Not Operate in an Explosive Atmosphere

TO AVOID INJURY OR FIRE HAZARD, DO NOT OPERATE THIS PRODUCT IN AN EXPLOSIVE ATMOSPHERE

THIS DEVICE SHOULD BE INSTALLED AND USED BY SKILLED TECHNICIAN ONLY OR UNDER HIS SUPERVISION

DO NOT OPERATE WITH SUSPECTED FAILURES.
IF YOU SUSPECT THIS PRODUCT TO BE DAMAGED, PLEASE CONTACT THE TECHNICAL SUPPORT

See Chap. **17** for the Technical Support contacts.

CAUTION: This product needs proper cooling

USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEATING MAY DEGRADE THE MODULE PERFORMANCES

CAUTION: This product needs proper handling

THIS DIGITIZER DOES NOT SUPPORT LIVE INSERTION (HOT SWAP) REMOVE OR INSERT THE BOARD WHEN THE CRATE IS POWERED OFF

ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE

1 Introduction

The Mod. N6742 is a NIM 16+1 Channels 12 bit 5 GS/s Digitizer based on the Switched Capacitor Array DRS4 (Domino Ring Sampler 4) chip[1].

The default input dynamic range is 1 V_{pp} (DC coupled) on single-ended MCX coaxial connectors with programmable DC Offset ($\pm$ 1 V range, controlled by a 16-bit DAC on each channel). The customization at 2 V_{pp} of input range is available by ordering option.

The analog input signal is continuously sampled by the 1024 capacitive cells of the DRS4 in a circular way, at a frequency that is software selectable amongst 5 GHz, 2.5 GHz, 1GHz, and 750 MHz.

The analog to digital conversion is not simultaneous with the chip sampling phase, and it starts as soon as the trigger condition is met. When the trigger stops the DRS4 chip sampling (holding phase), the analog memory buffer is frozen, and the cell content is made available to the 12 bit ADC for the digital conversion. The digital memory allows the subsequent events to be stored, even if the readout is not yet started. Moreover, since the digital memory buffers work like FIFOs, the readout activity from USB or Optical Link does not affect write operations of subsequent events.

The chip functioning has two major consequences:

1. there is an unavoidable dead-time when the DRS4 chip stops its acquisition and the ADC converts the capacitances (110 µs in case only the analog inputs are digitized, 181 µs when also TR0 is digitized).
2. the acquisition window is fixed to 1024 samples, that in case of 5 GHz corresponds to a maximum of about 200 ns. Refer to Sec. **9.2**.

Moreover, the trigger processing introduces a latency between the trigger arrival and the DRS4 holding phase that varies according to the trigger source. The user must consider it when choosing the proper trigger source for its setup and the type of signal. Four possible trigger sources are available:

1. *Software Trigger*, common to all enabled groups, mainly intended for debug purposes. Refer to Sec. **9.8.1**.
2. *External Trigger*, trigger on TRG-IN connector, common to all enabled groups. The external trigger latency makes this mode difficult to use at 5 GHz, while all other frequencies can be used with no problem. Refer to Sec. **9.8.2**.
3. *Fast (Low Latency) Local Trigger*, trigger on TR0 connector, common to all enabled 8-channels groups. This mode is called “Fast” or “Low Latency” since the trigger latency is reduced with respect to the external trigger. This trigger mode is convenient for high precision timing measurements, since the TR0 can be digitized and reported in the output data to be used as time reference. Refer to Sec. **9.8.3**.
4. *Self-trigger*, common to all enabled 8-channels groups. For each group is possible to select combinations of channels (logic OR) that provide a trigger whenever the input crosses the threshold. This mode cannot be used at 5 GHz due to the high trigger latency. Refer to Sec. **9.8.4** for additional details.

The module features a PLL for clock synthesis with a selectable internal reference (50 MHz oscillator) or external reference on CLK-IN connector.

By ordering options (see **Tab. 1.1**), the module is available with digital memory sizes of 128 event/ch or 1024 event/ch.

The board houses a USB2.0 compliant port supporting up to 30 MB/s transfer rate. The built-in daisy chainable Optical Link, implementing CONET proprietary protocol, is able to transfer data at 80 MB/s, thus it is possible to connect up to 8 boards to a single A2818 Controller or A4818 Adapter, or up to 32 boards to a single A3818 Controller (4-link version, see **Tab. 1.1**). Optical Link and USB access are internally arbitrated.

[1] Designed at Paul Scherrer Institute (PSI). Detailed documentation of the DRS4 chip is available at http://drs.web.psi.ch/

Board Models	Description
N6742	16+1 Ch. 12 bit 5 GS/s Switched-CapacitorDigitizer: 128 events/ch (1kS/event), EP3C16, SE
N6742B	16+1 Ch. 12 bit 5 GS/s Switched-Capacitor Digitizer: 1024 events/ch (1kS/event), EP3C16, SE
Personalizations	**Description**
VPERS1742	x742 Customization with 2 V_{pp} Input Range
Related Products	**Description**
A2818	A2818 – PCI Optical Link (Rhos compliant)
A3818A	A3818A – PCIe 1 Optical Link
A3818B	A3818B – PCIe 2 Optical Link
A3818C	A3818C – PCIe 4 Optical Link
A4818	A4818 – USB-3.0 to Optical Link
Accessories	**Description**
A317	A317 - Cable assembly for Clock distribution 3-pin AMPMODU IV female terminations - 18 cm
A317L	A317L - Cable assembly for Clock distribution 3-pin AMPMODU IV female terminations - 25 cm
DT4700	Clock Generator and FAN-OUT
A318	Adapter for Clock signal FISCHER S101A004 male to 3-pin AMPMODU IV female - 10 cm
A654	Cable assembly LEMO 00 male to MCX male – 1 m
A654 KIT4	4 Cable assembly LEMO 00 male to MCX male - 1 m
A654 KIT8	8 Cable assembly LEMO 00 male to MCX male - 1 m
A659	Cable assembly BNC male to MCX male – 1 m
A659 KIT4	4 MCX TO BNC Cable Adapter
A659 KIT8	8 MCX TO BNC Cable Adapter
AI2740	Optical Fibre 40 m simplex
AI2730	Optical Fibre 30 m simplex
AI2720	Optical Fibre 20 m simplex
AI2705	Optical Fibre 5 m simplex
AI2703	Optical Fibre 30 cm simplex
AY2730	Optical Fibre 30 m duplex
AY2720	Optical Fibre 20 m duplex
AY2705	Optical Fibre 5 m duplex (Rohs compliant)

Tab. 1.1: Table of models and related items

2 Block Diagram

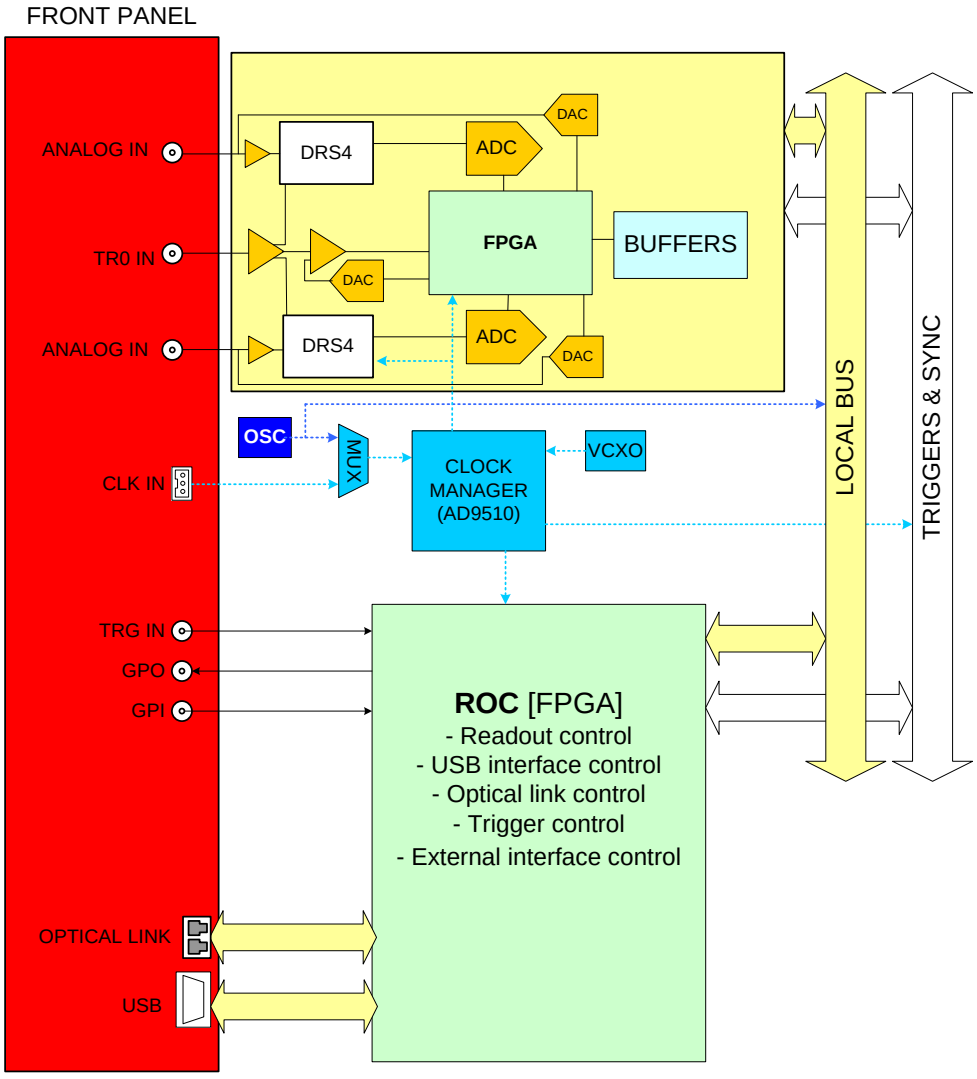


Fig. 2.1: Block Diagram

3 Technical Specifications

ANALOG INPUTS	**Number of Channels** 16 1 special channel (TR0) Single ended **Full Scale Range (FSR)** 1 V_{pp} (default) 2 V_{pp} (by customization) **Absolute max analog input voltage (for any DAC offset)** @1V_{pp} = 3 V_{pp} (with V_{rail} max +3V or -3V) @2V_{pp} = 6 V_{pp} (with V_{rail} max +6V or -6V)	**Impedance** Z_{in} = 50 Ω **DC Offset** Programmable 16-bit DAC for DC Offset adjustment on each channel. Range: ± 1 V	**Connector** MCX **Bandwidth** 500 MHz
DIGITAL CONVERSION	**Resolution** 12 bits **Switched Capacitor Array** Domino Ring Sampler chip (DRS4), 8+1 channels with 1024 storage cells each	**Sampling Rate** 5 GS/s - 2.5 GS/s - 1 GS/s - 0.75 GS/s SW selectable, simultaneously on each channel	**Dead Time (A/D Conversion)** 110 µs, analog inputs only 181 µs, digitizing TR0
FPGA	Altera Cyclone EP3C16 (one FPGA manages 16+1 channels)		
TRIGGER	**Trigger Source** - *Fast* (Low Latency) *trigger*: Common trigger by programmable threshold on TR0 - *Self-trigger*: Common trigger by combination of channels over/under threshold in logic OR - *External-trigger*: Common trigger by TRG IN connector - *Software-trigger*: Common trigger by software command		**Trigger Propagation** GPO programmable digital output **Trigger Time Stamp** 30-bit counter (extendable to 60-bit by sw) 8.5 ns resolution 9 s range Timer reset by GPI
ACQUISITION MEMORY	128 events/ch or 1024 events/ch (1024 S/event) Multi-event Buffer Independent read and write access; programmable event size and pre/post-trigger		
ADC CLOCK GENERATION	Clock source: internal/external. On-board programmable PLL provides generation of the main board clocks from internal (50 MHz local Oscillator) or external (front panel CLK-IN connector) reference		
DIGITAL I/O	**CLK-IN (AMP Modu II)** AC coupled differential input clock LVDS, ECL, PECL, LVPECL, CML (single ended NIM/TTL available by A318 adapter) Jitter < 100 ppm requested	**GPO (LEMO)** Trigger digital output NIM/TTL Z_{in} = 50 Ω **TRG-IN (LEMO)** External trigger digital input NIM/TTL Signal Width: > 17 ns Z_{in} = 50 Ω	**GPI (LEMO)** SYNC/START front panel digital input NIM/TTL Signal Width: > 17 ns Z_{in} = 50 Ω

SYNCHRONIZATION	**Clock Propagation** *One-to-many*: clock distribution from an external clock source to CLK-IN connector **Acquisition Synchronization** Sync, Start/Stop through digital I/O (GPI or TRG-IN input / GPO output)		**Trigger Time Stamps Alignment** By GPI input connector
COMMUNICATION INTERFACES	**Optical Link** CAEN CONET proprietary protocol Up to 80 MB/s transfer rate Daisy-chain capability		**USB** USB 2.0 compliant Up to 30 MB/s transfer rate
FIRMWARE	**Waveform Recording Firmware** Free firmware for waveform recording		**Upgrades** Supported via USB/Optical Link
SOFTWARE	**Readout SW** *WaveDump* readout software with C source files and VS project for developers (Windows® , Linux®)		**Libraries and Tools** General purpose C libraries with readout demos (Windows® , Linux® and LabVIEW™ support) and configuration tools
MECHANICAL	**Form Factor** 1-unit wide NIM	**Weight** *N/A*	**Dimension** 221.3 H x 34.3 W x 248.9 D mm^3
ENVIRONMENTAL	**Environment** **Operating Temperature** **Storage Temperature** **Operating Humidity** **Storage Humidity** **Altitude** **Pollution Degree** **Overvoltage Category** **EMC Environment** **IP Degree**	Indoor use 0°C to +40°C –10°C to +60°C 10% to 90% RH non condensing 5% to 90% RH non condensing < 2000m 2 II Commercial and light industrial IPX0 Enclosure, not for wet location	
REGULATORY COMPLIANCE	**EMC** CE 2014/30/EU Electromagnetic compatibility Directive		**Safety** CE 2014/35/EU Low Voltage Directive
POWER REQUIREMENTS	3.9 A @ +6 V 90 mA @ -6V		

Tab. 3.1: Specification table

4 Packaging and Compliancy

The NIM digitizer module is housed in a single-width NIM unit.

The device is inspected by CAEN before the shipment, and it is guaranteed to leave the factory free of mechanical or electrical defects.

The content of the delivered package standardly consists of the part list shown in the table below (**Tab. 4.1**).

	Part	Description	Qt
	N6742	16+1 Channel 12 bit 5 GS/s Switched Capacitor Digitizer	x1
	USB cable	USB A to B HI-SPEED cable L=2MT	x1
	Documentation	UM4295 - N6742 User Manual	-

Tab. 4.1: Delivered kit content

CAUTION: to manage the product, consult the operating instructions provided.

When receiving the unit, the user is strictly recommended to:

- Inspect containers for damage during shipment. Report any damage to the freight carrier for possible insurance claims.
- Check that all the components received match those listed on the enclosed packing list as in **Tab. 4.1** . (CAEN cannot accept responsibility for missing items unless any discrepancy is promptly notified.)
- Open shipping containers; be careful not to damage contents.
- Inspect contents and report any damage. The inspection should confirm that there is no exterior damage to the unit such as broken knobs or connectors and that the front panel is not scratched or cracked. Keep all packing material until the inspection has been completed.
- If damage is detected, file a claim with carrier immediately and notify CAEN service (see Chap. **17**).
- If equipment must be returned, carefully repack equipment in the original shipping container with original packing materials, if possible. Please contact CAEN service.

- If equipment is not installed when unpacked, place equipment in original shipping container and store in a safe place until ready to install.

DO NOT SUBJECT THE ITEM TO UNDUE SHOCK OF VIBRATIONS

DO NOT BUMP, DROP OR SLIDE SHIPPING CONTAINERS

DO NOT LEAVE ITEMS OR SHIPPING CONTAINERS UNSUPERVISED IN AREAS WHERE UNTRAINED PERSONNEL MAY MISHANDLE THE ITEMS

USE ONLY ACCESSORIES WICH MEET THE MANUFACTURER SPECIFICATIONS

For a correct and safe use of the module, refer to Chap. **6** and **7**.

5 PID (Product Identifier)

PID is the CAEN product identifier, an incremental number greater than 10000 that is unique for each product[1]. The PID is on a label affixed to the product (Fig. 5.1) and it is even stored in an on-board non-volatile memory readable at bit [7:0] of registers 0xF080 or 0xF084 **[RD1]**. The PID information is also available through CAENUpgrader Software, with the Get Information function of the GUI (for more details refer to **[RD2]**).

Note: The serial number is still valid to identify older boards, where the PID label is not present.

Fig. 5.1: PID location on N6742 (the number in the picture is purely indicative)

[1]The PID substitutes the serial number previously identifying the boards.

6 Power Requirements

The table below resumes the typical power consumption per relevant power supply voltage.

MODULE	SUPPLY VOLTAGE	
	+6 V	-6 V
N6742	3.9 A	90 mA

Tab. 6.1: Power requirements table

7 Cooling Management

The N6742 Digitizer can operate in the temperature range 0° ÷ +40°C **[RD3]**.

The NIM models must be operated in ventilated crates as recommended in the **Safety Notices**.

EXTERNAL FANS MUST BE USED WHEN THE BOARD IS INSTALLED IN A SETUP WITH POOR AIR FLOW

The User must take care to provide a proper cooling to the board with external fan if the board is used in an enclosure or if the board is installed in a setup with poor air flow.
Excessive temperature will, in first instance, reduce the performance and the quality of the measurements and can also damage the board.

If the board is stored in cold environment, please check for water condensation before power on.

The board has not been tested for radiation hardness. High energy particles can be source of errors and can damage the FPGA. If used in strong proton or neutron beams, arrange proper shielding, or remote the sensors with a custom cable.

7.1 Cleaning Air Vents

CAEN recommends to occasionally clean the air vents on all vented sides of the board or crate, if present. Lint, dust, and other foreign matter can block the vents and limit the airflow. Be sure to power off the board and disconnect it from the power by physically detach the power chord before cleaning the air vents and follow the general cleaning safety precautions.

IT IS UNDER THE RESPONSIBILITY OF THE CUSTOMER A NON-COMPLIANT USE OF THE PRODUCT

8 Panels Description

Fig. 8.1: Front panel view

8.1 Front Panel

ANALOG INPUT

DESCRIPTION
Analog input connectors.

FUNCTION
CH[i] (i = 0 to 15) receives signals from the detector.
TR0 receives the fast (low-latency) trigger.
Optionally it can be digitized.

ELECTRICAL SPECS
Input dynamics:

- 1 V_{pp}(default) or 2 V_{pp}(by customization) for CH0-CH15;
- 2 V_{pp} for TR0 (PCB Rev $\geq$ 1);
- 3 V_{pp} for TR0 (PCB Rev = 0).

Input impedance (Z_{in}): 50 Ω.
Absolute max analog input voltage (for any DAC offset in single ended configuration):

- 3 V_{pp} (with V_{rail} max +3 V or - 3 V) for 1 V_{pp} FSR.
- 6 V_{pp} (with V_{rail} max +6 V or - 6 V) for 2 V_{pp} FSR.

MECHANICAL SPECS
Series: MCX connectors.
Type: CS 85MCX-50-0-16 (jack/female).
Manufacturer: SUHNER.
Suggested plug/male: MCX-50-2-16 type.
Suggested cable: RG174 type.

CLOCK INPUT

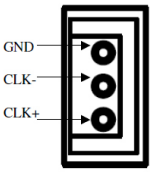
DESCRIPTION
Input connector for the external clock.

FUNCTION
CLK-IN permits locking to an external clock reference.

ELECTRICAL SPECS
Signal Level:
differential LVDS, ECL, PECL, LVPECL, CML.
Single-ended to differential A318 cable adapter available (see **Tab. 1.1**).
Coupling: AC.
Z_{diff}: 100 Ω.
Accuracy < 100 ppm.

MECHANICAL SPECS
Series: AMPMODU connectors.
Type: 3-102203-4 (3-pin).
Manufacturer: AMP Inc.

PINOUT



CLK IN LED (GREEN): indicates that the external clock is enabled

GENERAL PURPOSE OUTPUT

DESCRIPTION
General purpose programmable digital output connector.

FUNCTION
Can optionally provide out:

- internal trigger sources;
- probes from the mezzanines;
- GPI signal

according to 0x8110 and 0x811C register addresses **[RD1]**, or

- probes from the motherboard, like Run signal, ClkOut signal, ClockPhase signal, PLL_Unlock signal or Busy signal

according to 0x811C register address.

ELECTRICAL SPECS
Signal Level: single-ended NIM/TTL, SW selectable.
Requires 50 Ω termination.

MECHANICAL SPECS
Series: 101 A 004 connectors.
Type: DLP 101 A 004-28.
Manufacturer: FISCHER.
Alternatively:
Type: EPL 00 250 NTN.
Manufacturer: LEMO.

TRIGGER INPUT

DESCRIPTION
Digital input connector for external trigger.

FUNCTION
External trigger input.

ELECTRICAL SPECS
Signal Level: single-ended NIM/TTL, sw selectable.
Signal Width: > 17 ns (∼2 Trigger Clocks).
Input impedance (Z_{in}): 50 Ω.

MECHANICAL SPECS
Series: 101 A 004 connectors.
Type: DLP 101 A 004-28.
Manufacturer: FISCHER.
Alternatively:
Type: EPL 00 250 NTN.
Manufacturer: LEMO.

GENERAL PURPOSE INPUT

DESCRIPTION
General purpose programmable digital input connector.

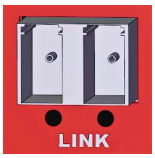
FUNCTION
Can optionally act as:

- Trigger Time Stamp reset (see **Sec. 9.11.3**);
- acquisition start/stop (see **Sec. 9.7.1**).

ELECTRICAL SPECS
Signal Level: single-ended NIM/TTL, sw selectable.
Signal Width: > 17 ns (∼2 Trigger Clocks).
Input impedance (Z_{in}): 50 Ω.

MECHANICAL SPECS
Series: 101 A 004 connectors.
Type: DLP 101 A 004-28.
Manufacturer: FISCHER.
Alternatively:
Type: EPL 00 250 NTN.
Manufacturer: LEMO.

OPTICAL LINK PORT



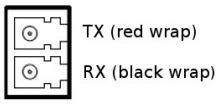
DESCRIPTION
Optical link port.

FUNCTION
Data readout and flow control through optical link. Daisy chainable. Compliant with optical fibers 50/125 µm OM2 and OM3 (back-compliant with 62.5/125 µm OM1) featuring LC connectors on both sides.

ELECTRICAL SPECS
Transfer rate: up to 80 MB/s.

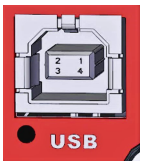
MECHANICAL SPECS
Series: SFF Transceivers.
Type: FTLF8519F-2KNL (LC connectors).
Manufacturer: FINISAR.

PINOUT



LINK LEDs (GREEN/YELOW): right LED (GREEN) indicates the network presence, while left LED (YELLOW) indicates the data transfer activity

USB PORT



DESCRIPTION
USB port.

FUNCTION
Data readout and flow control through the USB link.

ELECTRICAL SPECS
Standard: compliant with USB2.0 and USB1.0.
Transfer rate: up to 30 MB/s.

MECHANICAL SPECS
Series: USB connectors.
Type: 787780-2 (B-Type).
Manufacturer: AMP Inc.

USB LINK LED (GREEN): indicates that the USB communication is active

DIAGNOSTIC LEDs

TTL (GREEN): indicates that the standard TTL is set for GPO, TRG IN, GPI;
NIM (GREEN): indicates that the standard NIM is set for GPO, TRG IN, GPI;
PLL LOCK (GREEN): indicates that the PLL is locked to the reference clock;
PLL BYPS (GREEN): indicates that the PLL drives directly the ADCs. PLL circuit is switched off and PLL LOCK LED is turned off *(not used)*;
RUN (GREEN): indicates that the acquisition is running (data taking);
TRG (GREEN): indicates that the trigger is accepted;
DRDY (GREEN): indicates that the event/data is present in the Output Buffer;
BUSY (RED): indicates that all the buffers are full for at least one channel.

IDENTIFICATION LABELS	
	TOP: • Manufacturer • Board model • Input range • Function
	BOTTOM: • Product Identifier (PID)

9 Functional Description

9.1 Analog Input Stage

The default input dynamic is 1 V_{pp} on the single-ended MCX coaxial connectors (Z_{in} = 50 Ω). In order to preserve the full dynamic range according to the polarity of the input signal (bipolar, positive unipolar, negative unipolar), it is possible to add a DC offset by means of a 16-bit DAC, which is up to ± 1 V DC. The input bandwidth ranges from DC to 500 MHz (with 2^{nd} order linear phase anti-aliasing low-pass filter).
A customization with input range of 2 V_{pp} is available, with unchanged values for input impedance and bandwidth, and DC Offset range.

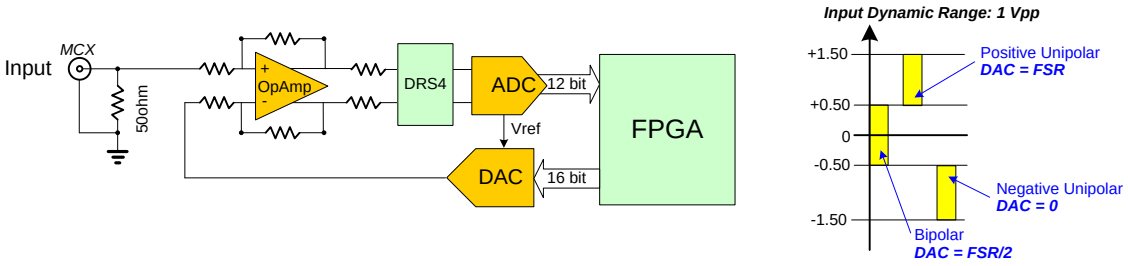


Fig. 9.1: Analog input diagram

9.1.1 DC Offset Setting

The DC Offset can optionally be set as common for a 8-channel group of the digitizer, or as individual for the 8 channels inside a group. In both cases, this can be done either by a direct write at 0x1n98 register addresses (or 0x8098 for common setting) **[RD1]**, or by library function (CAENDigitizerLib -> SetChannelDCOffset) **[RD4]**, or in the WaveDump readout software **[RD5]**.

9.1.2 Additional Input

An additional channel is available on the TR0 connector. The TR0 can act as a fast trigger (refer to Sec. **9.3** and **9.8.3**) and it can also be digitized and saved into memory. The TR0 appears as the ninth channel of each group in the final readout. The TR0 input dynamics is 2 V_{pp} for Mezzanine PCB revision $\geq$ 1, and 3 V_{pp} for Mezzanine PCB revision = 0[1]. The input dynamics is then attenuated by a factor of 2 (3 in the latter case) to make it compliant with the 1 V_{pp} dynamics of the other channels. The 16-bit DAC then allows the user to adjust the DC Offset making the TR0 suitable for positive and negative unipolar signals. The DC Offset of the TR0 input can be set either by writing at register address 0x1nDC **[RD1]**, or by library function (CAENDigitizerLib -> SetGroupFastTriggerDCOffset) **[RD4]**, or in the readout software **[RD5]**.

[1] To check the PCB revision number, read bit[9] of register 0x1n88 **[RD1]**

9.2 Domino Ring Sampling

The analog input signals are continuously sampled by the DRS4 (Domino Ring Sampler) chip[2] which consists of an on-chip inverter chain (domino wave circuit) generating a maximum of 5 GS/s sampling frequency; 2.5 GS/s, 1 GS/s, and 750 MS/s frequencies can be also programmed. The board has one chip per group, and each chip consists of 1024 capacitor cells per channel, which perform the analog sampling of the input (high frequency analog sampling). The record length of the acquisition is constrained by the cell number, and it is fixed to 1024 samples. Options 512, 256, and 136 can be selected by software to reduce the amount of data to be transferred, but all the 1024 cells are converted anyway (no dead-time reduction).

The DRS4 chip continuously samples the input in a circular way (samples are overwritten) until a trigger signal stops its acquisition (holding phase). Then the cells release their capacitances at a readout frequency controlled by the FPGA (Output Mode).

The analog samples are digitized by the 12-bit ADC at a frequency of 29.296 MHz (low frequency digital sampling). The ADC output is stored by the FPGA into the Digital Memory Buffer and data is then available for readout (for the data format refer to Sec. **9.7.2**).

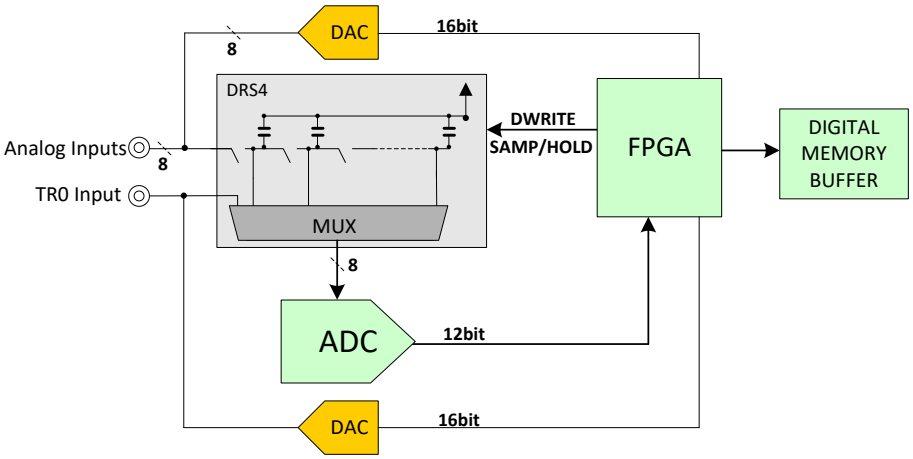


Fig. 9.2: Input Diagram

The single TR0 is split into the two DRS4 chips (see also Sec. **9.3**). Delay lines are equal in the two paths, anyway small differences in the digitized samples are possible due to differences in the chips and in the ADCs. When the digitization of the TR0 is enabled, there is a double conversion that increases the dead-time from 110 µs, when only the inputs are converted, to 181 µs when also the TR0 is converted.

[2] Detailed documentation of the DRS4 is available at http://drs.web.psi.ch/

9.3 TR0 Input

The module features one fast trigger input TR0 with extended level amplitude (NIM/LVTTL compliant); TR0 is common to group 0 (ch[7..0]) and group 1 (ch[15..8]). TR0 signal can be used as external trigger (see Sec. **9.8**). Moreover, it can be also sampled into the DRS4s analog memory buffers for applications where high resolution timing and time analysis with a common reference signal (like a trigger or system clock) is required; this is achieved by setting bit[11]=1 at 0x8000 **[RD1]**.

> **IMPORTANT**: The TR0 input is attenuated by a factor of 2 (PCB revision ≥ 1), or 3 (PCB revision 0) to make it compliant with the 1 V_{pp} dynamics of the DRS4 chip. For signals higher than 2 V_{pp} (3 V_{pp}) it is recommended to use an external attenuator.

To properly handle bipolar signals and also unipolar positive or negative signal, a 16-bit DAC allows the user to add a DC offset to TR0; offset value can be programmed via register 0x1nDC.

When the TR0 signal is used as trigger it is processed by an internal comparator, whose threshold can be programmed via register 0x1nD4: when the TR0 crosses the threshold, the FPGA stops the DRS4 acquisition and controls the sample digitalization. Examples of TR0 DC Offset and Threshold are reported in Sec. **9.8.3**

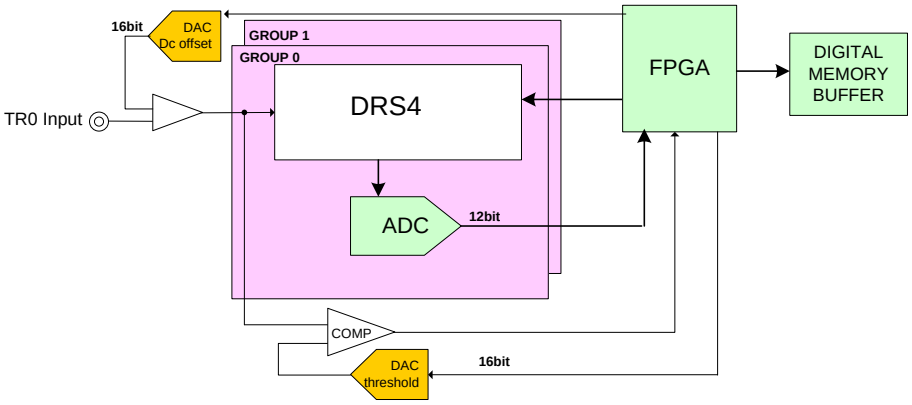


Fig. 9.3: TR0 logic block diagram

9.4 Clock Distribution

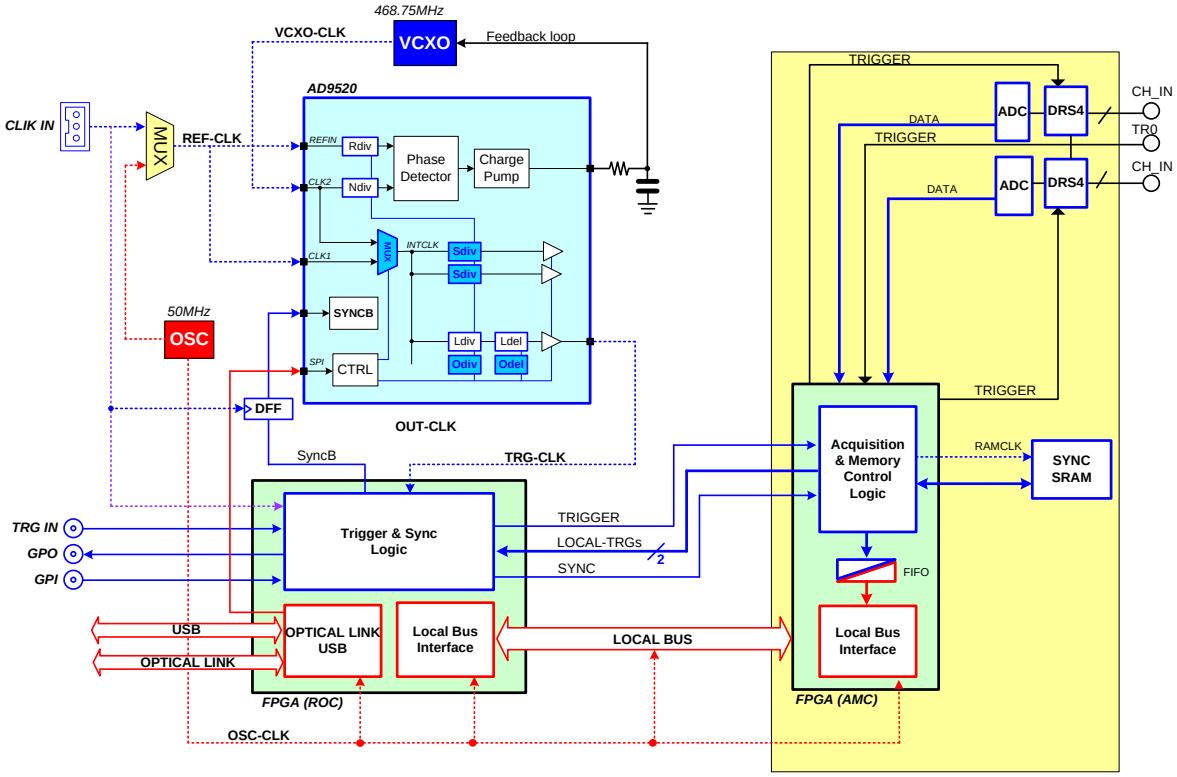


Fig. 9.4: Clock distribution diagram

The clock distribution of the module takes place on two domains: OSC-CLK and REF-CLK.

OSC-CLK is a fixed 50-MHz clock provided by a local oscillator which handles Local Bus (communication between motherboard and mezzanine boards; see red traces in the above figure).

REF-CLK handles ADC sampling, trigger logic, acquisition logic (samples storage into RAM, buffer freezing on trigger) through a clock chain. REF-CLK can be either an external (via front panel signal on CLK-IN connector) or an internal (via local oscillator) source. In the latter case, OSC-CLK and REF-CLK will be synchronous (the operating mode remains the same anyway).

REF-CLK clock source selection can be done by writing bit[6] at 0x8100:

- INT mode (default) means that REF-CLK is the 50 MHz of the local oscillator (REF-CLK = OSC-CLK);
- EXT mode means that REF-CLK is the external frequency fed on CLK-IN connector.

CLK-IN signal must be differential (LVDS, ECL, PECL, LVPECL, CML) with a jitter lower than 100 ppm. CAEN provides the A318 cable to adapt single-ended signals coming from an external clock unit into the differential CLK-IN connector.

The board mounts a phase-locked-loop (PLL) and clock distribution device, AD9520. It receives the REF-CLK (internal 50 MHz by default) and generates the sampling clock for ADCs and the mezzanine FPGA (SAMPCLK0 and SAMPCLK1), as well as the trigger logic synchronization clock (TRG-CLK) .

Refer to the AD9520 datasheet for more details:
http://www.analog.com/static/imported-files/data_sheets/AD9520-3.pdf
(in case the active link above does not work, copy and paste it on the internet browser)

9.5 PLL Mode

As introduced in Sec. **9.4**, the source of the REF-CLK signal (see **Fig. 9.4**) can be external on CLK-IN front panel connector or internal from the 50 MHz local oscillator. Selecting the REF-CLK source internal or external can be performed by changing the value of bit[6] of the board register 0x8100 to 0 (default value) or 1, respectively. This bit is reserved in case of VME boards. Selecting the external clock source, the CLK-IN front panel LED must be on (see Sec. **8.1**).

The following options are allowed:

1. 50 MHz internal clock source – This is the standard operating mode, where the default AD9520 configuration does not require to be changed: OSC-CLK = REF-CLK.

Note: The ClkOut frequency is a submultiple of the VCXO frequency. With a 50 MHz internal or external clock source, the ClkOut presents a frequency of 58.594 MHz.

2. 50 MHz external clock source – This external frequency does not require any change of the AD9520 configuration: CLK-IN = REF-CLK.

Note: It is not advisable to connect in FAN-IN an external clock source of 50 MHz to multiple boards. With this configuration, the boards will be PLL locked, but not synchronized, resulting in possible data misalignment.

3. 58.594 MHz external clock source – In this case, the user is required to program the AD9520 dividers to lock the VCXO to REF-CLK: CLK-IN = REF-CLK.
   Please contact CAEN to receive the PLL programming file (Chap. **17**).
4. External clock source different from 58.594 MHz – In this case, the AD9520 dividers must be reprogrammed to lock the VCXO to REF-CLK: CLK-IN = REF-CLK.
   In principle, the allowed external frequencies are submultiples of the VCXO frequency (468.75 MHz).
   Please contact CAEN indicating the required reference clock frequency to check the feasibility and receive the PLL programming file (Chap. **17**).

The PLL upgrade can be done through the CAENUpgrader tool **[RD2]**.
If the digitizer is locked, the PLL-LOCK front panel LED must be on (see Sec. **8.1**).

9.6 Data Correction

The DRS4 chip needs data corrections due to the unavoidable differences in the chip construction process. The corrections are managed at software level, while the firmware on-board retrieves the raw data. There are three available corrections:

1. **Cell Index Offset correction**, which compensates the signal offset for the differences in cell amplitudes;
2. **Sample Index Offset correction**, which corrects the signal offset for a noise over the last 30 samples;
3. **Time correction**, which compensates the differences of the delay line of the chips.

The default correction tables are provided by CAEN in the memory flash of the board. WaveDump software **[RD5]** (and the underlying CAENDigitizer library **[RD4]**) then can retrieve the tables and make the appropriate corrections.

The user can leave the software automatically apply all the corrections, or decide which correction applies to which group through the CORRECTION_LEVEL function of WaveDump.

If the user wants to apply its own corrections, he/she can use the CAENDigitizer function GetCorrectionTable **[RD4]** to retrieve the default correction files from the board and modify them with his/her own values.

The list of CAENDigitizer functions to be used on-line are:

- **LoadDRS4CorrectionData**, loads the correction parameters stored on board. The correction parameters to load depend on the operating sampling frequency.
- **DecodeEvent**, decode the event and apply the correction to data if LoadDRS4CorrectionData has been previously called.
- **Enable/Disable DRS4Correction**, enables/disables the data correction in the x742 series. When enabled, the data correction through the DecodeEvent function only applies if LoadDRS4CorrectionData has been previously called, otherwise the DecodeEvent runs the same, but data will be provided out not compensated.
- **GetCorrectionTables**, reads the correction tables from the x742 digitizer flash memory, related to the selected sampling frequency, and fills in a structure with the read values. In this way, the stored correction table become available for the user.

Finally, it is also possible to save the raw data and apply the corrections off-line. An example code is available in the CAENDigitizer library. To access the code, download and install the CAENDigitizer library (the prior installation of CAENVMELib **[RD6]** and CAENComm library **[RD7]** are required) and include the examples in the installation. Then access to the subfolder called ”x742_DataCorrection”:

C:/Program Files/CAEN/Digitizers/Library/Samples/x742_DataCorrection

Here the list of CAENDigitizer functions **[RD4]** to be used off-line:

- **LoadCorrectionTables**, loads the correction tables stored onto the board into a user defined structure.
- **ApplyDataCorrection**, applies the desired correction data (configured through a mask) to the raw data acquired by the user.
- **GetNumEvents**, gets the current number of events stored in the acquisition buffer.
- **GetEventPtr**, retrieves the event pointer of a specified event in the acquisition buffer.
- **X742_DecodeEvent**, decodes a specified event stored in the acquisition buffer writing data in Evt memory.

9.6.1 Cell Index Offset Correction

The analog capacitors of the DRS4 chip might have small differences between each other due to the construction processes. According to the cell index where the stop acquisition arrives, the same input signal can be reconstructed in different ways. For this reason, it is required a cell amplitude calibration to compensate for the amplitude differences in the capacitors. The correction adjusts the baseline of the input (i.e. its offset).

Taking into account the internal noise of each channel, **Fig. 9.5** shows the sampled waveform on the left and the noise distribution histogram on the right, measured as the occurrence of the ADC counts. Plots are made before the correction. **Fig. 9.6** shows the same quantities after the correction. As expected, the noise in **Fig. 9.6** is flatter with no patterns, and its distribution has a smaller RMS.

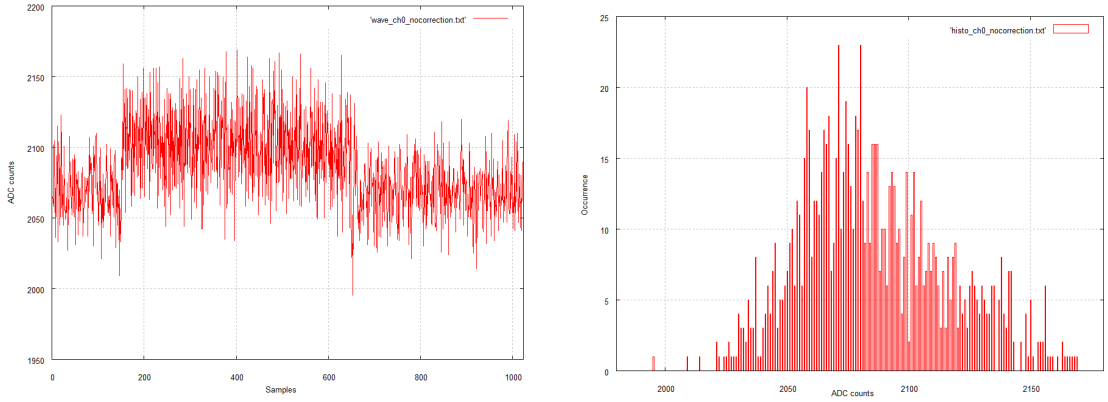


Fig. 9.5: Sampled waveform (left) and noise histogram (right) before cell index offset correction

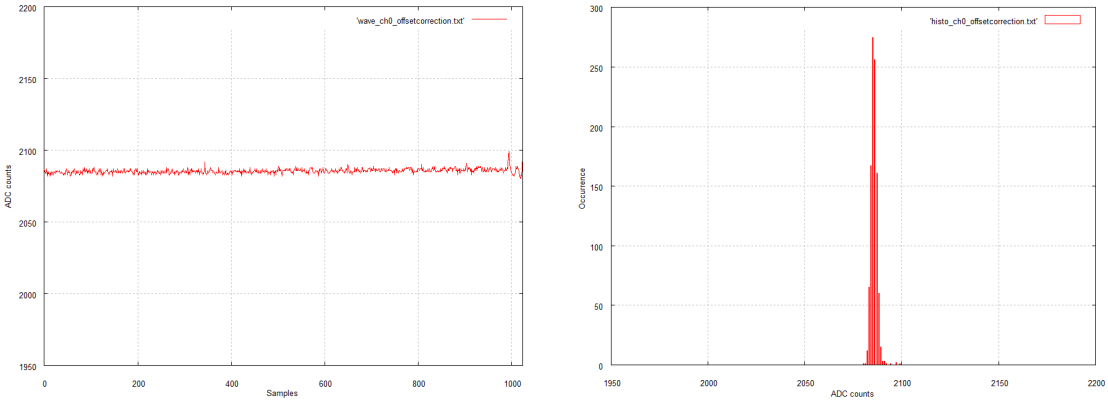


Fig. 9.6: Sampled waveform (left) and noise histogram (right) after cell index offset correction

9.6.2 Sample Index Offset Correction

From **Fig. 9.6** it is possible to see a fixed pattern over the last about 30 samples of the waveform. Therefore, it is required to perform an additional calibration, called ”Sample Index”, that corrects for the latest samples.

Fig. 9.7 shows the result on the baseline after the correction, where the pattern on the latest samples has been corrected.

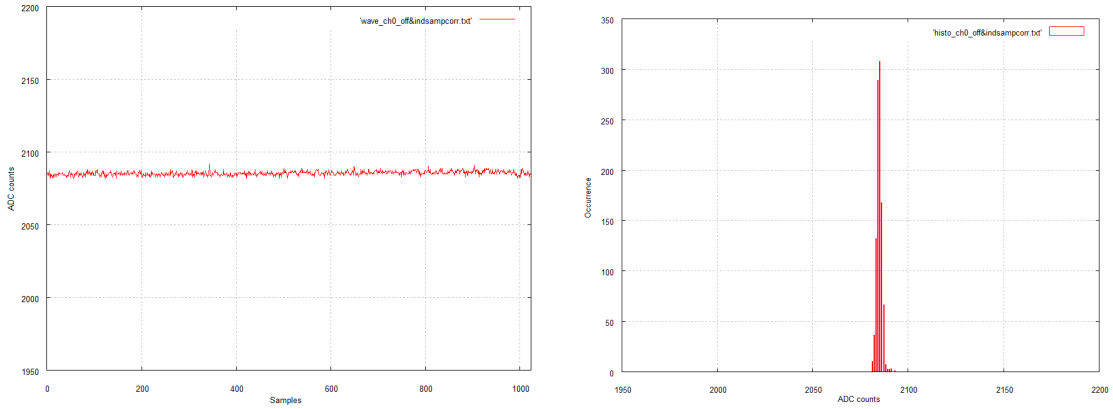


Fig. 9.7: Sampled waveform (left) and noise histogram (right) after sample index offset correction

9.6.3 Time Correction

The sampling sequence is handled by multiple DRS4 (one for each group of 8 channels) through 1024 physical delay lines each; the unavoidable construction differences between such delay lines and among the different DRS4 chips must be compensated through a time calibration.
The time corrections provided by CAEN are made by means of a very precise external clock sampled by the TR0 channel, i.e. by the DRS4 chip of Group 0 (GR0) and by the DRS4 chip of Group 1 (GR1) (see for example **Fig. 9.8**). The correction is made by supposing that the ideal sampling frequency is 200 ps (@ 5 GSps) and measuring how far is the voltage from the ideal voltage value at 200 ps.

Note: The time correction is an indirect measurement, the final information provided by the chip is a voltage, not a time.

All the contributions from the cells are summed in Integral Non-Linearity (INL) plots and the resulting trend is quite a sinusoidal shape for all chips (see **Fig. 9.10**). The final corrections are made by sampling thousands of times the square pulse and correcting at every cycle the cells by reporting the expected value of the voltage.

As mentioned, this method is an indirect method, and the final result can suffer from many contributions, like the intrinsic jitter of the pulse generator, the uncertainty of the edge shape of the pulse, the point where it is sampled, the approximation of the voltage value, etc. The sum of these factors gives a non-zero residual, as shown in **Fig. 9.11**. Due to the above factors, each board will show a different residual contribution.

Fig. 9.8 and **Fig. 9.9** show the fast trigger signal (TR0) sampled by the DRS4 chip related to GR0 and GR1, before and after the time correction respectively [3]. High discrepancies can be seen before the correction, while the differences after the correction are extremely reduced.

The corresponding INL plots are reported in **Fig. 9.10** and **Fig. 9.11** before and after the correction respectively. As expected, the INL shows a better agreement after the correction, with a reduction factor higher than x10 of the maximum time delay among cells. As mentioned, each board could have a different INL residual curve, anyway this general trend is expected for all boards.

[3] The figures, representing a single measurement performed on an individual module, have been chosen among others to highlight the efficiency of the time correction. Values could be different for each board.

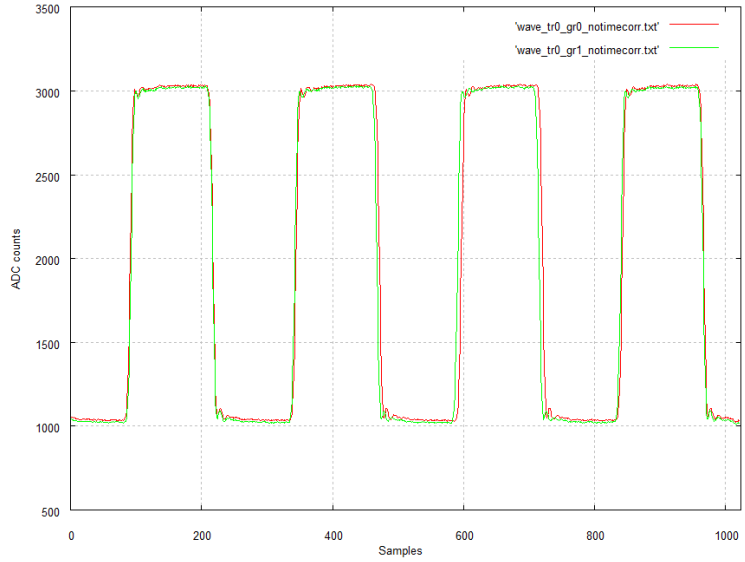


Fig. 9.8: Sampled TR0 signal in DRS4 chip for GR0 and GR1 before time correction

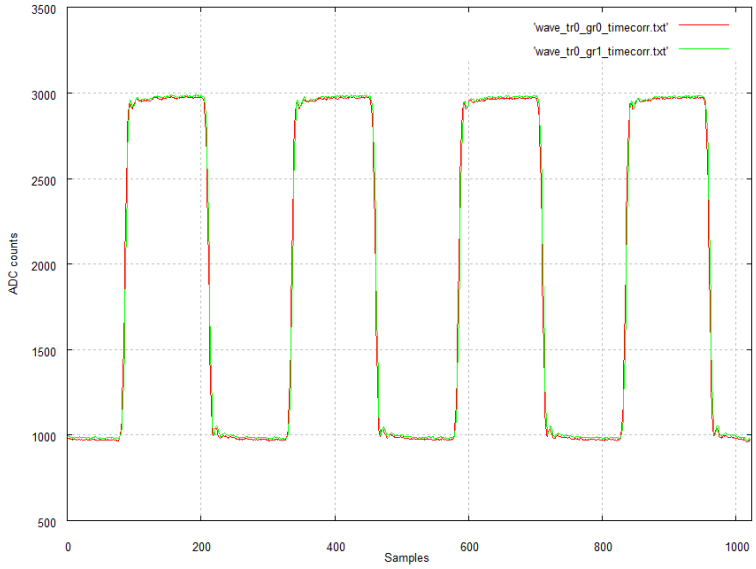


Fig. 9.9: Sampled TR0 signal in DRS4 chips for GR0 and GR1 after time correction

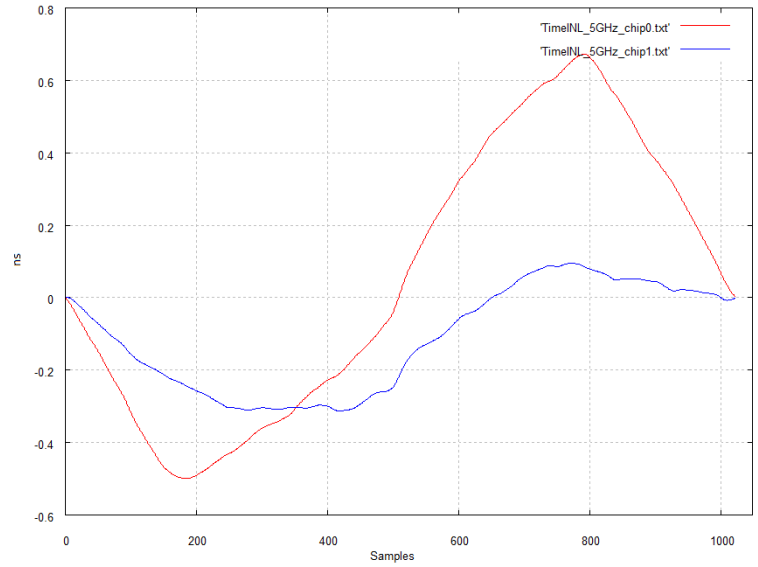


Fig. 9.10: INL time profile of DRS4 chips for GR0 and GR1 before time correction

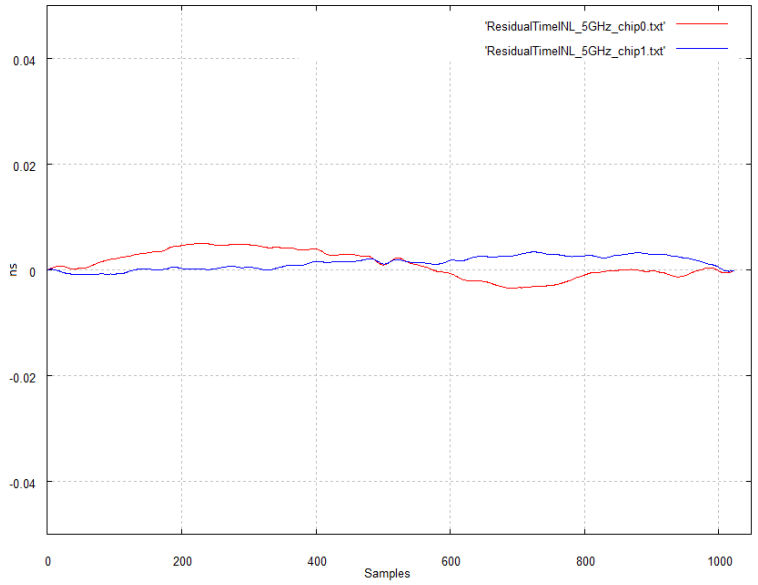


Fig. 9.11: INL time profile of DRS4 chips for GR0 and GR1 after time correction

9.7 Acquisition Modes

9.7.1 Acquisition Run/Stop

The acquisition can be started and stopped in different ways, according to bit[2:0] of 0x8100 register:

- SW CONTROLLED (bits[1:0] = 00): Start and Stop take place by software command. Bit[2] = 0 means stopped, while bit[2] = 1 means running.
- GPI CONTROLLED (bits[1:0] = 01): acquisition in armed by setting bit[2] = 1, then two options are selectable through bit [11]:
  - START/STOP ON LEVEL - If bit[11] = 0, then acquisition starts when the GPI signal is high and stops when it is low; if bit[2] = 0 (disarmed), the acquisition is always off.
  - START ON EDGE - If bit[11] = 1, then acquisition starts on the rising edge of the GPI signal and must be stopped by software command (bit[2] = 0).

Note: the START ON EDGE option is implemented from ROC FPGA firmware revision 4.22 on.

- FIRST TRIGGER CONTROLLED (bits[1:0] = 10): bit[2] = 1 arms the acquisition and the Start is issued on the first trigger pulse (rising edge) on the TRG-IN connector. This pulse is not used as a trigger; actual triggers start from the second pulse on TRG-IN. The Stop acquisition must be SW controlled (bit[2] is reset). For debugging purposes, the Start of the acquisition can be given also by Software Trigger.

9.7.2 Event Structure

The event can be read out via USB or Optical Link; data format is 32-bit long word (see **Fig. 9.12**).

An event is structured as:

- **Header** (four 32-bit words)
- **Data** (variable size and format)

The Header is composed by four words, namely:

- **TOTAL EVENT SIZE** (bit[27:0] of 1st header word) is the total size of the event, i.e. the number of 32-bit long words to be read;
- **BOARD FAIL FLAG** (bit[26] of 2nd header word), implemented from ROC FPGA firmware revision 4.5 on (reserved otherwise), is set to "1" in consequence of a hardware problem (e.g. PLL unlocking or over-temperature condition). The user can collect more information about the failure by reading at 0x8178 register address and contact CAEN Support Service if necessary (see Chap. **17**);
- **GROUP MASK** (bit[1:0] of the 2nd header word) is the mask of the groups participating in the event (e.g. GROUP 0 and GROUP 1 participating → Group Mask = 11). This information must be used by the software to retrieve to which groups the samples belong.
- **EVENT COUNTER** (bit[23:0] of 3rd header word) is the trigger counter;
- **EVENT TIME TAG** (4th header word) is a 31-bit counter for the event time tag (bit[30:0]) plus the overflow bit (bit[31]) indicating that the timestamp counter has overflowed at least once; the counter is reset when the acquisition starts or by an external signal (see Sec. **9.11.3**) and it is incremented at each trigger clock hit.

IMPORTANT NOTE: this time tag corresponds to the time when the event is created in the digitizer memory (so related to the readout), while is not related to the time when the event occurred at the group (i.e. channel) level, so it does not correspond to any physical quantity. **The physical time of arrival of the pulse can be read in the GROUP TRIGGER TIME TAG**.

After the header, the data from the enabled groups is reported consecutively. The group data format for group 0 is reported in **Fig. 9.13**.

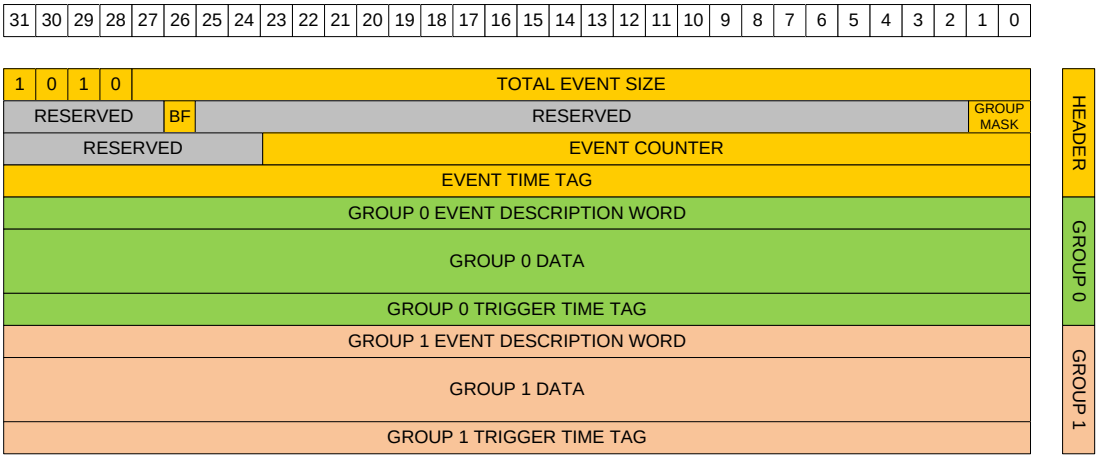


Fig. 9.12: Event Format

Each group is composed by 8 channels (GROUP 0 = CHANNEL 0 – 7, GROUP 1 = CHANNEL 8 – 15) and by the special channel TR0: such signal is common to two groups; it can be used as Local Trigger or "digitized" and stored with the data for high resolution timing analysis between the ADC channels and the TR0 itself (refer to Sec. **9.3**).

Note: TR0 is split into the two DRS4 chips of the mezzanine and follows two different path (two different ADCs and two memory buffers). This might imply that the digitized samples of TR0 might have small differences from one group to the other.

TR0 can trigger both GROUP 0 and GROUP 1 and it is stored in both group data (referring to **Fig. 9.13** the label $TR0_0$ indicates that the TR0 is saved into GROUP 0).

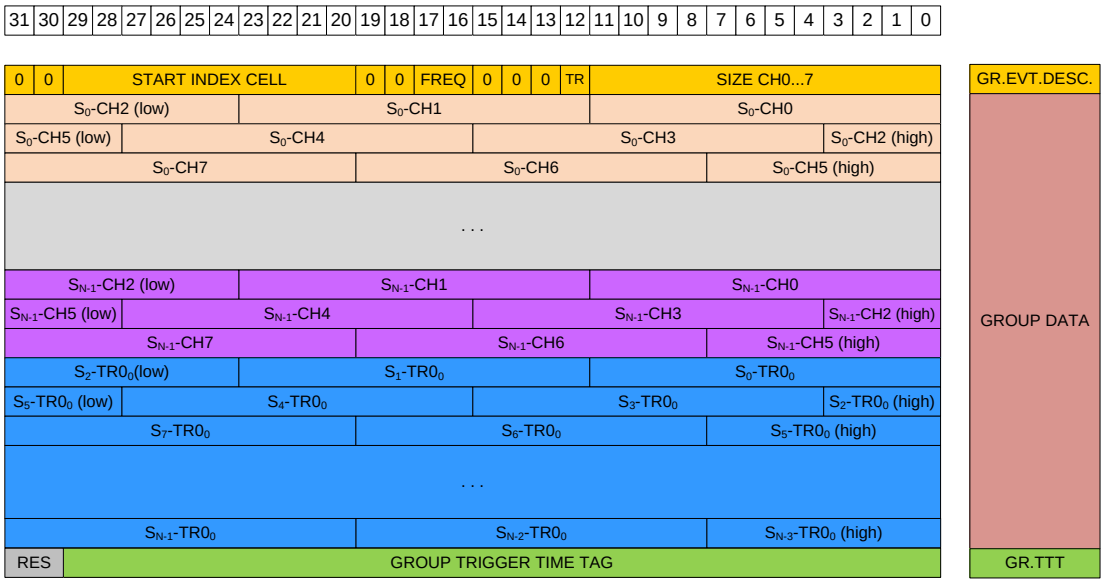


Fig. 9.13: Group Data Format

In the **Group Event Description** word (yellow row in **Fig. 9.13**) the following fields are shown:

- **START INDEX CELL** (Bits[29:20]) is the index cell of the DRS4 chip, corresponding to the first sample of the event;
- **FREQ** (Bit[17:16]) is the sampling frequency of the DRS4 chip, whose options are:
  - 00 = 5 GS/s;
  - 01 = 2.5 GS/s;
  - 10 = 1 GS/s;
  - 11 = 750 MS/s.
- **TR** (Bit[12]) flag indicates whether the TR0 has been digitized and it is available in the readout. Options are:
  - 0 = TR0 signal not present in the readout;
  - 1 = TR0 signal present in the readout.

- **SIZE CH0...7** (Bit[11:0]) is the number of words to be read for the CH0...7 samples. Considering that each channel has 1024 samples, and that one sample is written in three words, "SIZE CH0...7" is 0xC00.

The **GROUP DATA** corresponds to the waveform samples, where each sample is reported from the lowest channel index to the highest.

If the readout of TR0 is disabled, data related to such channel (light blue in **Fig. 9.13**) are not present in the event; if readout of TR0 is enabled, data size related to such channel is Size TR0 = (SIZE CH0...7)/8. The

GROUP TRIGGER TIME TAG records the Trigger arrival time into a 30-bit number (steps of 8.5 ns). This is the physical trigger information of the event.
From revision number **1.06** of the mezzanine firmware (AMC FPGA), the option to extend the Group Trigger Time Tag on 60 bits is available (same 8.5ns resolution). The Extended Group Trigger Time Tag (EGTTT) must be enabled by bit[2] of register 0x8000 **[RD1]**. Then, the 60-bit value for GROUP 0-1 is given by (GROUP 1 TRIGGER TIME TAG) & (GROUP 0 TRIGGER TIME TAG).

Note: Enabling only GROUP 0, the timestamp actually remains at 30 bits even if the EGTTT is set. Instead, enabling only GROUP 1, the EGTTT must not be set, as the resulting timestamp is inconsistent.

9.8 Trigger Management

Once a trigger condition is met, the DRS4 chip stops its sampling phase and the analog capacitances are converted (holding phase) by a 12-bit ADC. There are four possible trigger sources:

- **Software Trigger** (common to all enabled groups). The trigger is issued through a software write on the relevant FPGA register. This mode is mainly used for debugging purposes.
- **External Trigger** (trigger on TRG-IN connector, common to all enabled groups). The TRG-IN connector accepts NIM and TTL input logic, which can be programmed via software. More details are in Sec. **9.8.2**.
- **Fast (Low Latency) Local Trigger** (trigger on TR0 connector, common to all enabled groups). This mode is called “Fast” or “Low Latency” since the latency from the trigger arrival and the DRS4 stop acquisition is significantly reduced with respect to the External Trigger mode. See Sec. **9.8.3**.
- **Self-trigger** (common to all enabled groups), the acquisition is controlled by combinations in logic OR of the channel self-triggers. See Sec. **9.8.4**.

During the analog to digital conversion process, the board cannot handle other triggers. The corresponding dead-time is equal to 110 µs when only the inputs are digitized, and 181 µs when also the TR0 is digitized.

Fig. 9.14 shows the block diagram of the 742 trigger management.

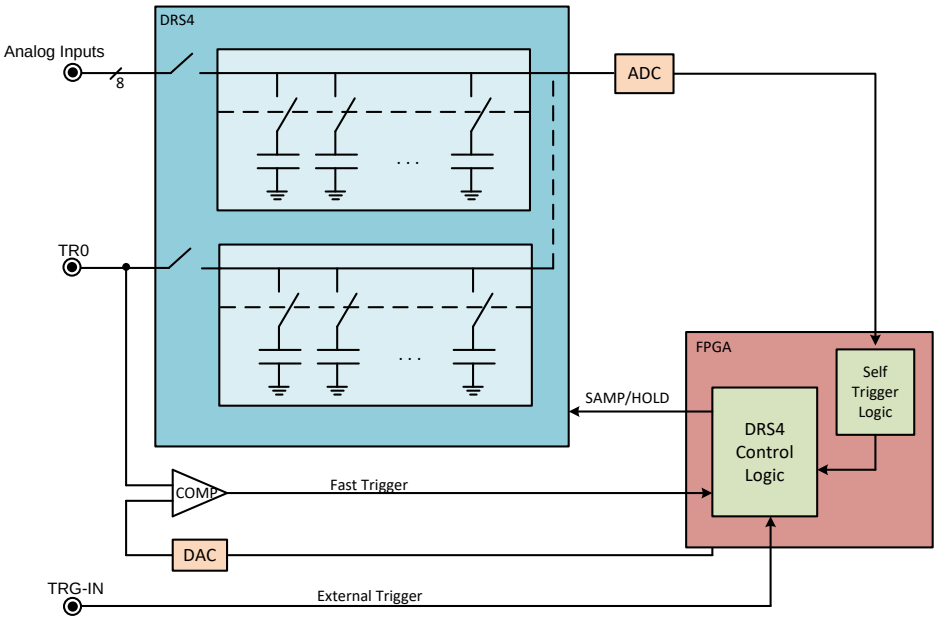


Fig. 9.14: Block diagram of Trigger management

9.8.1 Software Trigger

Software triggers are internally produced via a software command (write access at 0x8108 register address) through USB or Optical Link.

9.8.2 External Trigger

A TTL or NIM external signal can be provided in the front panel TRG-IN connector (configurable at 0x811C register address).

The TRG-IN signal is first processed by the mother board with a clock of about 58 MHz, and sent to the DRS4 to stop its acquisition with a latency of about 115 ns and a jitter of about 17 ns[4]. The latency of the external trigger makes this mode difficult to use at 5 GHz, where the maximum acquisition window is about 200 ns (1024 samples of 200 ps).

9.8.3 Fast ("Low Latency") Trigger

The trigger signal is fed into TR0 connector, and it is common to all enabled groups. The TR0 connector accepts signals with maximum amplitude of 2 V_{pp} in case of Mezzanine PCB revision ≥ 1 (3 V_{pp} in case of Mezzanine PCB revision = 0)[5].

> **IMPORTANT**: The TR0 input is attenuated by a factor of 2 (PCB revision ≥ 1), or 3 (PCB revision 0) to make it compliant with the 1 V_{pp} dynamics of the DRS4 chip. For signals higher than 2 V_{pp} (3 V_{pp}) it is recommended to use an external attenuator.

This mode is called "Fast" or "Low Latency" since the latency from the trigger arrival and the DRS4 holding phase is reduced to about 42 ns with a jitter of about 8.5 ns. The signal on TR0 is sent to a comparator with programmable threshold (no mother-board processing) whose output is sampled at about 117 MHz (twice the external trigger processing). When the TR0 signal crosses the threshold, the acquisition of the DRS4 chip is stopped and the digitalization process starts.
This trigger mode is convenient for high precision timing measurements, since the TR0 can be digitized as the other analog inputs and reported in the output data as channel number 8 of each group. The trigger can therefore be used as a time reference for the input. The DRS4 sampling period becomes the time jitter of the trigger with respect to an input of the same group, which can reach 200 ps in case of sampling at 5 GHz. The resolution in a time of flight measurement reaches up to 50 ps in case of signals and TR0 in the same TR0 group.

Note: TR0 is split into the two DRS4 of the mezzanine and follows two different path (two different ADCs and two memory buffers). This might imply that the digitized samples of TR0 might have small differences from one group to the other.

TR0 acting as input signal can manage several types of signal polarities (bi-polar, negative, and positive), thanks to the possibility to modify the DC Offset (i.e. the baseline position, or 0-Volt) and Trigger Threshold of the TR0 itself. From **Fig. 9.3**, a fast analog comparator is available in the board to identify when the TR0 crosses the threshold and to generate a trigger when the Low Latency trigger mode is enabled. The comparator has two inputs, one for TR0 plus its DC Offset, the other for the Threshold. Both DC Offset and Threshold come from two 16-bit DACs, and their corresponding registers (addresses 0x1nDC (Bit[15:0]) and 0x1nD4 (Bit[15:0]), respectively **[RD1]**) must be written as 16-bit numbers.

Due to the real design complexity of the TR0 input stage needed to fit its multiple functions (the schemes in

[4] The TRG-IN latency has been reduced to 115 ns from ROC firmware revision 4.07, while for firmware revisions less than 4.07 the latency was 255 ns with a jitter of about 34 ns.
[5] To check the PCB revision number, read bit[9] of 0x1n88 register **[RD1]**

this document are simplified), there is not a simple formula for setting the desired trigger Threshold value (even in mV) for different values of the DC Offset. For this reason, CAEN provides ready-to-use information: **Tab. 9.1** and **9.2** report the DC Offset and trigger Threshold values (hexadecimal / decimal) for typical signals that can be fed into the TR0 connector, where the Threshold values are set at half of the signal height. This information can be used directly to set the involved registers **[RD1]** or the software parameters **[RD5][RD4]**. A practical example of setting the TR0 triggering mode in the CAEN WaveDump software is described in **[RD8]**.

Mezzanine PCB Rev. $\geq$ 1	
ECL signal on TR0	TR0 DC Offset = 0x55A0 / 21920 TR0 Threshold = 0x6666 / 26214
NIM signal on TR0	TR0 DC Offset = 0x8000 / 32768 TR0 Threshold = 0x51C6 / 20934
Negative signal on TR0: V = 0 ÷ -400mV	TR0 DC Offset = 0x8000 / 32768 TR0 Threshold = 0x5C16 / 23574
Negative signal on TR0: V = 0 ÷ -200mV	TR0 DC Offset = 0x8000 / 32768 TR0 Threshold = 0x613E / 24894
Bipolar signal on TR0	TR0 DC Offset = 0x8000 / 32768 TR0 Threshold = 0x6666 / 26214
TTL on TR0 or Positive signal on TR0: V = 0 ÷ ≥ 2V	TR0 DC Offset = 0xA800 / 43008 TR0 Threshold = 0x6666 / 26214
Positive on TR0: V = 0 ÷ 2V	TR0 DC Offset = 0x91A7 / 37287 TR0 Threshold = 0x6666 / 26214

Tab. 9.1: Examples of DC Offset and Trigger Threshold (in hexadecimal / decimal) for typical signals on TR0 connector. Values are valid for mezzanine PCB revision ≥ 1.

Mezzanine PCB Rev. 0	
NIM signal on TR0	TR0 DC Offset = 0x1000 / 4096 TR0 Threshold = 0x717D / 29053
Negative signal on TR0: V = 0 ÷ -400mV	TR0 DC Offset = 0x1000 / 4096 TR0 Threshold = 0x6E72 / 28274
Bipolar signal on TR0	TR0 DC Offset = 0x1000 / 4096 TR0 Threshold = 0x6C80 / 27776
Positive on TR0: V = 0 ÷ 2V	TR0 DC Offset = 0x4000 / 16384 TR0 Threshold = 0x7158 / 29016

Tab. 9.2: Examples of DC Offset and Trigger Threshold (in hexadecimal / decimal) for typical signals on TR0 connector. Values are valid for mezzanine PCB revision 0.

For example, consider the case of a **NIM signal** (0, -800 mV), assuming to set the DC Offset at mid-scale and the Threshold at half of the amplitude of the TR0 signal.

Considering the 16-bit DAC of the comparator, in order to set the 0-Volt of the TR0 at mid-scale, the DC Offset parameter must be set to **0x8000** (i.e. the decimal value of **32768** = $(2^{16} - 1)/2$) on the 0x1nDC (Bit[15:0]) register. When the TR0 is digitized by the 12-bit ADC (@ 5 GS/s like the other analog channels of the digitizer), the 16-bit DC Offset of TR0 is scaled into the 12-bit range of the ADC and a factor of 16 must be considered, so that the 32768 value should ideally turn into around 2048 ADC counts.
Concerning the Trigger Threshold, the half of the amplitude of the TR0 signal corresponds to -400 mV with respect to the pulse 0-Volt.

The user must first consider that mid-scale of the ADC dynamics (that is 1 V in the [0:2] V range) corresponds

to write 0x6666 in the Trigger Threshold DAC, that is (1 V/2.5 V)$\times 2^{16}$, where 2.5 V is the input dynamic of the fast comparator. For example, this is also the value written in **Tab. 9.1** and **9.2** for the bipolar signal.

With respect to the mid-scale value, moving the threshold by 1 mV implies setting a value of, ideally, 13.2 in the DAC. In order to set the threshold at -400 mV, the following calculation must be done: 400 $\times$ 13.2 = 5280, which corresponds to 0x14A0. The last step is to subtract from the mid-scale value the desired threshold value, in our example: 0x6666-0x14A0 = **0x51C6** (i.e. the decimal value of **20934**) is the Trigger Threshold to be set in the 0x1nD4 (Bit[15:0]) register.

9.8.4 Self-Trigger

The self-trigger mode is available on 742 series from AMC firmware revision 0.4. In self-trigger mode each channel can self-trigger on its own input – leading edge discrimination – and logic OR combinations of the self-triggers enable the groups to acquire at the same time. Refer to 0x1nA8 register **[RD1]** for more details.

The DRS4 chip has two operating modes: "Transparent" and "Output". In Transparent mode (see **Fig. 9.15**), the input pulse is both sampled by the DRS4 capacitors (analog sampling) at high frequency, and made available at the output for the ADC digital sampling at a smaller rate, about 30 MHz. In transparent mode, the output stage is not a pure differential, since it has an offset and it is attenuated with respect to the signal correctly shaped. Transparent mode is the standard operating mode of the DRS4 chip, which continuously samples the input.

In Output mode (see **Fig. 9.16**), the input is no longer sampled and the capacitors hold the acquired samples and send them one at a time to the ADC at a frequency controlled by the FPGA (readout frequency). The Output mode starts when a trigger condition is met (see **Fig. 9.14**). Samples in Output mode are those available in the readout for the user and they are correctly shaped.

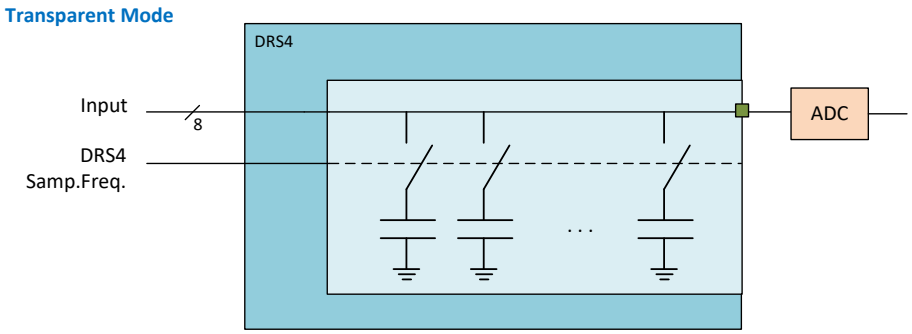


Fig. 9.15: Diagram showing the "Transparent Mode" functioning. The analog input is both sampled by the DRS4 capacitors (analog sampling) and made available at the output for the ADC digital sampling at a smaller rate. The output stage is distorted with respect to the Output mode.

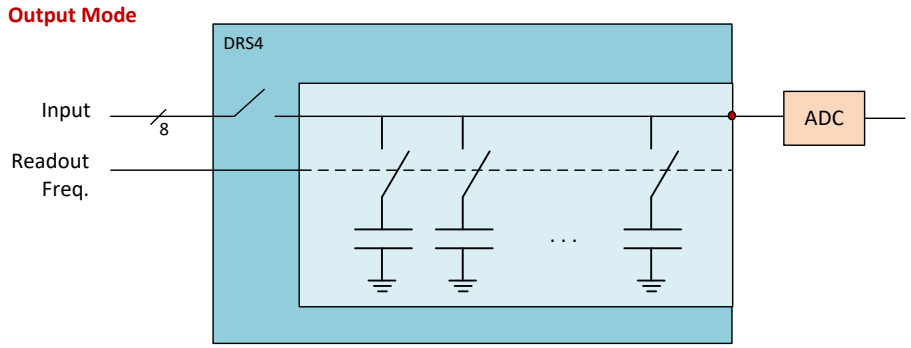


Fig. 9.16: Diagram showing the "Output Mode" functioning. the input is no longer sampled and the capacitors hold the acquired samples and send them one at a time to the ADC at a frequency controlled by the FPGA (readout frequency). The output stage is correctly differential.

Since the Self-Trigger Logic inside the FPGA reads data from the ADC while the DRS4 chip works in Transparent mode, the Trigger Threshold has to be referred to the values read in Transparent mode itself, rather to the values reported in Output mode.

To correctly set the threshold value, it is first required to make an acquisition in Transparent mode to visualize the waveform as sampled by the ADC.

Considering that the ADC frequency is about 30 MHz, it is important that the input can be sampled by the ADC itself. In particular, the pulse width should be greater than 30 ns, and the input frequency should be high enough to visualize some pulses.

IMPORTANT: The procedure of reading from the ADC and processing data by the FPGA introduces a latency of about 320 ns (with a jitter of 17 ns) before the DRS4 holding phase. This mode is therefore not compliant with the DRS4 frequency = 5 GHz, but it can be useful when the board works at 2.5 GS/s, 1 GS/s, or 750 MS/s.

9.8.5 How to work with Self-Trigger

To work with the channel self-trigger feature, the board must be configured appropriately according to the following steps.

- Set the DC Offset of each channel (at least those which are required to acquire) to ensure that the entire input signal is within the input dynamics of the board. To verify this, it is suggested to make acquisitions in the standard mode ("Output Mode") using the SW trigger.
- Set the board to perform the acquisition in "Transparent Mode" (set bit[13] = 1 of 0x8000 register).
- Make acquisitions in "Transparent Mode" using the SW trigger. *No corrections are made in Transparent mode*. For each channel of interest, check the value of the signal in this acquisition mode and choose the threshold for triggering.
- Set the threshold value for each channel of interest via 0x1n80 register, where n is the group index.
- Enable the channels of interest to generate a Channel Trigger via 0x1nA8 register.
- Set the board to perform the acquisition in "Output Mode" (set back bit[13] = 0 of 0x8000 register).

The board is so ready to acquire data when triggers are generated by the channels.

Refer also to **[RD8]** for a practical example and **[RD1]** for the registers description.

9.9 Multi-board Synchronization

When multi-board systems are involved in an experiment, it is necessary to synchronize different boards. In this way, the user can acquire from N boards each one with Y channels, like if they were just one board with (N · Y) channels.

While all the channels of the same board are simultaneously sampled at the same clock frequency by design, the main issue with a multi-board system is to guarantee the clock synchronization for the channels of all the boards. This is achieved by using an external clock unit, like CAEN DT4700, which generates the needed reference clock and can provide it in fan-out on the CLK-IN connector of up to ten digitizers.

Other issues are the synchronization of the start of the run to let all the boards have the same zero for time stamps, the trigger synchronization to propagate and combine the triggers from all the boards to have the same common acquisition trigger (by fan-in on the Tr0), and the event data synchronization to keep event data aligned across boards (busy/veto management). Please, contact CAEN for details (see Chap. **17**).

9.10 Test Pattern Generator

The FPGA can emulate the ADC and write into memory a saw tooth signal for test purposes. It can be enabled via Group Configuration register.

The following figure shows the test waveforms for even and odd groups respectively.

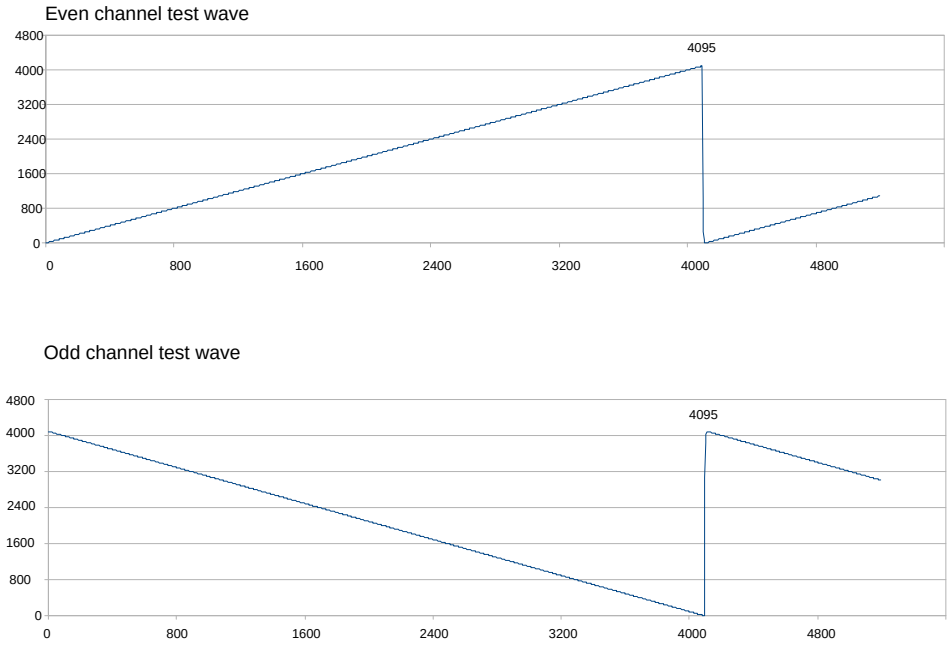


Fig. 9.17: FPGA test waveform

Since an event is made up of up to 1024 samples, the test event samples only a “portion” of the saw tooth; the start point of the sampling can be programmed via Initial Test Wave Value register; for example if this register is set to 0x0FF then the channels in the even groups sample the ramp between 255 and 1278; the channels in the odd groups instead sample the complementary value, therefore between 3840 and 2817.

9.11 Reset, Clear and Default Configuration

9.11.1 Global Reset

A global reset is performed at power-on of the module or can be issued via software by write access at 0xEF24 register address. By a global reset, the data from the Output Buffer are cleared, the event counters are reset and so all the board FPGAs which turn back to their default configuration. All counters are initialized to their initial state and all detected error conditions are cleared.

9.11.2 Memory Reset

The memory reset clears the data off the Output Buffer.
It can be issued by write access at 0xEF28 register address (whatever 32-bit value can be written).

9.11.3 Timer Reset

The timer reset initializes the time tag counters (Event Time Tag and Group Trigger Time Tag).
The timer reset can be issued either via software by a software clear command at 0xEF28 register address, or via hardware by sending a pulse to the front panel GPI input (leading edge sensitive). In case the GPI connector needs to be used to reset the trigger time stamps, no configurations or access to registers are necessary. The user only has to transmit a NIM or TTL signal to the input, depending on the software selected logic level for the GPI connector. The time stamps reset occurs at every leading edge of the logic signal sent to the GPI connector.

9.12 Data Transfer Capabilities and Events Readout

Once it is written in the memory, the event becomes available for the readout via USB or Optical Link. According to the board model (**Tab. 1.1**), up to 128 or 1024 events per channel (1024 samples per event) can be stored in the digitizer digital memory.

The events are read out sequentially and completely, starting from the Header of the first available event, followed by the samples of the enabled groups as reported in **Fig. 9.12**. It is not possible to read out an event partially.

The size of the event (EVENT SIZE) is configurable and depends on register addresses 0x8020 **[RD1]**, as well as on the number of enabled groups. Reducing the event size does not reduce the digitizer dead time.

The board supports D32 single data readout and Block Transfer BLT32. Theoretical maximum transfer rate is up to 30 MB/s by USB2.0 and up to 80 MB/s by optical link.

9.12.1 Block Transfer

The Block Transfer readout mode allows to read N complete events sequentially, where N is set at register address 0xEF1C **[RD1]**, or by using the SetMaxNumEventsBLT function of the CAENDigitizer library **[RD4]**.

When developing programs, the readout process can be implemented on different basis :

- Using **Interrupts**: as soon as the programmed number of events is available for readout, the board sends an interrupt to the PC over the optical communication link (not supported by USB).
- Using **Polling** (interrupts disabled): by performing periodic read accesses to a specific register of the board it is possible to know the number of events present in the board and perform a BLT read of the specific size to read them out.
- Using **Continuous Read** (interrupts disabled): continuous data read of the maximum allowed size (e.g. total memory size) is performed by the software without polling the board. The actual size of the block read is determined by the board that terminates the BLT access at the end of the data, according to the configuration of register address 0xEF1C, or the library function SetMaxNumEventsBLT above mentioned. If the board is empty, the BLT access is immediately terminated and the “Read Block” function will return 0 bytes (it is the ReadData function in the CAENDigitizer Library **[RD4]**).

Whatever the method from above, it is suggested to ask the board for the maximum of the events per block being set. Furthermore, the greater this maximum is, the greater the readout efficiency is, despite of a greater memory allocation required on the host station side. The latter is actually not a real drawback, considering the features of the personal computers available on the market.

9.12.2 Single Data Transfer

This mode allows the user to readout a word per time, from the header (actually 4 words) of the first available event, followed by all the words until the end of the event, then the second event is transferred. The exact sequence of the transferred words is shown in Sec. **9.7.2**.

It is suggested, after the 1st word is transferred, to check the EVENT SIZE information and then do as many cycles as necessary (actually EVENT SIZE -1) in order to read completely the event.

9.13 Optical Link and USB Access

The board houses a USB2.0 compliant port with a maximum theoretical transfer rate of 30 MB/s, and a Daisy chainable Optical Link (communication path which uses optical fiber cables as physical transmission line and CONET2 serial protocol) with a maximum theoretical transfer rate of 80 MB/s supported by CAEN A2818 PCI, A3818 PCIe controllers, and A4818 USB3 adapter (see **Tab. 1.1**).

A single link can connect up to 8 digitizers in Daisy chain, so a maximum of 8 boards can be Daisy chained by the single-link A2818 card or the A4818 adapter, and a maximum of 32 boards by the 4-link A3818 card (A3818C).

All the information on CAEN PCI/PCIe controllers and PCIe adapter can be found on CAEN website at the A2818, A3818, and A4818 pages.

The parameters for read/write accesses via optical link are Address Modifier, Base Address, Data Width, etc. Wrong parameter settings cause Bus Error.

Bit[3] at 0xEF00 register address enables the module to broadcast an interrupt request on the Optical Link (not supported on A4818); the enabled Optical Link Controllers propagate the interrupt on the PCI bus as a request from the Optical Link is sensed. Interrupts can also be managed at the CAENDigitizer library level **[RD4]**.

Note: CONET2 is CAEN proprietary serial protocol developed to communicate via the optical link between the host PC, equipped with a A2818 Controller, a A3818 Controller, or a A4818 Adapter, and CAEN CONET slaves. CONET2 is 50% more efficient in the data rate transfer than the previous CONET1 version. The two protocol versions are not compliant to each other and before to migrate from CONET1 to CONET2 it is recommended to read the instructions provided by CAEN in the dedicated Application Note **[RD9]**.

Note: The CONET protocol implemented in the A4818 adapter from USB-3.0 to Optical Link does not support the interrupts.

9.14 Trigger Rate

Introducing the trigger rate, it is worth remarking those features which are typical of the 742 digitizer family:

- The channels can only be enabled by 8-channel groups, not individually; each group counts on a 128-event or a 1024-event memory, depending on the board model (see **Tab. 1.1**); each event is composed by a number or samples of the digitized wave which are configurable as fixed values: 1024, 520, 256, or 136 samples.
- Due to the particular architecture of the analog-to-digital conversion based on switched-capacitors, there is a dead-time of 110 µs (if the TR fast local trigger is not digitized) or 181 µs (if TR is digitized).

The dead-time forces a ”peak” trigger rate, $\text{TRG-RATE}_{\text{peak}}$, which is:

$\text{TRG-RATE}_{\text{peak}} = \frac{1}{110}$ MHz $\simeq$ 9.09 kHz if TR is not digitized;

$\text{TRG-RATE}_{\text{peak}} = \frac{1}{181}$ MHz $\simeq$ 5.525 kHz if TR is digitized.

The dead-time represents the minimum time distance between a trigger event and the next one which makes the latter to be sensed and processed by the board. This means that a trigger occurring less than 110 µs after the last one in one case and less than 181 µs in the other will not be sensed, and the relevant event is lost (i.e. not stored in the digital memory and so not available for readout).

The ”peak” trigger rate is sustainable and valid only for the first 128 events (or 1024, in case of bigger size memory), then the reference becomes the ”average” trigger rate. Among the other things, the ”average” trigger rate is linked to the readout and represents the average data flow supported by the board without entering the memory full condition.

The ”average” trigger rate can only be computed theoretically, as it relies on the maximum transfer rate declared for the communication link being used, which is theoretical as well (i.e. guaranteed only under optimal conditions).

The board supports an Optical and a USB communication interface whose transfer rate specifications are:

- 80 MB/s for the Optical Link;
- 30 MB/s for the USB Link.

Basically, the ”average” trigger rate depends on multiple factors like the number of enabled channels, the size of the acquired wave, as well as the acquisition mode, and the readout software. The optimization of the code plays a critical role in the capability of getting the ”average” trigger rate the closer to its theoretical value. In this view, applying offline all the required corrections (see Sec. **9.6**) can help. Even data saving is a significant point, but it is of course an essential function of the software.

9.14.1 "Average" Trigger Rate Calculation

The "average" trigger rate can be computed by the following formula:

$$\frac{\text{TRANSFER\_RATE}}{\text{EVENT\_SIZE}} \tag{9.1}$$

where:

TRANSFER_RATE is the maximum theoretical declared for the specific communication link;
EVENT_SIZE is computed upon the event data format (refer to Sec. **9.7.2**).

For a single event of a x742 digitizer, the EVENT_SIZE is made of:

- 16 bytes from the HEADER field;
- 8 bytes per enabled channel group (i.e. the sum of EVENT DESCRIPTION field and GROUP EVENT TIME TAG field);
- $3 \cdot N_S \cdot 4$ bytes (N_S is the number of acquired samples; 1 sample is over 3 words that is to say 24 bytes).

In case the TR0 digitization is enabled, an additional factor of $\frac{3 \cdot N_S}{8} \cdot 4$ bytes must be considered.

The resulting EVENT_SIZE is finally:

$$\text{EVENT\_SIZE} = 16 + N_G \cdot \left[8 + 3 \cdot N_S \cdot 4 + \left(\frac{3 \cdot N_S}{8} \cdot 4 \right) \right] \text{Byte} \tag{9.2}$$

where N_G is the number of enabled channel groups.

The values of the theoretical "average" trigger rate, computed upon the formulas given above, are reported in the following tables for N_S = 1024 samples.

N_G	TR0 Not Digitized	TR0 Digitized
1	6.813 kHz	6.058 kHz
2	3.409 kHz	3.030 kHz

Tab. 9.3: Theoretical "average" trigger rate values for the Optical Link

N_G	TR0 Not Digitized	TR0 Digitized
1	2.556 kHz	2.272 kHz
2	1.278 kHz	1.136 kHz

Tab. 9.4: Theoretical "average" trigger rate values for the USB Link

10 Drivers & Libraries

10.1 Drivers

To interface with the board, CAEN provides Windows® and Linux® drivers for the different types of the supported physical communication links:

- **CONET Optical Link**, managed by the CAEN controllers A2818 (PCI) and A3818 (PCIe). The driver installation packages are downloadable for free on CAEN website at the A2818 and A3818 pages respectively (**login required**).

Note: For the installation of the Optical Link driver, refer to the controller User Manuals **[RD10]** and **[RD11]**.

- **USB 2.0 link**, the driver installation packages are downloadable for free on CAEN website at the digitizer page (**login required**).
- **USB 3.0 link**, managed by the A4818 Adapter. The driver installation packages (Windows users only) are downloadable for free on CAEN website at the A4818 page (**login required**).

Note: To install the USB link driver on Windows OS, refer to the dedicated Guide **[RD12]**. Linux users can follow the installation instructions of the ReadMe file included in the packet.

10.2 Libraries

CAEN libraries are a set of middleware software required by CAEN software tools for a correct functioning. These libraries, including also demo and example programs, represent a powerful base for users who want to develop customized applications for the digitizer control (communication, configuration, readout, etc.):

- **CAENDigitizer [RD4]** is a library of C functions specifically designed for the Digitizer families and supports both waveform recording and DPP firmware. The CAENDigitizer library is based on the CAENComm which, in turn, is based on CAENVMELib. For this reason, **the CAENVMELib and CAENComm libraries must be already installed on the host PC before installing the CAENDigitizer**.
- **CAENComm** library **[RD7]** manages the communication at low level (read and write access). The purpose of this library is to implement a common interface to the higher software layers, masking the details of the physical channel and its protocol, thus making the libraries and applications that rely on the CAENComm independent from the physical layer. **The CAENComm requires the CAENVMELib library (access to the VME bus), even in the cases where the VME is not used**.

Installation packages are available for free download on CAEN web site (*www.caen.it*) at each library page (**login required**).

WHEN TO INSTALL CAEN LIBRARIES:

WINDOWS® and LINUX® compliant customized software. The user must install the required libraries apart.

LINUX® compliant non-stand alone CAEN software. The user must install the required libraries apart to run the software.

CAENComm (and so the CAENDigitizer) supports the following communication channels (**Fig. 10.1**):

PC → USB → N6742

PC → PCI → A2818 → CONET → N6742

PC → PCIe → A3818 → CONET → N6742

PC → USB3 → A4818 → CONET → N6742

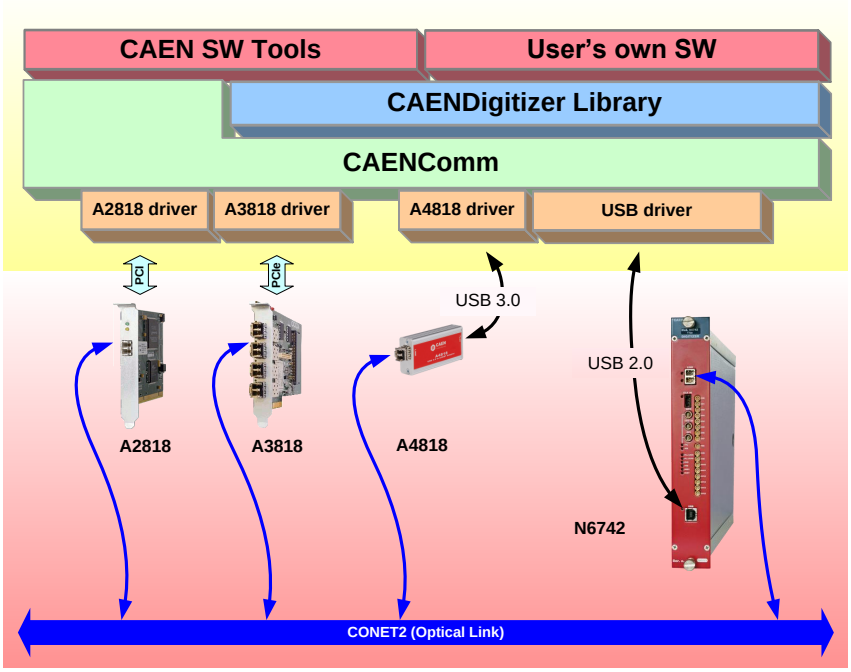


Fig. 10.1: Drivers and software layers

11 Software Tools

CAEN provides software tools to interface the 742 digitizer family, which are available for free download on CAEN web site (*www.caen.it*) in the software and firmware product pages **(login required).**

11.1 CAENUpgrader

CAENUpgrader is a software composed of command line tools together with a Java Graphical User Interface. With a x742 digitizer, CAENUpgrader allows the user to perform in a few easy steps:

- Upgrade the FPGA firmware of the board
- Read the FPGA firmware release of the board and the Controller (when included in the communication chain)
- Load a programming file to configure the internal PLL
- Get the Board Info file
- Manage the reboot of the FPGA firmware from the Backup or the Standard FLASH page.

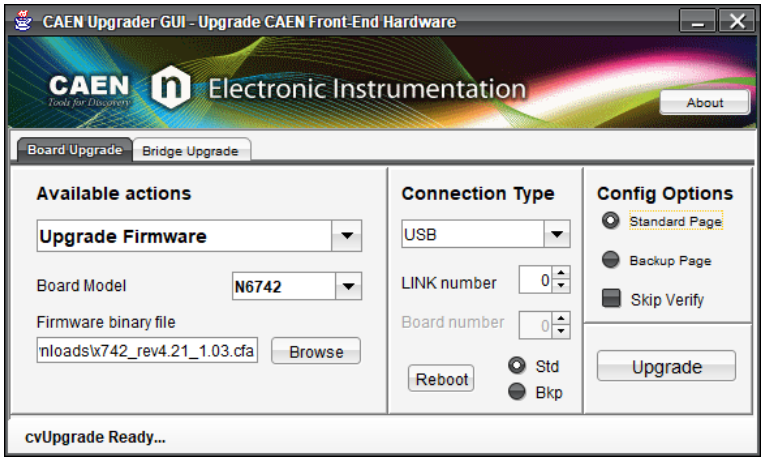


Fig. 11.1: CAENUpgrader Graphical User Interface

CAENUpgrader runs on Windows® and Linux® platforms, 32 and 64-bit operating systems. User must also install the required third-party Oracle Java RE 8 u40 or higher.

The software relies on the CAENComm library (see Chap. **10**).

Note: CAENUpgrader for Windows® is stand-alone, the user needs to install only the driver for the communication link, while the software locally installs the DLLs of the required libraries.
The Linux® version of the software needs the required CAENVME and CAENComm libraries to be installed apart by the user.

Refer to the CAENUpgrader documentation for installation instructions and for a detailed description **[RD2]**.

11.2 CAENComm Demo

CAENComm Demo is a simple program developed in C/C++ source code and provided both with Java™ and LabVIEW™ GUI interface. The demo mainly allows the user for a full board configuration at low level by direct read/write access to the registers, and may be used as a debug instrument.

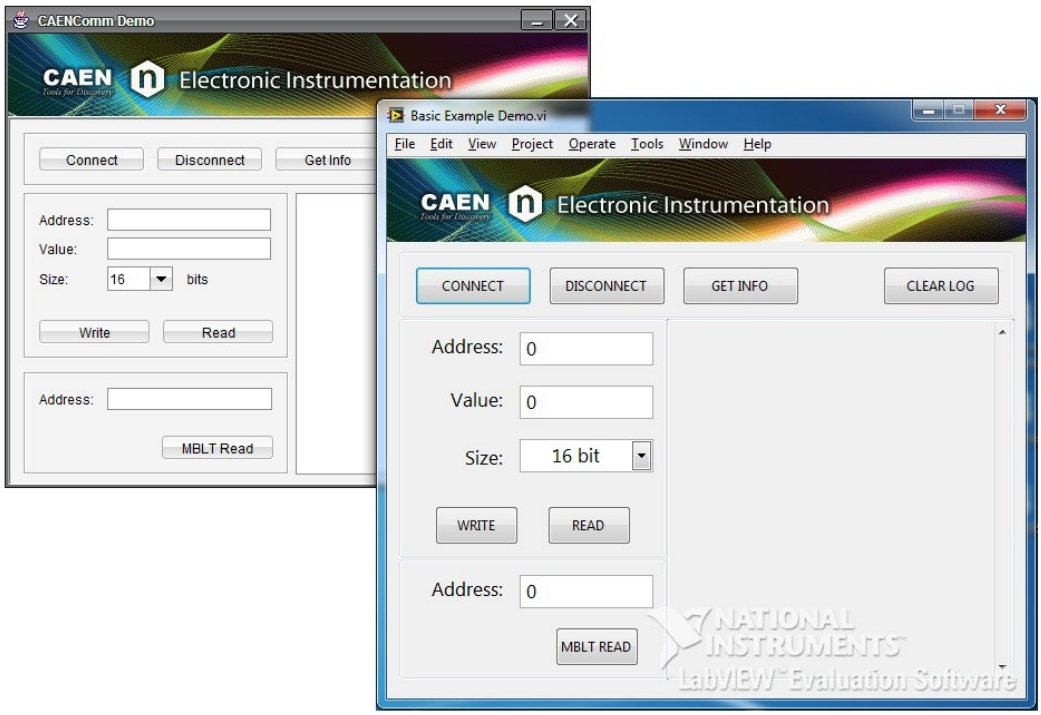


Fig. 11.2: CAENComm Demo Java™ and LabVIEW™ graphical interface

The Demo is included in the CAENComm library Windows® installation package only.

Refer to the CAENComm documentation for installation instructions and for a detailed description **[RD7]**.

11.3 CAEN WaveDump

WaveDump is a basic console application, with no graphics, supporting only CAEN digitizers running the waveform recording firmware. It allows the user to program a single board (according to a text configuration file containing a list of parameters and instructions), to start/stop the acquisition, read the data, display the readout and trigger rate, apply some post-processing (e.g. FFT and amplitude histogram), save data to a file and also plot the waveforms using Gnuplot third-party graphing utility (*www.gnuplot.info*).

WaveDump is a very helpful example of C code demonstrating the use of libraries and methods for an efficient readout and data analysis. Thanks to the included source files and the VS project, starting with this demo is strongly recommended to all those users willing to write the software on their own.

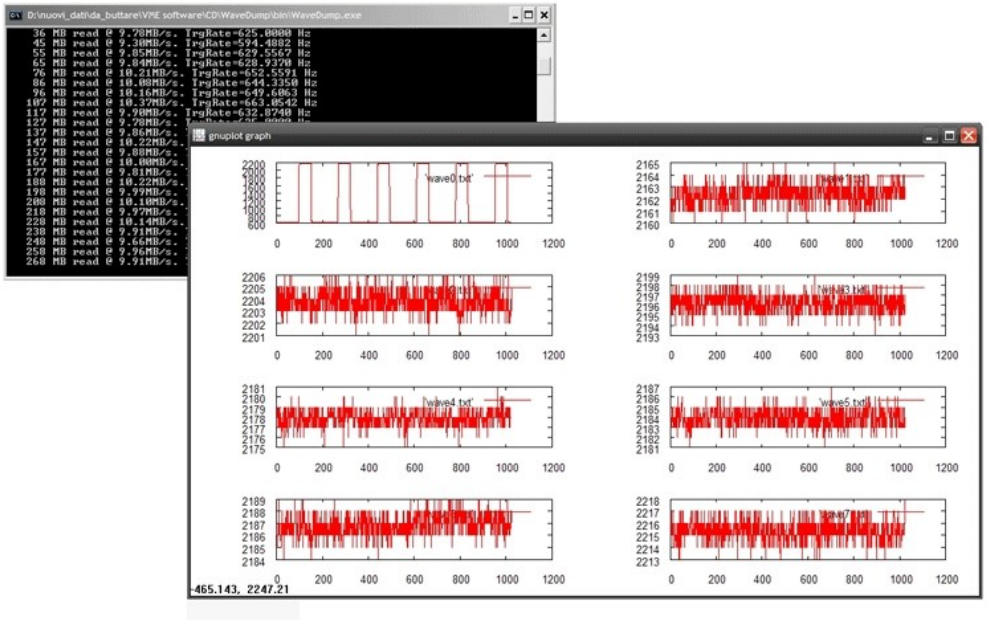


Fig. 11.3: CAEN WaveDump

CAEN WaveDump runs on Windows® and Linux® platforms; Linux users are required to install the third-party Gnuplot.

The software relies on the CAENDigitizer and CAENComm libraries (see Chap. **10**).

Note: WaveDump for Windows® is stand-alone, the user needs to install only the driver for the communication link, while the software locally installs the DLLs of the required libraries.
The Linux® version of the software needs the required CAENVMELib and CAENComm libraries to be installed apart by the user.

Refer to the WaveDump documentation for installation instructions and for a detailed description **[RD5] [RD8]**.

12 HW Installation

To power on the board, perform the following steps:

- Insert the N6742 into the crate - The Module fits into all NIM crates.
- Power up the crate.

ONLY QUALIFIED PERSONNEL SHOULD PERFORM INSTALLATION OPERATIONS

DO NOT INSTALL THE EQUIPMENT IN A SETUP WHERE IT IS DIFFICULT TO ACCESS THE BACK PANEL FOR DISCONNECTING THE DEVICE

IT IS RECOMMENDED THAT THE SWITCH OR CIRCUIT-BREAKER IS NEAR THE EQUIPMENT

THE SAFETY OF ANY SYSTEM THAT INCORPORATES THE DEVICE IS UNDER THE RESPONSIBILITY OF THE ASSEMBLER OF THE SYSTEM

12.1 Power-on Status

Power-on takes few seconds during which the front panel LEDs may flash.

At power-on, the module is in the following status:

- The Output Buffer is cleared;
- Registers are set to their default configuration;
- Only NIM and PLL LOCK LEDs must stay on (see **Fig. 12.1**).

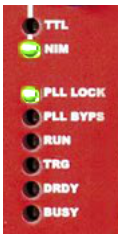


Fig. 12.1: Front panel LEDs status at power-on

13 Firmware and Upgrades

The board hosts one FPGA on the mainboard and one FPGA on the mezzanine (i.e. one FPGA manages 16+1 channels). The channel FPGAs firmware is identical. A unique file is provided that will update all the FPGAs at the same time.

ROC FPGA MAINBOARD FPGA (Readout Controller + Communication Interface):

FPGA Altera Cyclone EP1C20.

AMC FPGA MEZZANINE FPGA (ADC readout/Memory Controller):

FPGA Altera Cyclone EP3C16

The firmware is stored onto the on-board FLASH memory. Two copies of the firmware are stored in two different pages of the FLASH, referred to as Standard (STD) and Backup (BKP). In case of waveform recording firmware, the board is delivered equipped with the same firmware version on both pages.

At power-on, a microcontroller reads the FLASH memory and programs the module automatically loading the first working firmware copy, that is the STD one by default in normal operating.

It is possible to upgrade the board firmware via USB or Optical Link by writing the FLASH with the CAENUpgrader software (see Chap. **11**).

IT IS STRONGLY SUGGESTED TO OPERATE THE DIGITIZER UPON THE STD COPY OF THE FIRMWARE. UPGRADES ARE SO RECOMMENDED ONLY ON THE STD PAGE OF THE FLASH. THE BKP COPY IS TO BE INTENDED ONLY FOR RECOVERY USAGE. IF BOTH PAGES RESULT CORRUPTED, THE USER WILL NO LONGER BE ABLE TO UPLOAD THE FIRMWARE VIA USB OR OPTICAL LINK AGAIN AND THE BOARD NEEDS TO BE SENT TO CAEN FOR REPAIR!

13.1 Firmware Updates

Firmware updates are available for download on CAEN web site (*www.caen.it*) at the digitizer page (**login required**). The waveform recording is free firmware and updates are free downloadable.

13.2 Firmware File Description

The programming file is a CFA file (CAEN Firmware Archive). It is an archiving file format that aggregates all the programming files of the same firmware kind which are compatible with the same digitizer family.

The name of the CFA file follows a general convention:

- *<DIGITIZER>*_rev_X.Y_W.Z.CFA for the waveform recording firmware

where:
<DIGITIZER> are all the boards that can be updated by the CFA file;

options are:

- x742 (includes x742, x742B module versions);
  where x = DT5 for desktop, x = N6 for NIM, x = V1/VX1 for VME64/VME64x format;

X.Y is the major/minor revision number of the ROC FPGA;

W.Z is the major/minor revision number of the AMC FPGA.

13.3 Troubleshooting

In case of upgrade failure (e.g. STD FLASH page is corrupted), the user can try to reboot the board: after a power cycle, the system programs the board automatically from the alternative FLASH page (e.g. BKP FLASH page), if this is not corrupted as well (see Sec. **12.1**). The user can so perform a further upgrade attempt on the STD page to restore the firmware copy.

OLD FLASH MEMORIES

The STD and BKP firmware copy management by the onboard microcontroller is different in case of old versions of the digitizer motherboard, which mount a smaller size of the FLASH memory.

To know the size of the digitizer FLASH memory, there are two options:

- read access to the 0xF050 register (”0” means small size);
- look at the board info file generated by the Get Information function of CAENUpgrader revision 1.6.0 or higher **[RD2]** (FLASH TYPE = 0 means small size).

In event of an upgrade failure of the STD page occurs, the following recovery procedure can be performed:

- make sure to use the USB communication link;
- use the Reboot function of CAENUpgrader with the BKP setting to reboot from the BKP page firmware copy of the FLASH: LED status must be like in Sec. **12.1**;
- to check if the communication works, read out the firmware revision by the Get firmware Revision function of CAENUpgrader;
- in case of success, make a new attempt to **upgrade the STD page of the FLASH** with the proper programming file;
- wait until the process is successfully completed, then use the Reboot function of CAENUpgrader with the STD setting to reboot from the STD page firmware copy of the FLASH;
- if the LED status is like in Sec. **12.1**, then you can normally operate the board again.

When not connecting to the board neither by the STD nor the BKP page reboot, it is recommended to contact CAEN to send the board back for repair (see Chap. **17**).

14 Instructions for Cleaning

The equipment may be cleaned with isopropyl alcohol or deionized water and air dried. Clean the exterior of the product only.
Do not apply cleaner directly to the items or allow liquids to enter or spill on the product.

14.1 Cleaning the Touchscreen

To clean the touchscreen (if present), wipe the screen with a towelette designed for cleaning monitors or with a clean cloth moistened with water.
Do not use sprays or aerosols directly on the screen; the liquid may seep into the housing and damage a component. Never use solvents or flammable liquids on the screen.

14.2 Cleaning the Air Vents

It is recommended to occasionally clean the air vents (if present) on all vented sides of the board. Lint, dust, and other foreign matter can block the vents and limit the airflow. Be sure to unplug the board before cleaning the air vents and follow the general cleaning safety precautions.

14.3 General Cleaning Safety Precautions

CAEN recommends cleaning the device using the following precautions:

- Never use solvents or flammable solutions to clean the board.
- Never immerse any parts in water or cleaning solutions; apply any liquids to a clean cloth and then use the cloth on the component.
- Always unplug the board when cleaning with liquids or damp cloths.
- Always unplug the board before cleaning the air vents.
- Wear safety glasses equipped with side shields when cleaning the board.

15 Device Decommissioning

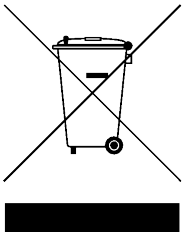
After its intended service, it is recommended to perform the following actions:

- Detach all the signal/input/output cable
- Wrap the device in its protective packaging
- Insert the device in its packaging (if present)

THE DEVICE SHALL BE STORED ONLY AT THE ENVIRONMENT CONDITIONS SPECIFIED IN THE MANUAL, OTHERWISE PERFORMANCES AND SAFETY WILL NOT BE GUARANTEED

16 Disposal

The disposal of the equipment must be managed in accordance with Directive 2012/19 / EU on waste electrical and electronic equipment (WEEE).



The crossed bin symbol indicates that the device shall not be disposed with regular residual waste.

17 Technical Support

To contact CAEN specialists for requests on the software, hardware, and board return and repair, it is necessary a MyCAEN+ account on www.caen.it:

https://www.caen.it/support-services/getting-started-with-mycaen-portal/

All the instructions for use the Support platform are in the document:

A paper copy of the document is delivered with CAEN boards.
The document is downloadable for free in PDF digital format at:

https://www.caen.it/wp-content/uploads/2022/11/Safety_information_Product_support_W.pdf

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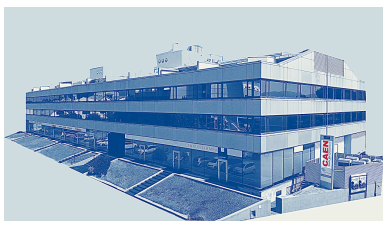

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UM4295 - N6742 - 16+1 Channel 12 bit 5 GS/s Switched Capacitor Digitizer rev. 12 - June 21st, 2023 00103/9:N6742.MUTX/12