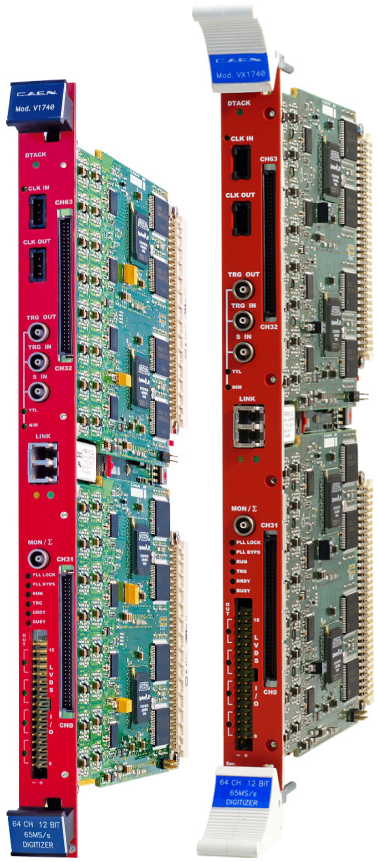
Rev. 21 - December 10th, 2024

V1740/VX1740

64 Channels 12bit 62.5 MS/s Digitizer



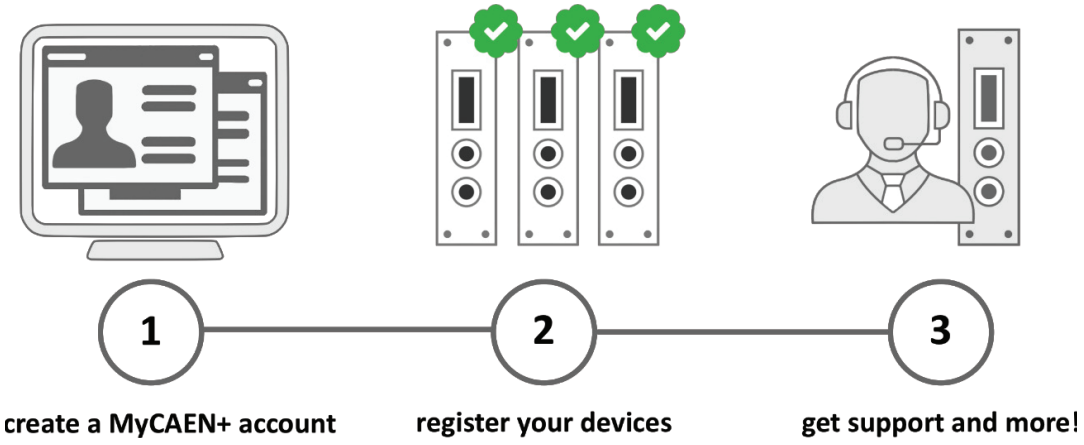
CAEN
Tools for Discovery

User Manual
UM3050

Register your device

Register your device to your **MyCAEN+** account and get access to our customer services, such as notification for new firmware or software upgrade, tracking service procedures or open a ticket for assistance. **MyCAEN+** accounts have a dedicated support service for their registered products. A set of basic information can be shared with the operator, speeding up the troubleshooting process and improving the efficiency of the support interactions.

MyCAEN+ dashboard is designed to offer you a direct access to all our after sales services. Registration is totally free, to create an account go to https://www.caen.it/become-mycaenplus-user and fill the registration form with your data.



https://www.caen.it/become-mycaenplus-user/

Purpose of this Manual

This document contains the full hardware description of the V1740 and VX1740 CAEN digitizers operating as **Waveform Recording Digitizer** (i.e running on the hereafter called **"waveform recording firmware"**).
The reference firmware revision is: **4.29_0.13**.
For higher releases compatibility, check in the firmware revision history files.
For any reference to registers in this user manual, please refer to document [RD1] on the digitizer web page.
For any reference to DPP firmware in this user manual, please refer to document [RD2] present on the firmware web page.

Change Document Record

Date	Revision	Changes
-	00-19	Old manuals are available on request (see Chap. **17**).
Jun 07th, 2018	20	Revised layout and improved contents. Updated Sec. **13.1.1** , Sec. **9.10.3**
Dec 10th, 2024	21	Reviewed Cover and End pages. Replaced references to CAENUpgrader with CAENToolbox. Updated **Safety Notices**, Tab. **1.1**, Chap. **4**, Tab. **6.1**, Sec. **8.1**, Sec. **9.4**, Sec. **9.7.1**, Sec. **9.7.4.1**, Sec. **9.8.2**, Sec. **9.10**, Fig. **9.14**, Sec. **9.13.3**, Sec. **9.16**, Chap. **10**, Chap. **11**, Chap. **12**, Sec. **13.2**, Chap. **17**. Added Chap. **5**, Chap. **7**, Note in Sec. **9.7.4.3**, Chap. **14**, Chap. **15**, Chap. **16**.

Symbols, Abbreviated Terms, and Notations

ADC	Analog-to-Digital Converter
AMC	ADC & Memory Controller
DAQ	Data Acquisition
DAC	Digital-to-Analog Converter
DC	Direct Current
LVDS	Low-Voltage Differential Signal
PLL	Phase-Locked Loop
ROC	ReadOut Controller
TTT	Trigger Time Tag
USB	Universal Serial Bus

Reference Documents

[RD1] UM5483 – 740 Registers Description
[RD2] UM4874 – DPP-QDC User Manual
[RD3] UM11111 – CAEN Toolbox User Manual
[RD4] Precautions for Handling, Storage and Installation
[RD5] AN6308 – Downsampling measurements with CAEN Digitizer 720/724/740/751 families
[RD6] GD2817 – How to make coincidences with CAEN digitizers

[RD7] AN2086 – Synchronization of a multi-board acquisition systems with CAEN digitizers
[RD8] UM1935 – CAENDigitizer User & Reference Manual
[RD9] AN2472 – CONET1 to CONET2 migration
[RD10] UM3121 A3818 Technical Information Manual
[RD11] UM10551 A5818 Technical Information Manual
[RD12] UM7685 - V3718 & VX3718 User & Reference Manual
[RD13] UM8305 - V4718 & VX4718 User & Reference Manual
[RD14] DS7799 A4818 Adapter Data Sheet
[RD15] UM1934 – CAENComm User & Reference Manual
[RD16] GD9764 – CAEN FELib Library User Guide
[RD17] UM2091 – CAEN WaveDump User Manual
[RD18] UM7934 – CAEN WaveDump2 User Manual
[RD19] UM5960 – CoMPASS User Manual

All CAEN documents can be downloaded at: *http://www.caen.it/csite/LibrarySearch.jsp*

Manufacturer Contacts

CAEN S.p.A.
Via Vetraia, 11 55049 Viareggio (LU) - ITALY
Tel. +39.0584.388.398 Fax +39.0584.388.959
www.caen.it | info@caen.it

Limitation of Responsibility

If the warnings contained in this manual are not followed, CAEN will not be responsible for damage caused by improper use of the device. The manufacturer declines all responsibility for damage resulting from failure to comply with the instructions for use of the product. The equipment must be used as described in the user manual, with particular regard to the intended use, using only accessories as specified by the manufacturer. No modification or repair can be performed.

Disclaimer

The information contained herein has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies. CAEN SpA reserves the right to modify its products specifications without giving any notice; for up to date information please visit www.caen.it.

Made in Italy

We remark that all our boards have been designed and assembled in Italy. In a challenging environment where a competitive edge is often obtained at the cost of lower wages and declining working conditions, we proudly acknowledge that all those who participated in the production and distribution process of our devices were reasonably paid and worked in a safe environment (while this is true for the boards marked ”MADE IN ITALY”, we cannot guarantee for third-party manufactures).

Index

List of Figures

List of Tables

Safety Notices

N.B. Read carefully the "Precautions for Handling, Storage and Installation document provided with the product before starting any operation.

The following HAZARD SYMBOLS may be reported on the unit:

	Caution, refer to product manual
	Caution, risk of electrical shock
	Protective conductor terminal
	Earth (Ground) Terminal
	Alternating Current
	Three-Phase Alternating Current

The following symbol may be reported in the present manual:

	General warning statement

The symbol could be accompanied by the following terms:

- **DANGER**: indicates a hazardous situation which, if not avoided, will result in serious injury or death.
- **WARNING**: indicates a hazardous situation which, if not avoided, could result in death or serious injury.
- **CAUTION**: indicates a situation or condition which, if not avoided, could cause physical injury or damage the product and / or the surrounding environment.

CAUTION: To avoid potential hazards

USE THE PRODUCT ONLY AS SPECIFIED.
ONLY QUALIFIED PERSONNEL SHOULD PERFORM SERVICE PROCEDURES

CAUTION: Avoid Electric Overload

TO AVOID ELECTRIC SHOCK OR FIRE HAZARD, DO NOT POWER A LOAD OUTSIDE OF ITS SPECIFIED RANGE

CAUTION: Avoid Electric Shock

TO AVOID INJURY OR LOSS OF LIFE, DO NOT CONNECT OR DISCONNECT CABLES WHILE THEY ARE CONNECTED TO A VOLTAGE SOURCE

CAUTION: Do Not Operate without Covers

TO AVOID ELECTRIC SHOCK OR FIRE HAZARD, DO NOT OPERATE THIS PRODUCT WITH COVERS OR PANELS REMOVED

CAUTION: Do Not Operate in Wet/Damp Conditions

TO AVOID ELECTRIC SHOCK, DO NOT OPERATE THIS PRODUCT IN WET OR DAMP CONDITIONS

CAUTION: Do Not Operate in an Explosive Atmosphere

TO AVOID INJURY OR FIRE HAZARD, DO NOT OPERATE THIS PRODUCT IN AN EXPLOSIVE ATMOSPHERE

THIS DEVICE SHOULD BE INSTALLED AND USED BY SKILLED TECHNICIAN ONLY OR UNDER HIS SUPERVISION

DO NOT OPERATE WITH SUSPECTED FAILURES.
IF YOU SUSPECT THIS PRODUCT TO BE DAMAGED, PLEASE CONTACT THE TECHNICAL SUPPORT

See Chap. **17** for the Technical Support contacts.

CAUTION: This product needs proper cooling.

USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEATING MAY DEGRADE THE MODULE PERFORMANCES

V1740 DIGITIZERS CANNOT BE OPERATED WITH CAEN CRATES VME8001, VME8002, VME8004, AND VME8004A. OVERHEAT MAY DAMAGE THE MODULE

CAUTION: This product needs proper handling.

THE VME DIGITIZER DOES NOT SUPPORT LIVE INSERTION (HOT-SWAP)
REMOVE OR INSERT THE BOARD WHEN THE CRATE IS POWERED OFF

ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE

1 Introduction

The V1740 is a 1-unit wide VME 6U module housing a 64 Channel 12 bit 62.5 MS/s Flash ADC Waveform Digitizer with 2 V_{pp} input dynamic range on single ended ERNI SMC input connectors. A 10-V_{pp} version is available, as well as an external adaptor from ERNI to LEMO inputs (see Tab. **1.1**).

The DC offset is adjustable via a 16-bit DAC on each channel in the full scale range.

Because of the high channel density and channel to ADC chip ratio, most channel settings are common to ”groups” of 8 adjacent channels.

Considering the sampling frequency and bit number, these digitizers are well suited for mid-slow signals as the ones coming from inorganic scintillators coupled with PMTs, gaseous detectors and others.

The acquisition trigger is common to all the channels and it can be issued externally (on TRG-IN), via software, or upon the channel self-trigger (when the input signal goes under/over a programmable threshold). The common acquisition trigger from the board can be propagated out through a dedicated front panel connector (TRG-OUT).

During the acquisition, data stream is continuously written in a circular memory buffer. When the trigger occurs, the digitizer writes further samples for the post trigger and freezes the buffer that can be read by one of the provided readout links.

Each channel has a SRAM digital memory (see Tab. **1.1** for a selection of the available sizes) divided into buffers of programmable size (1 ÷ 1024). The readout of a frozen buffer is independent from the write operations in the active circular buffer (ADC data storage).

A dedicated front panel connector (CLK-IN) and the internal PLL allow for clock synthesis from internal/external references.

V1740 is well suited for multi-board synchronization, where all V1740 can be synchronized to a common clock source ensuring Trigger Time Stamps and data alignment coherently across multiple V1740 boards. Clock distribution is supported by daisy chain on front panel connectors (CLK-IN / CLK-OUT).

16 FPGA-controlled general purpose LVDS I/Os can be programmed for Run, Busy, Veto, Trigger and other useful management. An Input Pattern (external signal) can be provided on the LVDS I/Os to be latched to each trigger as an event marker (see Sec. **9.10**).

An analog output (MON/Σ) from internal 12-bit 125-MHz DAC, controlled by the FPGA, allows the user to reproduce four types of outgoing information: Trigger Majority, Test Pulses, Memory Occupancy, Voltage Level (see Sec. **9.11**).

V1740 is equipped with a VME64 interface (VM64X in case of VX1740) where the data readout can be performed in Single Data Transfer (D32), 32/64-bit Block Transfer (BLT, MBLT, 2eVME. 2eSST) and 32/64-bit Chained Block Transfer (CBLT).

The module houses Optical Link interface (CAEN proprietary CONET protocol) supporting transfer rate up to 80 MB/s and offers daisy chain capability. Therefore, it is possible to connect up to 8 ADC modules to a single A2818 Optical Link Controller or A4818 adapter, while up to 32 using a 4-link A3818 version or A5818 card (see Tab. **1.1**). VME and Optical Link accesses take place on independent paths and are handled by the on-board controller, therefore when accessed through Optical Link the board can be operated outside the VME Crate.

Only the V1740D version, in addition to the waveform recording firmware, can run Digital Pulse Processing firmware for the Charge to Digital Conversion (DPP-QDC) [RD2], which combines the functions of a Single Gate QDC plus Discriminator and Gate Generator. This special firmware makes the digitizer an enhanced system for Physics Applications.

Board Model	Description
V1740	64 Ch. 12 bit 62.5 MS/s Digitizer: 192 kS/ch, EP3C16, SE
V1740A	64 Ch. 12 bit 62.5 MS/s Digitizer: 10 V_{pp} input range, 1.5 MS/ch, EP3C16, SE
V1740B	64 Ch. 12 bit 62.5 MS/s Digitizer: 1.5 MS/ch, EP3C16, SE
V1740C	64 Ch. 12 bit 62.5 MS/s Digitizer: 10 V_{pp} input range, 192 kS/ch, EP3C16, SE
V1740D	64 Ch. 12 bit 62.5 MS/s Digitizer: 192 kS/ch, EP3C40, SE
VX1740	64 Ch. 12 bit 62.5 MS/s Digitizer: 192kS/ch, EP3C16, SE
VX1740A	64 Ch. 12 bit 62.5 MS/s Digitizer: 10 V_{pp} input range, 1.5 MS/ch, EP3C16, SE
VX1740B	64 Ch. 12 bit 62.5 MS/s Digitizer: 1.5 MS/ch, EP3C16, SE
VX1740C	64 Ch. 12 bit 62.5 MS/s Digitizer: 10 V_{pp} input range, 192 KS/ch, EP3C16, SE
VX1740D	64 Ch. 12 bit 62.5 MS/s Digitizer: 192kSch, EP3C40, SE
DPP Firmware	**Description**
DPP-QDC 64 ch	DPP-QDC- Digital Pulse Processing for Time Stamped Digital QDC (64 ch x 740)
Related Products	**Description**
A2818	A2818 – PCI Optical Link (Obsolete)
A3818A	A3818A – PCIe 1 Optical Link
A3818B	A3818B – PCIe 2 Optical Link
A3818C	A3818C – PCIe 4 Optical Link
A4818	A4818 - USB3 to Conet2 Adapter
A5818	A5818 – PCIe 4 Optical Link, Gen. 3
V3718	V3718 - VME-USB Bridge
VX3718	VX3718 - VME-USB Bridge
V4718	V4718 - VME64-USB 3.0, Ethernet and Optical Link Bridge
VX4718	VX4718 - VME64-USB 3.0, Ethernet and Optical Link Bridge
Accessories	**Description**
DT4700	Clock Generator and FAN-OUT
A746B	64ch Adapter for LEMO connector
A316	2-pin Cable for LVDS I/Os
A317	Clock Distribution Cable
A318	SE to Differential Clock Adapter
A654	Single Channel MCX to LEMO Cable Adapter
A654 KIT4	4 MCX TO LEMO Cable Adapter
A654 KIT8	8 MCX TO LEMO Cable Adapter
A659	Single Channel MCX to BNC Cable Adapter
A659 KIT4	4 MCX TO BNC Cable Adapter
A659 KIT8	8 MCX TO BNC Cable Adapter
AI2740	Optical Fibre 40 m simplex
AI2730	Optical Fibre 30 m simplex
AI2720	Optical Fibre 20 m simplex
AI2705	Optical Fibre 5 m simplex
AI2703	Optical Fibre 30 cm simplex
AY2730	Optical Fibre 30 m duplex
AY2720	Optical Fibre 20 m duplex
AY2705	Optical Fibre 5 m duplex

Tab. 1.1: Table of versions and related items

2 Block Diagram

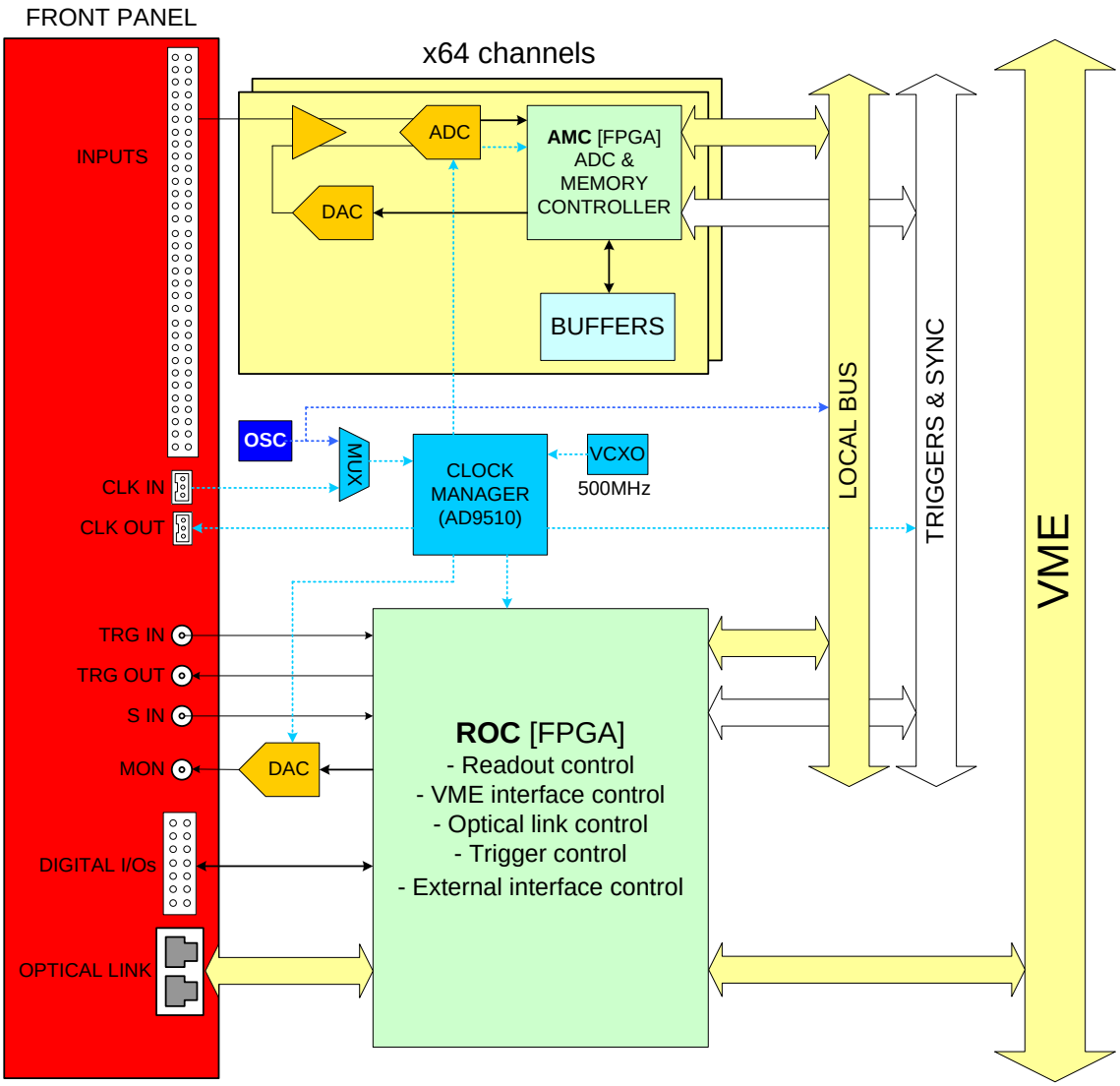


Fig. 2.1: Block Diagram

3 Technical Specifications

GENERAL	**Form Factor** 1-unit wide, 6U VME64 (V1740) and VME64X (VX1740)		**Weight** 535 g
ANALOG INPUT	**Channels** 64 channels Single ended **Impedance (Z_{in})** 50 Ω @2V_{pp} 1 kΩ @10V_{pp}	**Connector** 64-pin Dual Row ERNI SMC **Full Scale Range (FSR)** 2 V_{pp} or 10 V_{pp} **Abs Max Rating (@2V_{pp})** 6 V_{pp} (with V_{rail} max +6 V or –6 V) for any DAC offset value	**Bandwidth** 30 MHz **Offset** Programmable DAC for DC offset adjustment on each channel in the full range (±1V@2V_{pp} ±5V@10V_{pp})
DIGITAL CONVERSION	**Resolution** 12 bits	**Sampling Rate** 62.5 MS/s simultaneously on each channel	
SYSTEM PERFORMANCE	**ENOB** 11.20 (48 kS Buffer) **SINAD** 69.20 dB (48 kS Buffer, open input)	**THD** 87.10 dB **SFDR** 94.9 dB	**SIGMA** 0.50 LSB rms
ADC SAMPLING CLOCK GENERATION	Clock source: internal/external On-board programmable PLL provides generation of the main board clocks from an internal (50 MHz local Oscillator) or external (front panel CLK-IN connector) reference		
DIGITAL I/O	**CLK-IN (AMP Modu II)** AC coupled differential input clock: LVDS, ECL, PECL, LVPECL, CML Z_{diff} = 100 Ω Accuracy < 100 ppm **TRG-IN (LEMO)** External trigger or veto digital input: NIM/TTL Signal Width > 8 ns Z_{in} = 50 Ω	**CLK-OUT (AMP Modu IV)** DC coupled differential LVDS clock output locked to ADC sampling clock, Z_{diff} = 100 Ω **TRG-OUT (LEMO)** Multipurpose digital output (e.g. trigger, busy): NIM/TTL R_t = 50 Ω	**S-IN (LEMO)** SYNC/START front panel digital input NIM/TTL Signal Width > 8 ns Z_{in} = 50 Ω
MEMORY	192k sample/ch or 1.5M sample/ch Multi Event Buffer divisible into 1 ÷ 1024 Independent read and write access Programmable event size and pre/post trigger		
TRIGGER	**Trigger Source** - *Self-trigger*: channel over/under-threshold for common (waveform recording firmware) or individual (DPP firmware only) trigger generation - *External-trigger*: common trigger by TRG IN connector or individual by LVDS connector (DPP firmware only) - *Software-trigger*: common trigger by software command		**Trigger Propagation** TRG-OUT programmable digital output **Trigger Time Stamp** *Waveform recording FW*: 31-bit counter – 16 ns resolution - 17 s range; 48 bit fw extension *DPP-QDC*: 32-bit counter – 16 ns resolution - 68 s range; 48 bit fw extension; 64 bit sw extension

SYNCHRONIZATION	**Clock Propagation** *Daisy chain*: through CLK-IN/CLK-OUT connectors *One-to-many*: clock distribution from an external clock source on CLK-IN connector Clock Cable delay compensation	**Acquisition Synchronization** Sync, Start/Stop through digital I/O (S-IN or TRG-IN input / TRG-OUT output) **Trigger Time Stamps Alignment** By S-IN input connector
ADC & MEMORY CONTR.	Altera Cyclone EP1C16 or EP1C40 (V1740D); one FPGA serves 16 channels	
COMMUNICATION INTERFACE	**Optical Link** CAEN CONET proprietary protocol Up to 80 MB/s transfer rate Daisy-chain: it is possible to connect up to 8 or 32 ADC modules to a single Optical Link Controller (respectively A2818/A4818 or A3818/A5818)	**VME** VME 64X compliant Data transfer mode: BLT32, MBLT64 (70 MB/s using CAEN Bridge), CBLT32/64, 2eVME, 2eSST (up to 200 MB/s)
ANALOG MONITOR	12-bit / 125 MHz DAC FPGA controlled; operating modes: - Test pulses: 1 V_{pp} ramp generator - Majority signal: proportional to the nr. Of channels under/over threshold (steps of 125 mV) - Memory Occupancy signal: proportional to the Multi Event Buffer Occupancy (1 buffer 1mV) - Voltage level: programmable output voltage level	
LVDS I/O	16 general purpose LVDS I/O controlled by the FPGA: Run, Busy, Veto, Trigger and other functions can be programmed An Input Pattern from the LVDS I/O can be associated to each trigger as an event marker	
DPP FW SUPPORTED	DPP-QDC for the Charge to Digital Conversion (V1740D and VX1740D only)	
FIRMWARE UPGRADE	Firmware can be upgraded via VMEbus/Optical Link	
SOFTWARE	General purpose C libraries, configuration tools, readout software (Windows® and Linux® support), LabVIEW™ VIs and demos for Windows® only	
POWER CONSUMPTIONS	V1740: 4.5 A @ +5V; 250 mA @ +12V, -12V not used V1740D: 4.9 A @ +5V; 250 mA @ +12V, -12V not used	

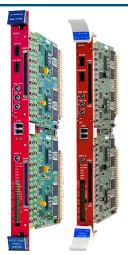
Tab. 3.1: Specification table

4 Packaging and Compliancy

The V1740/VX1740 digitizer modules are available in 1-unit wide VME64/VME64X boards, EMC compliant.

The devices are inspected by CAEN before the shipment, and they are guaranteed to leave the factory free of mechanical or electrical defects.

The content of the delivered package standardly consists of the part list shown in the table below (**Tab. 4.1**).

	Part	Description	Qt
	V1740/VX1740	64 Channels 12bit 62.5 MS/s Digitizer	x1
	Documentation	UM3050 - V1740/VX1740 User Manual	-

Tab. 4.1: Delivered kit content.

CAUTION: to manage the product, consult the operating instructions provided.

When receiving the unit, the user is strictly recommended to:

- Inspect containers for damage during shipment. Report any damage to the freight carrier for possible insurance claims.
- Check that all the components received match those listed on the enclosed packing list as in **Tab. 4.1** . (CAEN cannot accept responsibility for missing items unless any discrepancy is promptly notified.)
- Open shipping containers; be careful not to damage contents.
- Inspect contents and report any damage. The inspection should confirm that there is no exterior damage to the unit such as broken knobs or connectors and that the front panel is not scratched or cracked. Keep all packing material until the inspection has been completed.
- If damage is detected, file a claim with carrier immediately and notify CAEN service (see Chap. **17**).
- If equipment must be returned, carefully repack equipment in the original shipping container with original packing materials, if possible. Please contact CAEN service.
- If equipment is not installed when unpacked, place equipment in original shipping container and store in a safe place until ready to install.

DO NOT SUBJECT THE ITEM TO UNDUE SHOCK OF VIBRATIONS

DO NOT BUMP, DROP OR SLIDE SHIPPING CONTAINERS

DO NOT LEAVE ITEMS OR SHIPPING CONTAINERS UNSUPERVISED IN AREAS WHERE UNTRAINED PERSONNEL MAY MISHANDLE THE ITEMS

USE ONLY ACCESSORIES WICH MEET THE MANUFACTURER SPECIFICATIONS

For a correct and safe use of the module, refer to Chap. **6** and **7**.

5 PID (Product Identifier)

PID is the CAEN product identifier, an incremental number greater than 10000 that is unique for each product[1]. The PID is on a label affixed to the product (**Fig. 5.1**) and it is even stored in an on-board non-volatile memory readable at bit [7:0] of registers 0xF080 or 0xF084 **[RD1]**. The PID information is also available through CAENToolbox Software (for more details refer to **[RD3]**).

Note: The serial number is still valid to identify older boards, where the PID label is not present.

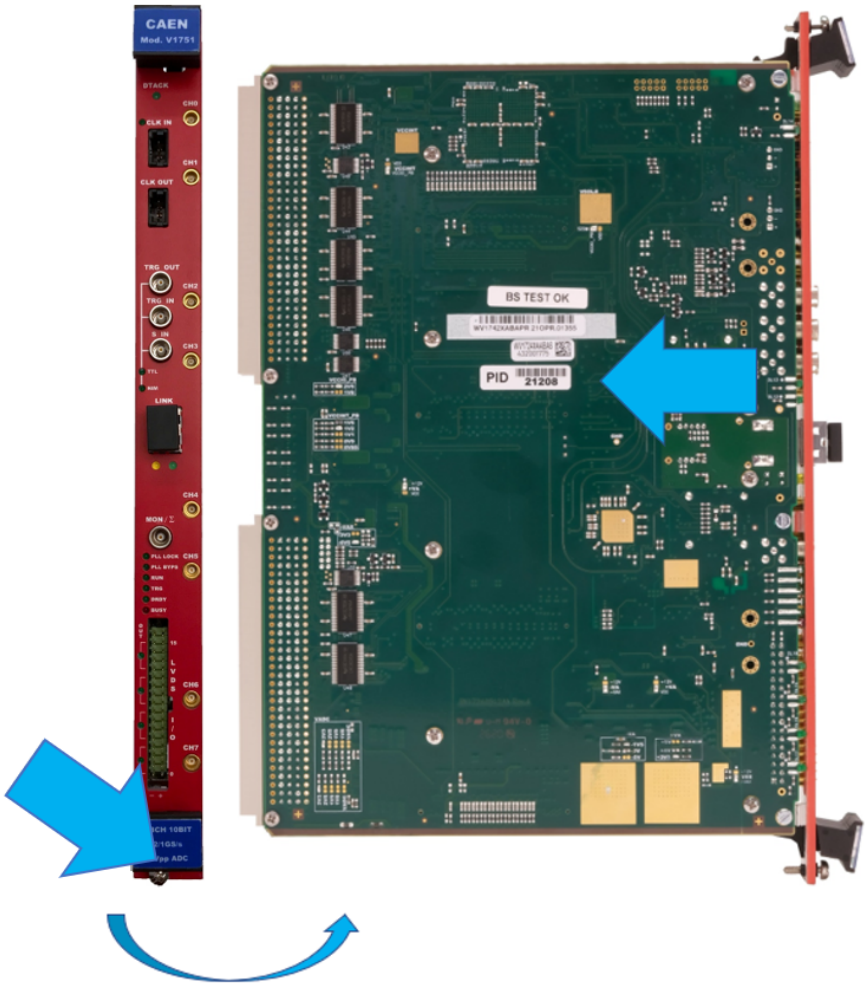


Fig. 5.1: PID location on VME digitizers (the device model and the number in the picture are purely indicative).

[1]The PID substitutes the serial number previously identifying the boards.

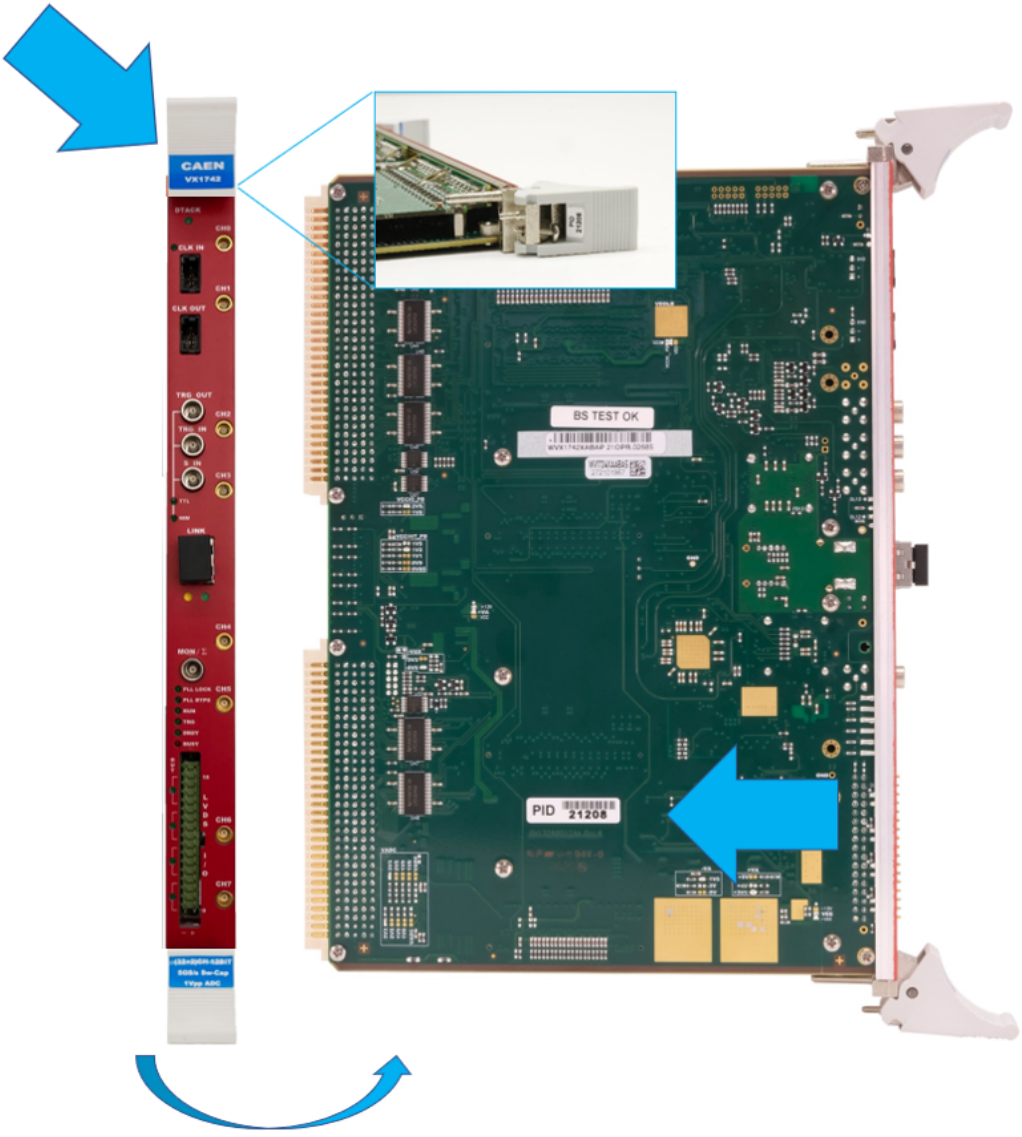


Fig. 5.2: PID location on VMEX digitizers (the device model and the number in the picture are purely indicative).

6 Power Requirements

The table below resumes the V1740/VX1740 power consumptions per relevant power supply rail.

MODULE	SUPPLY VOLTAGE		
	+5 V	+12 V	-12 V
V1740/VX1740	4.5 A	250 mA	Not used
V1740D/VX1740D	4.9 A	250 mA	Not used

Tab. 6.1: Power requirements table

Note: The reported power requirements are different in case of old motherboard revisions (rev.3 or lower). The revision number can be read at 0xF04C register. Please, contact CAEN for old power consumption specifications.

7 Cooling Management

The V1740/VX1740 Digitizers can operate in the temperature range 0° ÷ +40°C **[RD4]**.

The VME models must be operated in ventilated crates as recommended in the **Safety Notices**.

EXTERNAL FANS MUST BE USED WHEN THE BOARD IS INSTALLED IN A SETUP WITH POOR AIR FLOW

V1740 DIGITIZERS CANNOT BE OPERATED WITH CAEN CRATES VME8001, VME8002, VME8004, AND VME8004A. OVERHEAT MAY DAMAGE THE MODULE

The User must take care to provide a proper cooling to the board with external fan if the board is used in an enclosure or if the board is installed in a setup with poor air flow.
Excessive temperature will, in first instance, reduce the performance and the quality of the measurements and can also damage the board.

If the board is stored in cold environment, please check for water condensation before power on.

The board has not been tested for radiation hardness. High energy particles can be source of errors and can damage the FPGA. If used in strong proton or neutron beams, arrange proper shielding, or remote the sensors with a custom cable.

7.1 Cleaning Air Vents

CAEN recommends to occasionally clean the air vents on all vented sides of the board or crate, if present. Lint, dust, and other foreign matter can block the vents and limit the airflow. Be sure to power off the board and disconnect it from the power by physically detach the power chord before cleaning the air vents and follow the general cleaning safety precautions.

IT IS UNDER THE RESPONSIBILITY OF THE CUSTOMER A NON-COMPLIANT USE OF THE PRODUCT

8 Panels Description

Fig. 8.1: Front panel view of V1740

8.1 Front Panel

ANALOG INPUT

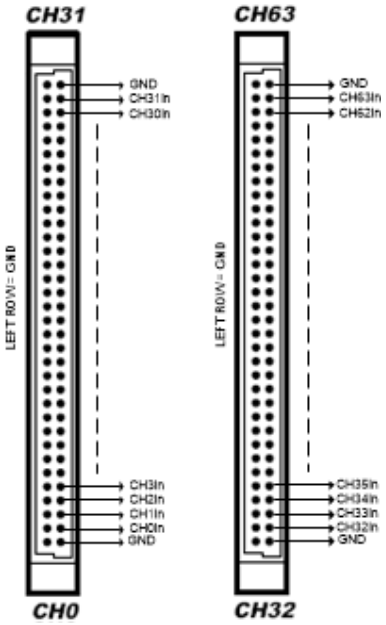
FUNCTION

Two input connectors from CH0 to CH31 and from CH32 to CH63 receive the input analog signals.

ELECTRICAL SPECS

Input dynamics: $2V_{pp}$ or $10V_{pp}$(see Tab. **1.1**)
Input impedance (Z_{in}): 50 Ω (1 kΩ @$10V_{pp}$).
Absolute max analog input voltage:
6 V_{pp} (with V_{rail} max +6 V or –6 V) for any DAC offset value.

PINOUT



Note: ensure that alignment is correct during insertion/extraction operations; incorrect alignment may lead to connector damage.

MECHANICAL SPECS

Series: ERNI SMC 68P connectors.
Type: ERNI SMC-15476.
Manufacturer: ERNI Electronics.

ACCESSORIES

All the 64 channels can be available on as many single-ended LEMO connectors by using the A746B adapter (see Tab. **1.1**).

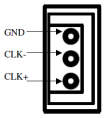
CLOCK IN/CLOCK OUT

FUNCTION
Input and output connectors for the external clock.

ELECTRICAL SPECS
Sign. type: differential (LVDS, ECL, PECL, LVPECL, CML). CAEN provides single ended-to-differential A318 cable adapter (see **Tab. 1.1**) for CLK-IN.
Coupling: AC (CLK-IN); DC (CLK-OUT).
Z_{diff}: 100 Ω.
Accuracy < 100 ppm.

MECHANICAL SPECS
Series: AMPMODU connectors.
Type: 3-102203-4 (3-pin).
Manufacturer: AMP Inc.

PINOUT



CLK IN LED (GREEN): indicates the external clock is enabled.

TRG-IN / TRG-OUT / S-IN

FUNCTION

- TRG-OUT: digital output connector to propagate:
  - the internal trigger sources;
  - signals (probes) from the mezzanines;
  - S-IN signal
  - signals (probes) from the motherboard, like Run, ClkOut, ClockPhase, PLL_Unlock or Busy signal

according to 0x8110 and 0x811C registers, or

- TRG-IN: digital input connector for the external trigger or veto signal.
- S-IN: SYNC/START/STOP digital input connector configurable as reset of the time stamp (see Sec. **9.13**) or to start/stop the acquisition (see Sec. **9.7.1**).

ELECTRICAL SPECS
Signal level: NIM or TTL.
TRG-IN/S-IN input Signal Width > 8 ns
TRG-IN/S-IN Input impedance (Z_{in}): 50 Ω
TRG-OUT requires 50 Ω termination.

MECHANICAL SPECS
Series: 101 A 004 connectors.
Type: DLP 101 A 004-28.
Manufacturer: FISCHER.
Alternatively:
Type: EPL 00 250 NTN.
Manufacturer: LEMO.

TTL (GREEN), NIM (GREEN): indicate the standard TTL or NIM set for TRG-OUT, TRG-IN, and S-IN.

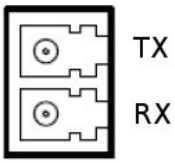
OPTICAL LINK PORT

FUNCTION
Optical LINK connector for data readout and flow control. Daisy chainable. Compliant with Multimode 62.5/125 µm cable featuring LC connectors on both sides.

ELECTRICAL SPECS
Transfer rate: up to 80 MB/s.

MECHANICAL SPECS
Series: SFF Transceivers.
Type: FTLF8519F-2KNL (LC connectors).
Manufacturer: FINISAR.

PINOUT



LINK LEDs (GREEN/YELOW): right LED (GREEN) indicates the network presence, while left LED (YELLOW) signals the data transfer activity.

ANALOG MONITOR

FUNCTION
Analog Monitor output connector with programmable modes (see Sec. **9.11**):

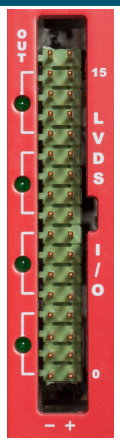
- Trigger Majority
- Test Pulses
- Memory Occupancy
- Voltage Level

ELECTRICAL SPECS
12-bit (125 MHz) DAC output.
1 V_{pp} on R_t = 50 Ω

MECHANICAL SPECS
Series: 101 A 004 connectors.
Type: DLP 101 A 004-28.
Manufacturer: FISCHER.
Alternatively:
Type: EPL 00 250 NTN.
Manufacturer: LEMO.

DIAGNOSTICS LEDs

DTACK (GREEN): indicates there is a VME read/write access to the board;
PLL LOCK (GREEN): indicates the PLL is locked to the reference clock;
PLL BYPS (GREEN): not used;
RUN (GREEN): indicates the acquisition is running (data taking). See Sec. **9.7.1**;
TRG (GREEN): indicates the trigger is accepted;
DRDY (GREEN): indicates the event/data is present in the Output Buffer;
BUSY (RED): indicates all the buffers are full for at least one channel.

LVDS I/Os CONNECTOR	
	**FUNCTION** 16-pin connector with programmable general purpose LVDS I/O signals organized in 4 independent signal groups: 0÷3; 4÷7; 8÷11; 12÷15. In/Out direction is software controlled. Different selectable modes (see Sec. **9.10**): - Register - Trigger - nBusy/nVeto - Legacy **ELECTRICAL SPECS** Level: differential LVDS Z_{diff}: 100 Ω **MECHANICAL SPECS** Series : TE - AMPMODU Mod II Series Type: 5-826634-0 34 pin (lead spacing: 2.54 mm; row pitch: 2.54 mm) Manufacturer: AMP Inc.

LVDS I/O LEDs (GREEN): Each LED close to a 4-pin group lights on if the pins are set as outputs.

IDENTIFICATION LABELS	
	On top and bottom of insertion/extraction handle: • Manufacturer • Model name • Brief ADC features
	On the bottom (V1740) or on the HANDLE (VX1740): • Product Identifier (PID) **Note:** For older boards, a 4-digit Serial Number (S/N) is reported on a little serigraph on the bottom of the VME board's front panel.

8.2 Internal Components

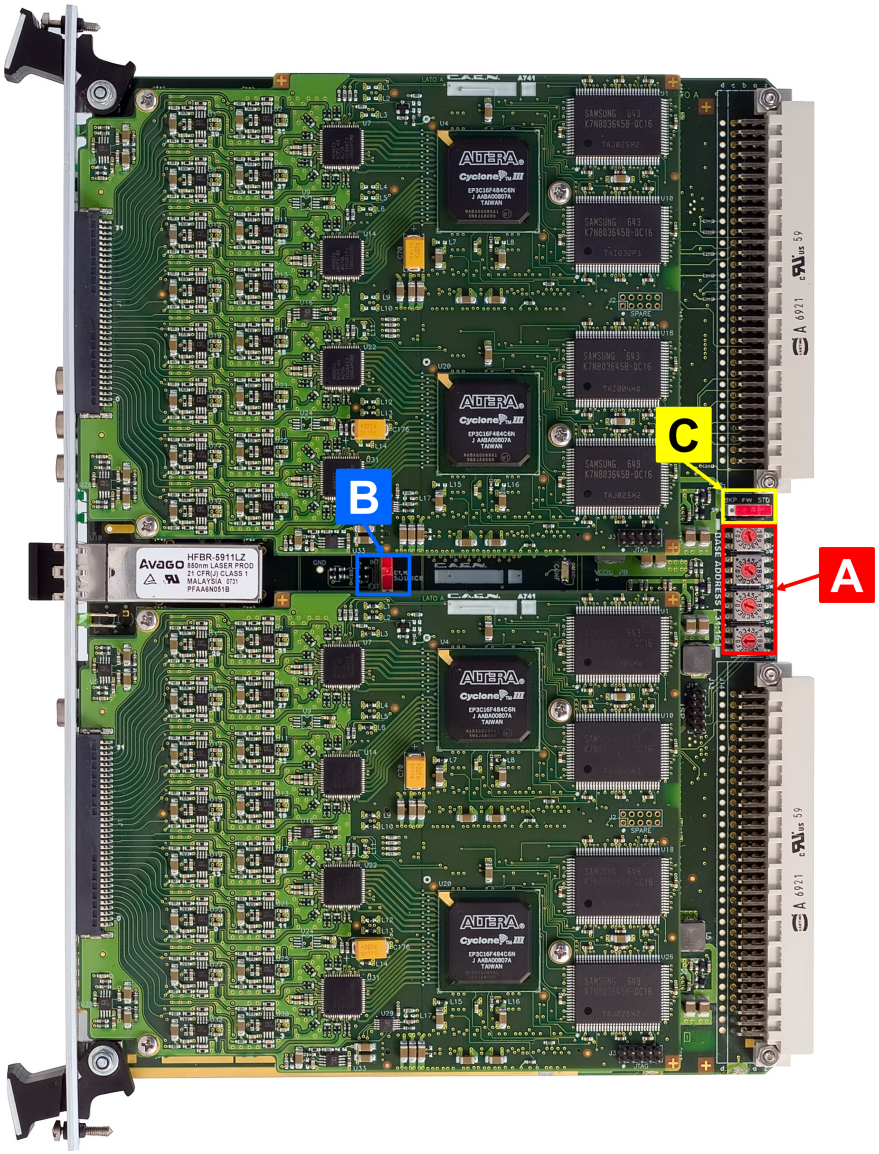


Fig. 8.2: Rotary and dip switches location

A	**SW3,4,5,6**: **"Base Address [31:16]"**	**Type**: Rotary Switches	**Function**: Set the VME Base Address of the module
B	**SW2**: **"CLOCK SOURCE" INT/EXT**	**Type**: Dip Switch	**Function**: Selects the clock source (External or Internal)
C	**SW7**: **"FW" BKP/STD**	**Type**: Dip Switch	**Function**: Selects "Standard" (STD) or "Backup" (BKP) FLASH page as first to be read at power-on to load the FW on the FPGAs (default position is STD); see Sec. **13.1**

9 Functional Description

9.1 Analog Input Stage

Input dynamic is 2 V_{pp} (Z_{in} = 50 Ω); a 10 V_{pp} version (Z_{in} = 1 kΩ) is available by ordering option (see Tab. **1.1**). In order to preserve the full dynamic range with unipolar input signal, positive or negative, it is possible to add a DC offset in the full rage (±1V @$2V_{pp}$, ±5V @$10V_{pp}$) by means of a 16 bit DAC. The input bandwidth ranges from DC to 125 MHz (with 2^{nd} order linear phase anti-aliasing low pass filter).

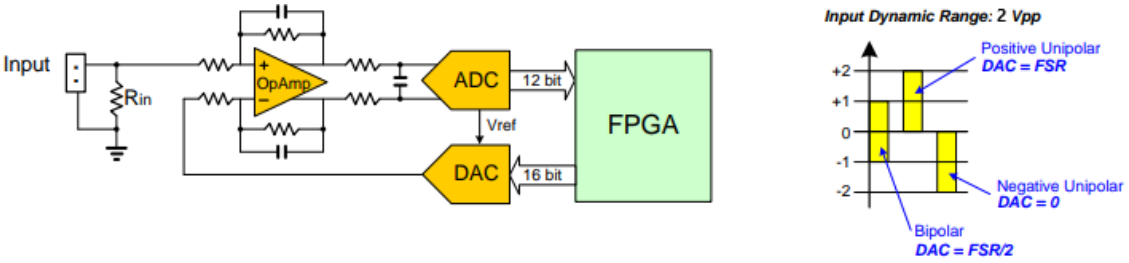


Fig. 9.1: Analog input diagram

9.1.1 DC Offset Common Setting

Setting the DC offset requires a write access at register addresses 0x1n98. The DC offset value will then apply to all the 8 channels of group n.

9.1.2 DC Offset Individual Setting

It is possible to apply a 8-bit positive digital offset individually to each channel inside a group to finely correct the baseline mismatch.
The two 32-bit registers that encode the eight unsigned values for group n (n = 0..7) are:

0x10C0 + 0x100· n -> Correction values for channel offset 0..3
0x10C4 + 0x100· n -> Correction values for channel offset 4..7

Note: DC Offset individual setting is supported from the mezzanine (AMC FPGA) firmware revision 0.10 on.

9.2 Clock Distribution

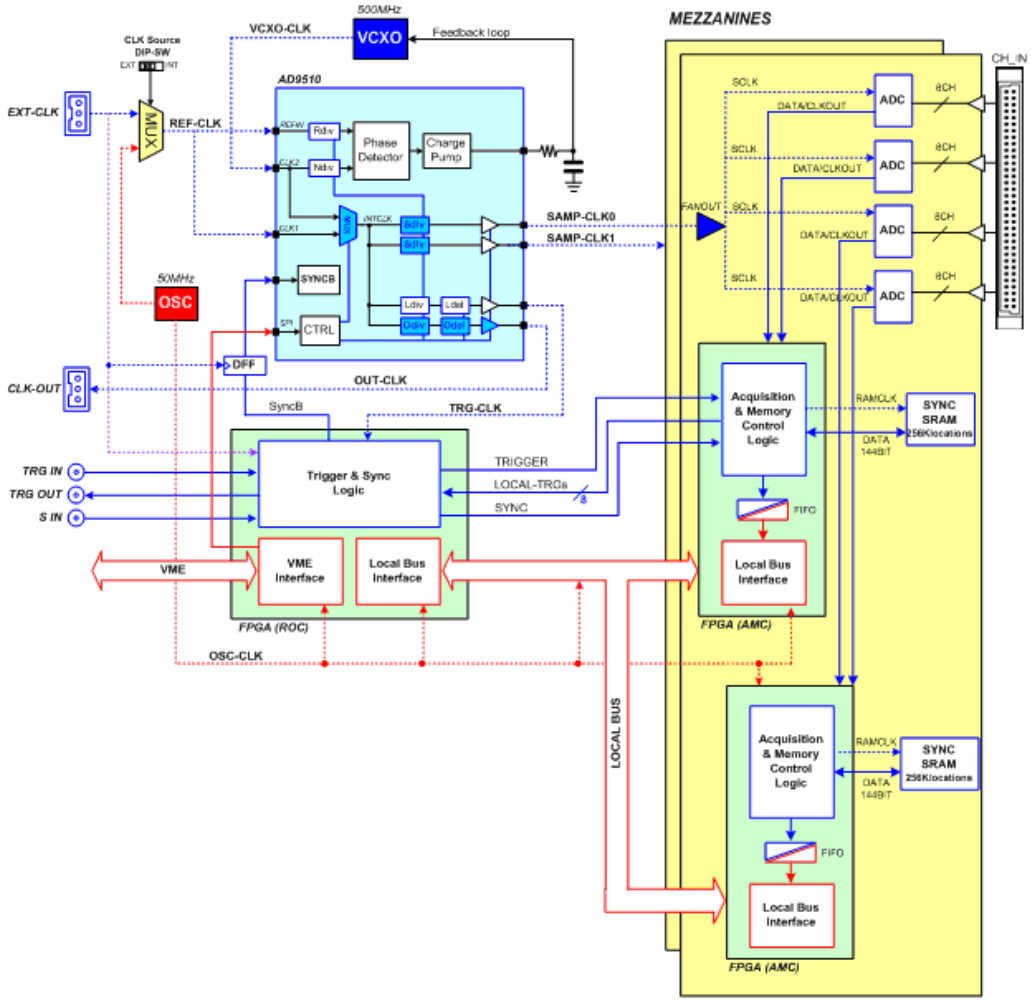


Fig. 9.2: Clock distribution diagram

The clock distribution of the module takes place on two domains: OSC-CLK and REF-CLK.

OSC-CLK is a fixed 50-MHz clock coming from a local oscillator which handles VMEbus, Optical Link and Local Bus, that takes care of the communication between motherboard and mezzanines (see red traces in Fig. **9.2**).

REF-CLK handles ADC sampling, trigger logic, and acquisition logic (samples storage into RAM, buffer freezing on trigger) through a clock chain. REF-CLK can be either an external (via the front panel CLK-IN connector) or an internal (via the 50-MHz local oscillator) source. In the latter mode, OSC-CLK and REF-CLK will be synchronous (the operation mode remains the same).

REF-CLK clock source selection can be done by an on-board dedicated dip switch (see Fig. **8.2**) between the following modes:

- INT mode (default) means REF-CLK is the 50 MHz of the local oscillator (REF-CLK = OSC-CLK);
- EXT mode means REF-CLK source is the external frequency fed on CLK-IN connector.

The external clock signal must be differential (LVDS, ECL, PECL, LVPECL, CML) with a jitter lower than 100 ppm (see Chap. **3**). CAEN provides the A318 cable to adapt single ended signals coming from an external clock unit into the differential CLK-IN connector (see Tab. **1.1**).

The V1740 is equipped with a phase-locked-loop (PLL) and clock distribution device, AD9510. It receives the REF-CLK and generates the sampling clock for ADCs and the mezzanine FPGA (SAMP-CLK0 up to SAMP-CLK3), as well as the trigger logic synchronization clock (TRG-CLK) and the output clock (CLK-OUT).

AD9510 configuration can be changed and stored into non-volatile memory. Changing the AD9510 configuration is primarily intended to be used for external PLL reference clock frequency change (see Sec. **9.3**). The V1740 locks to an external 50 MHz reference clock with default AD9510 configuration.

Refer to the AD9510 datasheet for more details:
http://www.analog.com/UploadedFiles/Data_Sheets/AD9510.pdf
(in case the active link above does not work, copy and paste it on the internet browser)

9.3 PLL Mode

The Phase Detector inside the AD9510 device allows to couple REF-CLK with an external VCXO, which provides the nominal ADC frequency (62.5 MS/s).

As introduced in Sec. **9.2**, the source of the REF-CLK signal (see Fig. **9.2**) can be external on CLK-IN front panel connector or internal from the 50 MHz local oscillator. Programming the REF-CLK source internal or external can be performed by acting on the on-board dip switch SW2 (see Sec. **8.2**).

The following options are allowed:

1. 50 MHz internal clock source - this is the standard operation mode: the AD9510 dividers do not require to be reprogrammed (the digitizer works in the AD9510 default configuration). The clock source selection dip switch SW2 is in default INT mode. REF-CLK = OSC-CLK.
2. 50 MHz external clock source - in this case, the clock source is taken from an external device; the AD9510 dividers do not need to be reprogrammed as the external frequency is the same as the default one. The clock source selection dip switch must be set in EXT mode. CLK-IN = REF-CLK = OSC-CLK.
3. External clock source different from 50 MHz - the clock source is externally provided as in point 2, but the AD9510 dividers must now be reprogrammed to lock the VCXO to the new REF-CLK in order to provide out the nominal sampling frequency at 62.5 MS/s. The clock source selection dip switch must be set in EXT mode. CLK-IN = REF-CLK $\neq$ OSC-CLK.

If the digitizer is locked, the PLL-LOCK front panel LED must be on.

Note: the user can configure the clock parameters, generate the PLL programming file and load it on the board by using the CAEN Toolbox software (see Chap. **11**).

9.4 Reducing the Sampling Frequency

In case the board is required to work at a sampling frequency (SAMP-CLK) lower than the nominal, it can be alternatively achieved:

1. In a direct way, by reprogramming the AD9510 dividers to lock the VCXO to REF-CLK and provide the desired SAMP-CLK. REF-CLK can be configured as in Sec. **9.3**. Not all the frequencies are admitted and a lower frequency limit must be considered, due to the internal electronics **[RD5]**.

Note: the user can configure the clock parameters, generate the PLL programming file and load it on the board by using the CAEN Toolbox software (see Chap. **11**).

2. In an indirect way, by enabling the decimation option (see Sec. **9.4.1**).

Note: The mimimum sampling frequency is:

- 16.1 MS/s by hardware downsampling (direct way). The minimum value may depend on the digitizer model, on the firmware or on the hardware downsampling mode **[RD5]**.
- 488 KS/s by firmware decimation (indirect way).

9.4.1 Decimation

This function is a firmware option based on the programmability of a decimation factor n. During the acquisition, the firmware processes the digitized input waveforms calculating an averaged value of the "decimated" 2·n consecutive samples. The self-trigger is then issued as soon as an averaged value exceeds the programmed threshold (see Sec. **9.8.3**). Software trigger and external trigger are not affected by decimation option.

While the real sampling frequency doesn't change (i.e. 62.5 MS/s), the decimation effect is to change the rate the data are written into the digitizer memory. So, the readout data result at a sampling frequency changed according to the formula:

$$\frac{62.5}{2^n}\text{MS/s}$$

where n = [0,1,…,7]. The n parameter is set through the register address 0x8044.

Note: Decimation function is supported by:

- CAENDigitizerlibrary revision ≥ 2.5.0
- WaveDump software revision ≥ 3.6.4

Note: Decimation is supported only by 740 series running a AMC FPGA firmware revision ≥ 0.7 (see Chap. **13**).

9.5 Trigger Clock

The Trigger logic works at 125 MHz, equal to 2·SAMP-CLK, while triggers are sensed, generated and distributed by the motherboard at 62.5 MHz. The actual trigger clock has so the same frequency as the sampling clock (TRG-CLK = SAMPL-CLK).

9.6 Output Clock

The AD9510 output can be available on the front panel CLK-OUT connector (see Fig. **9.2**). This option is particularly useful in case of multi-board synchronization to propagate the clock reference source in Daisy Chain. This option can be enabled by the user while configuring the PLL programming file in the CAEN Toolbox software (see Chap. **11**).

9.7 Acquisition Modes

9.7.1 Acquisition Run/Stop

The acquisition can be started and stopped in different ways, according to bits[2:0] of register 0x8100 **[RD1]**:

- SW CONTROLLED (bits[1:0] = 00): Start and Stop take place by software command. Bit[2] = 0 means stopped, while bit[2] = 1 means running.
- S-IN CONTROLLED (bits[1:0] = 01): acquisition is armed by setting bit[2] = 1, the two options are selectable throuh bit[11] of the same register:
  - START/STOP ON LEVEL - If bit[11] = 0, then acquisition starts when the S-IN signal is high and stops when it is low; if bit[2] = 0 (disarmed), the acquisition is always off.
  - START ON EDGE - If bit[11] = 1, then acquisition starts on the rising edge of the S-IN signal and must be stopped by software command (bit[2] = 0).

Note: the START ON EDGE option is implemented from ROC FPGA fw revision 4.22 on.

- FIRST TRIGGER CONTROLLED (bits[1:0] = 10): bit[2] = 1 arms the acquisition and the Start is issued on the first trigger pulse (rising edge) on the TRG-IN connector. This pulse is not used as a trigger; actual triggers start from the second pulse on TRG-IN. The Stop acquisition must be SW controlled (i.e. reset of bit[2]).
- LVDS I/Os CONTROLLED: this mode acts like the S-IN CONTROLLED (bits[1:0] = 01), but using the configurable features of the signals on the LVDS I/Os connector (see Sec. **9.10**).

9.7.2 Acquisition Triggering: Samples and Events

When the acquisition is running, a trigger signal allows to:

- store a 31-bit counter value of the Trigger Time Tag (TTT).
  The counter (representing a time reference), like the Trigger Logic Unit (see Fig. **9.2**), operates at a frequency of 125 MHz (i.e. 8 ns, that is to say $\frac{1}{2}$ADC clock cycles). Due to the way acquired data is written into the board internal memory (i.e. in 4-sample bunches), the TTT counter is read every 2 trigger logic clock cycles, which means the trigger time stamp resolution results in 16 ns (i.e. 62.5 MHz). Basing on that, the LSB of the TTT is always “0”;
- increment the EVENT COUNTER;
- fill the active buffer with the pre/post-trigger samples, whose number is programmable via register address 0x8114 **[RD1]**; the acquisition window width (also referred to as record length) is determined via register addresses 0x800C and 0x8020; then, the buffer is frozen for readout purposes, while the acquisition continues on another buffer.

An event is therefore composed by the trigger time tag, pre- and post-trigger samples and the event counter.

Overlap between “acquisition windows” may occur (a new trigger occurs while the board is still storing the samples related to the previous trigger); this overlap can be either rejected or accepted (programmable via software).

If the board is programmed to accept the overlapping triggers (by writing at register address 0x8000 **[RD1]**), as the overlapping trigger arrives, the current active buffer is filled up, then the samples storage continues on the subsequent one. In this case, not all events will have the same size (see Fig. **9.3**).

A trigger can be refused for the following causes:

- Acquisition is not active.

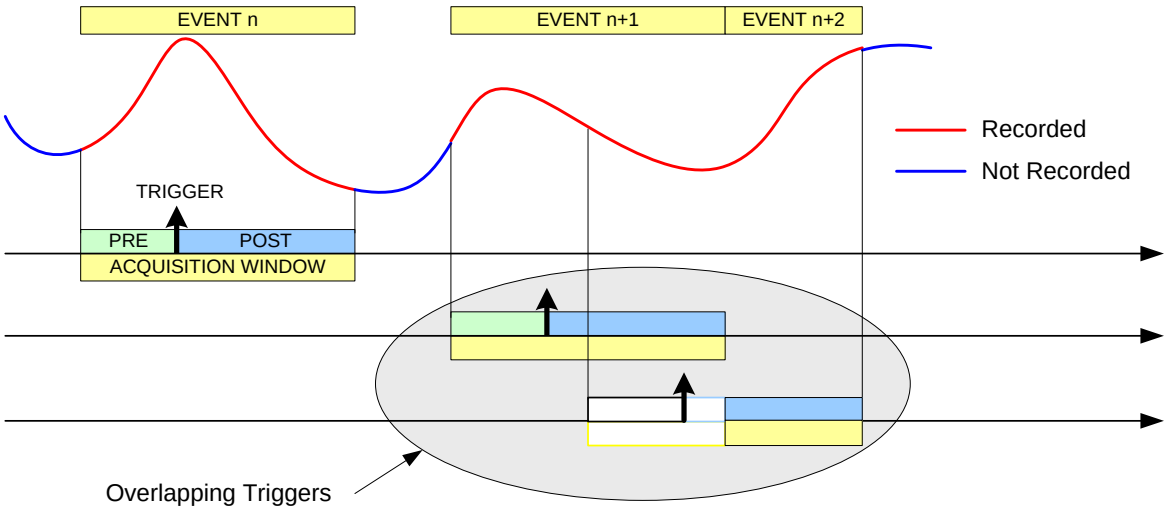


Fig. 9.3: Trigger Overlap

- Memory is FULL and therefore there are no available buffers.
- The required number of samples for building the event pre-trigger is not reached yet; this happens typically as the trigger occurs too early either with respect to the RUN Acquisition command (see Sec. **9.7.1**) or with respect to a buffer emptying after a Memory FULL status (see Sec. **9.7.5**).
- The trigger overlaps the previous one and the board is not enabled for accepting overlapped triggers.

As a trigger is refused, the current buffer is not frozen and the acquisition continues writing on it. The EVENT COUNTER can be programmed in order to be either incremented or not. If this function is enabled, the EVENT COUNTER value identifies the trigger number sent (but the event number sequence is lost); if the function is not enabled, the EVENT COUNTER value coincides with the sequence of buffers saved and read out.

9.7.3 Multi-Event Memory Organization

Each channel of the V1740 features a SRAM memory to store the acquired events. The memory size for the event storage per each channel is 192 kS or 1.5 MS, according to the board version (see Tab **. 1.1**). The channel memory can be divided into a programmable number of buffers, N_b (N_b from 1 up to 1024), by the register address 0x800C **[RD1]**, as described in Tab. **9.1**.

Register Value BUFFER_CODE	Number of Buffers (N_b)	Size of one Buffer SRAM 288 kB/ch (192 kS)	Size of one Buffer SRAM 2.25 MB/ch (1.5 MS)
0x0	1	288 kB/ch (192 kS)	2.25 MB/ch (1.5 MS)
0x1	2	144 kB/ch (96 kS)	1.125 MB/ch (750 kS)
0x2	4	72 kB/ch (48 kS)	576 kB (384 kS)
0x3	8	36 kB/ch (24 kS)	288 MB/ch (192 kS)
0x4	16	18 kB/ch (12 kS)	144 MB/ch (96 kS)
0x5	32	9 kB/ch (6 kS)	72 kB/ch (48 kS)
0x6	64	4.5 kB/ch (3 kS)	36 kB/ch (24 kS)
0x7	128	2.25 kB/ch (1.5 kS)	18 kB/ch (12 kS)
0x8	256	1.125 kB/ch (768 S)	9 kB/ch (6 kS)
0x9	512	576 B/ch (384 S)	4.5 kB/ch (3 kS)
0xA	1024	288 B/ch (192 S)	2.25 kB/ch (1.5 kS)

Tab. 9.1: Buffer organization of 740 family series. For each value of buffer size it is reported the memory size and the number of samples of one buffer, where k = 1024 and M = 1024 · 1024.

Having 192 kS memory size as reference, this means that each buffer contains $^{192k}/_{N_b}$ samples (e.g. N_b = 1024 means 1024 samples in each buffer).

9.7.3.1 Custom size events

In case an event size less than the buffer size is needed, the user can set the N_LOC value at register address 0x8020 **[RD1]**, where N_LOC is the number of memory locations. The size of the event is so forced to be according to the formula:

$$3 \cdot N\_LOC = 2 \cdot N_{Sample} \text{ (normal mode)}$$

When N_LOC = 0 the custom size is disabled.

Note: The value of N_LOC must be set in order that the relevant number of samples does not exceed the buffer size and it must not be modified while the acquisition is running. Even using the custom size setting, the number of buffers and the buffer size are not affected by N_LOC, but they are still determined by N_b.

The concepts of buffer organization and custom size directly affect the width of the acquisition window (i.e. number of the digitized waveform samples per event). The Record Length parameter defined in CAEN software (such as WaveDump and WaveDump2 introduced in Chap. **11**) and the *Set/GetRecordLength()* functions of the CAENDigitizer library (see Sec. **10.2**) rely on these concepts.

9.7.4 Event structure

The event can be read out via VMEbus or Optical Link; data format is 32-bit long word (see Fig. **9.6**).

An event is structured as:

- **Header** (four 32-bit words)
- **Data** (variable size and format)

9.7.4.1 Header

The Header consists of four words including the following information:

- **EVENT SIZE** (bits[27:0] of 1st header word) is the total size of the event, i.e. the number of 32-bit long words to be read.
- **BOARD ID** (bits[31:27] of 2nd header word) is the GEO address, meaningful for VME64X modules.
- **BOARD FAIL FLAG** (bit[26] of 2nd header word) implemented from ROC FPGA firmware revision 4.5 on (reserved otherwise), it is set to "1" in consequence of a hardware problem (e.g. PLL unlocking). The user can collect more information about the cause by reading at register address 0x8178 and contact CAEN Support Service if necessary (see Chap. **17**).
- **PATTERN** (bits[23:8] of 2nd header word) is the 16-bit PATTERN latched on the LVDS I/Os as the trigger arrives.

Note: Starting from revision **4.6** of the ROC FPGA firmware, these 16 bits can be programmed to provide trigger information according to the setting of the bits[22:21] at register address 0x811C (see Tab **9.2**).

REGISTER 0x811C Bits[22:21]	FUNCTIONAL DESCRIPTION	PATTERN /TRG OPTIONS INFORMATION (16 bits in the 2nd header word)
00 (default)	PATTERN	Pattern of the 16 LVDS signals .
01	Event Trigger Source	Indicates the trigger source causing the event acquisition: Bits[23:19] = 00000 Bit[18] = Software Trigger Bit[17] = External Trigger Bit[16] = Trigger from LVDS connector Bits[15:8] = Trigger requests from the groups (refer to Sec. **9.8.3**).
10	Extended Trigger Time Tag (ETTT)	A 48-bit Trigger Time Tag (ETTT) information is configured, where Bits[23:8] contributes as the 16 most significant bits together to the 32-bit TTT field (4th header word). **Note**: in the ETTT option, the overflow bit is not provided.
11	Not used	If configured, it acts like "00" setting.

Tab. 9.2: Pattern/Trg Options configuration table.

- **GROUP MASK** (bits[7:0] of 2nd header word) is the mask of the groups participating in the event (e.g. GR5 and GR7 participating → Group Mask = 0xA). This information must be used by the software to acknowledge from which channel the samples are coming (the first event contains the samples from the channel with the lowest number).

- **EVENT COUNTER** (bits[23:0] of 3rd header word) is the trigger counter; it can count either accepted triggers only, or all triggers (bit[3] of register address 0x8100).
- **TRIGGER TIME TAG** (bits[31:0] of 4th header word) is the 31-bit Trigger Time Tag (TTT) information (31 bit counter and 32nd bit as roll-over flag), which is the trigger time reference. The word is composed of the value of the 31-bit counter of the Trigger Time Tag (bit[30:0]) plus the overflow bit (bit[31]) indicating that the timestamp counter has overflowed at least once (**Fig. 9.4**). If the ETTT option is enabled, then this field becomes the 32 less significant bits of the 48-bit Extended Trigger Time Tag information in addition to the 16 bits (MSB) of the TRG OPTIONS field (2nd event word). Note that, in the ETTT case, the roll-over flag is no more provided (**Fig. 9.5**). The trigger time tag is reset either at the start of acquisition, or via front panel signal on S-IN or LVDS I/O connectors, and increments with 125 MHz frequency (i.e. every 8 ns, that is $\frac{1}{2}$ ADC clock cycle). The TTT value is read at half this frequency (i.e. 62.5 MHz) so that the specifications are 16 ns resolution and 17 s range (8 ns $\times$ (2^{31} – 1)), which can be extended to 625 h (8 ns $\times$ (2^{48} – 1)) if ETTT is enabled.

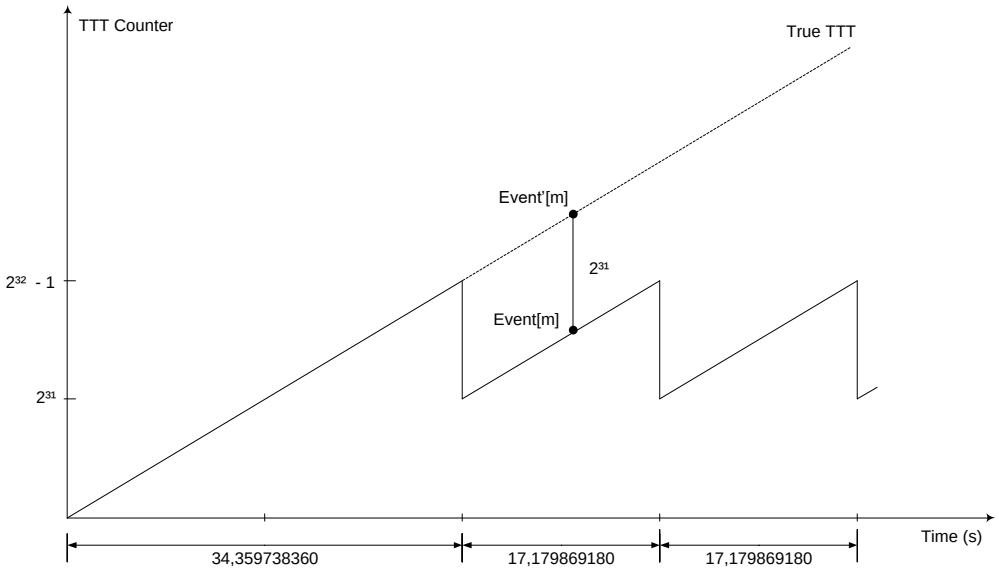


Fig. 9.4: TTT description.

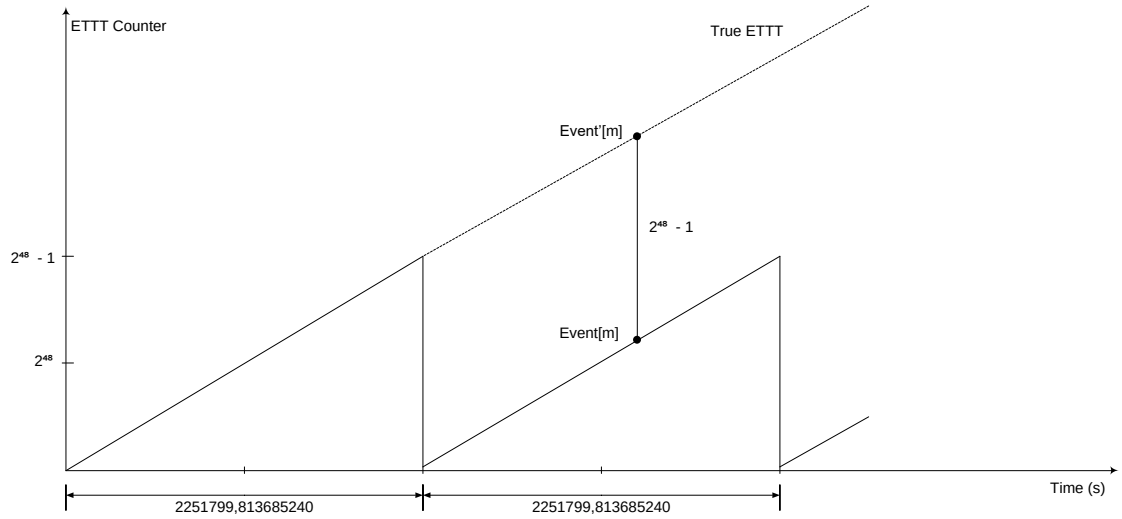


Fig. 9.5: ETTT description.

9.7.4.2 Data

Data are the stored samples. Data from masked channels are not read.

9.7.4.3 Event Format Examples

The event format is described in the following figure:

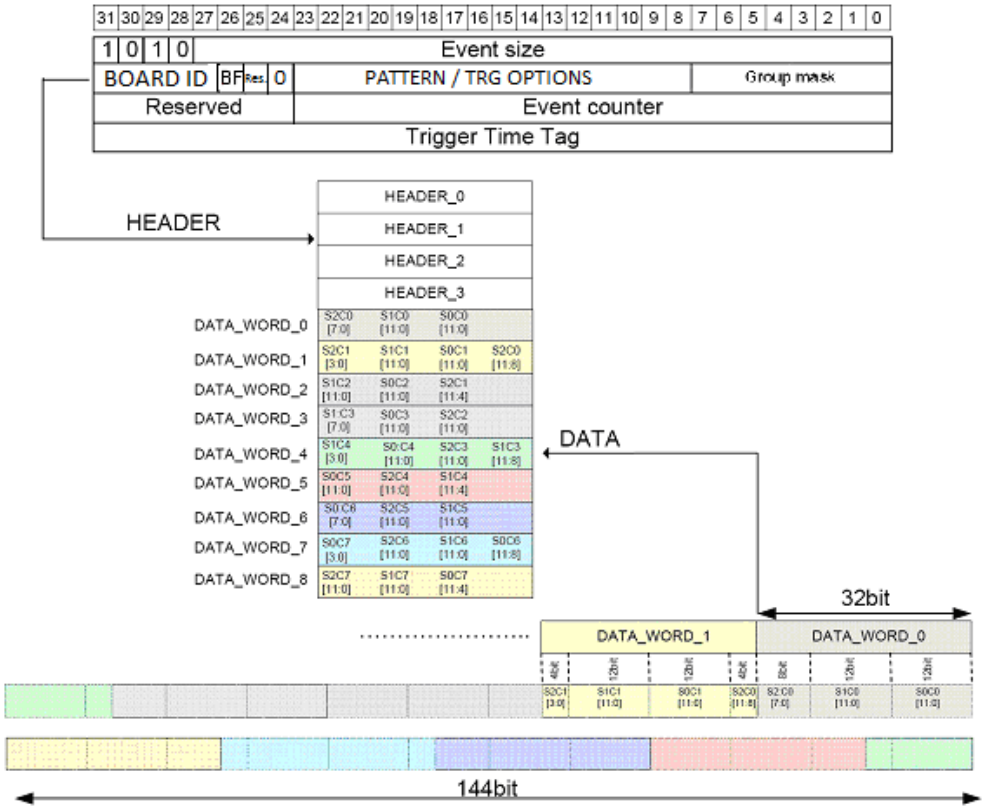


Fig. 9.6: Event format example

Note: Data transfer starts from Channel 0 of Group 0; once all the data from one Group are transferred, data transfer from the subsequent Group begins.

Note: The firmware saves the waveforms in the memory of the digitizer with a granularity of n (i.e. in groups of n samples). This way of writing the waveforms in memory allows for a potential ΔT between the instant when the trigger physically arrives and when it is sensed by the digitizer. The resulting effect is a jitter in the acquisition window between one event and the next. This jitter can be observed by graphing the waveforms of the enabled channels using an acquisition software. The channels may jitter together between one event and the next, but not among themselves.

9.7.5 Acquisition Synchronization

Each channel of the digitizer is provided with a SRAM memory that can be organized in a programmable number N_b of circular buffers (N_b = [1 : 1024], see Tab. **9.1**). When the trigger occurs, the FPGA writes further a programmable number of samples for the post-trigger and freezes the buffer, so that the stored data can be read via VME or Optical Link. The acquisition can continue in a new buffer.

When all buffers are filled, the board is considered FULL: no trigger is accepted and the acquisition stops (i.e. the samples coming from the ADC are not written into the memory, so they are lost). As soon as one buffer is read out and freed, the board exits the FULL condition and acquisition restarts.

IMPORTANT: When the acquisition restarts, no trigger is accepted until at least the entire buffer is written. This means that the dead time is extended for a certain time (depending on the size of the acquisition window) after the board exits the FULL condition.

A way to eliminate this extra dead time is by setting bit[5] = 1 at register address 0x8100. The board is so programmed to enter the FULL condition when $N_b - 1$ buffers are filled: no trigger is then accepted, but samples writing continues in the last available buffer. As soon as one buffer is read out and becomes free, the boards exits the FULL condition and can immediately accept a new trigger. This way, the FULL reflects the BUSY condition of the board (i.e. inability to accept triggers).

Note: when bit[5] = 1, the minimum number of circular buffers to be programmed is N_b = 2.

In some cases, the BUSY propagation from the digitizer to other parts of the system has some latency and it can happen that one or more triggers occur while the digitizer is already FULL and unable to accept those triggers. This condition causes event loss and it is particularly unsuitable when there are multiple digitizers running synchronously, because the triggers accepted by one board and not by other boards cause event misalignment.

In these cases, it is possible to program the BUSY signal to be asserted when the digitizer is close to FULL condition, but it has still some free buffers (Almost FULL condition). In this mode, the digitizer remains able to accept some more triggers even after the BUSY assertion and the system can tolerate a delay in the inhibit of the trigger generation. When the Almost FULL condition is enabled by setting the Almost FULL level to “X” (register address 0x816C), the BUSY signal is asserted as soon as X buffers are filled, although the board still goes FULL (and rejects triggers) when the number of filled buffers is N_b or $N_b - 1$, depending on bit[5] at register address 0x8100 as above described.

It is possible to provide the BUSY signal on the digitizer front panel TRG-OUT output (bit[20], bits[19:18] and bits[17:16] of register address 0x811C are involved). In case of multi-board setup, the BUSY signal can be propagated among boards through the front panel LVDS I/O connector (see Sec. **9.10**).

9.8 Trigger Management

When operating the waveform recording firmware, all board channels share the same trigger (board common trigger), so they acquire an event simultaneously and in the same way (determined number of samples according to buffer organization and custom size settings, as well as position with respect to the trigger defined by the post-trigger).

The generation of the board common trigger is based on different trigger sources (configurable by the 0x810C register):

- **Software Trigger**
- **External Trigger**
- **Self-trigger**
- **Coincidences**
- **TRG-IN as Gate**
- **LVDS I/O Trigger**

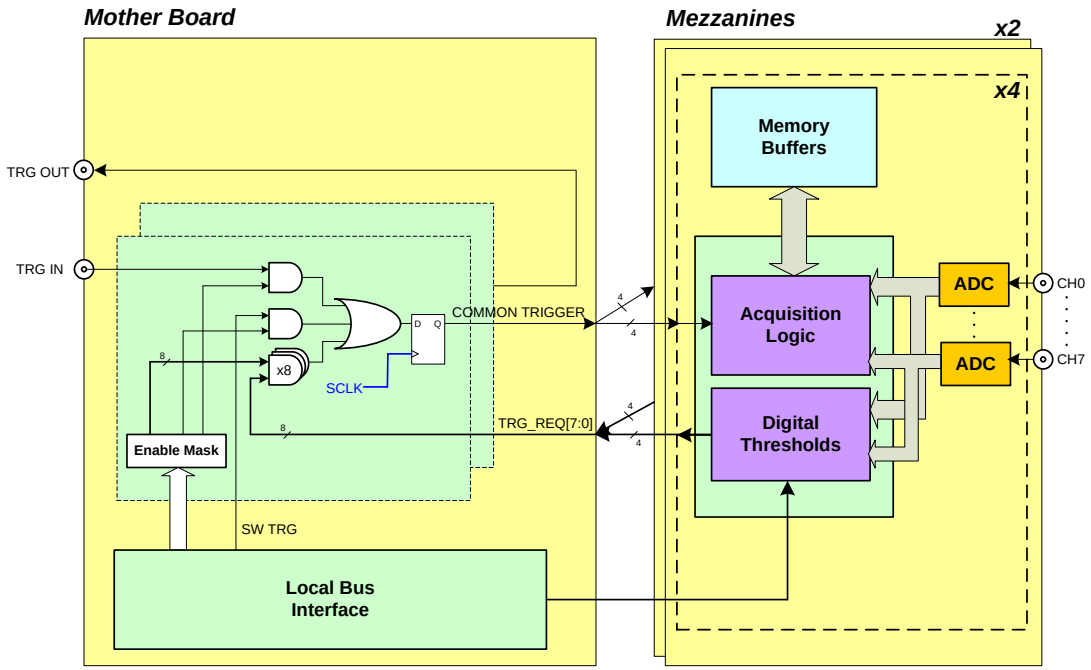


Fig. 9.7: Block diagram of trigger management.

9.8.1 Software Trigger

Software triggers are internally produced via software command (write access at register address 0x8108) through VMEbus or Optical Link.

9.8.2 External Trigger

A TTL or NIM external signal can be provided to the front panel TRG-IN connector (configurable at register address 0x811C). When setting up a system of multiple digitizers (see Sec. **9.9**), there could be a random jitter of 1 TRG-CLK hit (see Sec. **9.5**) if the external signal is provided asynchronously with the internal clock of the boards (e.g. from external trigger FAN-IN on TRG-IN). One board could then sense the trigger at clock_hit[N], while another board at clock_hit[N+1] and the same jitter is then present between the pulse acquired by one board and that acquired by the other board.

9.8.3 Self-Trigger

In the trigger domain, the input channels of the V1740 are managed as 8-channel groups: [0:7], [8:15], [16:23], [24:31], [32:39], [40:47], [48:54], [55:63]. Each channel in a group (GRx_CHy_IN) can generate a self-trigger signal (SELF-TRG) when the digitized input pulse exceeds a configurable threshold, common to the group, set through the register address 0x1n80. The individual self-triggers from all channels of each group are ORed to generate a group trigger request (TRG_REQ). The trigger requests of the groups are propagated to the central trigger logic on the motherboard (see Fig. **9.7**) where they participate in logic OR to produce the board common trigger, which is finally distributed back to all channels on the mezzanines causing the event acquisition (see Sec. **9.8.7**).

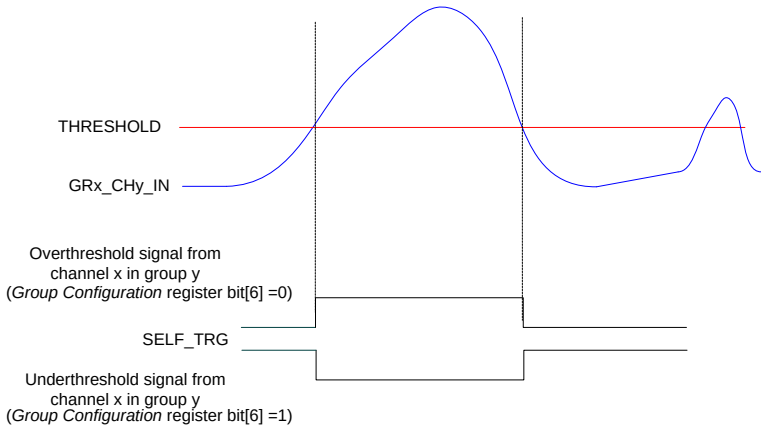


Fig. 9.8: Self-trigger generation.

Bit[7:0] of register 0x1nA8 decide which channel of group n will participate in the trigger request generation.

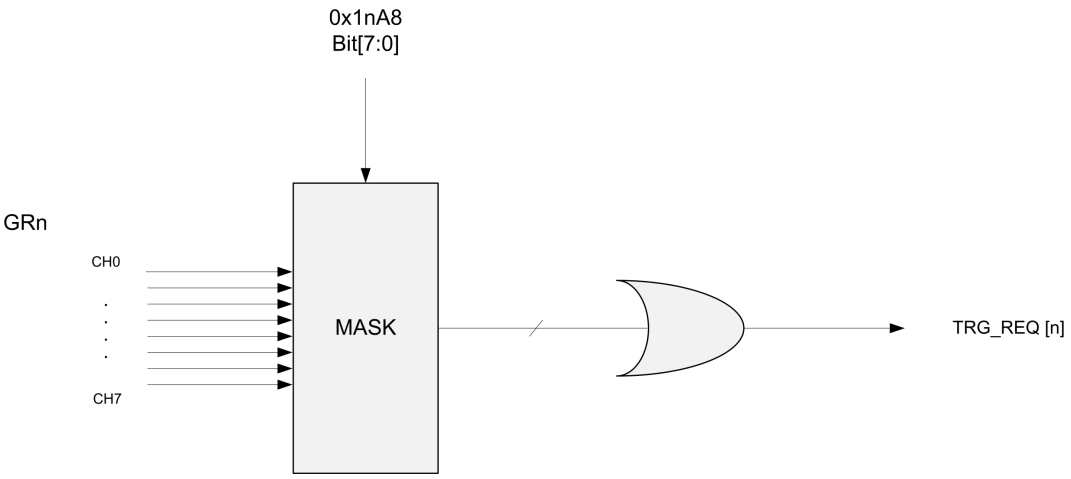


Fig. 9.9: Trigger request mask.

Bit[7:0] of register 0x810C allows the user to program which group participate in the global trigger generation (see Sec. **9.8.7**).

9.8.4 LVDS I/O Trigger

LVDS I/O specific pins on the front panel dedicated connector can be programmed as trigger inputs and enabled to participate in the common trigger generation with other trigger sources. See Fig. **9.13** and refer to Sec. **9.10** for details.

9.8.5 Trigger coincidence level

Operating the waveform recording firmware, the acquisition trigger is common to the whole board. This common trigger allows the coincidence acquisition mode to be performed through the Majority operation.

Enabling the coincidences is possible by writing at register address 0x810C :

- Bits[7:0] enable a specific group (trigger request) to participate in the coincidence;
- Bits[23:20] set the coincidence window (T_{TVAW}) linearly in steps of the Trigger clock (8 ns);
- Bits[26:24] set the Majority (i.e. Coincidence) level; the coincidence takes place when:

Number of enabled groups > Majority level

Supposing that bits[7:0] = FF (i.e. all groups are enabled) and bits[26:24] = 01 (i.e. Majority level = 1), a common trigger is issued whenever the trigger requests of at least two of the enabled groups are in coincidence within the programmed T_{TVAW}.

The Majority level must be smaller than the number of groups enabled via bits[7:0] mask. By default, bits[26:24] = 00 (i.e. Majority level = 0), which means the coincidence acquisition mode is disabled and the T_{TVAW} is meaningless. In this case, the common trigger is simple OR of the enabled group trigger requests.

Note: in the following figures, in order not to overload the plots but preserve the clearness of concept, only GR0 and GR1 are enabled, and so only the first channel of each group.

Fig. **9.10** shows the trigger management in case the coincidences are disabled.

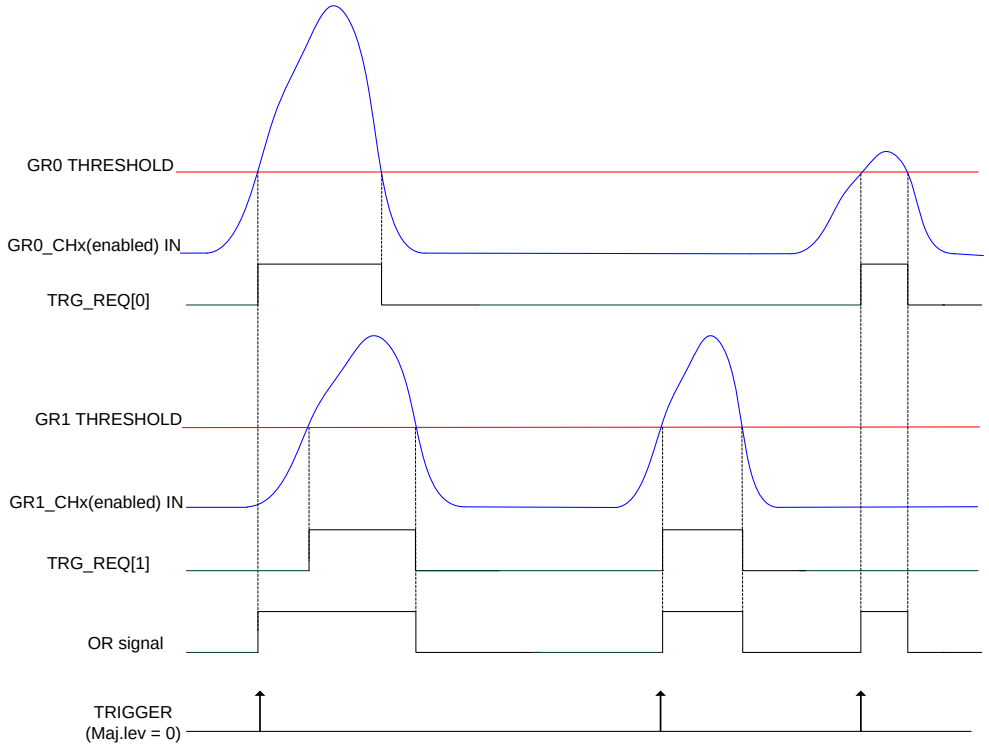


Fig. 9.10: Trigger request relationship with Majority level = 0.

Fig. **9.11** shows the trigger management in case the coincidences are enabled with Majority level = 1 and T_{TVAW} is a value different from 0.

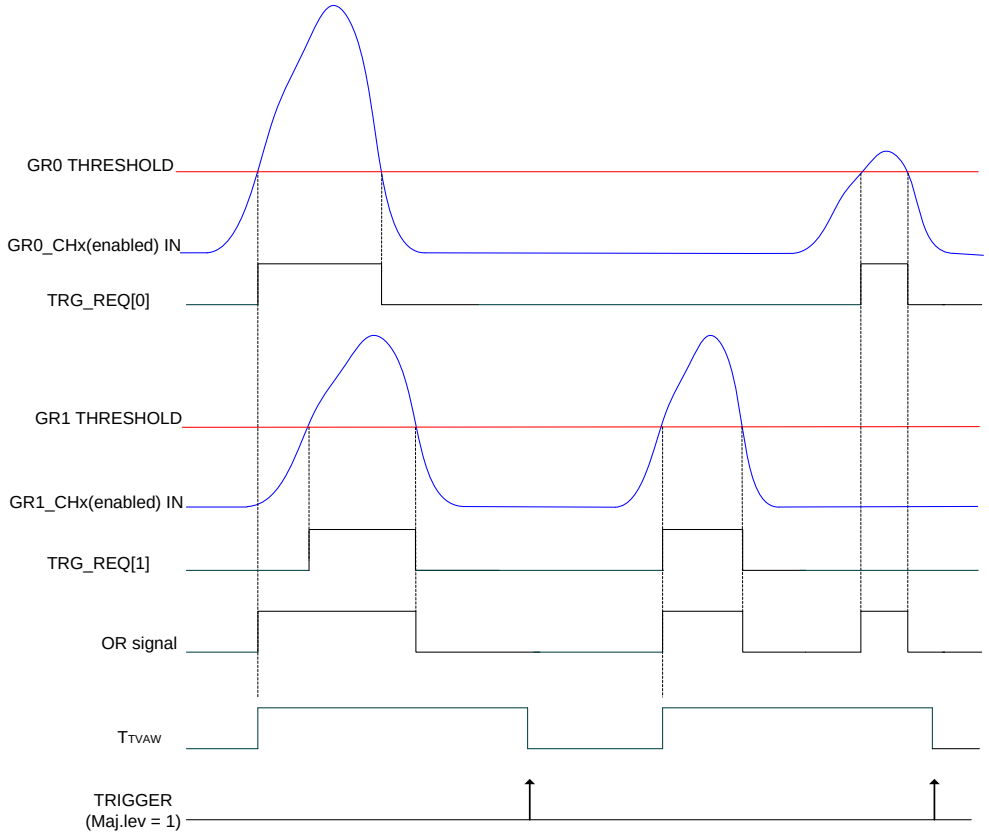


Fig. 9.11: Trigger request relationship with Majority level = 1 and $T_{TVAW} \neq 0$.

Note: with respect to the position where the common trigger is generated, the portion of input signal stored depends on the programmed length of the acquisition window and on the post trigger setting.

Fig. **9.12** shows the trigger management in case the coincidences are enabled with Majority level = 1 and T_{TVAW} = 0 (i.e. 1 clock cycle).

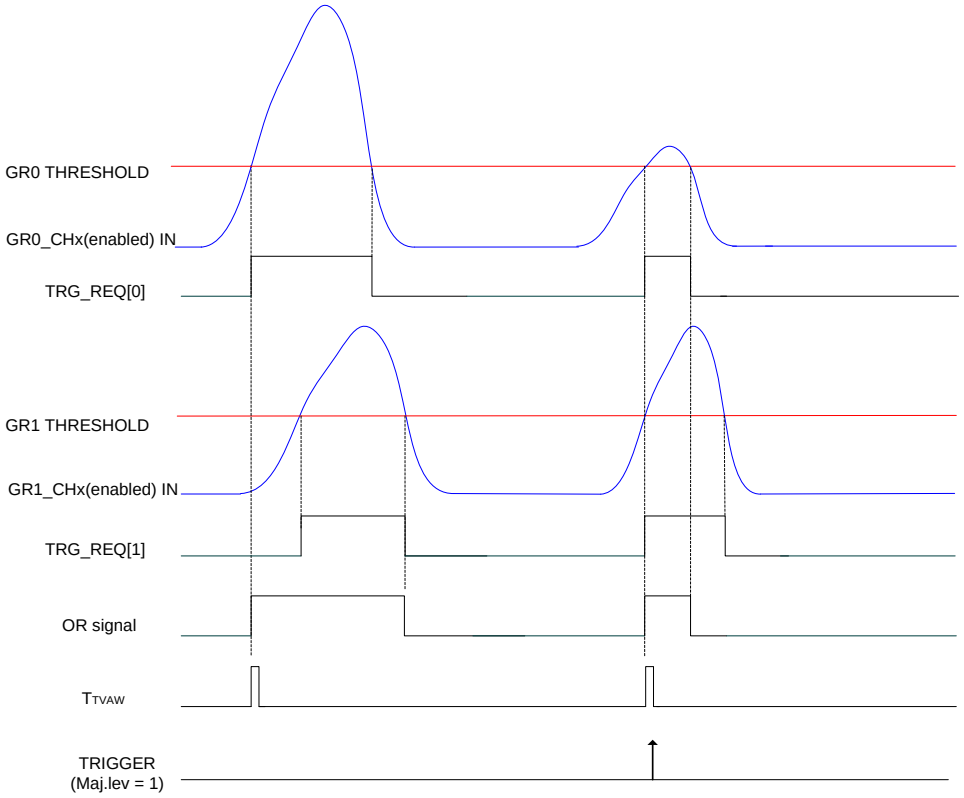


Fig. 9.12: Trigger request relationship with Majority level = 1 and T_{TVAW} = 0.

Note: CAEN provides a guide to coincidences including a practical example of making coincidences with the waveform recording firmware **[RD6]**.

9.8.6 TRG-IN as Gate

It is possible to configure TRG-IN as a gate for trigger anti-veto function. The common acquisition trigger is then issued upon the AND between the external signal on TRG-IN and the other trigger sources but the software trigger (i.e. the software trigger cannot participate in the Trigger as Gate mode). This mode is enabled by setting bit[27] = 1 of register 0x810C and bit[10] = 1 of register 0x811C . The trigger sources participating in AND with TRG-IN are configurable through register 0x810C as well.

9.8.7 Trigger distribution

As described in Sec. **9.8**, the OR of all the enabled trigger sources, synchronized with the internal clock, becomes the common trigger of the board that is fed in parallel to all channels, consequently causing the capture of an event. By default, only the Software Trigger and the External Trigger participate in the common acquisition trigger (refer to the red path on top of Fig. **9.13**).

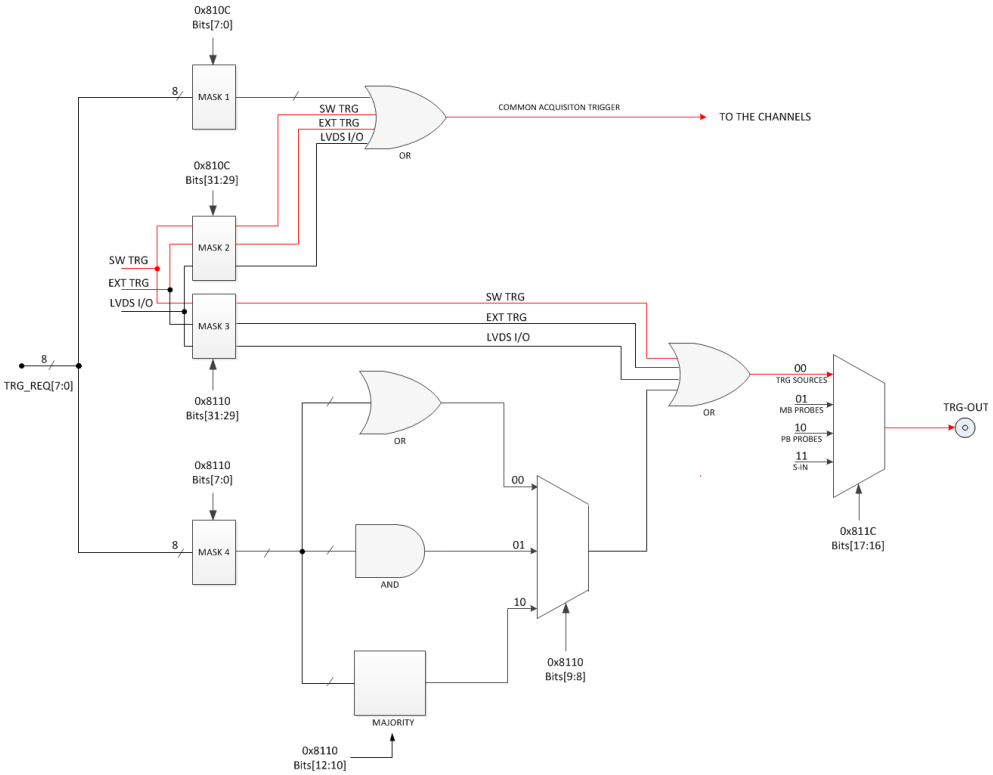


Fig. 9.13: Trigger configuration of TRG-OUT front panel connector.

A Trigger Out signal is also generated on the relevant front panel TRG-OUT connector (NIM or TTL), and allows to extend the trigger signal to other boards. Thanks to its configurability, TRG-OUT can propagate out:

- the OR of all the enabled trigger sources (only the Software Trigger is provided by default, as in the red path of Fig. **9.13**);
- the OR, AND or MAJORITY exclusively of the group trigger requests.

The registers involved in the TRG-OUT programming are:

- Register address 0x8110;
- Register address 0x811C.

9.8.7.1 Example

It could be required to start the acquisition on all the channels of a multi-board system as soon as one of the groups of board ”n” generates a trigger request. Trigger Out signal is then fed to an external Fan Out logic unit (e.g. CAEN V2495 board); the obtained signal has then to be provided to the external trigger input TRG-IN of all the boards in the system (including the board which generated the Trigger Out signal). In this case, the programming steps to perform are thereafter described.

1. Register 0x8110 on board “n”:
   - Enable the desired group to propagate the trigger request as Trigger Out signal (by bit[7:0] mask).
   - Disable Software Trigger, External Trigger and LVDS I/O Trigger as Trigger Out signal (bits[31:29] = 000).
   - Set Trigger Out signal as the OR of the enabled group trigger requests (bits[9:8] = 00).
2. Register 0x10A8 on board “n”:
   - Enable which channels of ”group 0” (in this example) must participate in the trigger request generation (by bits[7:0] mask).
3. Register 0x811C on board “n”:
   - Configure the digitizer to propagates on TRG-OUT the internal trigger sources according to the 0x8110 settings, which are the group trigger requests in this example (bits[17:16] = 00).
4. Register 0x810C on all the boards in the system (including board “n”):
   - Enable External Trigger to participate in the board common acquisition trigger, disable Software Trigger , LVDS I/O Trigger and the group trigger requests (bits[31:29] = 010; bits[7:0] = 00000000)

9.9 Multi-board Synchronization Overview

When multi-board systems are involved in an experiment, it is necessary to synchronize different boards. In the end, the user will be able to acquire from a system of N boards with Y channels each like if they were just one board with N · Y channels.

Synchronizing CAEN digitizers mainly means:

- **Clock synchronization:** the goal is to have the same sampling clock in all the channels. There are two possible modes:
  - Clock Fan-Out. The reference clock signal from an external source is split and provided to all the boards in parallel (for example by using CAEN DT4700 unit).
  - Clock Daisy chain. The first board acts as clock master; it can use internal 50 MHz or an external clock, then generates a clock-out that is provided to the first slave board that propagates it to the second one, and so on. If a board uses the external clock or must generate the clock-out, it is required to reconfigure the PLL (see Sec. **9.3**);
- **Time Stamp synchronization:** the goal is to have the same start/stop of the acquisition and same zero for the time stamp on all the boards at the start of run.
- **Trigger synchronization:** the goal is to propagate and combine the triggers from all the boards to have the same global trigger for the event acquisition.
- **Event data synchronization:** the goal is to keep the event data aligned across boards (same trigger => same data). Each board asserts the Busy signal when its memory buffer is almost full (see Sec. **9.7.5**); the principle is to have a system Busy (global) to veto the acquisition of all the boards as soon as at least one board goes busy, and as long as the system Busy is asserted.

For details about multi-board synchronization, on how to implement the points above and configure the board accordingly, please refer to the dedicated Application Note **[RD7]** or contact CAEN for support (see Chap. **17**).

9.10 Front Panel LVDS I/Os

The V1740 is provided with 16 general purpose programmable LVDS I/O signals (see Chap. **8**). From the ROC FPGA firmware revision 3.8 on, a more flexible configuration management has been introduced, which allows these signals to be programmed in terms of direction (INPUT/OUTPUT) and function by groups of 4.

THE USER MUST SET BIT[8] = 1 AT 0x811C IN ORDER TO ENABLE THE NEW LVDS I/Os CONFIGURATION MODES

NOTE ABOUT LVDS I/Os CONFIGURATIONS IMPLEMENTED IN ROC FW RELEASES <3.8

THE WAVEFORM RECORDING FIRMWARE MAKES ALSO AVAILABLE THE OLD CONFIGURATIONS (bit[8] = 0). USERS WHOSE SOFTWARE BASES ON THE OLD LVDS I/Os CONFIGURATION MANAGEMENT CAN REFER TO THE USER MANUAL OF THE RELEVANT DIGITIZER OR CAN CONTACT CAEN FOR INFORMATION (see Chap. **17**).
SINCE THIS COULD BE NO LONGER GUARANTEED IN THE FUTURE, THE USER IS HEARTLY RECOMMENDED TO TAKE THE NEW CONFIGURATION MANAGEMENT AS REFERENCE!

The direction of the signals are set by the bits[5:2] at register address 0x811C:

Bit[2] → LVDS I/O[3:0]

Bit[3] → LVDS I/O[7:4]

Bit[4] → LVDS I/O[11:8]

Bit[5] → LVDS I/O[15:12]

Where setting the bit to 0 enables the relevant signals in the group as INPUT, while 1 enables them as OUTPUT.

By default, the new modes are disabled (i.e. bit[8] = 0) and the status of the LVDS I/O signals is congruent with the old Programmed I/O mode (see Tab. **9.3**).

Nr.	Direction	Function	Description
0	out	GR 0 trigger request	Over-threshold information
1	out	GR 1 trigger request	
2	out	GR 2 trigger request	
3	out	GR 3 trigger request	
4	out	GR 4 trigger request	
5	out	GR 5 trigger request	
6	out	GR 6 trigger request	
7	out	GR 7 trigger request	
8	out	Memory Full	Memory full flag
9	out	Event Data Ready	Board event data ready flag
10	out	Channels Trigger	OR of the ”new event to be read” signal
11	out	RUN Status	Board run flag
12	in	Trigger Time Tag Reset (active low)	Reset of the trigger time tag counter
13	in	Memory Clear (active low)	Clear command of all channel memories
14	-	reserved	N.A.
15	-	reserved	N.A.

Tab. 9.3: Front Panel LVDS I/Os default settings.

When enabled (i.e. bit[8] = 1), the new management allows each group of 4 signals of the LVDS I/O 16-pin connector to be configured in one of the 4 following modes (according to bits[15:0] at register address 0x81A0):

- Mode 0 (bits[n+3:n] = 0000): REGISTER
- Mode 1 (bits[n+3:n] = 0001): TRIGGER
- Mode 2 (bits[n+3:n] = 0010): nBUSY/nVETO
- Mode 3 (bits[n+3:n] = 0011): LEGACY

where n = 0, 4, 8, 12.

Note: Whatever option is set, the LVDS I/Os are always latched with the trigger and the relevant status of the 16 signals is always written into the header Pattern field (see Sec. **9.7.4**); the user can then choose to read it out or not.

	REGISTER	TRIGGER	nBUSY/nVETO	LEGACY
LVDS IN [15:12]	Reg[15:12]	*Not available*	15: nRunIn 14: nTriggerIn 13: nVetoIn 12: nBusyIn	15: reserved 14: reserved 13: reserved 12: nClear_TTT
LVDS IN [11:8]	Reg[11:8]	*Not available*	11: nRunIn 10: nTriggerIn 9: nVetoIn 8: nBusyIn	11: reserved 10: reserved 9: reserved 8: nClear_TTT
LVDS IN [7:4]	Reg[7:4]	*Not available*	7: nRunIn 6: nTriggerIn 5: nVetoIn 4: nBusyIn	7: reserved 6: reserved 5: reserved 4: nClear_TTT
LVDS IN [3:0]	Reg[3:0]	*Not available*	3: nRunIn 2: nTriggerIn 1: nVetoIn 0: nBusyIn	3: reserved 2: reserved 1: reserved 0: nClear_TTT

Tab. 9.4: Features description when LVDS group is configured as INPUT (waveform recording firmware)

	REGISTER	TRIGGER	nBUSY/nVETO	LEGACY
LVDS IN [15:12]	Reg[15:12]	*Not available*	15: nRunIn 14: reserved 13: reserved 12: reserved	15: reserved 14: reserved 13: reserved 12: reserved
LVDS IN [11:8]	Reg[11:8]	*Not available*	11: nRunIn 10: reserved 9: reserved 8: reserved	11: reserved 10: reserved 9: reserved 8: reserved
LVDS IN [7:4]	Reg[7:4]	*Not available*	7: nRunIn 6: reserved 5: reserved 4: reserved	7: reserved 6: reserved 5: reserved 4: reserved
LVDS IN [3:0]	Reg[3:0]	*Not available*	3: nRunIn 2: reserved 1: reserved 0: reserved	3: reserved 2: reserved 1: reserved 0: reserved

Tab. 9.5: Features description when LVDS group is configured as INPUT (DPP firmware).

	REGISTER	TRIGGER	nBUSY/nVETO	LEGACY
LVDS OUT [15:12]	Reg[15:12]	TrigOut_GR[7:4]	15: nRun 14: nTrigger 13: nVeto 12: nBusy	15: Run 14: Trigger 13: DataReady 12: Busy
LVDS OUT [11:8]	Reg[11:8]	TrigOut_GR[3:0]	11: nRun 10: nTrigger 9: nVeto 8: nBusy	11: Run 10: Trigger 9: DataReady 8: Busy
LVDS OUT [7:4]	Reg[7:4]	TrigOut_GR[7:4]	7: nRun 6: nTrigger 5: nVeto 4: nBusy	7: Run 6: Trigger 5: DataReady 4: Busy
LVDS OUT [3:0]	Reg[3:0]	TrigOut_GR[3:0]	3: nRun 2: nTrigger 3: nVeto 0: nBusy	3: Run 2: Trigger 1: DataReady 0: Busy

Tab. 9.6: Features description when LVDS group is configured as OUTPUT (waveform recording firmware)

	REGISTER	TRIGGER	nBUSY/nVETO	LEGACY
LVDS OUT [15:12]	Reg[15:12]	TrigOut_GR[7:4]	15: nRun 14: reserved 13: reserved 12: reserved	15: Run 14: reserved 13: reserved 12: reserved
LVDS OUT [11:8]	Reg[11:8]	TrigOut_GR[3:0]	11: nRun 10: reserved 9: reserved 8: reserved	11: Run 10: reserved 9: reserved 8: reserved
LVDS OUT [7:4]	Reg[7:4]	TrigOut_GR[7:4]	7: nRun 6: reserved 5: reserved 4: reserved	7: Run 6: reserved 5: reserved 4: reserved
LVDS OUT [3:0]	Reg[3:0]	TrigOut_GR[3:0]	3: nRun 2: reserved 3: reserved 0: reserved	3: Run 2: reserved 1: reserved 0: reserved

Tab. 9.7: Features description when LVDS group is configured as OUTPUT (DPP firmware).

9.10.1 Mode 0: REGISTER

Direction is INPUT: the logic level of the LVDS I/O signals can be read at register address 0x8118.

Direction is OUTPUT: the logic level of the LVDS I/O signals can be written at register address 0x8118.

9.10.2 Mode 1: TRIGGER

Direction is INPUT: Not available.

Direction is OUTPUT: the TrgOut_GR[(n + 3) : n] signals ($n = 0, 4$) consist of the group trigger requests coming directly from the mezzanines.

9.10.3 Mode 2: nBUSY/nVETO

Note: In case a DPP firmware is loaded on the FLASH page, only the nRun signal (among those described below) is available in the nBusy/nVETO mode (see **Tab. 9.5** and **Tab. 9.7**).

nBusy Signal

nBusyIn (INPUT) is an active low signal which, if enabled, is used to generate the nBusy signal (OUTPUT) as below.

The Busy signal (fed out on LVDS I/Os or TRG-OUT LEMO connector) is:

Almost_Full OR **(LVDS_BusyIn** AND **BusyIn_enable)**

where

- **Almost_Full** indicates the filling of the Buffer Memory up to a programmable level (12-bit range) set at register address 0x816C;
- **LVDS_BusyIn** is available in nBUSY/nVETO configuration (see Tab. **9.6**);
- **BusyIn_enable** is set at register address 0x8100, bit[8].

nVETO Signal

Direction is INPUT: nVETOIn is an active low signal which, if enabled (register address 0x8100, bit[9] = 1), is used to veto the generation of the common trigger propagated to the channels for the event acquisition. NVETOIn can optionally be used to disable the TRG-OUT generation (TRG-OUT VETO). The TRG-OUT VETO is enabled by setting bit[12] = 1 a register address 0x8100, while the TRG-OUT VETO duration can be extended by the register 0x81C4.

Direction is OUTPUT: the nVETO signal is the copy of nVETOIn.

nTrigger Signal

Direction is INPUT: nTriggerIn is an active low signal which, if enabled, is a real trigger able to cause the event acquisition. It can be propagated to TRG-OUT LEMO connector or to the individual triggers.

Direction is OUTPUT: nTrigger signal is the copy of the trigger signal propagated to the TRG-OUT LEMO connector or copy of the acquisition common trigger. This is selected by bit[16] of the 0x81A0 register.

nRun Signal

Direction is INPUT: nRunIn is an active low signal which can be used as Start for the digitizer (register address 0x8100, bits[1:0] = 11). It is possible to program the Start on the level or on the edge of the nRunIn signal (register address 0x8100, bit[11]).

Direction is OUTPUT: nRun signal is the inverse of the internal Run of the board.

9.10.4 Mode 3: LEGACY

Note: In case a DPP firmware is loaded on the FLASH page, no signal is available if the direction is INPUT, while only the Run signal is available if the direction is OUTPUT in the Legacy mode (see **Tab. 9.5** and **Tab. 9.7**).

Legacy Mode has been introduced in order the LVDS connector (properly programmed) to be able to feature the same I/O signals available in the ROC FPGA firmware revisions lower than 3.8.

nClear_TTT Signal

Direction is INPUT: It is the Trigger Time Tag (TTT) reset, like in the old configuration.

Direction is OUTPUT: not implemented.

Busy Signal

Direction is INPUT: not used.

Direction is OUTPUT: the Busy signal is active high and it is exactly the inverse of the nBusy signal (see Sec. **9.10.3**). In case register address 0x816C is set to 0 and the BusyIn signal is disabled, the Busy is the FULL signal present in the old configuration.

DataReady Signal

Direction is INPUT: not used.

Direction is OUTPUT: the DataReady is an active high signal indicating that the board has data available for readout (the same as the DataReady front panel LED does).

Trigger Signal

Direction is INPUT: not used.

Direction is OUTPUT: the active high Trigger signal is the copy of the acquisition trigger (common trigger) sent from the motherboard to the mezzanines (it is neither the signal provided out on the TRG-OUT LEMO connector nor the inverse of the signal sent to the LVDS connector).

Run Signal

Direction is INPUT: not used.

Direction is OUTPUT: the Run signal is active high and represents the inverse of the nRun signal (see Sec. **9.10.3**).

Note: The Memory Clear signal of the LVDS I/O features is not implemented in the LEGACY LVDS configuration mode.

9.11 Analog Monitor

The board houses a 12-bit (125 MHz) DAC with 0 ÷ 1 V dynamics on a 50 Ω load, whose input is controlled by the ROC FPGA and the signal output (driving 50 Ω) is available on the MON/Σ output connector. MON output of more boards can be summed by an external Linear Fan In.

The DAC control logic implements four operating modes according to the value of bit[2:0] at register address 0x8144:

MODE	0x8144 VALUE
Trigger Majority	0x0
Test	0x1
Not Used	0x2
Buffer Occupancy	0x3
Voltage Level	0x4

9.11.1 Trigger Majority Mode

It is possible to generate a Majority signal with the DAC: a voltage signal whose amplitude is proportional to the number of triggering groups (i.e those enabled groups where at least one of the enabled channels in the group exceeded the programmed threshold) ; 1 step = 125 mV. This information can be exploited, via an external discriminator, to produce a common trigger signal when the number of triggering groups has exceeded a particular threshold.

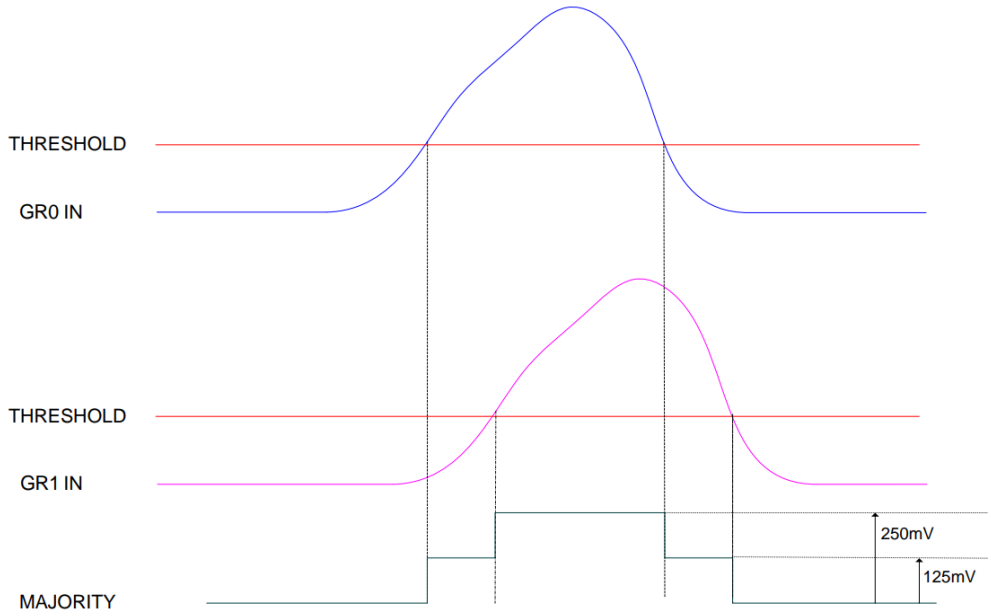


Fig. 9.14: Majority logic (2 triggering groups; bit[6]=0 at register address 0x8000).

In the example depicted in Fig. **9.14**, the MON output provides a signal whose amplitude is proportional to the number of groups exceeding the trigger threshold.

9.11.2 Test Mode

In this mode, the MON output provides a sawtooth signal with 1 V amplitude and 30.52 kHz frequency.

9.11.3 Buffer Occupancy Mode

In this mode, MON output connector provides a voltage value increasing, proportionally with the number of buffers filled with events, in fixed steps of 0.976 mV given by:

$$\frac{V_{max}}{N_{bmax}}$$

where $V_{max} \approx 1$ V and $N_{bmax} = 1024$ is the Maximum_Number_of_Buffers (i.e. the value of the register address 0x800C, as introduced in Sec. **9.7.3**).

Example: if 0x800C = 0x4 (i.e. 16 buffers), the maximum Buffer Occupancy output voltage level is given by 0.976 mV $\times$ 16.

This mode allows to test the readout efficiency: in fact, if the average event readout throughput is as fast as trigger rate, then MON out value remains constant; otherwise if MON out value grows in time, this means that readout rate is slower than trigger rate.

Starting from revision **4.9** of the ROC FPGA (motherboard) firmware, it is possible to apply a digital gain to the fixed step, particularly when the memory is organized in a small number of buffers. The gain can be set as powers of two ranging between $2^0 = 1$ (no gain, which is the default setting) and 2^A, where the exponent is the value to write at register address 0x81B4.

9.11.4 Voltage Level Mode

In this mode, MON out provides a voltage value programmable via the 12-bit 'N' parameter written in the 0x8138 register, with: $V_{mon} = 1/4096 \times N$ (Volt).

9.12 Test Pattern Generator

The AMC FPGA can emulate the ADC and write into memory a triangular shape from 0 to 3FFF and back from 3FFF to 0 for test purposes. It can be enabled via register address 0x8000.

9.13 Reset, Clear and Default Configuration

9.13.1 Global Reset

Global Reset is performed at power-on of the module or via software by write access at register address 0xEF24 . It allows to clear the data off the Output Buffer, the event counter and performs a FPGAs global reset, which restores the FPGAs to the default configuration. It initializes all counters to their initial state and clears all detected error conditions.

9.13.2 Memory Reset

The Memory Reset clears the data off the Output Buffer.

The Memory Reset can be forwarded via a write access at register address 0xEF28 **[RD1]**. In the old LVDS I/O configuration (ROC FPGA revision before **3.8**), it is also possible to perform a memory clear by sending a pulse to the front panel dedicated Memory Clear input (see Tab. **9.3**).

9.13.3 Timer Reset

The timer reset initializes the time tag counters (Event Time Tag and Group Trigger Time Tag).
The timer reset can be issued either via software by a software clear command at 0xEF28 register address, or via hardware by sending a pulse to the front panel Trigger Time Tag Reset input of LVDS I/Os (see Sec. **9.10**), or to the S-IN input (leading edge sensitive). In case the S-IN connector needs to be used to reset the trigger time stamps, no configuration or access to registers is necessary. The user only has to transmit a NIM or TTL signal to the input, depending on the software selected logic level for the S-IN connector. The time stamps reset occurs at every leading edge of the logic signal sent to the S-IN connector.

9.14 VMEBus Interface

The module is provided with a fully compliant VME64/VME64X interface, whose main features are:

- EUROCARD 9U Format
- J1/P1 and J2/P2 with either 160 pins (5 rows) or 96 (3 rows) connectors
- A24, A32 and CR-CSR address modes
- D32, BLT/MBLT, 2eVME, 2eSST data modes
- MCST write capability
- CBLT data transfers
- RORA interrupter
- Configuration ROM

9.14.1 Addressing Capabilities

- Base address: the module works in A24/A32 mode The Base Address of the module is selected through four rotary switches (see Fig. **8.2**), then it is validated only with either a power-ON cycle or a System Reset (see Sec. **9.13**).

ADDRESS MODE	ADDRESS RANGE	NOTES
A24	[0x000000:0xFF0000]	SW2 and SW3 ignored

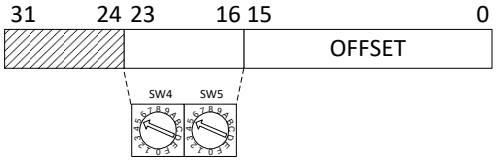


Fig. 9.15: A24 addressing.

ADDRESS MODE	ADDRESS RANGE	NOTES
A32	[0x00000000:0xFFFF0000]	

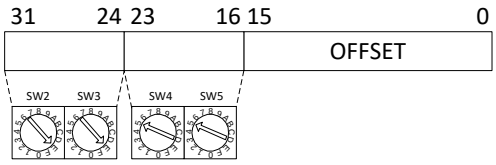


Fig. 9.16: A32 addressing.

- CR/CSR address: the addressing is based on the slot number taken from the relevant backplane lines. The recognised Address Modifier for this cycle is 2F. *This feature is implemented only on versions with 160-pin connectors.*

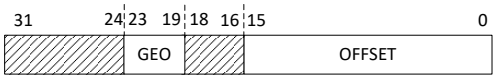


Fig. 9.17: CR/CSR addressing.

9.14.2 Address Relocation

The bit[15:0] of register address 0xEF10 allow to set via software the board Base Address (valid values ≠ 0). Such register allows to overwrite the rotary switches settings; its setting is enabled via bit[6] of the register address 0xEF00. The used addresses are:

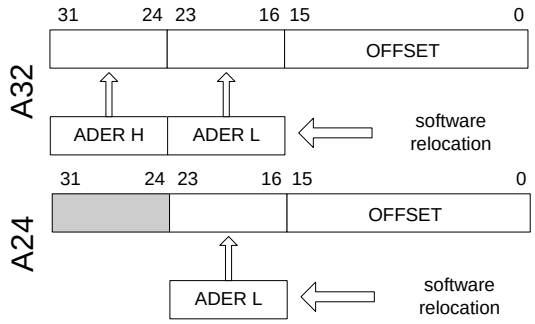


Fig. 9.18: Software relocation of base address

9.15 Data Transfer Capabilities and Events Readout

The board features a Multi-Event digital memory per channel, configurable by the user to be divided into 1 up to 1024 buffers, as detailed in Sec. **9.7.3**. Once they are written in the memory, the events become available for readout via VMEbus or Optical Link. During the memory readout, the board can store other events (independently from the readout) on the available free buffers.

The events are read out sequentially and completely, starting from the Header of the first available event, followed by the the data from the enabled groups (from 0 to 7) as reported in Fig. **9.6**. Once an event is completed, the relevant memory buffer becomes free and ready to be written again (old data are lost). After the last word in an event, the first word (Header) of the subsequent event is readout. It is not possible to read out an event partially.

The size of an event (EVENT SIZE) is configurable and depends on register addresses 0x8020 and 0x800C , as well as on the number of enabled channels. The board supports D32 single data readout, Block Transfer BLT32 and MBLT64, 2eVME and 2eSST cycles. Sustained readout rate is up to 70 MB/s with MBLT64, up to 200 MB/s with 2eSST.

9.15.1 Block Transfer D32/D64, 2eVME, and 2eSST

The Block Transfer readout mode allows to read N complete events sequentially, where N is set at register address 0xEF1C, or by using the *SetMaxNumEventsBLT* function of the CAENDigitizer library **[RD8]**.

When developing programs, the readout process can be implemented on different basis:

- Using **Interrupts**: as soon as the programmed number of events is available for readout, the board sends an interrupt to the PC over the optical communication link **(not supported by USB)**.
- Using **Polling** (interrupts disabled): by performing periodic read accesses to a specific register of the board it is possible to know the number of events present in the board and perform a BLT read of the specific size to read them out.
- Using **Continuous Read** (interrupts disabled): continuous data read of the maximum allowed size (e.g. total memory size) is performed by the software without polling the board. The actual size of the block read is determined by the board that terminates the BLT access at the end of the data, according to the configuration of register address 0xEF1C, or the library function *SetMaxNumEventsBLT* mentioned above. If the board is empty, the BLT access is immediately terminated and the “Read Block” function will return 0 bytes (it is the *ReadData* function in the CAENDigitizer Library).

The event is configurable as indicated in the introduction of the paragraph, namely:

[Event Size] = [8*(Buffer Size)] + [16 bytes]

Then, it is necessary to perform as many cycles as required in order to readout the programmed number of events.

It is suggested to enable BERR signal during BLT32 cycles, in order to end the cycle avoiding filler readout. The last BLT32 cycle will not be completed, it will be ended by BERR after the #N event in memory is transferred (see example in the figure below).

Since some 64-bit CPU cut off the last 32- bit word of a transferred block, if the number of words composing such block is odd, it is necessary to add a dummy word (which has then to be removed via software) in order to avoid data loss. This can be achieved by setting the ALIGN64 bit (bit[5]) at register address 0xEF00.

MBLT64 cycle is similar to the BLT32 cycle, except that the address and data lines are multiplexed to form 64-bit address and data buses.

The 2eVME allows to achieve higher transfer rates thanks to the requirement of only two edges of the two control signals (DS and DTACK) to complete a data cycle.

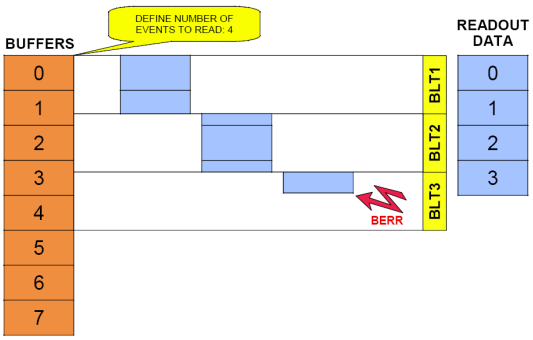


Fig. 9.19: Example of BLT readout

9.15.2 Chained Block Transfer D32/D64

The V1740 allows to readout events from more Daisy chained boards (Chained Block Transfer mode).

The technique which handles the CBLT is based on the passing of a token between the boards (it is necessary to verify that the used VME crate supports such cycles).

Several contiguous boards, in order to be Daisy chained, must be configured as “first”, “intermediate” or “last” via register address 0xEF0C. A common Base Address is then defined via the same register; when a BLT cycle is executed at the address CBLT_Base + 0x0000 ÷ 0x0FFC, the “first” board starts to transfer its data, driving DTACK properly; once the transfer is completed, the token is passed to the second board via the IACKIN-IACKOUT lines of the crate, and so on until the “last” board, which completes the data transfer and asserts BERR (which has to be enabled): the Master then ends the cycle and the slave boards are rearmed for a new acquisition.

If the size of the BLT cycle is smaller than the events size, the board which has the token waits for another BLT cycle to begin (from the point where the previous cycle has ended).

9.15.3 Single D32 Transfer

This mode allows the user to readout a word per time, from the header (actually 4 words) of the first available event, followed by all the words until the end of the event, then the second event is transferred. The exact sequence of the transferred words is shown in Sec. **9.7.4**.

It is suggested, after the 1^{st} word is transferred, to check the EVENT SIZE information and then do as many cycles as necessary (actually EVENT SIZE -1) in order to completely read the event.

9.16 Optical Link Access

The digitizer houses an interface for optical link communication which uses optical fiber cables as physical transmission line, with a maximum transfer data rate of 80 MB/s.

CONET is the proprietary serial protocol designed by CAEN to enable optical link communication between digitizers (acting as CONET slaves) and the host PC. This communication needs CONET master such as the A2818, A3818, and A5818 controllers, or the A4818 adapter.

CONET2 is the latest protocol version, implemented at the firmware level on digitizers and controllers, that improves the data transfer rate efficiency by 50% compared to the earlier CONET1 version.

Note: CONET1 and CONET2 protocol versions are incompatible; communication will fail in any optical chain containing both CONET1 and CONET2 boards.

To update your system from CONET1 to CONET2, it is recommended to follow the instructions provided by CAEN in the dedicated Application Note **[RD9]**.

The optical link interface has Daisy-chain capability. Therefore, it is possible to connect up to eight digitizers to a single Optical Link Controller by using the A2818 PCI card or A4818 adapter, while up to thirty- two digitizers with the A3818C PCIe (4-link version) card or A5818 PCIe card. Detailed information can be found at the relevant controller web page on CAEN website.

The parameters for read/write accesses via Optical Link are the same used by VME cycles (Address Modifier, Base Address, data Width, etc); wrong parameter settings cause Bus Error.

Setting bit[3] at register address 0xEF00 enables the module to broadcast an interrupt request on the Optical Link; the enabled Optical Link Controllers propagate the interrupt on the PCI bus when a request from the Optical Link is sensed. Interrupts can also be managed at the CAENDigitizer library level **[RD8]**.

VME and Optical Link accesses take place on independent paths and are handled by board internal controller, with VME having higher priority; anyway it is better to avoid accessing the board via VME and Optical Link simultaneously.

10 Drivers & Libraries

10.1 Drivers

In order to interface with the board, CAEN provides the drivers for the supported physical communication channels and compliant with Windows® and Linux® OS:

- **CONET Optical Link**, managed by the A2818 PCI card (Obsolete), the A3818 e A5818 PCIe cards. The driver installation package is available on CAEN website in the "Software/Firmware" tab at the A2818, A3818 or A5818 pages, respectively (**login required**).

Note: For the installation of the Optical Link driver, refer to the User Manual of the specific card **[RD10] [RD11]**.

- **USB 2.0 Link**, managed by CAEN (USB-to-VME) Bridges V3718. The driver installation package are downloadable for free on CAEN website at the V3718 page (**login required**).
- **USB 3.0 Link**, managed by the V4718 USB-to-VME Bridge and by the A4818 (USB3-to-CONET) Adapter. The driver installation packages are downloadable for free on CAEN website at the V4718 and A4818 page respectively (**login required**). The driver for the V4718 has to be installed for Linux users only, while the driver for the A4818 is reserved to Windows users only.

Note: To install the USB Link driver, follow the instructions inside the ReadMe file included in the packet or refer to the V3718, V4718 User Manuals **[RD12][RD13]** or A4818 adapter Data Sheet **[RD14]** .

10.2 Libraries

CAEN libraries are a set of middleware software required by CAEN software tools for a correct functioning. These libraries, including also demo and example programs, represent a powerful base for users who want to develop customized applications for the digitizer control (communication, configuration, readout, etc.):

- **CAENDigitizer [RD8]** is a library of C functions specifically designed for the Digitizer families and supports both waveform recording and DPP firmware. The CAENDigitizer library is based on the CAENComm which, in turn, is based on CAENVMELib. For this reason, **the CAENVMELib and CAENComm libraries must be already installed on the host PC before installing the CAENDigitizer**.
- **CAENComm** library **[RD15]** manages the communication at low level (read and write access). The purpose of this library is to implement a common interface to the higher software layers, masking the details of the physical channel and its protocol, thus making the libraries and applications that rely on the CAENComm independent from the physical layer. **The CAENComm requires the CAENVMELib library (access to the VME bus), even in the cases where the VME is not used**.

Installation packages are available for free download on CAEN web site (*www.caen.it*) at each library page (**login required**).

As an alternative to the libraries mentioned above, a more recent set of libraries can be used:

- **CAEN_FE_lib [RD16]** is a library that can be used to control and acquire data from CAEN digitizers. This library is just an interface and does not includes support to any digitizer family. In order to use a digitizer you must install first the respective underlying CAEN_Digx library.

- **CAEN_DIG1_lib [RD16]** is the high level library of functions designed specifically for CAEN V/VX17xx, DT57xx, N67xx first generation digitizers. The CAEN_FE_Lib library must be already installed on the host PC before installing the CAEN_Dig1.
- **CAEN_DIG2_lib [RD16]** is the high level library of functions designed specifically for CAEN 27xx second generation digitizers. The CAEN_FE_Lib library must be already installed on the host PC before installing the CAEN_Dig2.

Installation packages are available for free download on CAEN web site (*www.caen.it*) at CAEN_FELib page (**login required**).

All the libraries here described supports the following communication channels (Fig. **10.1**):

PC → USB3 → A4818 → CONET → V1740(VX1740) Digitizer

PC → USB → V3718/VX3718 → VMEbus → V1740(VX1740) Digitizer

PC → USB3 → V4718/VX4718 → VMEbus → V1740(VX1740) Digitizer

PC → USB3 → A4818 → CONET → V3718/VX3718 → VMEbus → V1740(VX1740) Digitizer

PC → USB3 → A4818 → CONET → V4718/VX4718 → VMEbus → V1740(VX1740) Digitizer

PC → PCI/PCIe A2818/A3818/A5818 → CONET → V1740(VX1740) Digitizer

PC → PCI/PCIe → A2818/A3818/A5818 → CONET → V3718/VX3718 → VMEbus → V1740(VX1740) Digitizer

PC → PCI/PCIe → A2818/A3818/A5818 → CONET → V4718/VX4718 → VMEbus → V1740(VX1740) Digitizer

PC → ETHERNET → V4718/VX4718 → VMEbus → V1740(VX1740) Digitizer

WHEN TO INSTALL CAEN LIBRARIES:

WINDOWS® and LINUX® compliant customized software. The user must install the required libraries apart.

LINUX® compliant non-stand alone CAEN software. The user must install the required libraries apart to run the software.

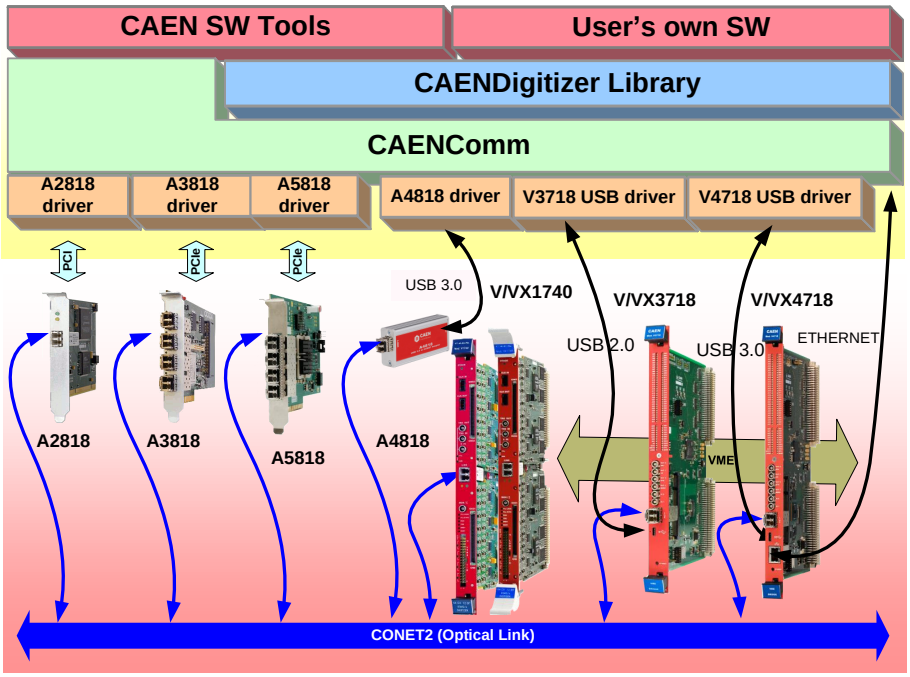


Fig. 10.1: Drivers and software layers based on CAENComm and CAENDigitizer libraries.

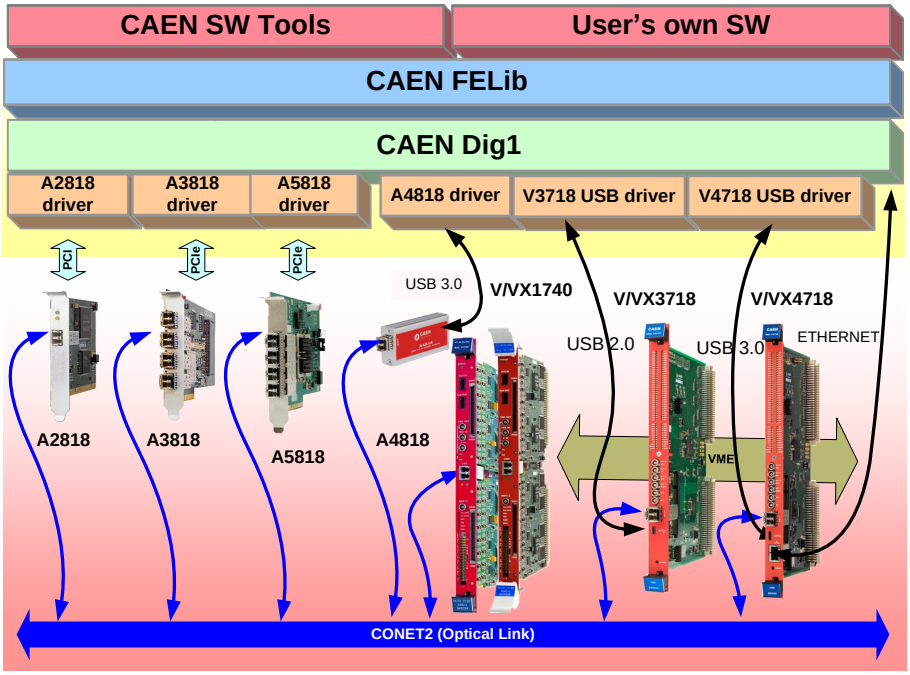


Fig. 10.2: Drivers and software layers based on CAEN_FELib and CAEN_Dig1 libraries.

11 Software Tools

CAEN provides software tools to interface the 740 digitizer family, which are available for free download at the ”Digitizer Software” section on CAEN website.

11.1 CAEN Toolbox

CAEN Toolbox is the comprehensive software suite designed for CAEN Front-End boards.

With V1740, CAEN Toolbox simplifies various tasks into a few easy steps, including:

- Uploading different FPGA firmware versions to the digitizer
- Reading the firmware release of the digitizer
- Managing firmware licenses, particularly for DPP firmware
- Upgrading the internal PLL
- Obtaining the Board Info file, useful for support
- Managing the reboot of the FPGA firmware from either the Backup or the Standard FLASH page
- Debugging your setup using the Manual Controller

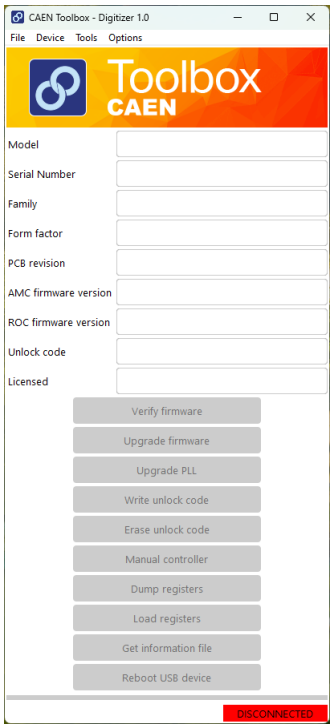


Fig. 11.1: CAEN Toolbox Graphical User Interface

Related to V1740/VX1740, CAEN Toolbox is based on the CAENComm library (see Sec. **10.2**). The software is compatible with both Windows® and Linux® platforms, operating as a standalone application on each available version. For installation instructions and a detailed description of its features, refer to the CAEN Toolbox documentation **[RD3]**. Both the documentation and software packages can be downloaded directly from the dedicated webpage on the CAEN website (**login required**).

11.2 CAENComm Demo

CAENComm Demo is simple software developed in C/C++ source code and provided both with Java™ and LabVIEW™ GUI interface. The demo mainly allows for a full board configuration at low level by direct read/write access to the registers and may be used as a debug instrument.

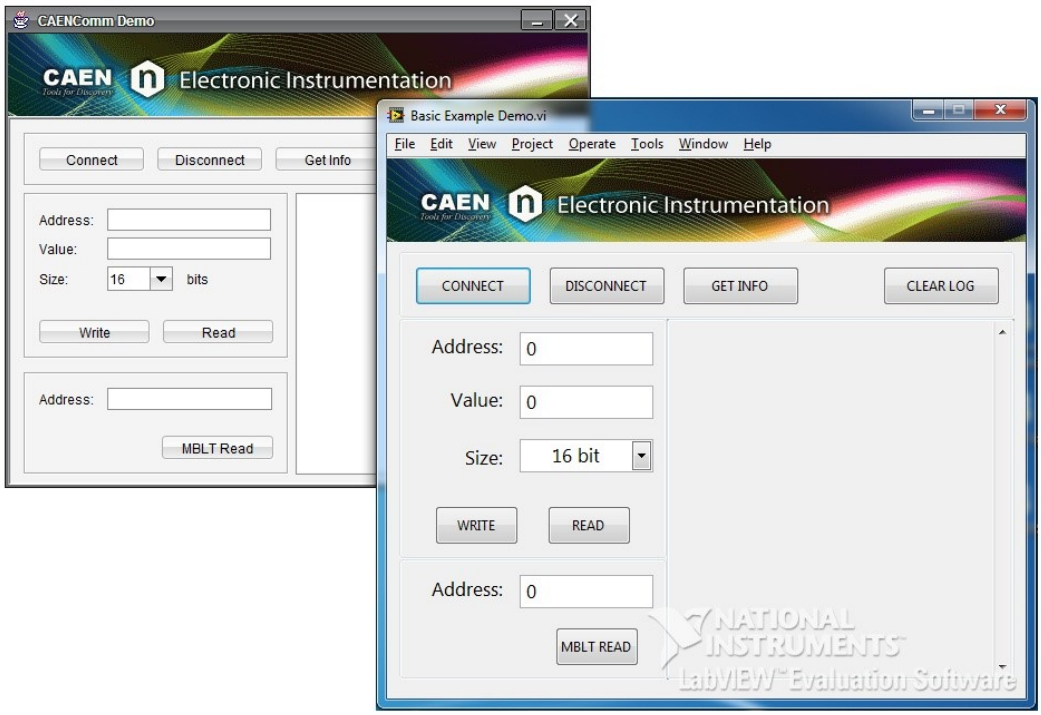


Fig. 11.2: CAENComm Demo Java and LabVIEW graphical interface

CAENComm Demo is based on the CAENComm library (see Sec. **10.2**) and it is included in the installation package of the library. The software is available only for Windows® platforms.

The software installation package and the documentation **[RD15]** can be downloaded from the CAEN website (**login required**).

11.3 CAEN WaveDump

WaveDump is a basic console application, with no graphics, supporting only CAEN digitizers running the waveform recording firmware. It allows the user to program a single board (according to a text configuration file containing a list of parameters and instructions), to start/stop the acquisition, read the data, display the readout and trigger rate, apply some post-processing (e.g. FFT and amplitude histogram), save data to a file and also plot the waveforms using Gnuplot (third-party graphing utility: www.gnuplot.info).

WaveDump is a very helpful example of C code demonstrating the use of libraries and methods for an efficient readout and data analysis. Thanks to the included source files and the VS project, starting with this demo is strongly recommended to all those users willing to write the software on their own.

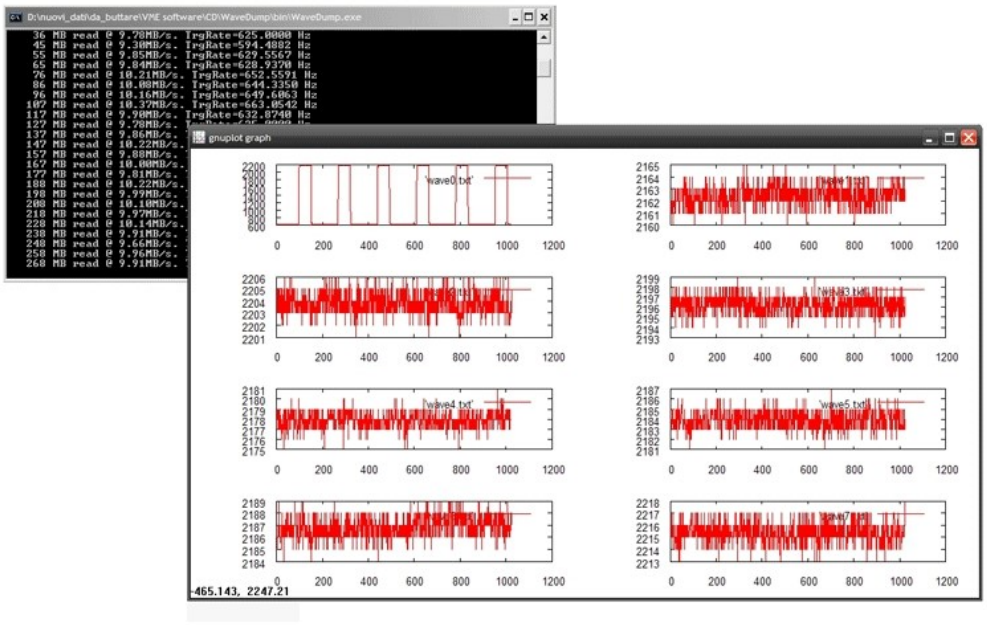


Fig. 11.3: CAEN WaveDump

CAEN WaveDump relies on the CAENDigitizer library (see Sec. **10.2**) and it can run on Windows® and Linux® platforms. Windows® versions of WaveDump are stand-alone (all required libraries are present within the software package), while the Linux® versions need the required libraries to be previously installed by the user. Moreover Linux® users are required to install the third-party Gnuplot.

The installation packages, the software User Manual **[RD17]** and a guide for getting started with it can be downloaded from CAEN website (**login required**).

> CAEN WaveDump does not work with digitizers running DPP firmware.

11.4 CAEN WaveDump2

WaveDump2 has been developed to support the Digitizer 2.0 new generation of CAEN digitizers, including the 2740, 2745, 2730, and future series, running the waveform recording firmware (D-Wave).

Starting from **revision 2.0.0**, support has been extended to pre-existing CAEN Digitizer 1.0 series: DT57XX, N67XX, V17XX, VX17XX.

WaveDump2 is a C++ software developed upon Qt cross-platform application development framework. Through an advanced and user-friendly configuration GUI, it provides all the necessary tools and functionalities for managing any hardware parameters. The settings can be conveniently stored into or loaded from a configuration file, or a sequence of operations can be recorded to script files and then loaded to be re-executed. From a single board to multiple boards and multi-board synchronized systems, data acquisition is managed through a dedicated toolbar and upon different start/stop criteria. Live monitoring of the acquisition statistics can be enabled.

Waveforms are live plotted in a dedicated section emulating an 8-channel digital oscilloscope, which also provides cursors to make on-screen measurements, as well as marker lines to indicate the trigger position and the trigger threshold level. Traces can be individually enabled/disabled, and a zooming control in both vertical and horizontal directions is also possible. Basic processing like FFT and samples histogram is provided runtime. The collected waveform data can be saved to ASCII or binary files for offline analysis.

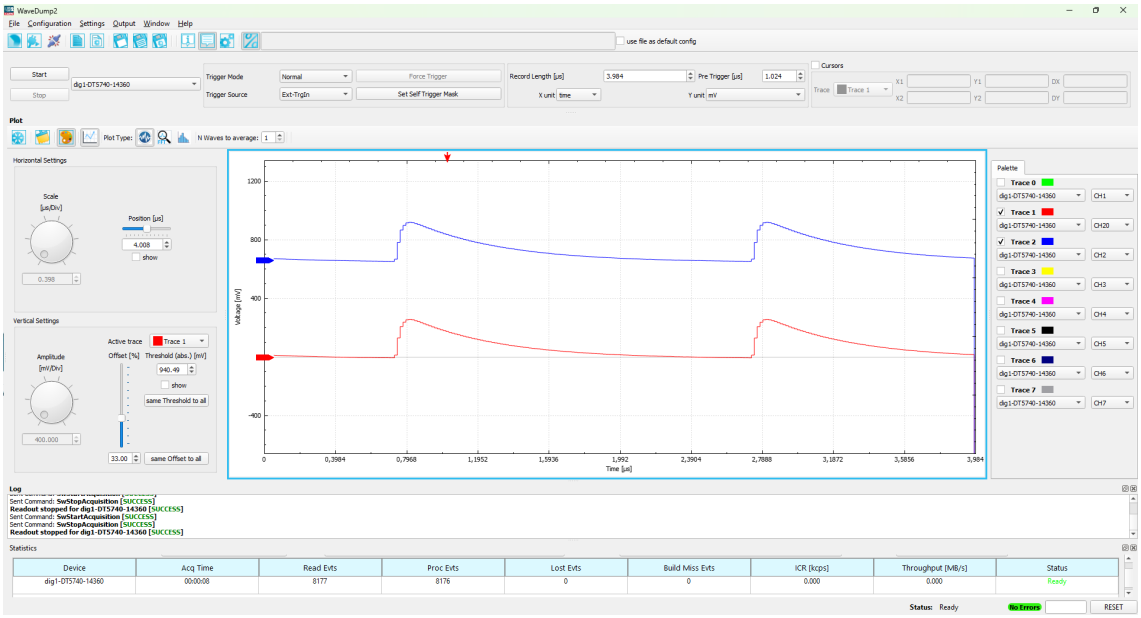


Fig. 11.4: CAEN WaveDump2

Related to Digitizer 1.0, WaveDump2 is based on the CAEN FELib and Dig1 libraries (see Sec. **10.2**). The software can run on 64-bit Windows® and Linux® operating systems. Regardless of the platform, the CAEN FELib is automatically installed along with the software, while the Dig1 library must be manually installed by the user.

The installation packages, the required libraries and the software User Manual **[RD18]** can be downloaded on CAEN website (**login required**).

CAEN WaveDump2 does not work with digitizers running DPP firmware.

11.5 DPP-QDC Demo

DPP-QDC Demo is a is C demo software that manages the communication and the data acquisition from 740D digitizer series running the DPP-QDC firmware. It is possible to set the communication parameters and DPP settings; waveforms and histograms can also be plotted in real time for one channel at a time, and both waveforms and lists of time stamp and energy can be saved. DPP-QDC Demo Software is provided including C source files and VS project for developers.

DPP-QDC Demo relies on the CAENDigitizer library (see Sec. **10.2**). The software is available only for Windows® platforms and it is stand-alone.
DPP-QDC Demo installation package and the firmware User Manual **[RD2]** can be downloaded from CAEN website at the DPP-QDC Firmware webpage (**login required**).

DPP-QDC Demo works only with x740D digitizers running the DPP-QDC firmware.

DPP-QDC Demo does not work with waveform recording firmware.

11.6 CoMPASS

CoMPASS (CAEN Multi-PArameter Spectroscopy Software) is the new software from CAEN able to implement a Multi-parametric DAQ for Physics Applications, where the detectors can be connected directly to the digitizers inputs and the software acquires energy, timing, and PSD spectra.

CoMPASS software has been designed as a user-friendly interface to manage the acquisition with all the CAEN DPP algorithm. CoMPASS can manage multiple boards, even in synchronized mode, and the event correlation between different channels (hardware and/or software), apply energy and PSD cuts, calculate and show the statistics (trigger rates, data throughput, etc...), save the output data files (raw data, lists, waveforms, spectra) and use the saved files to run off-line with different processing parameters.

CoMPASS Software supports CAEN first generation digitizers x720, x724, x725, x730, x740D, x751 digitizer families running the DPP-PSD, DPP-PHA and DPP-QDC firmware, the x780, x781 and x782 MCA family, the DT5790 Pulse Processor and the second generation digitizer x2740, x2745 and x2730 running the DPP-PSD and DPP-PHA firmware.

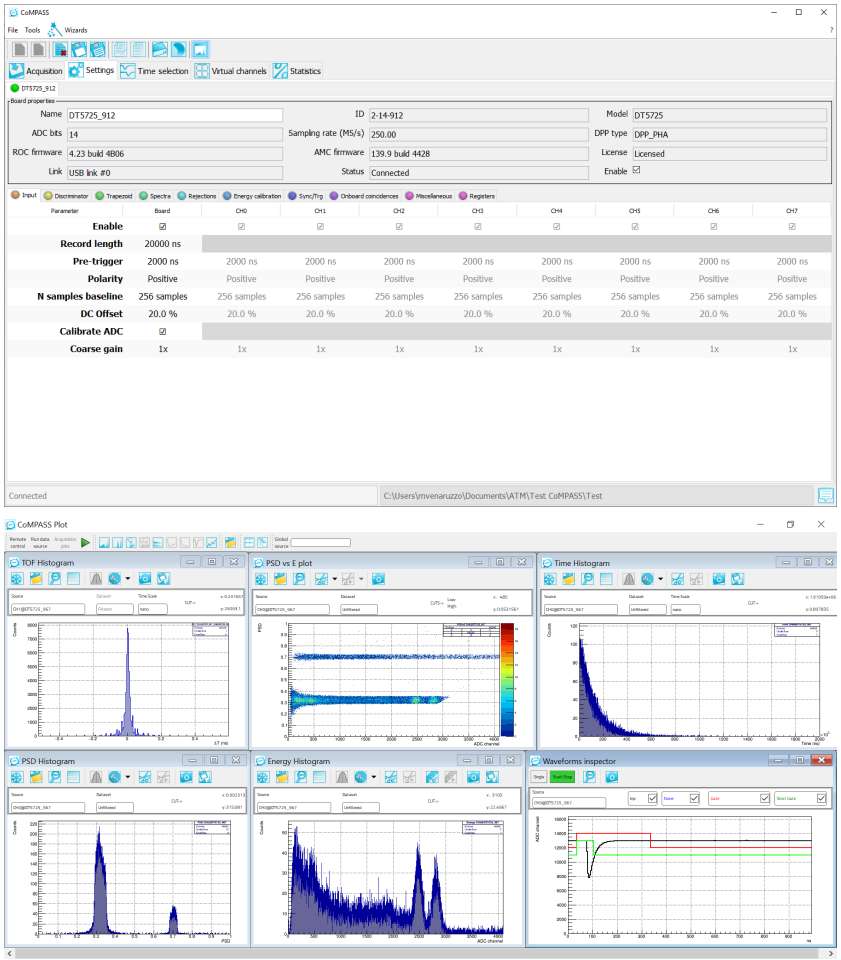


Fig. 11.5: CoMPASS software tool.

CoMPASSs relies on the CAENDigitizer library (see Sec. **10.2**). The software is compatible with both Windows® and Linux® platforms, operating as a standalone application on each available version. The installation packages, the required libraries and the software User Manual **[RD19]** can be downloaded from CAEN website (**login required**).

> CoMPASS does not work with waveform recording firmware.

12 HW Installation

To power on the board, perform the following steps:

1. Insert the V1740 into the crate;
2. power up the crate.

ONLY QUALIFIED PERSONNEL SHOULD PERFORM INSTALLATION OPERATIONS

DO NOT INSTALL THE EQUIPMENT IN A SETUP WHERE IT IS DIFFICULT TO ACCESS THE BACK PANEL FOR DISCONNECTING THE DEVICE

IT IS RECOMMENDED THAT THE SWITCH OR CIRCUIT-BREAKER IS NEAR THE EQUIPMENT

THE SAFETY OF ANY SYSTEM THAT INCORPORATES THE DEVICE IS UNDER THE RESPONSIBILITY OF THE ASSEMBLER OF THE SYSTEM

12.1 Power-on Status

At power-on, the module is in the following status:

- the Output Buffer is cleared;
- registers are set to their default configuration

After the power-on, only the NIM and PLL LOCK LEDs must stay ON (see Fig. **12.1**).

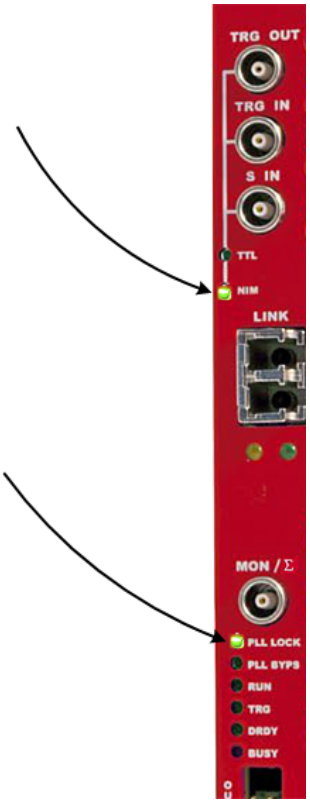


Fig. 12.1: Front panel LEDs status at power-on.

13 Firmware and Upgrades

The board hosts one FPGA on the mainboard (ROC FPGA) and two FPGAs per mezzanine (AMC FPGAs), so that each AMC FPGA serves 16 channels. The AMC FPGAs firmware is identical. The digitizer firmware file is a unique file which will update all the board FPGAs (ROC and AMCs) at the same time.

ROC FPGA MAINBOARD FPGA (Readout Controller + VME interface):

FPGA Altera Cyclone EP1C20

AMC FPGA MEZZANINE FPGA (ADC readout/Memory Controller):

FPGA Altera Cyclone EP3C16

FPGA Altera Cyclone EP3C40 (740D version only)

The firmware is stored onto the on-board FLASH memory. Two copies of the firmware are stored in two different pages of the FLASH, referred to as Standard (STD) and Backup (BKP). In case of waveform recording firmware, the board is delivered equipped with the same firmware version on both pages.
At power-on, a micro-controller reads the FLASH memory and programs the module automatically loading the first working firmware copy, that is the STD one in normal operating.

The on-board dedicated SW7 dip switch, set on STD position by default, allows to select the first FLASH page to be read at power-on (see Sec. **8.2**).

It is possible to upgrade the board firmware via VMEbus or Optical Link by writing the FLASH with the CAEN Toolbox software (see Chap. **11**).

IT IS STRONGLY SUGGESTED TO OPERATE THE DIGITIZER UPON THE STD COPY OF THE FIRMWARE. UPGRADES ARE SO RECOMMENDED ONLY ON THE STD PAGE OF THE FLASH. THE BKP COPY IS TO BE INTENDED ONLY FOR RECOVERY USAGE. IF BOTH PAGES RESULT CORRUPTED, THE USER WILL NO LONGER BE ABLE TO UPLOAD THE FIRMWARE VIA VMEbus OR OPTICAL LINK AGAIN AND THE BOARD NEEDS TO BE SENT TO CAEN FOR REPAIR!

13.1 Firmware Upgrade

The firmware types supported by the 740 family are:

- The waveform recording firmware;
- The special DPP firmware for Physics Applications:
  - DPP-QDC firmware to use the digitizer as a digital replacement of QDC, Discriminator and Gate Generator (SUPPORTED ONLY BY THE 740D VERSION FAMILY).

All firmware updates are available for download on CAEN website in the Software/Firmware tab at the digitizer web page (**login required**).

13.1.1 Firmware File Description

The firmware programming file extension is ".CFA" (CAEN Firmware Archive). It is an archiving file format that aggregates all the programming files of the same firmware kind which are compatible with the same digitizer family.

The CFA naming convention follows this general scheme:

- x<FAMILY>_rev_X.Y_W.Z.CFA for the waveform recording firmware
- x740D_DPP-QDC_rev_X.Y_135.Z.CFA for the DPP-QDC firmware

where:

- x<FAMILY> are all the supported boards (the x740 includes DT5740, N6740, V1740, VX1740 and their D versions);
- X.Y is the major/minor revision number of the ROC FPGA;
- W.Z is the major/minor revision number of the AMC FPGA.

It is possible to dinstinguish a DPP firmware from a Waveform Recording firmware by the major release number of the AMC FPGA:

- AMC FPGA major release number < "128" -> it is a Waveform Recording firmware
- AMC FPGA major release number >= "128" -> it is DPP firmware

In case of DPP firmware, the AMC FPGA major revision number is then a fixed number associated both to the kind of DPP (i.e. algorithm) and to the Digitizer family.

For example:
"135" is the AMC FPGA major revision number for the DPP-QDC firmware of the 740D family.

Note: The Waveform Recording firmware is a free firmware that doesn't require any license.

Note: DPP special firmware is a pay firmware requiring a license to be purchased by ordering option. If not licensed, the firmware can be loaded but it will run in trial mode, that is fully functional with a time limitation per power cycle (30 minutes).

13.2 Troubleshooting

In case of upgrade failure (e.g. STD FLASH page is corrupted), the user can try to reboot the board: after a power cycle, the system programs the board automatically from the alternative FLASH page (e.g. BKP FLASH page), if this is not corrupted as well. The user can so perform a further upgrade attempt on the corrupted page to restore the firmware copy.

BECAUSE OF AN UPGRADE FAILURE, THE SW7 DIP SWITCH POSITION MAY NOT CORRESPOND TO THE FLASH PAGE FIRMWARE COPY LOADED ON THE BOARD FPGAs.

Note: old versions of the digitizer motherboard have a slightly different FLASH management and the firmware selection switch is SW7. To obtain information about the FLASH type of the digitizer, you can download the BoardInfoFile (text file) through the "Get information file" tab in CAENToolbox (see. Chap. **11**) and check the value of the FLASH_TYPE parameter: FLASH_TYPE=0 indicates an older version. Alternatively, you can use CAENComm or the "Manual Controller" available in CAENToolbox to directly access register 0xF050 and check the status of bit [7]. If so, it means that, at power-on, the microcontroller loads exactly the firmware copy from the FLASH page.

When a failure occurs during the upgrade of the STD page of the FLASH, which compromises the communication with the V1740 , the user can perform the following recovering procedure as first attempt:

- force the board to reboot loading the copy of the firmware stored on the BKP page of the FLASH. To do that, power off the crate, switch the dedicated SW7 switch to BKP position and power on the crate;
- use CAEN Toolbox to read the firmware revision (in this case the one of the BKP copy). If this succeeds, it is so possible to communicate again with the board;
- use CAEN Toolbox to load the proper firmware file on the STD page, then power off the crate, switch SW7 back to STD position and power on the crate.

If neither of the procedures here described succeeds, it is recommended to send the board back to CAEN in repair (see Chap. **17**).

14 Instructions for Cleaning

The equipment may be cleaned with isopropyl alcohol or deionized water and air dried. Clean the exterior of the product only.
Do not apply cleaner directly to the items or allow liquids to enter or spill on the product.

14.1 Cleaning the Touchscreen

To clean the touchscreen (if present), wipe the screen with a towelette designed for cleaning monitors or with a clean cloth moistened with water.
Do not use sprays or aerosols directly on the screen; the liquid may seep into the housing and damage a component. Never use solvents or flammable liquids on the screen.

14.2 Cleaning the Air Vents

It is recommended to occasionally clean the air vents (if present) on all vented sides of the board. Lint, dust, and other foreign matter can block the vents and limit the airflow. Be sure to unplug the board before cleaning the air vents and follow the general cleaning safety precautions.

14.3 General Cleaning Safety Precautions

CAEN recommends cleaning the device using the following precautions:

- Never use solvents or flammable solutions to clean the board.
- Never immerse any parts in water or cleaning solutions; apply any liquids to a clean cloth and then use the cloth on the component.
- Always unplug the board when cleaning with liquids or damp cloths.
- Always unplug the board before cleaning the air vents.
- Wear safety glasses equipped with side shields when cleaning the board.

15 Device Decommissioning

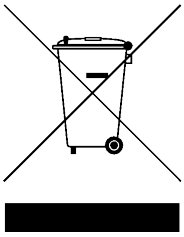
After its intended service, it is recommended to perform the following actions:

- Detach all the signal/input/output cable
- Wrap the device in its protective packaging
- Insert the device in its packaging (if present)

THE DEVICE SHALL BE STORED ONLY AT THE ENVIRONMENT CONDITIONS SPECIFIED IN THE MANUAL, OTHERWISE PERFORMANCES AND SAFETY WILL NOT BE GUARANTEED

16 Disposal

The disposal of the equipment must be managed in accordance with Directive 2012/19 / EU on waste electrical and electronic equipment (WEEE).



The crossed bin symbol indicates that the device shall not be disposed with regular residual waste.

17 Technical Support

To contact CAEN specialists for requests on the software, hardware, and board return and repair, it is necessary a MyCAEN+ account on www.caen.it:

https://www.caen.it/support-services/getting-started-with-mycaen-portal/

All the instructions for use the Support platform are in the document:

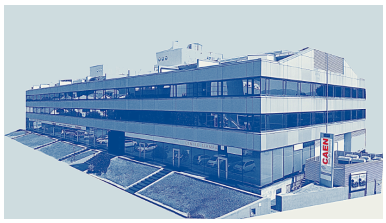
A paper copy of the document is delivered with CAEN boards.
The document is downloadable for free in PDF digital format at:

https:/www.caen.it/safety-information-product-support

User Manual V1740/VX1740

64 Channels 12bit 62.5 MS/s Digitizer

CAEN S.p.A.
Via Vetraia 11
55049 - Viareggio
Italy
Phone +39 0584 388 398
Fax +39 0584 388 959
info@caen.it
www.caen.it



CAEN GmbH
Brunnenweg 9
64331 Weiterstadt
Germany
Phone +49 212 254 40 77
Fax +49 212 254 40 79
info@caen-de.com
www.caen-de.com

CAEN Technologies, Inc.
1 Edgewater Street - Suite 101
Staten Island, NY 10305
USA
Phone: +1 (718) 981-0401
Fax: +1 (718) 556-9185
info@caentechnologies.com
www.caentechnologies.com

CAENspa INDIA Private Limited
B205, BLDG42, B Wing,
Azad Nagar Sangam CHS,
Mhada Layout, Azad Nagar, Andheri (W)
Mumbai, Mumbai City,
Maharashtra, India, 400053
info@caen-india.in
www.caen-india.in

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