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Technical Information Manual

Revision n. 7
1 October 2021

MOD. N842-N843
*8-16 CHANNEL
CONSTANT FRACTION
DISCRIMINATOR*

NPO:
00103/00:842-3.MUTx/07

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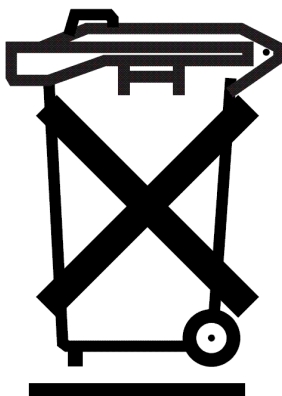
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Change Document Record

Date	Revision	Changes
1 October 2021	Rev. 7	Updated Output width and Dead time values throughout manual

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1. General description

1.1. Functional description

The CAEN Model N843 is a 16 CHANNEL CONSTANT FRACTION DISCRIMINATOR housed in a single width NIM module.

The module accepts 16 negative inputs and produces 16 NIM outputs + 16 /NIM outputs (complementary) on 48 front panel LEMO 00 connectors (NIM outputs are provided with a Fan-Out of two); a functional block diagram is shown in Fig. 1.1.

A 8 Channel version, the CAEN Model N842, sharing the same functional features with the 16 Channel Model N843, is also available.

The constant fraction delay is defined by a delay line network of 20 ns with 5 taps (see fig. 2.2). The timing stage of the discriminator produces an output pulse whose width is adjustable in a range from 15 ns to 245 ns. Moreover, in order to protect against multiple pulsing, it is possible to program a Dead Time during which the discriminator is inhibited from retriggering.

The maximum time walk is ± 400 ps (for input signals in the range from -50 mV to -5 V with 25 ns rise time). The constant fraction is 20%. The individual discriminating thresholds are settable in a range from -1 mV to -255 mV (1 mV step) via an 8-bit DAC.

The module can operate also with small (below 10 mV) input signals, though in this case the Constant Fraction operation is not performed, i.e. the jitter is higher. The channels' threshold, output width and dead time can be programmed via two switches and one rotary handle placed on the front panel.

The back panel houses VETO and TEST inputs, the logical OR output (the relevant "OR" LED lights up if at least one channel is over threshold) and the Current Sum (Σ) output, which generates a current proportional to the input multiplicity, i.e. to the number of channels over threshold, at a rate of -1.0 mA per hit (-50 mV per hit into a 50 Ohm load) $\pm 20\%$.

1.2. Block diagram

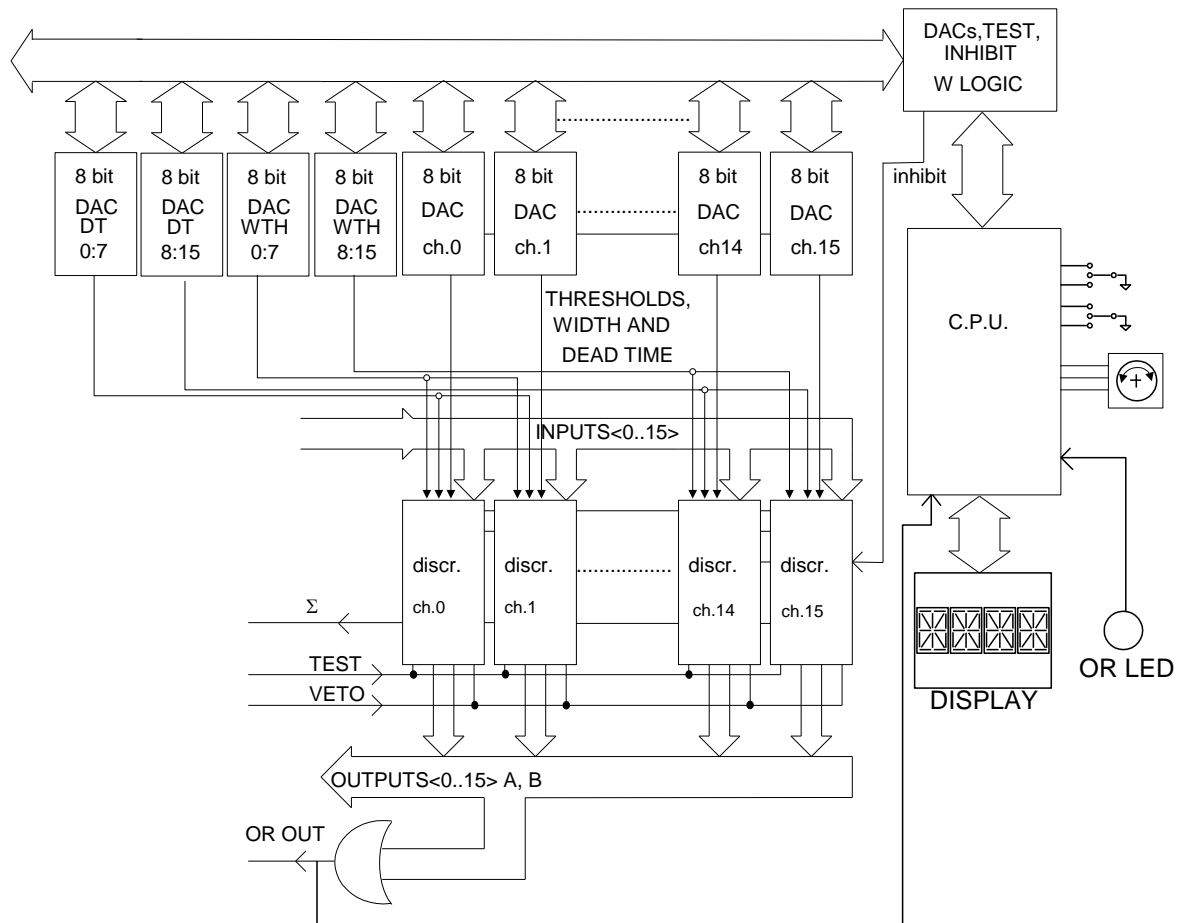


Fig. 1.1: Mod. N843 Block Diagram (16 Channel)

2. Technical Specifications

2.1. Packaging

The Model N842-N843 is housed in a 1U-wide NIM unit.

2.2. Power requirements

The power requirements of the Mod. N842-N843 are as follows:

Table 2.1: Power requirements

Power Supply	N842	N843
+ 12 V	40 mA	60 mA
- 12 V	30 mA	30 mA
+ 6 V	500 mA	1.1 A
- 6 V	1.8 A	3.4 A

2.3. Front and back panel

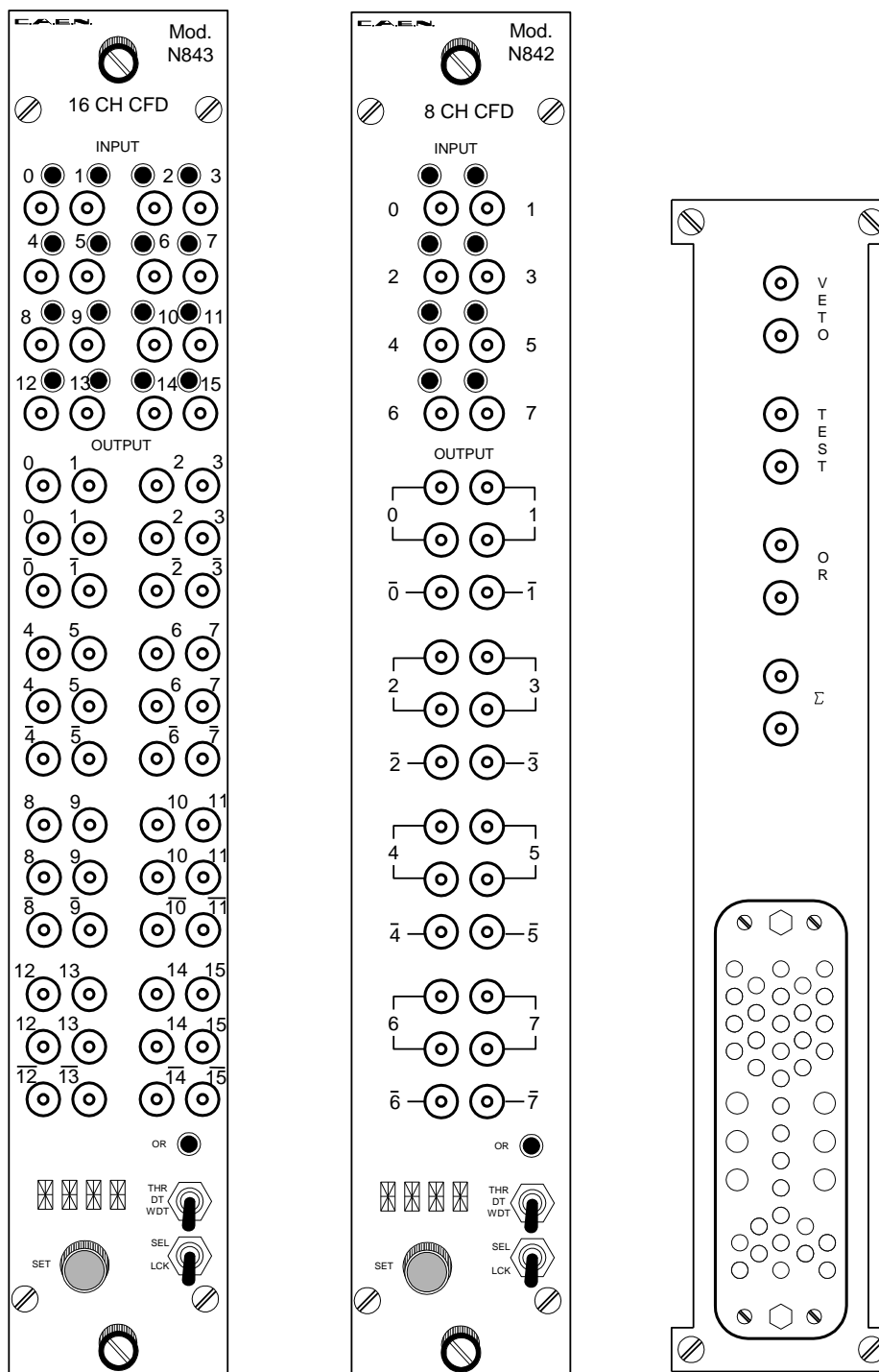


Fig. 2.1: Mod. N843-N842 front panel and back panel

2.4. Input/Output connections

The location of the Mod. N842-N843 connectors is shown in Fig. 2.1. Their function and electromechanical specifications are listed in the following subsections and are referred to the Mod. N843 (the Mod. N842 features specified between []).

2.4.1. INPUT features

INPUT CHANNELS:Mechanical specifications:

16 [8] LEMO 00 type connectors.

Electrical specifications:

negative polarity, 50 Ohm impedance;
minimum ratings: -5 mV; maximum
ratings: -5 V.

VETO INPUT:Mechanical specifications:

2 bridged LEMO 00 type connectors.

Electrical specifications:

standard NIM signal, high impedance, 15 ns
minimum FWHM; leading edge of the VETO
signal must precede of at least 10 ns the
leading edge of the input and overlap
completely the input signal; acts on all
signals.

TEST INPUT:Mechanical specifications:

2 bridged LEMO 00 type connectors.

Electrical specifications:

standard NIM signal, high impedance, 5 ns
minimum FWHM, 30 MHz Max. frequency,
Test/Output delay: 10 ns.

2.4.2. OUTPUT features

OUTPUT CHANNELS:Mechanical specifications:

48 [24] (32 [16] Fan-Out of two for OUT and
16 [8] single for /OUT) LEMO 00 connectors.

Electrical specifications:

NIM level on 50 Ohm impedance; pulse width
adjustment from 15 ns to 245 ns; maximum
time walk is ± 400 ps for input signals in the
range from -50 mV to -5 V with 25 ns rise
time.

Input/Output delay: 24 ns (typical).

OR OUTPUT:Mechanical specifications:

2 LEMO 00 type connectors, Fan-Out of two.

Electrical specifications:

Σ OUTPUT:

standard NIM signal, 50 Ω impedance, 30 ns minimum FWHM, 25 MHz maximum frequency.

Mechanical specifications:

2 bridged LEMO 00 type connectors.

Electrical specifications:

current output (-1 mA \pm 20% per hit), high impedance, 18 ns minimum FWHM, 25 MHz maximum frequency.

2.5. Other components

2.5.1. Displays

The front panel hosts the following LEDs:

INPUT

Type: 16 [8] red LEDs

Function: channel selected; they light up when the channels are being programmed (SEL mode) and when they are inhibited (LCK mode)

OR

Type: 1 green LED

Function: it lights up if at least one output signal is present.

4 DIGIT DISPLAY

Type: 4 digit red LED display

Function: it indicates the channels' status and programmed parameters' values

2.5.2. Front panel switches

UPPER SWITCH

Function: it allows to select the parameter which must be programmed

LOWER SWITCH

Function: it allows to select the channel/block which must be programmed (SEL mode), and to "freeze" the programmed values (LCK mode)

2.5.3. Rotary handle

Function: it allows to set the value of the parameter which is being programmed.

2.5.4. Jumpers

DELAY JUMPERS

Function: these 5-position jumpers allow to set the Delay. The Delay values range up to 20 ns with 4 ns steps.

Factory setting is 20 ns (8 ÷ 20 ns range).

Optionally is also available 5ns full scale with 1ns steps (4 ÷ 5 ns range), 50ns full scale with 10ns steps (10 ÷ 50 ns range) and 100ns full scale with 20ns steps (20 ÷ 100 ns range).

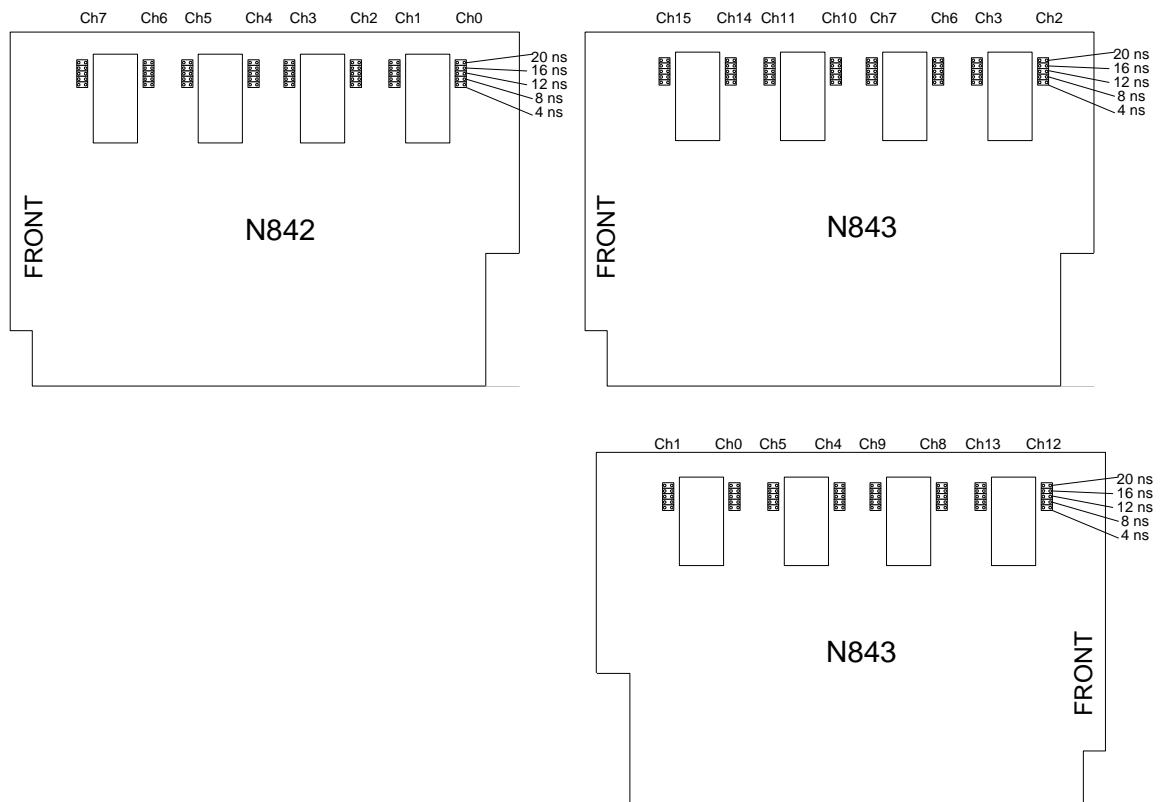


Fig. 2.2: Jumpers location

2.6. Technical specification table

Table 2.2: Technical specification table

Features referred to Mod. N843 (Mod. N842 features specified between [])

Packaging	1U-wide NIM unit
Input channels	16 [8] inputs (negative polarity, 50 Ω impedance)
Max. input voltage	-5 V
Min. detectable signal	-5 mV
Threshold range	-1 mV to -255 mV (1 mV step)
Constant fraction	20%
Delay	20ns full scale with 4 ns steps (8 ÷ 20 ns operating range) Optional: <ul style="list-style-type: none"> • 5ns full scale with 1ns steps (4 ÷ 5 ns operating range) • 50ns full scale with 10ns steps (10 ÷ 50 ns operating range) • 100ns full scale with 20ns steps (20 ÷ 100 ns operating range)
Output channels	32 [16] NIM (Fan-Out of 2) + 16 [8] /NIM (single) (50 Ω impedance)
Input/output delay	24 ns
Output width	Programmable from 15 ns to 245 ns (typical values)
Output rise/fall time	OUT: 1.2 ns; /OUT: 2.5 ns
Dead Time	Programmable from 137 ns to 1865 ns (typical values)
Interchannel insulation	50 dB for 2.5 ns rise time input signals
Max outputs time walk	± 400 ps for input signals in the range from -50 mV to -5 V with 25 ns rise time
Autowalk	Automatic adjustment to input offset and low frequency input noise of ± 40 mV
Control signals	VETO IN: NIM signal, high impedance, allows vetoing of all channels simultaneously TEST IN: triggers all the enabled channels at once OR OUT: standard NIM signal, 50 Ohm impedance; logic OR of outputs Σ OUT: current proportional to input multiplicity (-1 mA $\pm 20\%$ per hit), high impedance

3. Operating Modes

3.1. The Constant Fraction Discrimination technique

The Constant Fraction Discrimination technique is based on summing a delayed, full height input signal to an inverted and attenuated signal. The resulting signal is fed into a zero-crossing comparator, thus obtaining a precise timing information that eliminates any walk error induced by constant rise time and varying amplitude signals.

For correct operation the maximum of the attenuated pulse has to cross the delayed pulse at the selected fraction. This condition leads to the following relation:

$$T_{\text{delay}} = T_{\text{rise}} \cdot (1 - F)$$

where:

T_{delay} = selected delay on the Constant Fraction Discriminator

T_{rise} = rise time of the input signals

F = Constant Fraction value

The Mod. N842-N843 Constant Fraction Discriminator features a factory setting of 20% for the fraction and 20 ns for the full scale delay. The Delay values range up to 20 ns with 4 ns steps, Factory setting is 20 ns (8 ÷ 20 ns range).

Optionally is also available 5ns full scale with 1ns steps (4 ÷ 5 ns range), 50ns full scale with 10ns steps (10 ÷ 50 ns range) and 100ns full scale with 20ns steps (20 ÷ 100 ns range).

3.2. Power ON Status

At Power ON the values of all the module's parameters are those programmed before the last turning off. If one parameter's value is meaningless, the unit sets it at half of its range.

3.3. Setting the delay

Each channel is provided with a 5-position jumper which allows to set the Delay according to the formula expressed in § 3.1 (see Fig. 2.2) for the jumpers location on board). The Delay values range up to 20 ns with 4 ns steps. Factory setting is 20 ns (8 ÷ 20 ns range).

Optionally is also available 5ns full scale with 1ns steps (4 ÷ 5 ns range), 50ns full scale with 10ns steps (10 ÷ 50 ns range) and 100ns full scale with 20ns steps (20 ÷ 100 ns range).

3.4. Back panel signals

Some operations can be performed via two external NIM input signals:

- **TEST:** an input signal sent through this connector triggers all the enabled channels at once. This feature allows a complete test of the module without removing any input cable as well as it allows generation of a pattern of pulses suitable to test any following electronics.
- **VETO:** an input signal sent through this connector allows vetoing of all channels simultaneously. A veto pulse of width T will veto the input during this time T . Its leading edge must precede the output leading edge by at least 10 ns and overlap completely the input signal. VETO does not affect the TEST signal.

Each one of these high impedance inputs is provided via two bridged connectors for daisy chaining.

Note that since these are high impedance inputs, the chain has thus to be terminated on $50\ \Omega$ on the last module; the same is needed whenever one module only is used, whose inputs have thus to be properly matched

Moreover the back panel houses a Current Sum (Σ) output (on two bridged connectors) which generates a current proportional to the input signal multiplicity, i. e. to the number of channels over threshold, at a rate of -1.0 mA per hit (-50 mV per hit into a $50\ \Omega$ load) $\pm 20\%$. An OR output (with a Fan-Out of two) provides the logical OR of the output channels.

3.5. Setting the threshold and disabling the channels

For each channel of the N842-N843 the discriminator threshold is set up via an 8 bit DAC. The threshold values can be programmed in a range from -1 mV to -255 mV with -1 mV steps. As in all Constant Fraction Discriminators, these thresholds must be set above the noise level: they do NOT correspond to the actual level that triggers the discriminator outputs, the latter being a “constant fraction” of the input signals.

In order to set the threshold the Upper Switch (see § 2.5.2) must be placed on the THR position and the Lower Switch removed from the LCK position, then the channel that must be programmed is selected pulling up repeatedly the Lower Switch (the selected channel's Led lights up). Note that after the last channel, by pulling up the lower switch, the Leds light up all together and, at this point, the threshold setting is performed over all the channels (this value must be confirmed by placing the Lower Switch on the LCK position, otherwise it is ignored). The threshold value is set via the front panel Rotary handle (see § 2.5.3) and shown on the 4-Digit Display: 1 leads to a -1mV and 255 to a -255 mV threshold value; 1 leads to a -1mV and 255 to a -255 mV threshold value; the step which follows 255 is four “*” appearing on the display (the relevant channel is inhibited), then again 0, 1, 2 etc; inhibited channels' Leds are always lit when the lower switch is in lock (LCK) position. Once all the channels' thresholds have been set to the desired value the Lower Switch must be placed on the LCK (lower) position and the word **LOCK** appears on the display.

3.6. Setting the output pulse width

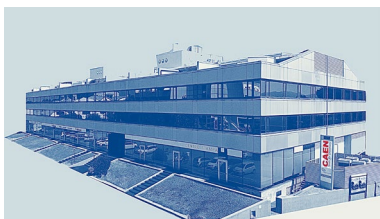
The output pulse width is adjustable on 8 bit from 18 to 318 ns and the chosen value is applied to a group of 8 channels each. The Mod. N843 has two groups (Ch. 0, 1, 4, 5, 8, 9, 12, 13 and Ch. 2, 3, 6, 7, 10, 11, 14, 15, respectively), the Mod. N842 has only one group. The Upper Switch must be placed on the WDT position and the Lower Switch removed from the LCK position, then the group is selected pulling up repeatedly the Lower Switch (the selected group's Leds light up all together). The width's value is set via the Rotary Handle and shown on the display (0 leads to a 15 ns and 255 to a 245 ns width with a non-linear relation for intermediate values); the step which follows 255 is again 0, then 1, 2 etc. Once the Pulse Widths have been programmed the Lower Switch must be placed on the LCK position and the word *LOCK* appears on the display.

3.7. Setting the Dead Time

It is possible to set a Dead Time value, common to a group of 8 channels. The Mod. N843 has two groups (Ch. 0, 1, 4, 5, 8, 9, 12, 13 and Ch. 2, 3, 6, 7, 10, 11, 14, 15, respectively), the Mod. N842 has only one group. This prevents the triggering of the discriminator by unwanted pulses occurring within the Dead Time programmed value. The Upper Switch must be placed on the DT position and the Lower Switch on the SEL position then the group is selected pulling up repeatedly the Lower Switch (the selected group's Leds light up all together). The dead time value is set via the Rotary Handle. The displayed value corresponds to the Dead Time as follows: 255 leads to a 1865 ns value, 0 leads to a 137 ns value with a non-linear interpolation for intermediate values; the step which follows 255 is again 0, then 1, 2 etc. Once the Dead Times have been programmed the Lower Switch must be placed on the LCK position and the word *LOCK* appears on the display.

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