Rev. 00 - 10/03/2010

SIPM Kit

Digital Pulse processing for SiPM Kit

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User Manual
UM7873

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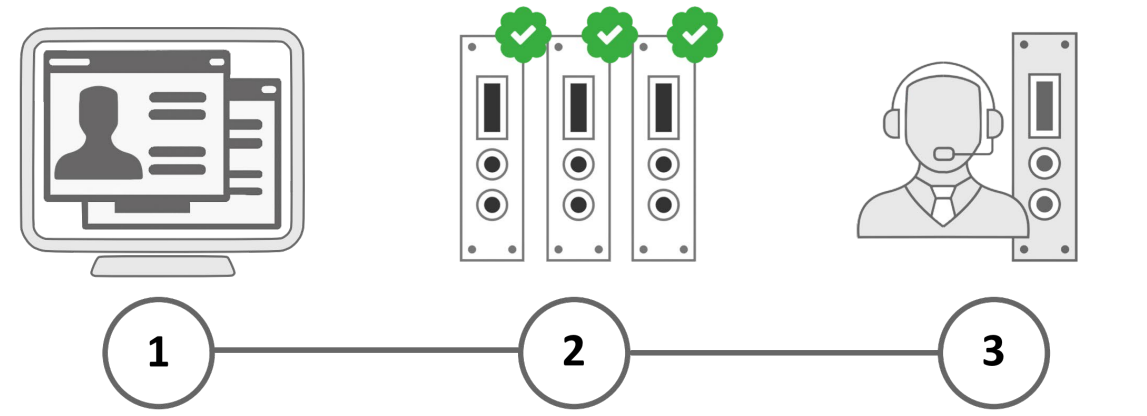

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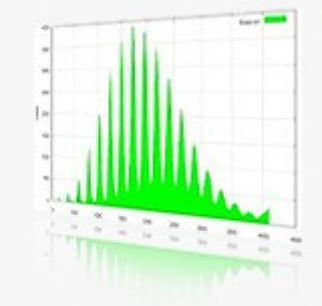
DIGITAL PULSE PROCESSING FOR SIPM KIT



PRELIMINARY USER'S GUIDE

Revision n. 0
10 December 2010

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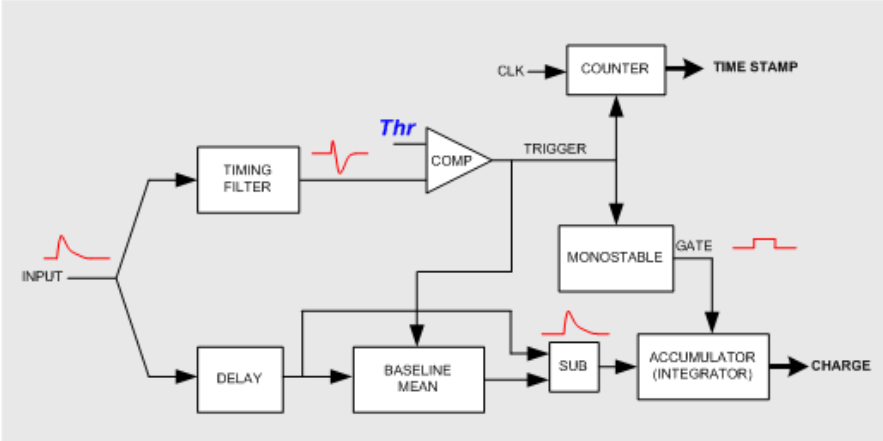
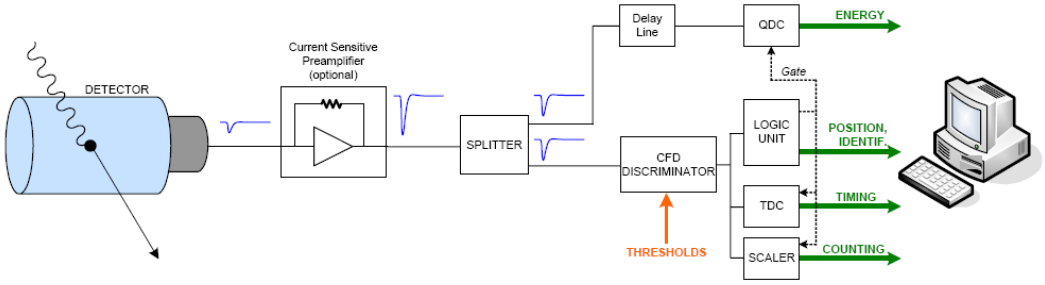
1 Digital Pulse Processing Overview

This document shows how to perform Digital Pulse Processing (DPP) for Charge to Digital Conversion (named DPP-CI) using the SiPM Development Kit modular set-up.

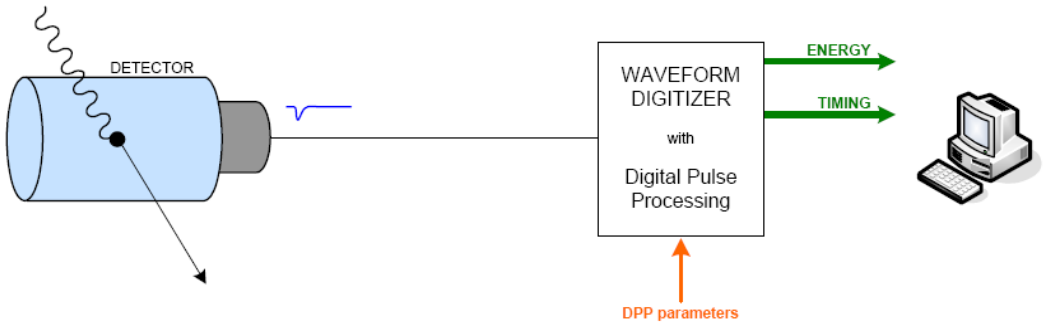


Digital Pulse Processing for Charge to Digital Conversion

Figure below shows a traditional analog chain based on Charge to Digital Converter (QDC). The QDC is a pure integrator that requires a gate signal to define the integrating window. In some applications (most likely in beam experiments) the gate is provided by the system that knows in advance when the signals have to be integrated. Unfortunately, when this is not the case, it is necessary to generate the gate from the detector signals; to do that, you need to split the signals, send one branch to the discriminators and use a coincidence logic. It is also necessary to add a delay line (typically a long cable) on the signal path to the QDC input in order to match the pulses with the gate (which arrives with some latency respect to the analog pulses that produced it).

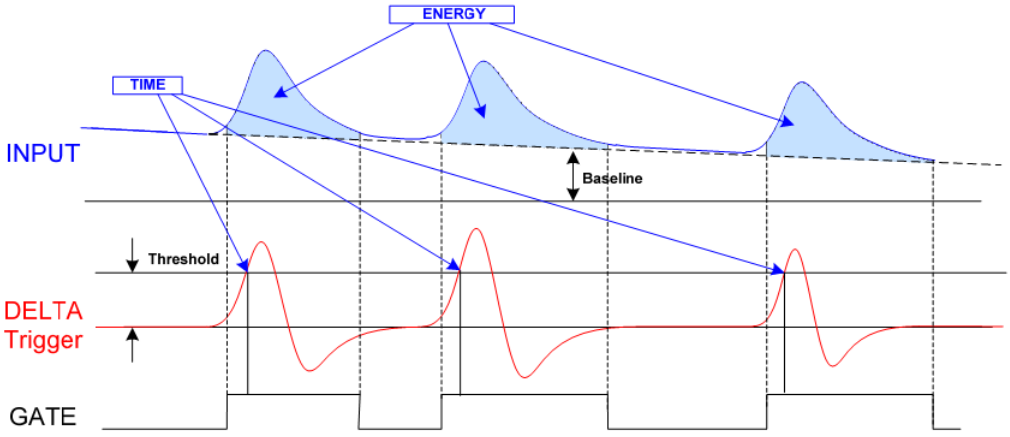


The following figure shows instead the block diagram of the digital QDC solution based on a waveform digitizer equipped with Digital Pulse Processing (DPP) firmware for Charge to Digital Conversion.



The DPP-CI algorithm main features are:
• Smart auto-Trigger for pulse detection
• Automatic GATE generation
• Advanced input signal Baseline calculation
• Charge integration with Baseline subtraction
• Data storage upon two channels Coincidence detection

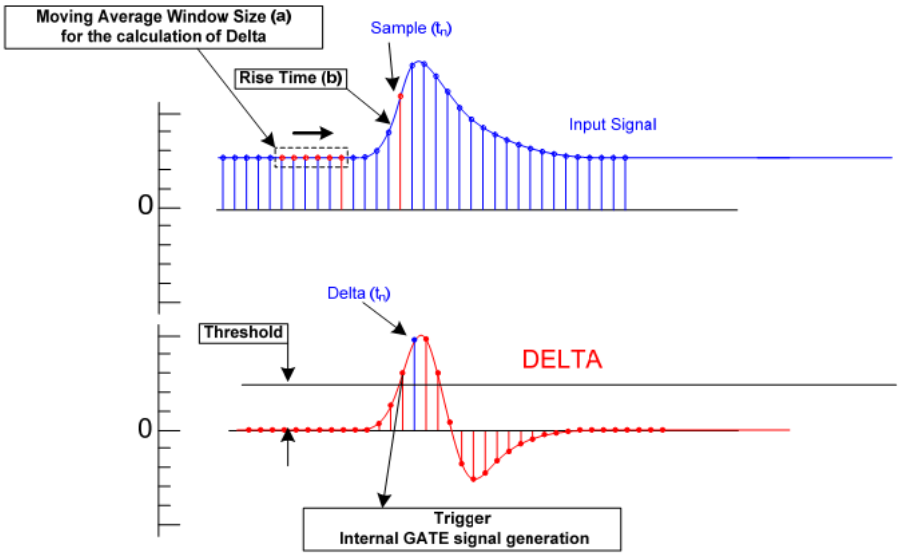
The following plot shows Digital QDC main signals



The delta signal recognizes the input pulses mitigating the influence of noise and baseline fluctuations, the trigger (identifying the arrival time) is generated as soon as this 'delta' is greater than a programmable digital threshold.
• The GATE is auto generated and indicates when the input pulse has to be integrated.
• The Energy is the integral of the input pulse with baseline subtraction.

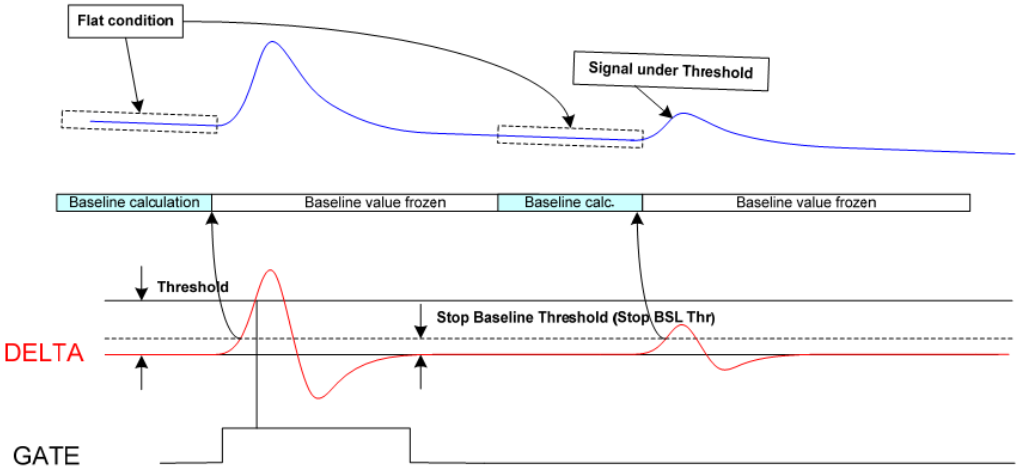
Smart trigger for pulse detection and automatic gate generation

The DPP algorithm for digital QDC can run in self triggered mode; this means that the algorithm can recognize the input pulses and thus generate internal gate signals.
The self triggering works in this way (Figure below): after the digitization of the input signal, the DPP evaluate the difference between the current sample, i.e. the input signal sampled at time *t*, and the average of some samples digitized before *t*. This difference is called **delta**. Now, it is possible to set a threshold over delta in order to recognize the pulses to integrate with the digital QDC and a gate is generated.



Advanced input signal Baseline calculation

Once evaluated by the DPP algorithm, it is possible to use delta in order to know when the input signal is flat, i.e. there are no input pulses, and thus calculate its baseline. In the flat condition, a moving window averages a number of samples of the input signal; the calculated value is the baseline.
In order to recognize when the input signal is not flat, it is possible to set a threshold over delta, different from the one relative to the self trigger; when delta exceeds this threshold, the baseline evaluation is **frozen** to the last calculated value (Figure below).



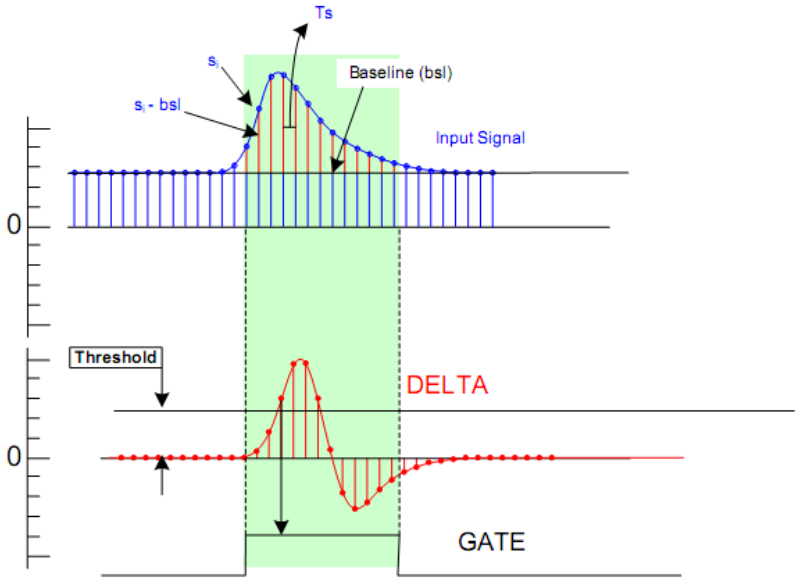
Charge integration with baseline subtraction

When a gate is generated, the DPP algorithm for digital QDC starts to calculate the charge, i.e. the area, of the input signal. While the gate is active, the DPP algorithm subtracts the baseline from the samples, and sums these unbiased samples [Equation below]:

$$Q_{FPGA} = \sum_{i \in gate} (s_i - bsl)$$

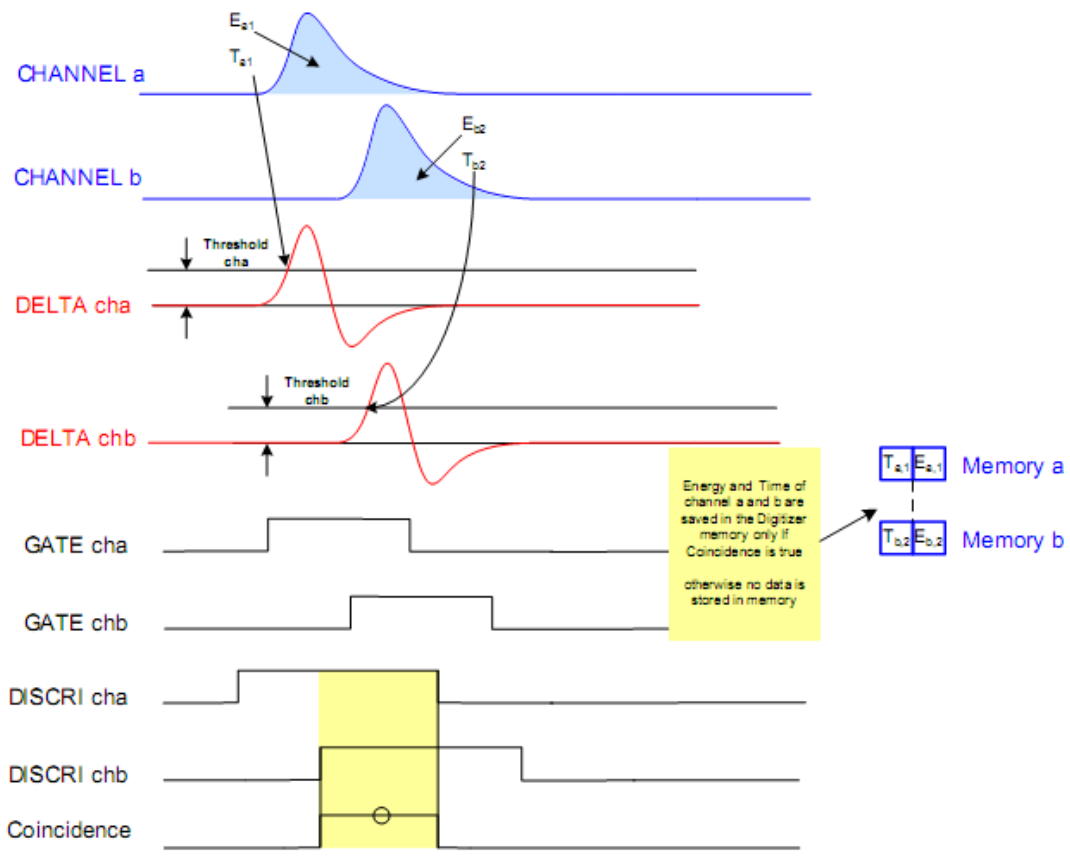
$$Q = Q_{FPGA} \cdot \Theta$$

Where Q is the charge value (Energy information), Q_{FPGA} is the Charge value expressed in ADC count (1 count ≈ 40 fC), s_i is a sample of the input signal digitized while the gate was active, bsl is the evaluated baseline, Θ represents the gain (≈40 fC/count) of the digital QDC.



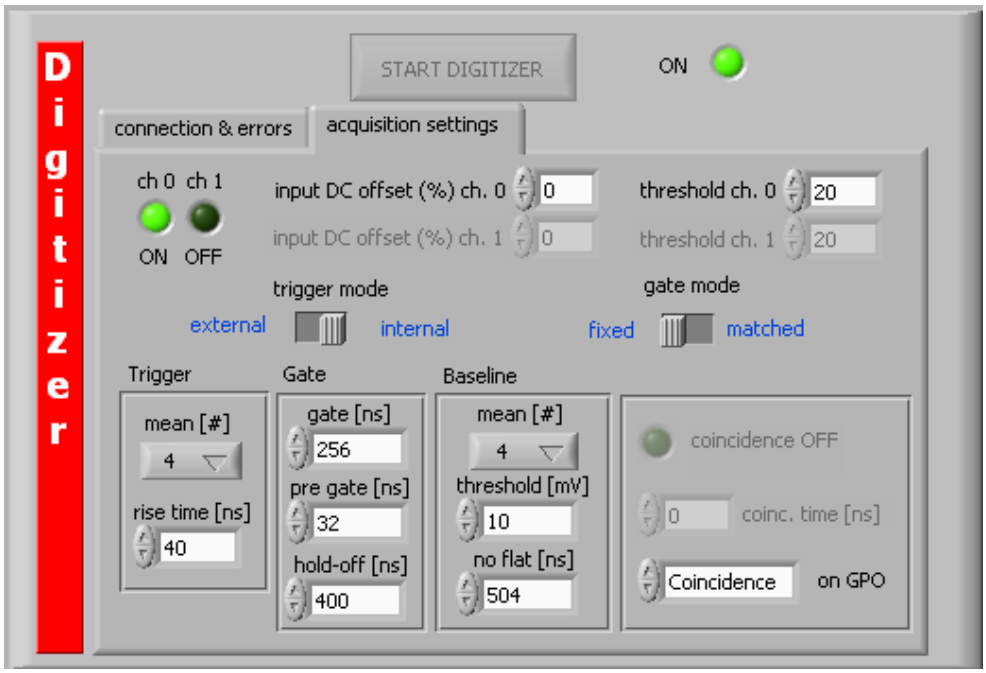
Data storage upon 2 channels Coincidence detection

A 2 channels coincidence algorithm is implemented in the DPP for digital QDC (see Figure below). When a gate is generated a discriminator signal starts too. The width of this signal can be set to a different value than the gate's one.
If the discriminator signals of the two channels overlap, a coincidence signal switchs to active; once the charge integration of the two signals is complete, the values are stored in the digitizer's memory.

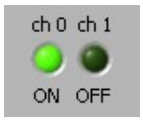

CHANNEL a
CHANNEL b
DELTA cha
DELTA chb
GATE cha
GATE chb
DISCRI cha
DISCRI chb
Coincidence
Threshold cha
Threshold chb
Energy and Time of channel a and b are saved in the Digitizer memory only if Coincidence is true
otherwise no data is stored in memory
Memory a
Memory b

2 Waveform Digitizer settings

This chapter shows how to set the Waveform Digitizer DPP-CI parameters through the Graphical Users' Interface (GUI) provided with the SiPM Development Kit.
The digitizer settings are provided by the following tab:



Channel Enable

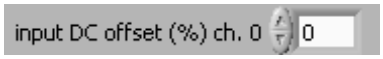


It allows to enable/disable the channels of the digitizer. If one channel is enabled, it will participate to the data readout.

Active Channel

All plots and statistics (waveforms, spectra, rates, etc…) are referred to the active channel that is selected here. The active channel can be changed runtime.

Input DC offset



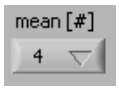
The input stage of the digitizer gives the possibility to add a DC level to the input signal (offset). The input dynamic range is 2.00 Vpp; the DC offset adjust allows the dynamic range to be shifted from –2.00/0 up to 0/2.00. The DAC used for this purpose has a dynamic range of 16 bit (from 0 to 65535); however, the input DC offset is here expressed in percent of the full scale: 50% is the maximum value and correspond to a DC offset of FSR/2 (the input

dynamic range goes from 0 to 2.00V); -50% is the minimum value and correspond to a DC offset of -FSR/2 (the input dynamic range goes from –2.00V to 0); 0% correspond to a null DC offset (the input dynamic range goes from –1.00V to 1.00V). Input DC offset setting is independent for each channel.

Trigger Threshold

The threshold is used to generate the trigger: when the signal delta exceeds the threshold the trigger is generated. Spurious triggers can be generated due to the high frequency noise; the problem is partially reduced averaging the input signal over a certain number of samples (parameter “mean” of DPP); the threshold must be set in order to stay over the residual noise. Threshold setting is independent for each channel.

Trigger Mean



Before the calculation of the delta signal, the input signal is filtered in order to reduce the high frequency noise. This is done using a low pass filter that averages a certain number of samples within a moving window. The parameter a represents the number of double sampling periods used by the average window; allowed values for the parameter are 1, 2, 4, 8, 16 and 32.

Trigger Rise Time

Pulse rise time of the input signal. This parameter is used in the calculation of the signal delta in such a way that the amplitude of the derived signal is maximized respect to the voltage step of the input. There is a correlation between the parameters “mean” and “rise time”; when the former is increased, also the values of “rise time” must be increased. The best way to find the optimum setting is to start from a value equal to the input pulses rise time, then look at the signal delta on the plot and increase this parameter until the signal reaches the maximum amplitude.

Gate Mode

Acting on the Gate Mode switch it is possible to select two different ways to generate the gate used in the charge integration, Fixed and Matched.

• If Fixed is selected, the gate starts before the trigger with an advance equal to the Pre Gate value set in the Gate settings and it is generated with a width equal to the Gate Width value set in the same part of the GUI.

• If Matched is selected, the width of the gate is no more fixed; it starts before the trigger with an advance equal to the Pre Gate as in Fixed mode, but the gate width is proportional to the over threshold width of the input signal. Gate Width parameter is now the time between the under threshold crossing and the end of the gate.

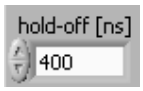
Gate Width

• If Gate Fixed is selected in Digitizer tab, it is the width of the gate signal.
• If Gate Matched is selected, it is the width of the gate between the input signal under threshold crossing and the end of the gate.

Pre Gate Width

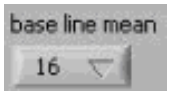
The Pre Gate is the advance between the gate generation and the trigger leading edge.

Holdoff Width



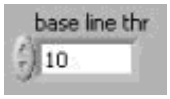
When a gate is generated, a Holdoff signal is also produced. This signal acts as an inhibit for the generation of other gates due to further triggers that can start because of noise pulses on the input signal near the threshold level or afterpulses that the user wants to ignore.

Baseline Mean



A baseline restoration algorithm is implemented in the DPP. It calculates the baseline value through a moving average window working on the input signal and subtracts this value to the samples during the charge integration.
The BSL Mean parameter is the number of samples to average to calculate the baseline expressed in samples. If 0 is selected, no baseline restoration is applied. Allowed values for the parameter are 0,1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024 and 2048.

Baseline Inhibit Threshold

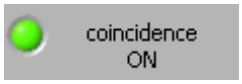


The baseline calculation must run only if the input signal is flat, i.e. there are no pulses in the input signal, in order to not introduce bias in the charge integration. For this reason, a BSL Inhibit Threshold can be set on the delta signal; it should be placed under the trigger threshold, just above the noise. If delta is above this threshold, the baseline calculation is frozen.

No Flat Time

When delta signal is above the BSL Inhibit Threshold an inhibit signal is generated in order to freeze the baseline calculation. The width of this inhibit signal is set by No Flat.

Coincidence Enable



Two channels coincidence enable/disable button.

Coincidence Time

Width of the discriminator signals used for the two channels coincidence algorithm; If the discriminator signals of the two channels overlap, a coincidence signal switchs to active.

GPO Output

Select the output of the GPO connector in the front panel of the digitizer.

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