DT5550

32-channel DAQ system with user programmable FPGA and sequencer

32-channel readout system with integrated sequencer and user programmable FPGA for analog ASICs.

Features

- Integrated system for the management of ASICs with multiplexed analog output and multi-channel detectors
- 32 analog input acquisition channels (fully differential, 2 Vpp dynamic range)
- 80 MS/s 14-bit ADC
- 96 digital (48 differential) I/O on VHDCI connector with selectable 3.3V, 1.8V CMOS or LVDS for the sequencer and the management of external circuits
- 8 digital CMOS I/O on LEMO connector for external synchronization
- 8 dedicated I/O for UART/I2C/SPI.
- Standard high density VHDCI I/O and analog connector:
  - 1 analog connector with 32 analog channels and a I2C bus
  - 2 digital connectors with 48 digital channels (each) and programmable power supply
- USB3.0 bus for fast data transfer, integrated SPI master core and I2C/UART core
- Fully supported by SCI-Compiler, graphical programmable compiler for user application development (INCLUDED)
- 0 ÷ 5.5 V 2A power supply
- 12 V powered
- User firmware can be designed to easy implement most common readout system feature:
  - Readout of both analog and digital front-end ASIC with user customizable pre-processing logic like zero suppression, pedestal subtraction
  - Multichannel analyzer based on both trapezoidal filter or charge integration with user customizable filtering chain
  - Time to digital conversion and time tagging application
  - Digitalization of waveforms
  - Complex triggering logic involving both analog and digital processing

Developed in collaboration with Nuclear Instruments

Overview

The DT5550 is a 32 channels digitizer that integrates an open FPGA programmable by the user to implement most common readout features, like a sequencer to handle the readout of both analog and digital front end ASIC, complex trigger logic, pulse height analysis and time tagging feature to readout multi-channel detectors (for example SiPM matrix).

The readout system is based on 32 14-bit 80 MS/s ADCs used to sample up to 32 analog inputs. The data acquired by the ADCs is then forwarded to an FPGA that can be configured by the user through a graphical developing platform (SCI-Compiler) and used as the sequencer for the system readout.

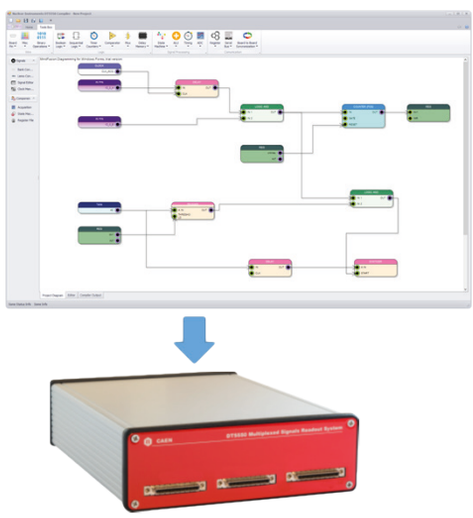
The DT5550 also integrates a reconfigurable area where it is possible to implement trigger logic, external circuit management, and real time signal processing. To facilitate

the development process, a graphical software automatically generates the VHDL source code and C libraries, with no need for the user to learn VHDL or Verilog to configure the board. The generated code is still available to the user that can customize it as needed. To let the user easily develop a custom firmware, a license of SCI-Compiler software is included in the product.

Software

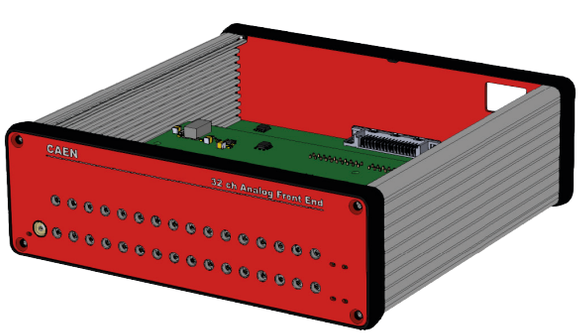
SCI-Compiler

DT5550 supports the SCI-Compiler software, a graphic tool which allows the user to realize a whole readout logic for ASICs connected to the module. The software generates the VHDL source code, C libraries, drivers and a C example code (to be compiled on Windows or Linux) to help integrating firmware vs software automatically without requiring to be a VHDL expert. Refer to page 14 for a detailed description.



DT5550AFE:

DT5550AFE is a useful single-ended-to-differential adaptor, with programmable analog offset and 1x fixed gain, to drive the differential inputs of the DT5550. It receives the single-ended signals on 32 MCX connectors and provides differential analog output and control signals on a single cable to the DT5550. HV channel for SiPM (20-85 V) available on LEMO dedicated connector.



DT5550AFE Single-Ended-to-Differential 32 ch adaptor

Ordering Option

Code	Description
WDT5550XAAAA	DT5550 - 32 ch DAQ System with Programmable FPGA and Sequencer
WDT5550AFEXA	DT5550-AFE - Single-Ended-to-Differential 32 ch Adaptor

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