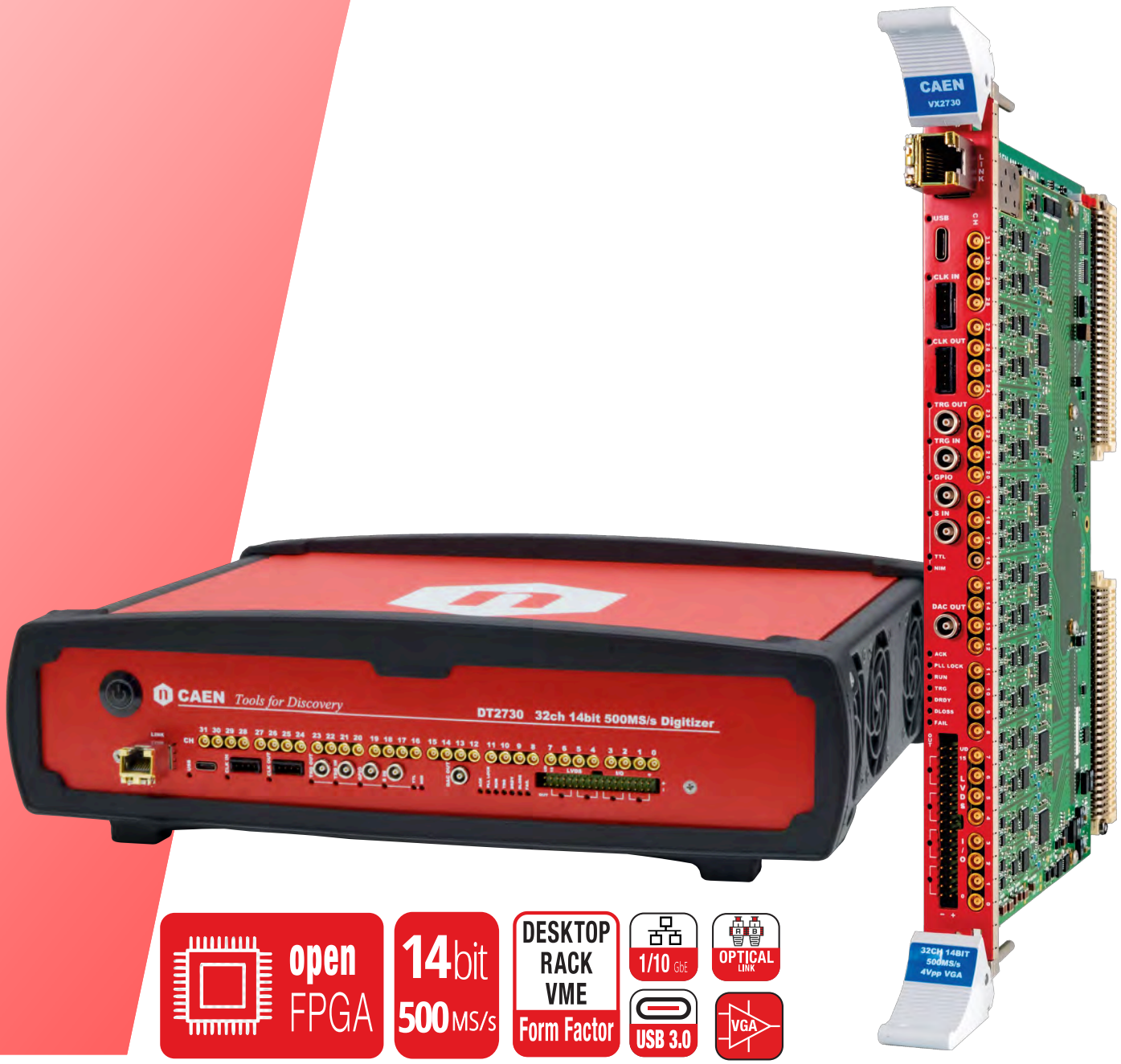
CAEN
Tools for Discovery

2730

Digitizer Family

32-Channel 14-bit 500 MS/s



open FPGA

14bit 500MS/s

DESKTOP RACK VME Form Factor

1/10 GbE

OPTICAL LINK

USB 3.0

VGA

The perfect mix of sampling rate, resolution and channel density

Overview

The 2730 Digitizer is a 32-channel digital signal processor designed for radiation detectors, available in VME64X (VX2730) and Desktop (DT2730) form factors. It not only offers waveform digitization and recording but also supports Multi-Channel Analysis, making it suitable for a wide range of applications in nuclear and particle physics, high-timing resolution, fast neutron spectroscopy, and homeland security. The embedded CPU provides powerful computational resources, allowing the 2730 to accommodate various pulse processing algorithms, including pulse height analysis (PHA), constant fraction discrimination (CFD), and pulse shape discrimination (PSD), which can be independently applied to each of the 32 channels. Additionally, the 2730 offers software programmable analog gain of up to x20.

Highlights

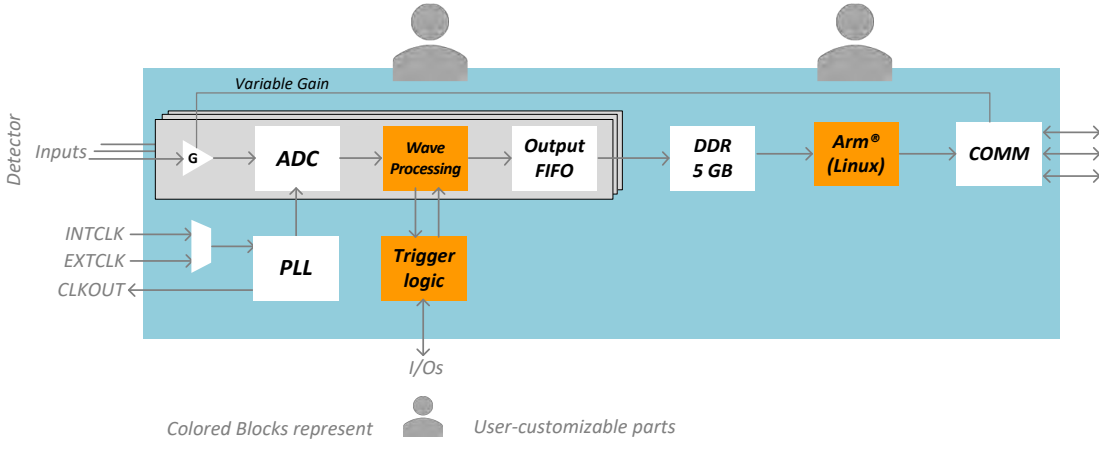
- High channel density: 32-channel, 500MS/s 14-bit ADC with individual DC offset adjustment.
- Available in VME64X and Desktop form factors.
- Software selectable analog gain.
- Front panel readout via USB-3.0, 1/10 GbE, optical link (CONET2*)
- 5 GB of total acquisition memory (DDR4)
- Onboard Zynq® UltraScale+™ MPSoC integrating an Arm®-based CPU running Linux®
- Open FPGA architecture allows customization of pulse analysis algorithms
- Supports digital pulse processing and waveform recording of 32 independent detectors.
- Advanced waveform readout modes with Zero Length Encoding* (ZLE)
- Suited for signals from liquid or inorganic scintillators coupled to PMTs or SiPMs, or Silicon and HPGe detectors.
- High-resolution Nuclear Spectroscopy: multiport MCA operating in PHA, PSD modes
- Digital CFD* for sub-ns timing measurements
- DAC output (125 MS/s, 4Vpp) for signal inspection, pulse generation, majority level

Software

- User-friendly readout software available for multiparametric spectroscopy (CoMPASS) or waveform recording (WaveDump2)
- Firmware/software generator and compiler for the Open FPGA (Sci-Compiler), eliminating the need for FPGA programming skills.
- Libraries (FELib) and demo codes are provided for software customization

(*) Future Developments

2730 DIGITIZER ARCHITECTURE



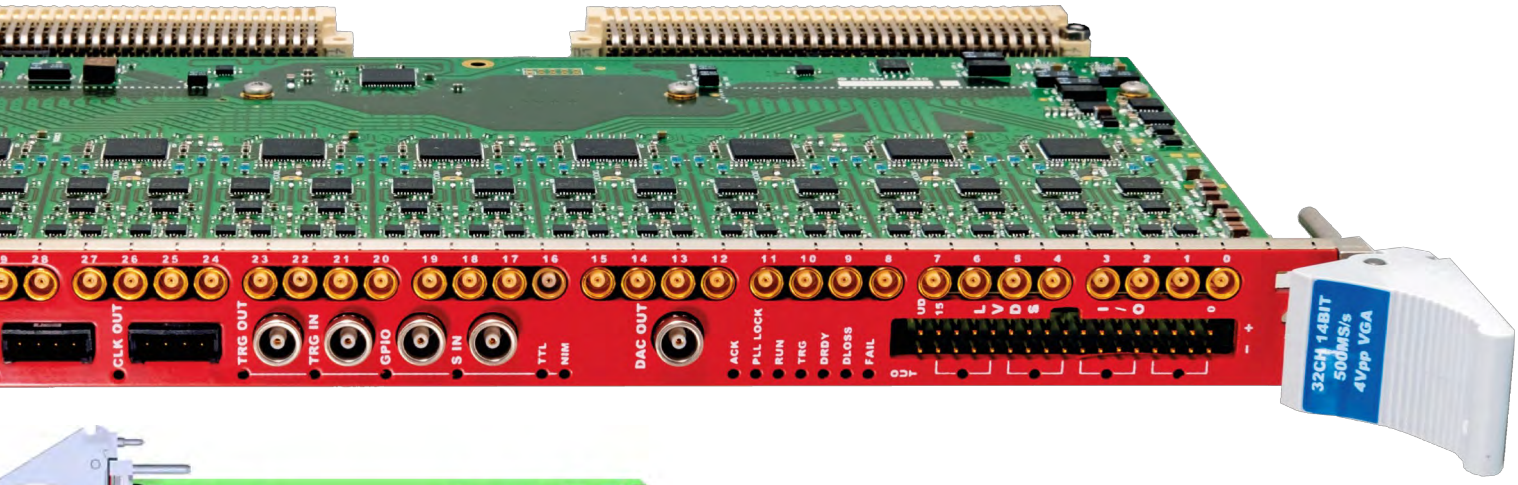
Operating Modes

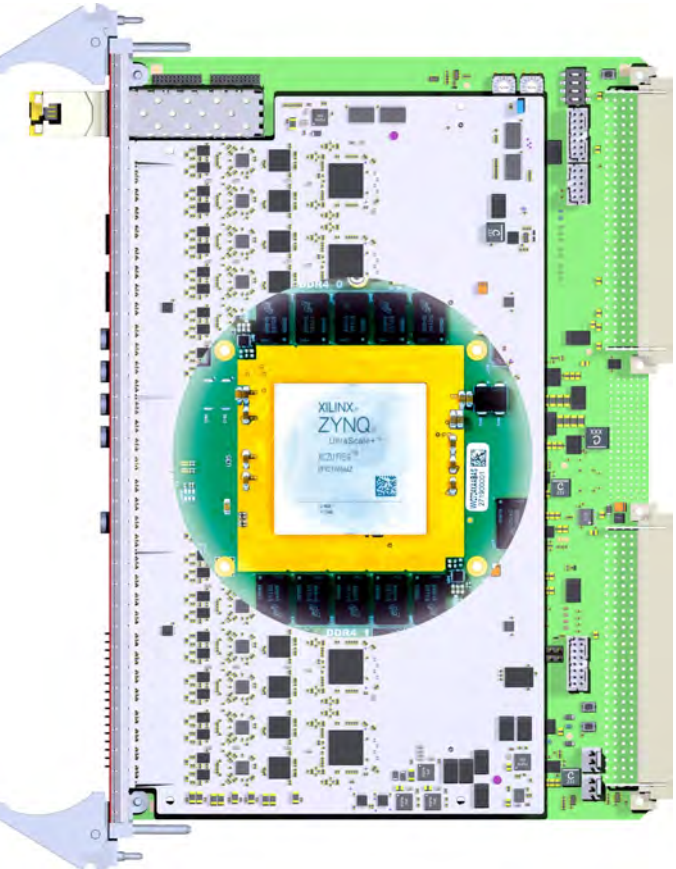
The analog input channels are provided in a single-ended configuration. Each channel of the module digitizes the analog input signal, which can originate from a physics detector, using a 14-bit, 500 MS/s ADC. The sampled data are then used to initiate the digital pulse processing sequence, which is managed at the firmware level in the FPGA. Different firmware types can be selected via software, based on the specific setup and acquisition mode .

Common trigger: In this mode, all channels acquire data simultaneously with a common trigger. The trigger can be received externally or generated through a combination of individual channel discriminators. This mode is primarily intended for waveform acquisition, similar to a digital oscilloscope. Options for zero suppression are available to remove insignificant data.

Independent trigger: This mode is suited for trigger-less applications where a global trigger is not required. Instead, each channel independently acquires waveforms based on its self-trigger, which is initiated through a digital discriminator. This process is independent of the other channels. .

DPP (Digital Pulse Processing): Real-time processing in the FPGA enables the extraction of physical parameters from the waveform, such as pulse height, charge, timestamp, and PSD (Pulse Shape Discrimination). This mode is well-suited for high counting rate applications. It is also possible to save both raw waveforms and extracted parameters.





FPGA

For users who wish to personalize the acquisition by implementing their own pulse processing algorithms in the Open FPGA, Sci-Compiler is a user-friendly graphical tool capable of generating and compiling customized firmware and software, even without FPGA programming skills.

The Open FPGA also allows for controlling the data output information and customizing the trigger logic to achieve various combinations of self-triggers and I/O signals to validate or discard the events. The onboard CPU enables the execution of custom software for data reduction and analysis.

Synchronization

Multi-board synchronization can be achieved through either backplane* or front panel easy-cabling options.
(*) Future Development

Connectivity

Multiple interface options are available: USB-3.0 and CONET** optical link or 1/10 Gb Ethernet (switchable on the same socket)
(**) *CONET: CAEN Daisy Chainable Optical Link Protocol*

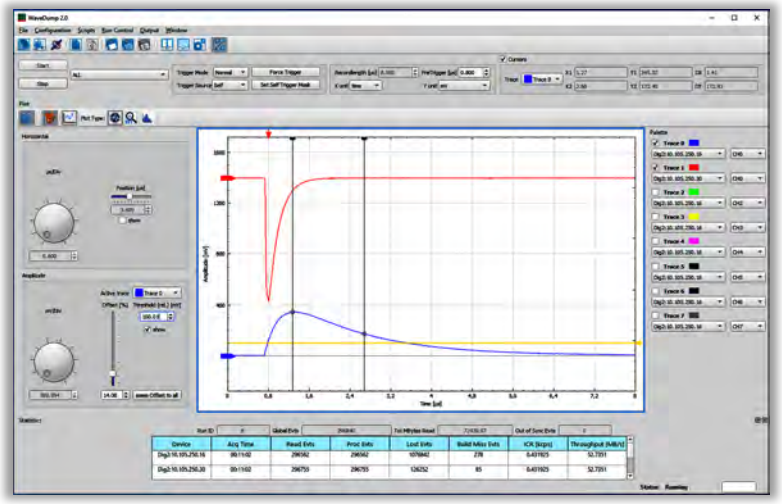
Data Acquisition

The 2730 Digitizer is capable of handling the complete acquisition chain, starting from sampling the input signal in the ADC to signal processing and readout. With its open FPGA architecture and the Sci-Compiler tool, users can customize the firmware for pulse processing. Additionally, the onboard Arm processor allows for the development of custom software. These features make the Digitizer a highly versatile and compact readout module that can be adapted to various applications. Some examples include nuclear spectroscopy with segmented germanium detectors, Silicon strip readout, gamma-ray tracking with waveform capture, and sub-ns timing measurement .

For users who do not require customization of the digital pulse processing, we offer a range of firmware and software options, including:

- Waveform recording using common-trigger
- Energy Spectrum recording using PHA (PSD) mode
- Pulse shape discrimination
- Sub-ns timing measurements using digital CFD
- Advanced Waveform readout using ZLE (Zero Length Encoding)

CAEN provides two user-friendly readout software options: WaveDump2 for waveform recording using common-trigger firmware, and CoMPASS, a multiparametric DAQ software that manages other Digital Pulse Processing algorithms. It is even possible to simultaneously plot waveforms and other relevant quantities when managing multiple boards.



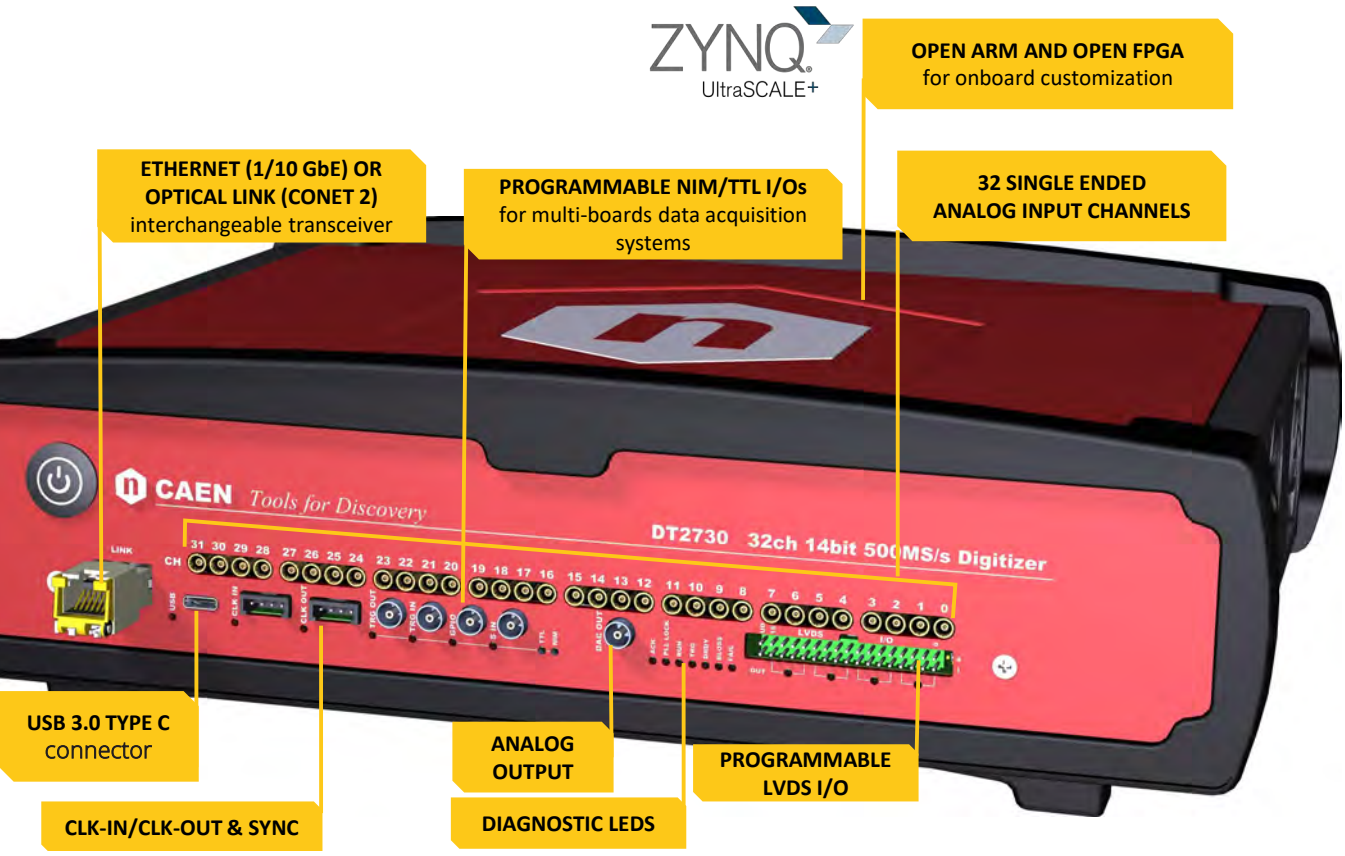
WaveDump2 software

- Waveform recording application
- Multi-board management
- Simultaneous plot of waveforms from up to 8 input channels
- Flexible and easy configuration of channel and trigger settings
- Runtime FFT analysis

WaveDump2 is a C++ software designed to support the Digitizer Series 2.0, running the scope firmware for waveform recording provided by CAEN. Developed using the Qt cross-platform application development framework, this software offers an advanced and user-friendly configuration GUI. It provides a comprehensive range of tools and functionalities to manage various hardware parameters, from basic settings to more specific ones. Configuration settings can be conveniently stored in or loaded from configuration files. The software also facilitates data acquisition from multiple boards and synchronized systems through a dedicated toolbar. The collected data can be saved in ASCII or binary file formats for offline analysis.

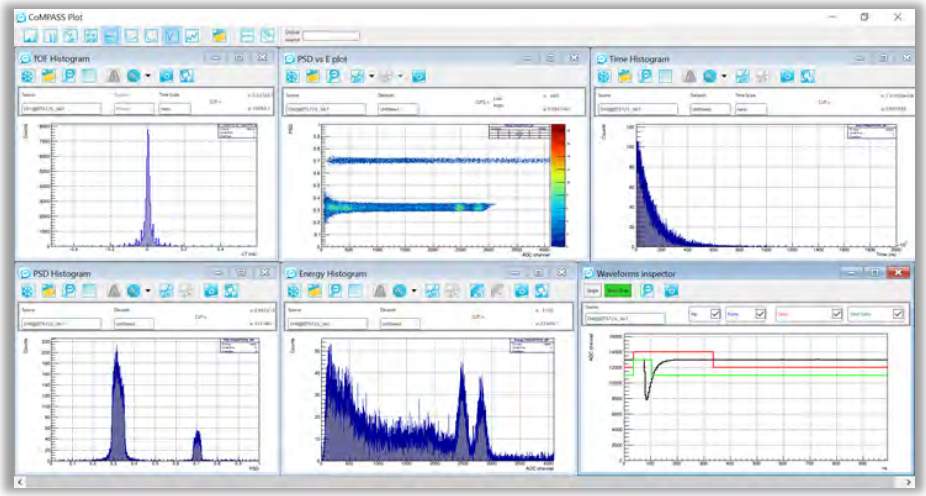
The program includes a plot section that functions as an 8-channel digital oscilloscope emulator. This tool allows users to review acquired waveforms, fine-tune device settings, and troubleshoot potential issues. The oscilloscope interface features cursors for on-screen measurements, as well as marker lines to indicate the trigger position and trigger threshold level. Traces can be individually enabled or disabled, and a legend is provided to easily identify displayed signals. The graphical tool offers zooming controls in both the vertical and horizontal directions. Basic processing capabilities, such as FFT (Fast Fourier Transform) and samples histogramming, are available in real-time.

WaveDump2 is compatible for Windows® and Linux® platforms.



CoMPASS multiparametric software

- Simultaneous plot of waveforms, Time, Energy, PSD, and TOF spectra
- Online filtering (Time, Energy, PSD)
- Multi-board management
- Advanced data saving
- ROOT format data saving



CAEN Multi-PArameter Spectroscopy Software (CoMPASS) is the data acquisition (DAQ) software designed for both Digitizer Series 1.0 and 2.0, running the DPP (Digital Pulse Processing) firmware provided by CAEN. It enables Multiparametric Data Acquisition for Physics Applications, where detectors can be directly connected to the digitizers/MCAs inputs, allowing simultaneous acquisition of energy, timing, and PSD (Pulse Shape Discrimination) spectra.

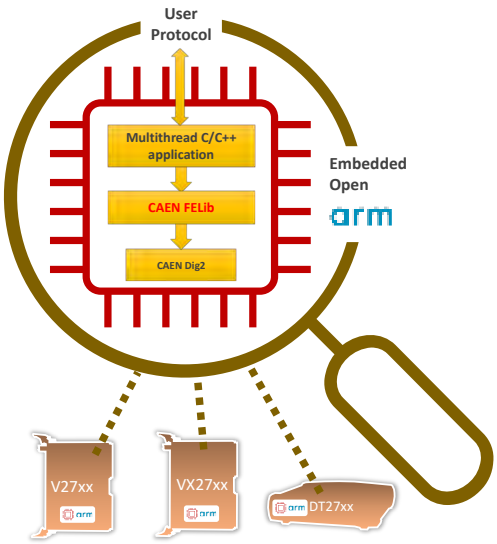
CoMPASS software offers a user-friendly interface designed to manage the acquisition process using all the CAEN DPP algorithms. It provides easy configuration of acquisition parameters and allows up to six different plots and histograms to be displayed simultaneously. CoMPASS can handle multiple boards and enables straightforward synchronization of multiboard systems. Some of the key features of CoMPASS include event correlation between different channels (both in hardware and software), energy, PSD, and time selections, calculation and display of acquisition statistics (trigger rates, data throughput, percentage of discarded events due to selections, etc.), basic mathematical analysis of recorded spectra (ROI selection, background subtraction, peak fitting, etc.), saving output data files (raw data, lists, waveforms, spectra), and offline processing using saved files with different processing parameters.

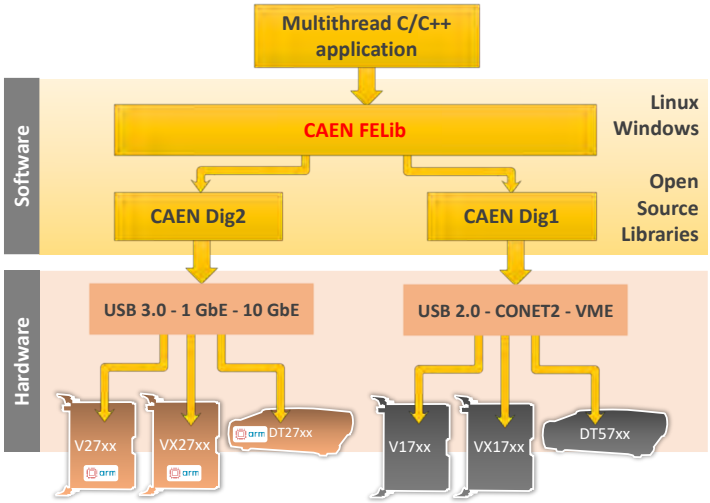
For users familiar with the ROOT Analysis Framework, CoMPASS provides the option to save output files (lists, waveforms, and spectra) in the ROOT TTree format, allowing easy post-processing with customized analysis code .

CoMPASS is available for Windows® and Linux® platforms.

CAEN FELib Library

- Set of functions designed for controlling and utilizing Digitizers 2.0 (2740, 2745, and 2730 family).
- Available in C/C++ and Python for both Windows and Linux operating systems.
- Distributed as an open-source software under the GNU Lesser General Public License 3.
- Provides multithread support for enhanced performance.
- Support for CAEN Digitizer 1.0 is also available.

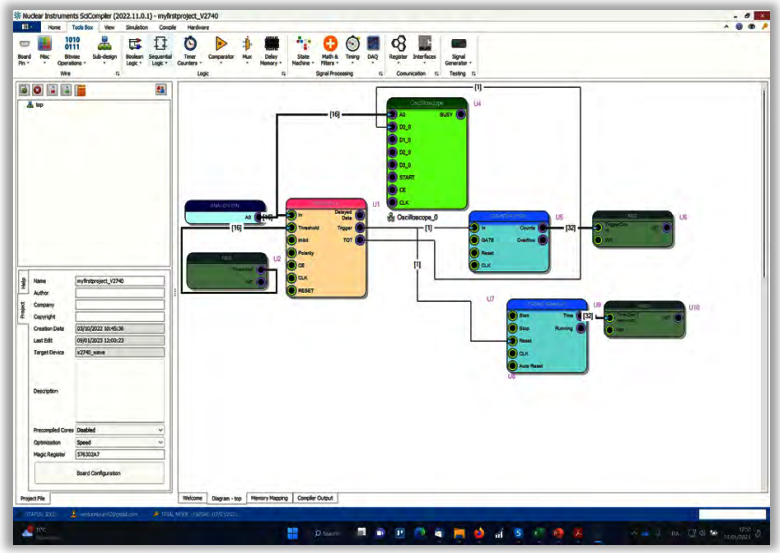




CAEN Waveform digitizers x27xx introduce a new way of accessing the firmware parameters, providing an abstraction of the registers in the form of library parameters that are much easier to understand and use.

This new way is designed to simplify the life of those users who need to build their own DAQ system and software and access the digitizer firmware parameters. CAEN FELib can be used to control and acquire data from the new generation of CAEN digitizers. This library is only an interface and does not include support for any digitizer family. To use a digitizer, the user must also install the corresponding CAEN Digx library.

FELib is compatible for Windows® and Linux® (x86 and Arm) platforms.



SCI-COMPILER
Open FPGA

Sci-Compiler

- Block-diagram-based programming tool for CAEN Open FPGA boards
- Designed to make FPGA access easier, even for non-expert programmers
- Offers 100+ advanced signal processing blocks for Physics and Nuclear Engineering
- Provides Remote Customization Service for compilation and simulation with minimal local setup
- Includes embedded tools for debugging and firmware testing

Sci-Compiler, short for Scientific Compiler, is a graphical software tool designed to simplify and expedite the implementation of firmware in physics applications for open FPGA CAEN boards. By creating a block diagram, the software can automatically generate firmware that can be directly deployed on compatible hardware. This means that even users without expertise in VHDL/Verilog programming can create their own firmware code. It is a unique tool that generates and compiles FPGA code, downloads it onto the target device, and allows real-time data acquisition on a host computer.

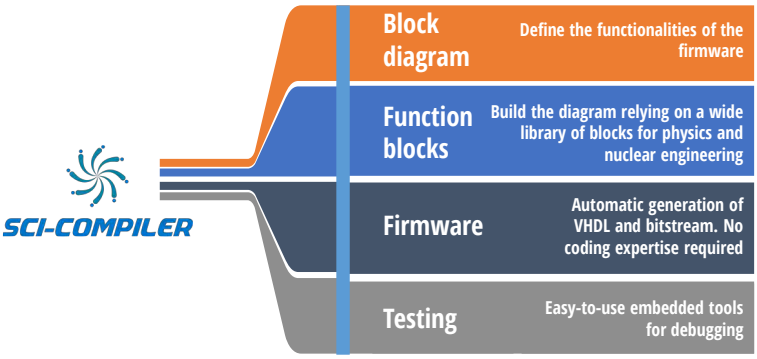
The Sci-Compiler tool includes over 100 virtual blocks that implement complex functions commonly used in physics applications. These functions include waveform recording, logic gates, TDC (Time-to-Digital Converter), spectrum reconstruction, pulse shape discrimination, and more.

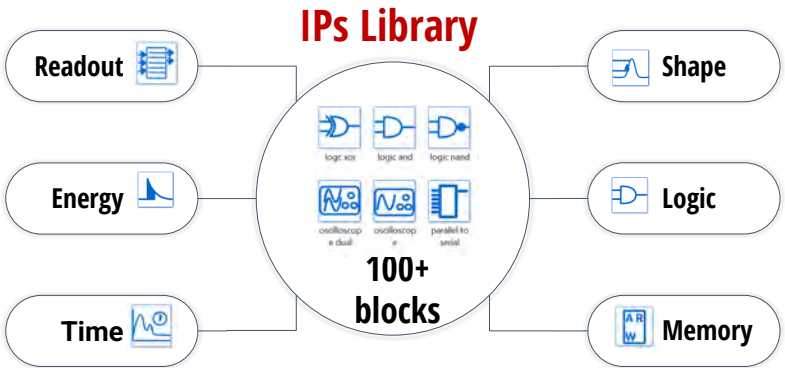
Sci-Compiler is currently available for Windows® platforms.

Sci-Compiler is a software tool that simplifies and accelerates the R&D phase. It allows users to create a diagram by placing and connecting different blocks (e.g. oscilloscope, TDC, MCA, charge integration, etc.) that represent the desired functions. Sci-Compiler then automatically generates and deploys a VHDL code to the FPGA that implements those functions.

This way, even users who are not familiar with VHDL/Verilog can write their own firmware code by focusing on the functional blocks of their application.

In addition, Sci-Compiler provides a Software Development Kit (Sci-SDK) for Windows and Linux that is compatible with the custom firmware for any supported board. The SDK consists of drivers, libraries and example codes in C++ and Python, making it easy to create a custom DAQ software that can run on Windows or Linux.





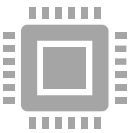
The Sci-Compiler software enables the development of both purely digital applications, using blocks such as logic gates, scaler, state machine, and analog processing applications, such as custom Multichannel Analyzers, charge integration, Pulse Shape Discrimination, Waveform recording with custom trigger logic, and many more.

Sci-Compiler is capable of automatically generating VHDL firmware code that implements the functions specified in the block diagram.

The compilation process is made highly accessible through the optional Remote Customization Service, which allows you to generate an operating firmware even if you don't have a complete FPGA compiler software installed on your local PC. This greatly simplifies the software setup. By utilizing the Remote Customization Service, Sci-Compiler handles the addition of hard-coded components to your project that remain consistent in each firmware, and generates the final firmware file within the Remote Center and the MyCAEN+ area. This file is then ready to be deployed onboard. CAEN provides the Remote Customization Service and Yearly Upgrade Plan to deliver a high-quality software product with the necessary flexibility to meet the users' requirements.

Sci-Compiler license

A single Sci-Compiler license can run on a PC relying on a dedicated USB Dongle



Runtime license

Using a single Sci-Compiler license, it is possible to compile and deploy firmware for multiple compatible boards that have been activated through a runtime license. A different runtime license is needed for each board.

Remote Customization / Upgrade

Remote customization service allows to generate the firmware code with minimal local resources

Stay up-to-date with the newest Sci-Compiler features by subscribing the yearly upgrade service

Ordering Option

Description	Code
SW555 - Sci-Compiler PRO License	WSW555PROXAA
SCI-Compiler runtime license for Digitizers	WSW55RUNTIME
1 year remote customization service + upgrade for Sci-Compiler	WSW55RCSXAAA
5 years remote customization service + upgrade for Sci-Compiler	WSW55RCSX5YA

Technical Specifications

General Features

Analog Inputs		
Number of Channels	32	Single-ended
Impedance	50 Ω	
Connector	MCX	
Full scale range (FSR)	4 V_{pp} ÷ 0.2 V_{pp}	
Individual Offset adjustable in the range	±2.5V	
Bandwidth (-3 dB)	250 MHz	
Gain	x1 ÷ x20 software programmable In steps of 1 dB independently on each channel	
Digital Conversion / System Performance		
Resolution	14 bits	
Sampling Rate	500 MS/s (simultaneously on each input), Scalable by 2^n decimation factor, n = 1 to 10 (Scope firmware only)	
ENOB (Typ)	10.5 (@50MHz, -3dB, Gain x2)	
RMS (Typ)	2.4 LSB RMS (@Gain x2)	
Digital I/O and Analog Output		
CLK-IN	Two differential pairs: - CLK: reference clock signal - SYNC: synchronization signal (start/stop, T0, etc.)	AC-coupled LVDS, ECL, PECL, LVPECL, CML Zdiff = 100 Ω 2.54mm 4-pin AMPMODU Mod II male connector
CLK-OUT	Same functionalities as CLK-IN Daisy chainable in multi-board synchronization	LVDS 2.54mm 4-pin AMPMODU Mod II male connector
TRG-IN/TRG-OUT/GPIO/S-IN	General-purpose I/Os Software programmable (trigger, gate, veto, busy, etc.) - TRG-IN/S-IN internally terminated with 50 Ω (Zin = 50 Ω) - TRG-OUT requires Rt = 50 Ω - GPIO as Input must be terminated with 50 Ω - GPIO as TTL Output requires Rt = 50 Ω - GPIO as NIM Output requires Rt = 50 Ω or 25 Ω	Sigle-ended TTL/NIM (SW programmable) LEMO 00 male connector
LVDS I/O	16 differential pairs Software programmable I/O (individual self-trigger outputs, trigger validations, Veto, Busy, Start, Stop, Pattern Input, etc.)	LVDS Zdiff = 100 Ω (when set as inputs) 2.54mm 34-pin AMPMODU Mod II male connector
DAC OUT	DAC output for signal inspection, pulse generation, majority level 14-bit Digital-to-Analog Converter (DAC) 125 MS/s Update Rate	±1 V @ 50Ω load ±2 V @ hi-Z load Output Range LEMO 00 connector

Acquisition Memory

	5 GB total DDR4 memory size (83.886 MS/ch) divisible in multiple buffers Maximum record length: ~ 84 ms @ 500 MS/s (total memory size divided by 2)[1] *[1] Value referred to the Scope firmware (minimum of two buffers admitted)*	

Communication Interfaces

1 GbE	Copper RJ45 or optical LC connector on SFP+ transceiver TCP/IP protocol	Transfer rate: 110 MB/s
10 GbE *(coming Soon)*	Copper RJ45 or LC optical connector on SFP+ transceiver Protocol: TCP/IP, UDP	Transfer rate: 280 MB/s (TCP/IP), t.b.d. (UDP)
CONET *(Available on Request)*	Optical LC connector on SFP+ transceiver CONET2 protocol (CAEN proprietary)	Transfer rate: 80 MB/s
USB 3.0	USB-C type connector USB 3.1 GEN1 protocol	Transfer rate: 280 MB/s

Technical Specifications (continued)

Trigger and Synchronization

Trigger Modes		
Common	All channels acquire simultaneously with the trigger (software, external or logic combination of self-triggers)	
Individual	Each channel acquires independently with its self-trigger	
Correlated	The individual self-trigger of each channel is validated by the coincidence/anticoincidence logic between other self-triggers and/or external I/Os	
Trigger Time Stamp	**Scope Firmware**	**DPP firmware**
Resolution:	8 ns coarse time stamp,	2 ns coarse timestamp 2 ps fine time stamp
Counter range:	48 bits	48 bits
Full-scale range:	~625 h	156 h
Synchronization		
Clock Propagation	Typical 62.5MHz frequency distributed by daisy chain through CLK-IN/CLK-OUT or by fan-out to CLK-IN Custom frequencies can be supported	
Acquisition Start/Stop	Daisy chain or fan-out propagation through CLK-IN/CLK-OUT or NIM/TTL, LVDS I/O	
Data Sync	Busy/Veto logic on LVDS I/Os or NIM/TTL I/Os for event building synchronization	
Trigger Time Stamp Reset	Software from START run command or Hardware from S-IN/GPIO input (Scope Firmware only)	
Trigger Distribution	TRG-IN/TRG-OUT NIM/TTL LEMO I/Os (common trigger) or LVDS I/Os (common or individual trigger)	

Firmware and FPGA

FPGA	
Device	Xilinx Zynq UltraScale+ Multiprocessor System-on-Chip mod. XCZU19EG Processing System based on Quad-core Arm with 2GB DDR4 memory @2400 MT/s (Linux OS onboard) Programmable logic with more than 1100K system logic cells and 80Mbit memory
CAEN Firmware	**Developed by CAEN, storedi in the on-board FLASH memory, and live rebootable by Web Interface**
DPP Firmware	Firmware implementing Digital Pulse Processing algorithms: - DPP-PHA: Pulse Height Analysis - DPP-PSD: Pulse Shape Discrimination - DPP-ZLE: Zero Length Encoding
Scope Firmware	Firmware for the waveform recording
Upgrades	CAEN firmware can be uploaded via Web Interface (scope and DPP firmware, and their updates)
User Firmware (Open FPGA)	
SCI-Compiler	User Firmware Generator and Compiler Graphical Tool for CAEN Programmable Boards
Scope Personalization	Customizable features of the Scope firmware: - Common trigger - Simultaneous waveform recording on 32 channels management - Trigger logic - Wave processing
DPP Personalization	Customizable features of the DPP firmware: - Individual trigger and channel acquisition management - DPP algorithm - Trigger logic - Event data information

Technical Specifications (continued)

Software

Readout Software
CoMPASS spectroscopy software (CAEN DPP firmware only) for Windows® and Linux®
WaveDump2 (CAEN scope firmware only) for Windows® and Linux®
SCI-Compiler (Open FPGA): Automatic generation of drivers (USB, ethernet), libraries, and demo software for Windows®
Web Interface
Firmware management (e,g. upgrades and on-the-fly selection of the firmware to run), board information, PLL and Ethernet configuration, board status monitoring, DPP license management
SDK and Tools
General-purpose C libraries with demo samples for host Windows® and Linux® PC, and embedded Arm processor

Mechanical

	VX2730	DT2730	
Form Factor	1-unit wide VME64X	Desktop	Desktop / Rack
Weight	700 g	3120 g	3170 g
Dimension	6U x 160 mm	338 W x 100 H x 295 L mm³ (including connectors)	19" rack mount

Environmental

Environmental	Indoor use
Operating Temperature	0°C ÷ +40°C
Storage Temperature	-10°C ÷ +60°C
Operating Humidity	10% ÷ 90% RH non condensing
Storage Humidity	5% ÷ 90% RH non condensing
Pollution Degree	2
Altitude	≤2000 m
Overvoltage Category	II
EMC Environment	Commercial and light industrial
IP Degree	Enclosure (desktop models), not for wet location

Regulatory

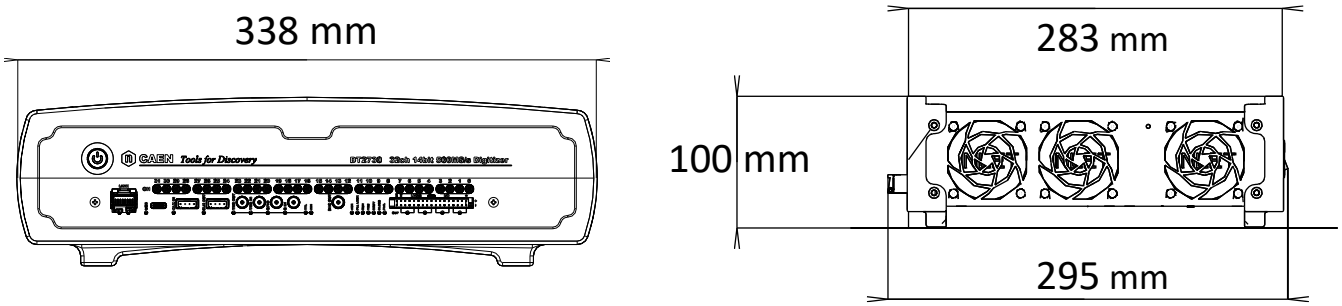
Compliance	EMC:	CE 2014/30/EU Electromagnetic compatibility Directive
	Safety:	CE 2014/35/EU Low Voltage Directive

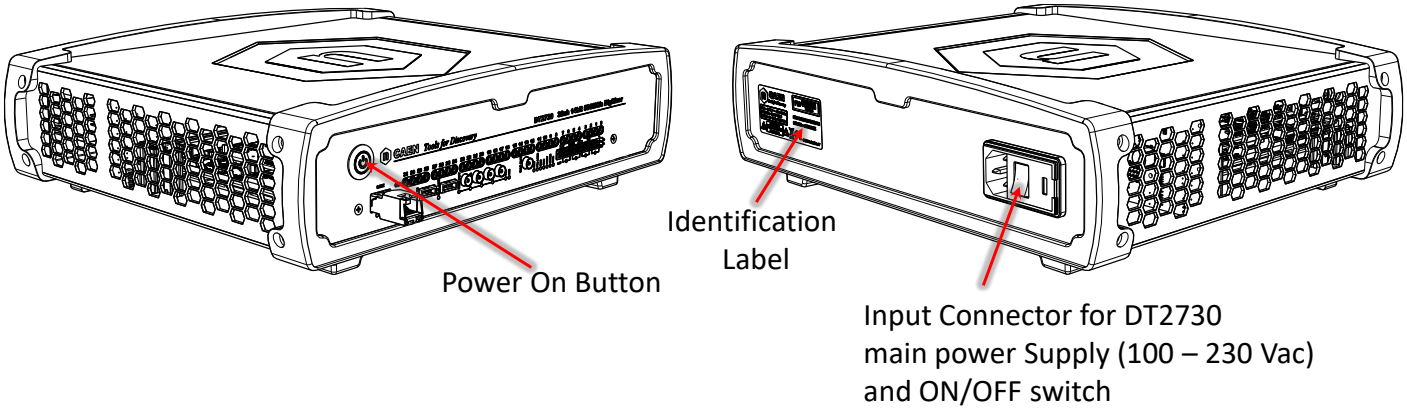
Power Requirements

	VX2730 (*)	DT2730
+ 12V	0.5 A	n.a. -
+ 5 V	4.8 A	n.a. -
+ 3.3 V	8.9 A	n.a. -
		Mains Powered (Max. 130 Watt @ 110/220V)

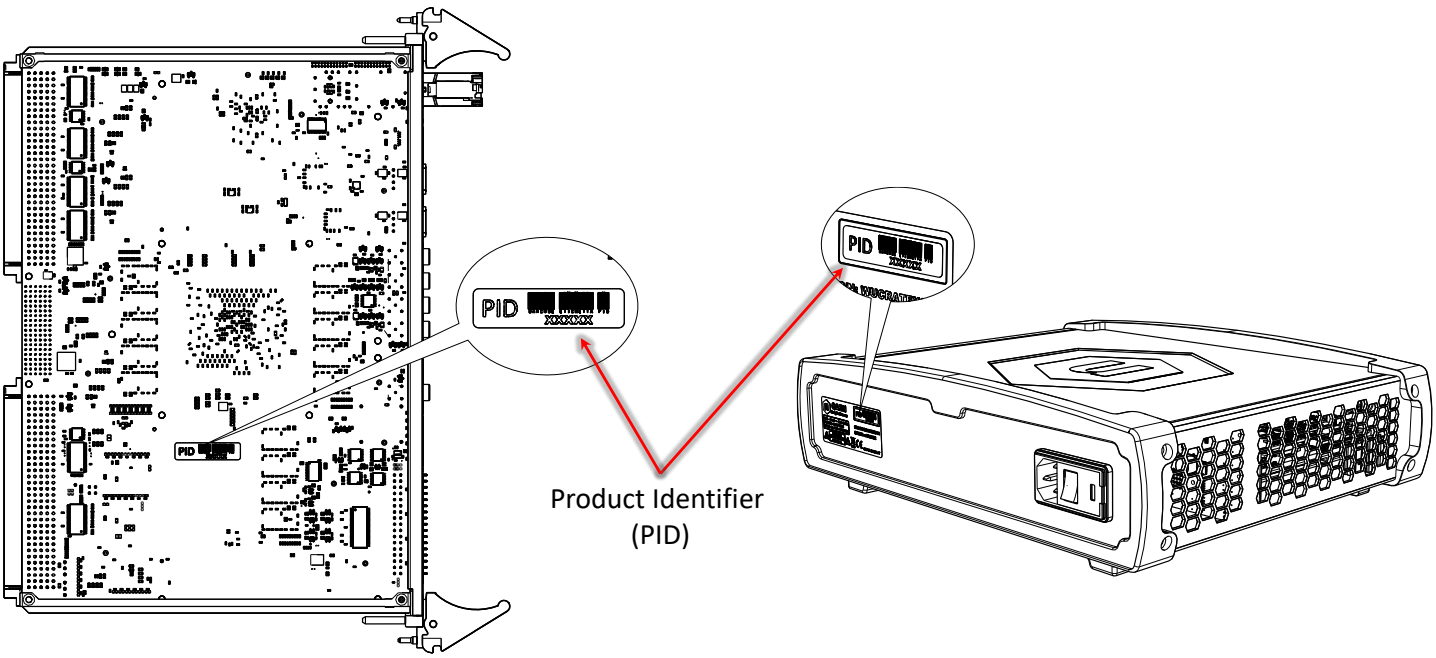
(*) These are preliminary values, referred to a 1-GbE Scope firmware, that could vary depending on the firmware type

DT2730 Mechanical Dimension





2730 PID (Product Identifier)



PID (Product Identifier) is a unique incremental number greater than 10000 assigned to each CAEN product It can be found on a label attached to the product (refer to the figure) and is also stored in an onboard non-volatile memory that can be read via the Web Interface.

2730 Front Panel and LED behavior

LINK Ethernet network indicator
- Ethernet link unavailable (cable off)
- Ethernet link available (cable in)
- Data activity on the ethernet link

USB USB Link Indicator
- USB link unavailable (cable off)
- USB link available (cable in)
- Data activity on the USB link

CLK IN Reference Clock indicator
- Internal clock reference enabled
- External clock reference enabled

CLK OUT Reference Clock indicator
- Reference clock propagation disabled
- Reference clock propagation enabled

TRG OUT
TRG IN
GPIO
S IN
LEMO I/O level indicator
- No activity on the relevant connector
- Signal activity on the relevant connector

TTL / NIM LEMO I/O level indicator
- NIM or TTL level enabled for the 4 LEMO I/Os

ACK Readout activity indicator
- No readout access to the board through USB or Ethernet
- Read or Write access to the board through USB or Ethernet

PLL LOCK PLL lock indicator
- The PLL is not locked to the reference clock
- The PLL is locked to the reference clock

RUN Acquisition (data taking) indicator
- The acquisition is off
- The acquisition is running

TRG Accepted Trigger indicator
- The trigger is accepted

DRDY Data ready indicator
- Event/Data is present in the Output Buffer

DLOST Data loss indicator
- The trigger arrived while the board is in busy state. This trigger is rejected and the relevant event/data is lost

FAIL Board fail indicator
- A power fail, over temperature condition or PLL lock loss occurred

OUT LVDS I/O direction indicator
- LVDS I/O 4-pin group direction is INPUT
- LVDS I/O 4-pin group direction is OUTPUT

LINK Ethernet Transceiver (inserted in the SFP+ receptacle)

USB Type-C Connector

CLK-IN / CLK-OUT 2.54mm 4-pin AMPMODU Mod II male connector

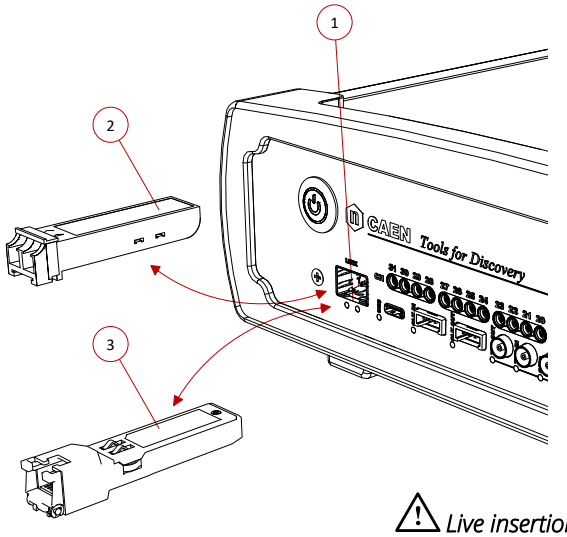
General Purpose I/O
TRG-IN / TRG-OUT / GPIO / S-IN
LEMO 00 connector

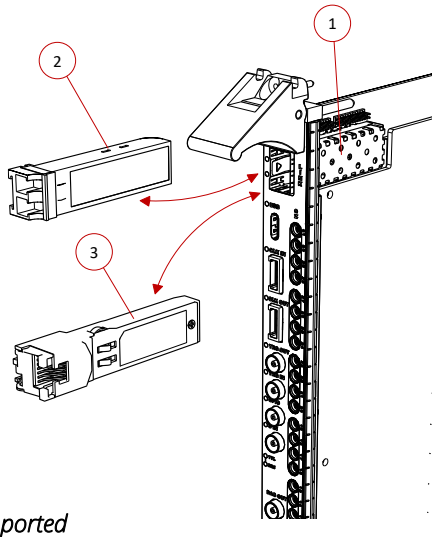
DAC-OUT LEMO 00 connector

LVDS I/O 16 differential pairs

LED mode
- OFF
- ON (COLOR)
- BLINKING (COLOR)

2730 SFP+ receptacle for Ethernet interface



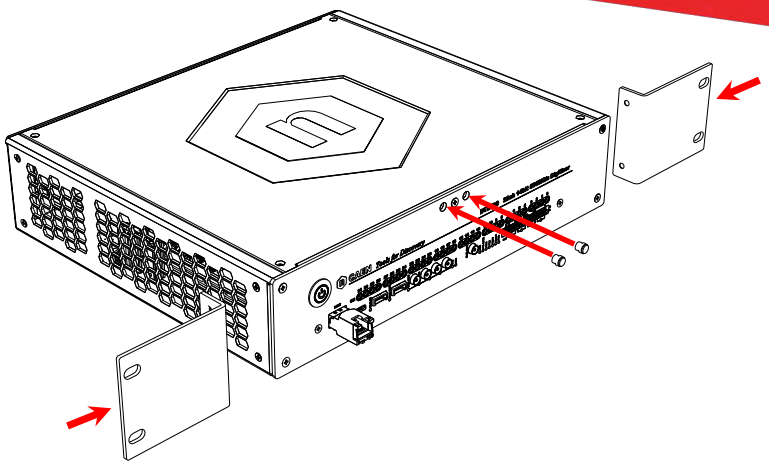


⚠ *Live insertion "Hot swap" not supported*

1. SFP+ receptacle for 1/10 GbE or Optical link
2. 1/10 GbE Optical Transceiver
   Type: AFBR-710DMZ Manufacturer: Avago
3. 1 Gb Ethernet Transceiver
   Cisco Compatible 1000Base-T Copper SFP (mini-GBIC) Transceiver

Rack Mounting:

Desktop version (DT2730) can be rack mounted using 2 brackets included in the product-kit.



2730 Accessories

A319A
Clock & Sync cable assembly

The The A319A is a cable assembly designed for the distribution of Clock and Sync signals in the 27xx Digitizer families. Utilizing the front panel CLK-OUT / CLK-IN daisy chain, this 4-contact cable facilitates the transmission of two differential signals from one digitizer to another, enabling the synchronization of multiple boards.

A319B
Clock cable assembly from Digitizer 2.0 series to Digitizers 1.0 series

The A319B is a cable assembly utilized for the distribution of Clock signals between non-homogeneous digitizer series. It connects the 3-contact connector on the Digitizer series 1.0 to the 4-pin connector on the Digitizer series 2,0. Similar to the A319A, this cable enables the transmission of the differential clock signal from one digitizer to another through the front panel CLK-OUT / CLK-IN daisy chain, allowing for the synchronization of multiple boards.

µ-crate
Desktop single-slot VME64X Crate

- Mechanical compatibility: 1-unit VME 6U x 160 mm modules
- Standard power: 10.5 A @+3.3 V, 10 A @+5 V, 2 A @+12 V, 2 A @-12 V
- Fan speed control:
  - Manual adjustment via hardware button (high/low state)
  - Automatic control available only with Digitizer 2.0 series
- Mains power: 100 - 240 V AC (130 W) @ 50 / 60 Hz
- Includes a 19" rack mount kit adapter

The µ-Crate is a mains-powered desktop device integrating a low-noise cooling vents system. The desktop form factor can be optionally converted into a 19” rack thanks to the included metal brackets.

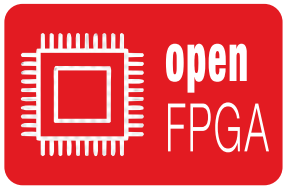
The single-slot backplane supports VME64 and VME64X CAEN boards of the Digitizer 1.0, Digitizer 2.0 Families, the V2495 Programmable Logic Unit, as well as other CAEN boards. Only VME Modules (one-unit, 6U x 160mm) with direct connection on the front panel (via USB-2.0/3.0, CONET optical link or 1/10 GbE) and/or not requiring VME bus control (VME protocols not supported) are compatible with the µ-Crate.

The images above show the µ-Crate product with a Digitizer from the 2.0 Family (VX2740) installed, as well as the two possible configurations: Desktop and rack-mountable (using the two brackets included in the sales kit).

Ordering Option

Description	Code
VX2730 - 32 Ch. 14 bit 500MS/s Digitizer with Programmable Input Gain	WVX2730XAAAA
DT2730 - 32 Ch. 14 bit 500MS/s Digitizer with Programmable Input Gain	WDT2730XAAAA
Accessories	
A319A - Clock & Sync Cable for Digitizers Series 2.0 interconnection (L=20cm)	WA372MXAAAAA
A319B - Clock Cable for Digitizer Series 1.0 to 2.0 interconnection (L=20cm)	WA319BXAAAAA
µ-Crate - Desktop single-slot VME64X Crate	WUCRATEX001A

2730
Digitizer Family



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