CAEN Electronic Instrumentation

742 Digitizer Family

32+2/16+1 Ch. 12-bit 5 GS/s Digitizer

APPLICATIONS

- Nuclear and Particle Physics
- Astroparticle Physics
- Time of Flight
- Medical Imaging (PET)

FORM FACTOR

VME64 VME64X NIM DESKTOP

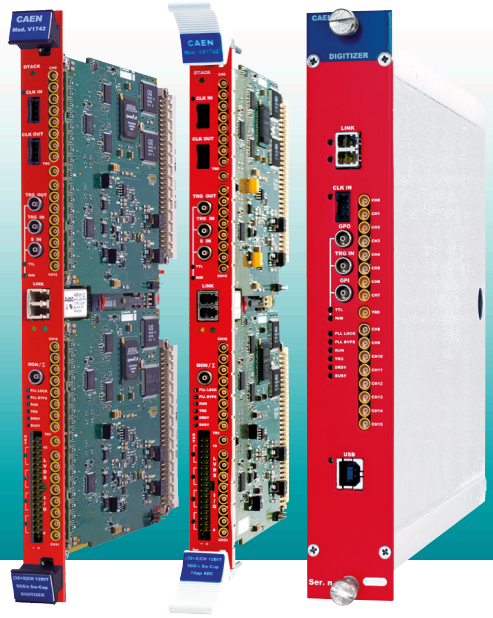
FUNCTIONS

WV TS

Very fast Switched Capacitor Digitizer with high channel density

APPLICATION NOTES

- AN3251
- GD2783



Overview

The 742 is the Switched Capacitor Digitizer family, based on the DRS4 chip by PSI, with the highest sampling frequency (5GS/s) and channel density. It can record very fast signals from scintillators coupled to PMTs, Silicon Photomultipliers, APD, Diamond detectors and others, and save them with high efficiency and precision for advanced timing analysis. The 742 family has an additional channel (two channels in case of VME boards) which can be used as time reference for time of flight measurements. The resolution of this kind of measurements can reach up to 50 ps.

The analog inputs are continuously sampled by the 1024 capacitive cells in the DRS4 chip at a frequency that is software selectable amongst 5 GS/s, 2.5 GS/s, 1 GS/s and 750 MS/s. Once the trigger condition is met, the capacitors are released, data is converted by a 12-bit ADC at a lower frequency and stored into a digital memory buffer. As the sampling and the analog-to-digital conversion are not simultaneous, a dead-time is introduced, during which the board cannot accept other triggers. Multiple boards can be synchronized to build up complex systems.

The acquisition is fully controlled by the WaveDump software, which manages the settings, plots and saves the waveforms. Libraries and demo software in C and LabView are available for integration and customization of specific acquisition systems.

742 family comes in three form factors: VME (32 input channels + 2 additional channels), NIM (16 input channels + 1 additional channel) and Desktop (16 input channels + 1 additional channel). The communication to and from the board is provided through the following interfaces: USB (Desktop and NIM form factors), VMEbus (VME form factor), and Optical Link (all form factors).

Features

- 12-bit @ 5 GS/s, 1024 samples per event
- 5, 2.5, 1 and 0.75 GS/s software selectable sampling frequencies
- Analog inputs on MCX coaxial connectors
- VME64/VME64X (32+2 ch.), NIM (16+1 ch.) and Desktop (16+1 ch.) modules
- 1 Vpp input dynamic range with programmable DC offset adjustment
- VME, USB and Optical Link communication interfaces
- Multi-board synchronization features
- Daisy chain capability
- Demo software tools, C and LabVIEW libraries, Readout Software

x742 is based on the DRS4 a Switched Capacitor Array. This technology

relies on a set of capacitors that continuously sample the analog input signals. As soon as the trigger is issued, capacitors are decoupled from the input signals with a time interval from each other that is the sampling period.

The trigger therefore freezes the currently stored signal in the sampling capacitance cells. Subsequently the cells are multiplexed into the 12-bit ADC.

Firmware	Software	WV	TS
WAVEFORM RECORDING	WAVE DUMP CAEN	•	•

Principle of Operation

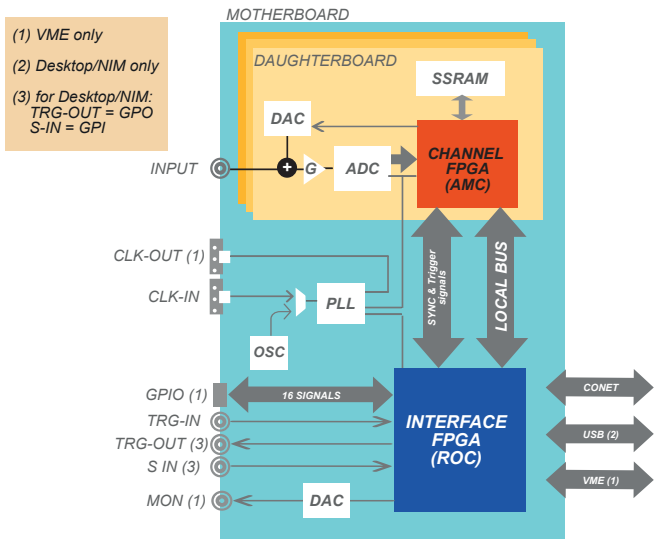
CAEN Waveform Digitizers are devices able to continuously acquire analog input signals, which are sampled by fast ADCs and stored into digital memories where they are avaiable for readout through different communication interfaces (USB, VMEBus, Optical Link). Depending on the FPGA firmware, the digitizer can work like an oscilloscope to acquire raw waveforms, or perform online processing to calculate parameters such as pulse height, charge, time stamp, pulse shape discrimination. In the latter case, the output data is a time-stamped list of parameters. Data reductions and zero suppression algorithms are also available. Digitization in CAEN digitizers is based on two main technics: **Flash ADC** and **Switched Capacitor Arrays**. Flash ADC are the fastest A/D converters, where the sampling and the analog-to-digital conversion are made practically at the same time. Flash ADC are so not affected by dead-time due to conversion. In the Switched Capacitor Arrays, the sampling and the A/D conversion take place at different times, thus introducing a dead-time. Despite of the dead-time, the Switched Capacitor Array Digitizers are able to sample the input pulse at very high frequency, up to 5 GS/s, with high channel density, while the highest Flash ADC frequency is 4 GS/s with a quite low number of channels. If compared to a commercial digital oscilloscope, the waveform digitizer presents a list of differences which make it an advanced instrument for many applications:

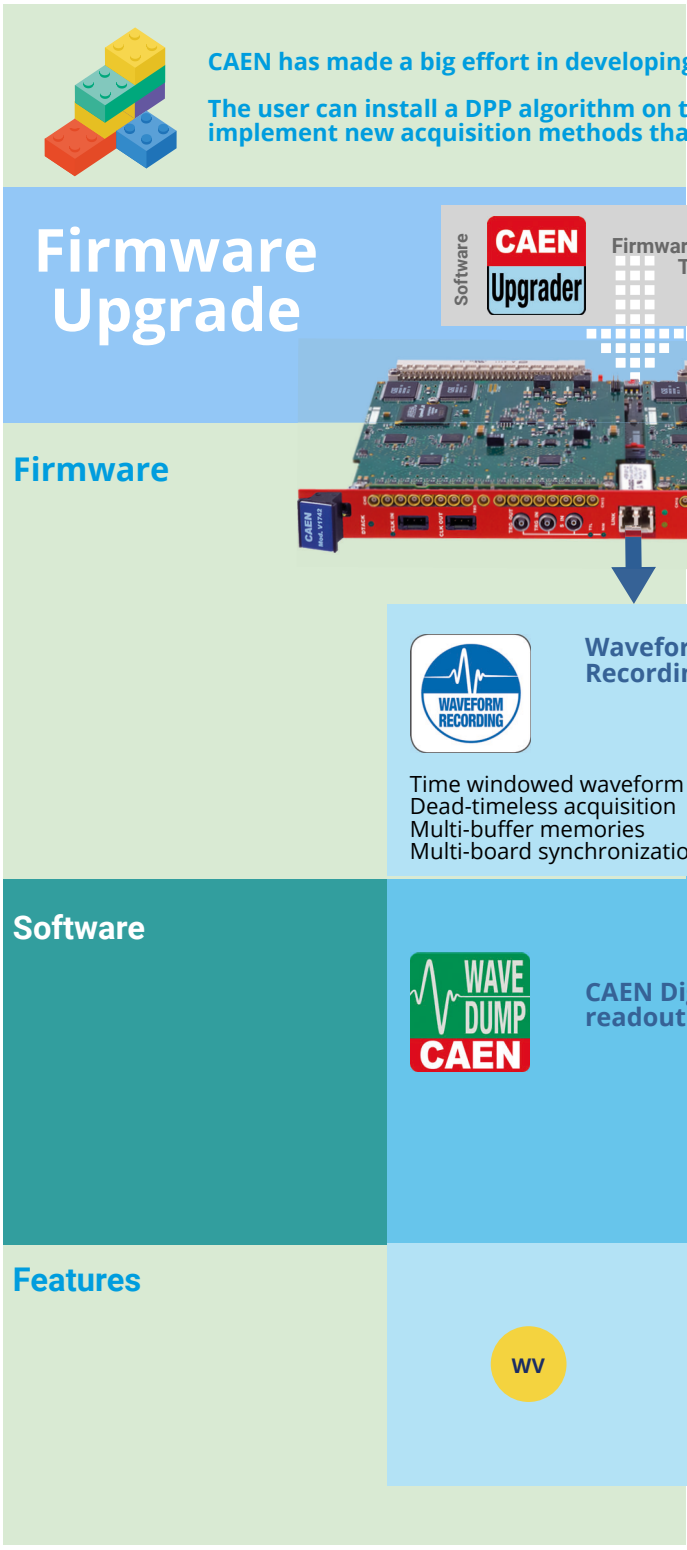
- Waveform recording with no dead-time due to conversion (Flash ADC digitizers)
- Independent channel self-triggering and event acquisition
- On-line digital pulse processing (DPP) algorithms
- Data reduction
- Multi-board synchronization for system scalability
- Communication interfaces with high bandwidth readout

The benefits of the digital approach are great stability and reproducibility, ability to reprogram and adjust the algorithms to the application, ability to preserve the information of the signal along the entire acquisition chain, flexibility, better correction of baseline fluctuation, pile-up, ballistic deficit, etc.. All in one board.

CAEN Digitizer block diagram:

- A motherboard which contains one FPGA for the readout interfaces and the services, and defines the form factor.





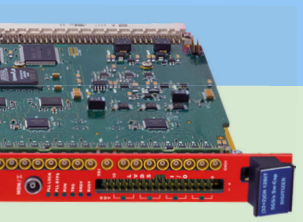
- One or more daughterboards which define the type of digitizer and contain the signal conditioning input stage, the ADCs, the FPGA for the data processing and the memories.

g algorithms for the Digital Pulse Processing (DPP).

he FPGA of the digitizer (firmware upgrade), run it on-line and t go beyond the simple waveform recording.

re Upgrade
Tool

742 Digitizer Family



rm
ng Firmware

recording

on

gitizer
application

TS

Feature Acronyms Legenda

WV (**Waveforms**): acquisition of a programmable number of ADC samples (raw waveforms)

TS (**Timestamp**): trigger coarse time stamp with low resolution (10-20 ns)

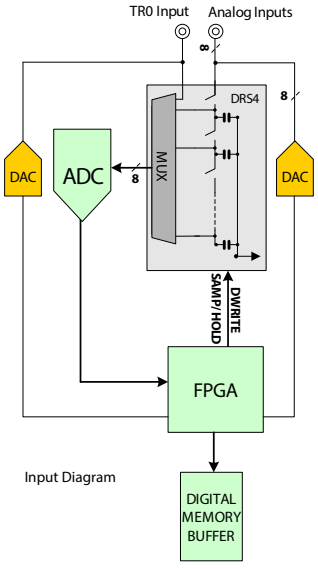
Domino Ring Sampling

The analog input signals are continuously sampled by the DRS4 (Domino Ring Sampler) chip* which consists of an on-chip inverter chain (domino wave circuit) generating a maximum of 5 GS/s sampling frequency; 2.5 GS/s, 1 GS/s, and 750 MS/s frequencies can be also programmed. The board has one chip per group, and each chip consists of 1024 capacitor cells per channel, which perform the analog sampling of the input (high frequency analog sampling).

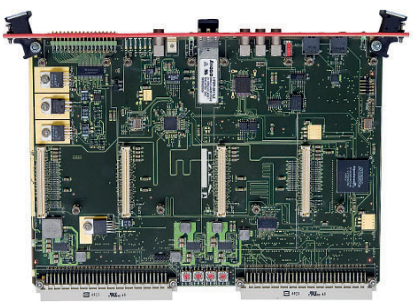
The record length of the acquisition is constrained by the cell number, and it is fixed to 1024 samples. The DRS4 chip continuously samples the input in a circular way (samples are overwritten) until a trigger signal stops its acquisition (holding phase). Then the cells release their capacitances at a readout frequency controlled by the FPGA (Output Mode).

The analog samples are digitized by the 12-bit ADC at a frequency of 29.296 MHz (low frequency digital sampling). The ADC output is stored by the FPGA into the Digital Memory Buffer. The single TR0 is split into the two DRS4 chips. Delay lines are equal in the two paths, anyway small differences in the digitized samples are possible due to differences in the chips and in the ADCs. When the digitization of the TR0 is enabled, there is a double conversion that increases the dead-time from 110 µs when only the inputs are converted to 181 µs when also the TR0 is converted.

** Detailed documentation of the DRS4 is available at http://drs.web.psi.ch/*



Input Diagram



MOTHERBOARD

DAUGHTERBOARD

Technical Specifications

GENERAL

Form Factor

1-unit wide, 6U VME64/VME64X
1-unit wide NIM
154x50x164 mm^3 (WxHxD) Desktop

ANALOG INPUT

Channels

32+2 channels, single ended (VME)
16+1 channels, single ended (NIM, Desktop)

Impedance

50 Ω

Connector

MCX

Full Scale Range (FSR)

1 Vpp (2 Vpp by customization code)

Bandwidth

500 MHz

Offset

Programmable DAC for DC offset adjustment per channel or 8-channel group. Range: ±1 V

TR0 TR1 Analog Inputs

Special inputs (MCX, 50 Ω) for fast local trigger and high resolution timing reference NIM/LVTTL signals also supported

DIGITAL CONVERSION

Switched Capacitor array

Domino Ring Sampler chip (DRS4) serving 8+1 channels
1024 storage cells per channel (200 ns minimum recorded time per event)

Resolution

12 bits

Sampling rate

5 GS/s simultaneously on each channel (2.5 - 1 - 0.75 GS/s software selectable)

Dead Time for Event A/D Conversion

110 µs analog inputs only; 181 µs analog inputs + TR0, TR1 inputs

CLOCK GENERATION

Synchronization clock source: internal/external

On-Board PLL provides generation of main board clocks from an internal (50 MHz loc. oscillator) or external reference (50 MHz or 58 MHz; other options on request) on front panel CLK-IN connector.

MEMORY

128 kS/ch or 1 MS/ch (1 event = 1024 samples per event) Multi-Event Buffer

TRIGGER

Trigger source

Self-trigger: logic OR combination of channels under/over threshold (each channel self-trigger drives two 8-ch groups)
Fast (Low Latency) trigger programmable threshold on TR0 and TR1 (each TRn signal drives two 8-ch groups)
External-trigger: Common by TRG-IN connector
Software-trigger: Common by software command

Trigger propagation

TRG-OUT (VME) / GPO (NIM and Desktop) digital output

Trigger Time Stamp

30-bit counter, 8.5 ns resolution, 9 s range

LVDS I/O (VME only)

16 general purpose LVDS I/Os controlled by FPGA

Busy, Data Ready, Memory full, Individual Trig-Out and other functions can be programmed An Input Pattern from the LVDS I/Os can be associated to each trigger as an event marker

SYNCHRONIZATION

Clock propagation

Daisy chain (VME only) through CLK-IN/CLK-OUT connectors
One-to-many clock distribution from an external clock source
Clock Cable delay compensation

Acquisition Synchronization

Sync Start/Stop through digital I/O (S-IN, TRG-IN or GPI input, TRG-OUT or GPO output)

External Trigger Time Stamp reset

COMMUNICATION INTEFRACE

Optical Link

CAEN CONET proprietary protocol, up to 80 MB/s transfer rate

Daisy chainable: it is possible to connect up to 8/32 ADC modules to a single Optical Link Controller (Mod. A2818/A3818)

USB (NIM & Desktop direct, VME via V1718 bridge)

USB 2.0 compliant
Transfer rate up to 30 MB/s

VME

VME 64X compliant

Data transfer mode: BLT32, MBLT64 (70 MB/s using CAEN Bridge), CBLT32/64, 2eVME, 2eSST (up to 200 MB/s)

POWER CONSUMPTIONS

Desktop: 1.7 A @ 12 V (Typ.)
NIM: 3.9 A @ +6 V, 90 mA @ -6 V
VME: 5.5 A @ +5 V, 200 mA @ +12 V, 300 mA @ -12 V

Ordering Options

Code	Description	Form Factor
WDT5742XAAAA	DT5742 - 16+1 Ch. 12 bit 5 GS/s Switched-Capacitor Digitizer: 128 events/ch (1kS/event), EP3C16, SE	Desktop
WDT5742BXAAA	DT5742B - 16+1 Ch. 12 bit 5 GS/s Switched-Capacitor Digitizer: 1024 events/ch (1kS/event), EP3C16, SE	Desktop
WN6742XAAAAA	N6742 - 16+1 Ch. 12 bit 5 GS/s Switched-Capacitor Digitizer: 128 events/ch (1kS/event), EP3C16, SE	NIM
WN6742BXAAAA	N6742B - 16+1 Ch. 12 bit 5 GS/s Switched-Capacitor Digitizer: 1024 events/ch (1kS/event),EP3C16, SE	NIM
WV1742XAAAAA	V1742 - 32+2 Ch. 12 bit 5 GS/s Switched-Capacitor Digitizer: 128 events/ch (1kS/event), EP3C16, SE	6U-VME64
WV1742BXAAAA	V1742B - 32+2 Ch. 12 bit 5 GS/s Switched-Capacitor Digitizer: 1024 events/ch (1kS/events), EP3C16, SE	6U-VME64
WVX1742XAAAA	VX1742 - 32+2 Ch. 12 bit 5 GS/s Switched-Capacitor Digitizer: 128 events/ch (1kS/event), EP3C16, SE	6U-VME64X
WVX1742BXAAA	VX1742B - 32+2 Ch. 12 bit 5GS/s Switched-Capacitor Digitizer: 1024 events/ch (1kS/event), EP3C16, SE	6U-VME64X
WPERS0174201	X742 Customization - 2 Vpp Input Range	ALL

Accessories

A2818
PCI CONET Controller

A3818
PCI Express CONET2 Controller

A654
MCX to LEMO Cable Adapter

A659
MCX to BNC Cable Adapter

A317
Clock Distribution Cable

A318
SE to Differential Clock Cable Adapter

AI2700
Optical Fiber Series

Cables for CONET Optical Link Networks

DT4700
Clock Generator and FAN-OUT

CAEN
Tools for Discovery

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