CAEN Electronic Instrumentation

724 Digitizer Family

8/4/2 Ch. 14-bit 100 MS/s Digitizer

APPLICATIONS

- Nuclear and Particle Physics
- X-ray and Gamma Spectroscopy with HPGe, Silicon detectors
- Spectroscopic Imaging for Homeland Security
- Segmented detectors, Medical Imaging, Material science

FORM FACTOR

VME64 VME64X NIM DESKTOP

FUNCTIONS

ICH WV TS PHA ZS DAW

Ideal for high resolution detectors

APPLICATION NOTES

- AN2508
- AN2086
- AN5157
- AN6308
- GD2783
- GD2827

Overview

The 724 is a family of CAEN Waveform Digitizers able to perform basic waveform recording and run online advanced algorithms (DPP) of pulse height analysis and dynamic acquisition window. Data is read by a Flash ADC, 14-bit resolution and 100 MS/s sampling rate, which is well suited for high resolution detectors as Silicon, HPGe or inorganic scintillators like NaI or CsI coupled with Charge Sensitive Preamplifiers. In the waveform recording mode, algorithms of zero suppression are also implemented to reduce the data throughput. The acquisition can be channel independent and it is possible to make coincidence/anti-coincidence logic among different channels and external veto/gating. Multiple boards can be synchronized to build up complex systems.

In case of DPP mode, data can be saved in time-stamped list mode to support higher input rates and improving the throughput performances. Piled-up events can be rejected or saved for offline analysis. The acquisition in DPP mode is fully controlled by the CoMPASS and MC^{2}Analyzer software, which manage the algorithm parameters, build the plots and saves the relevant energy and time spectra. In case of waveform recording mode, the user can take advantage of the CAENScope and WaveDump software to access and save the waveforms. Libraries and demo software in C and LabView are available for integration and customization of specific acquisition systems.

724 family comes in three form factors: VME (8 input channels), NIM (4 or 2 input channels) and Desktop (4 or 2 input channels). The communication to and from the board is provided through the following interfaces: USB (Desktop and NIM form factors), VMEbus (VME form factor), and Optical Link (all form factors).

Features

- 14-bit @ 100 MS/s
- Analog inputs on MCX coax. connectors
- VME64/VME64X (8 ch.), NIM (4 or 2 ch.) and Desktop (4 or 2 ch.) modules
- 0.5, 2.25 or 10 Vpp input dynamic range with programmable DC offset adjustment
- Sampling rate decimation factor (software selectable)
- Algorithms for Digital Pulse Processing (DPP)
- VME, USB and Optical Link communication interfaces
- Multi-board synchronization features
- Daisy chain capability
- Demo software tools, Control Software for waveform recording and DPP firmware, C and LabVIEW libraries

Firmware	Software	ICH	WV	TS	PHA	ZS	DAW
WAVEFORM RECORDING	WAVE DUMP CAEN, SCOPE CAEN		•	•		•	
DPP PHA	MC^2 CAEN, CoMPASS CAEN	•	•	•	•		
DPP DAW	DAW CAEN	•	•	•			•

Principle of Operation

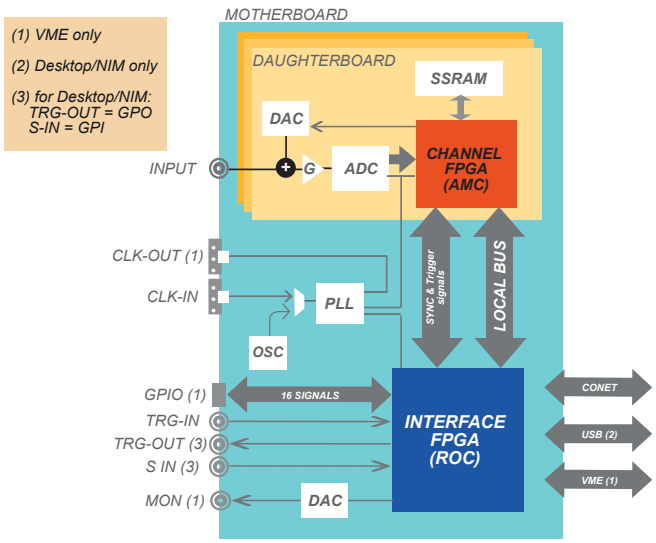
CAEN Waveform Digitizers are devices able to continuously acquire analog input signals, which are sampled by fast ADCs and stored into digital memories where they are avaiable for readout through different communication interfaces (USB, VMEBus, Optical Link). Depending on the FPGA firmware, the digitizer can work like an oscilloscope to acquire raw waveforms, or perform online processing to calculate parameters such as pulse height, charge, time stamp, pulse shape discrimination. In the latter case, the output data is a time-stamped list of parameters. Data reductions and zero suppression algorithms are also available. Digitization in CAEN digitizers is based on two main technics: **Flash ADC** and **Switched Capacitor Arrays**. Flash ADC are the fastest A/D converters, where the sampling and the analog-to-digital conversion are made practically at the same time. Flash ADC are so not affected by dead-time due to conversion. In the Switched Capacitor Arrays, the sampling and the A/D conversion take place at different times, thus introducing a dead-time. Despite of the dead-time, the Switched Capacitor Array Digitizers are able to sample the input pulse at very high frequency, up to 5 GS/s, with high channel density, while the highest Flash ADC frequency is 4 GS/s with a quite low number of channels. If compared to a commercial digital oscilloscope, the waveform digitizer presents a list of differences which make it an advanced instrument for many applications:

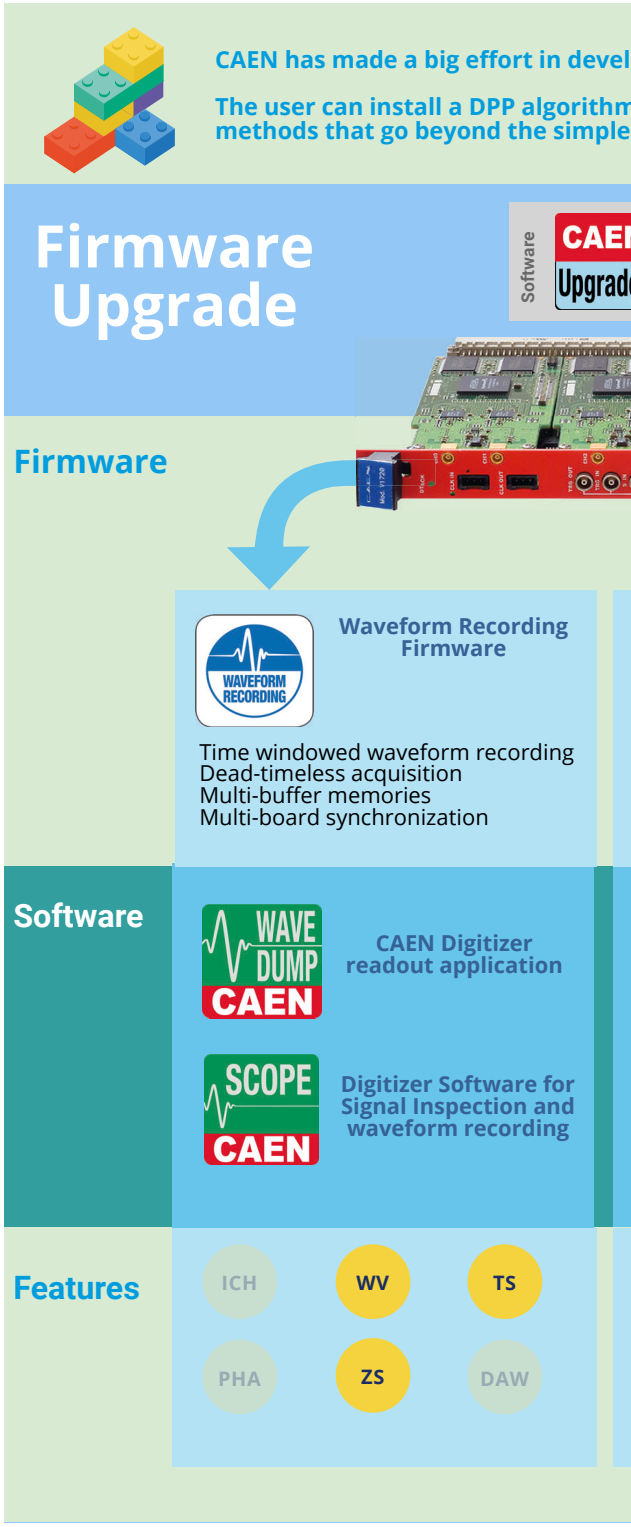
- Waveform recording with no dead-time due to conversion (Flash ADC digitizers)
- Independent channel self-triggering and event acquisition
- On-line digital pulse processing (DPP) algorithms
- Data reduction
- Multi-board synchronization for system scalability
- Communication interfaces with high bandwidth readout

The benefits of the digital approach are great stability and reproducibility, ability to reprogram and adjust the algorithms to the application, ability to preserve the information of the signal along the entire acquisition chain, flexibility, better correction of baseline fluctuation, pile-up, ballistic deficit, etc.. All in one board.

CAEN Digitizer block diagram:

- A motherboard which contains one FPGA for the readout interfaces and the services, and defines the form factor.





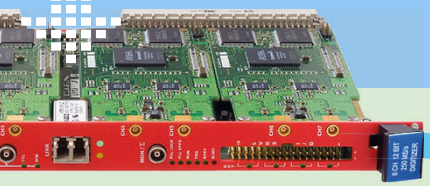
- One or more daughterboards which define the type of digitizer and contain the signal conditioning input stage, the ADCs, the FPGA for the data processing and the memories.

oping algorithms for the Digital Pulse Processing (DPP).

n on the FPGA of the digitizer (firmware upgrade), run it on-line and implement new acquisition waveform recording.

724 Digitizer Family

Firmware Upgrade Tool



Pulse Height Analysis

Digitizer running DPP-PHA firmware becomes a digital replacement of Shaping Amplifier and Peak Sensing ADC (Multi-Channel Analyzer) by means of digital trapezoidal filters.

Dynamic Acquistion Window

Coming Soon

Digitizer running DPP-DAW firmware allows the user to acquire data from each channel independently and to adapt the acquisition window to the real pulse duration (over-threshold).

Multiparametric DAQ Software for Physics Applications

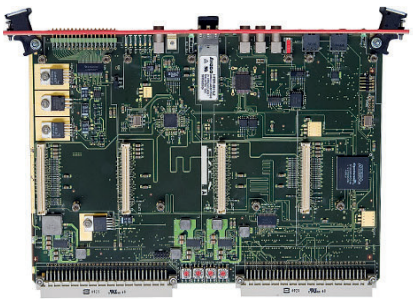
Digital MCA Data Acquisition and Analysis Software

Software interface for DPP-DAW management

DPP-PHA			DPP-DAW		
ICH	WV	TS	ICH	WV	TS
PHA	ZS	DAW	PHA	ZS	DAW

Feature Acronyms Legenda

- **ICH** — (**Independent channels**): the channels can trigger and acquire data independently and can be corelated using a user-defined (anti) coincidence logic criteria
- **WV** — (**Waveforms**): acquisition of a programmable number of ADC samples (raw waveforms)
- **TS** — (**Timestamp**): trigger coarse time stamp with low resolution (10-20 ns)
- **PHA** — (**Pulse Height Analysis**): pulse height of any exponential signals or coming from charge sensitive preamplifier
- **ZS** — (**Zero Suppression**): acquisition of a programmable number of ADC samples with zero suppression
- **DAW** — (**Dynamic Acquisition Window**): acquisition of a dynamically adjusted number of ADC samples



MOTHERBOARD

DAUGHTERBOARD

Technical Specifications

GENERAL

Form Factor

1-unit wide, 6U VME64/VME64X

1-unit wide NIM

154x50x164 mm^3 (WxHxD) Desktop

ANALOG INPUT

Channels

8 channels, single ended (VME)

4/2 channels, single ended (NIM, Desktop)

Impedance

50 Ω (2.25 and 0.5 Vpp), 1 kΩ (10 Vpp)

Connector

MCX

Full Scale Range (FSR)

2.25 Vpp (0.5 or 10 Vpp by ordering code)

Bandwidth

40 MHz

Offset

Programmable DAC for DC offset adjustment. Range: ±1.125 @ 2.25 Vpp, ±0.25 @ 0.5 Vpp, ±5 V @ 10 Vpp

DIGITAL CONVERSION

Resolution

14 bits

Sampling rate

100 MS/s simultaneously on each channel

16.1 MS/s minimum by hardware downsampling (*)

781 kS/s minimum by firmware decimation (8-step programmable)

ADC CLOCK GENERATION

Clock source: internal/external

On-Board PLL provides ADC sampling clock generation from an internal (50 MHz loc. oscillator) or external reference (50 MHz; other options on request) on front panel CLK-IN connector

MEMORY

512 kS/ch or 4 MS/ch Multi-Event Buffer divisible into 1 ÷ 1024 buffers with independent read and write access

Programmable event size and pre- / post-trigger

TRIGGER

Trigger sources

Self-trigger: channel over/under threshold for either Common or Individual (DPP firmware only) trigger generation

External-trigger: Common by TRG-IN or Individual by LVDS connectors (DPP firmware only)

Software-trigger: Common by software command

Trigger propagation

TRG-OUT (VME) / GPO (NIM and Desktop) digital output

Trigger Time Stamp

Waveform recording FW: 31-bit counter, 20 ns resolution, 21 s range (**); 48-bit extension by FW

DPP-PHA Firmware: 30-bit counter, 10 ns resolution, 10 s range; 46-bit extension by firmware; 64-bit extension by software

DPP-DAW Firmware: 31-bit counter, 10 ns resolution, 21 s range; 64-bit extension by software

SYNCHRONIZATION

Clock propagation

Daisy chain (VME only) through CLK-IN/CLK-OUT connectors

One-to-many clock distribution from an external clock source

Clock Cable delay compensation

Acquisition Synchronization

Sync Start/Stop through digital I/O (S-IN, TRG-IN or GPI input, TRG-OUT or GPO output)

External Trigger Time Stamp reset

LVDS I/O (VME only)

16 general purpose LVDS I/Os controlled by FPGA

Busy, Data Ready, Memory full, Individual Trig-Out and other functions can be programmed

An Input Pattern from the LVDS I/Os can be associated to each trigger as an event marker

ANALOG MONITOR (VME only)

12-bit/100 MHz DAC FPGA controlled output with five operating modes: Inspection / Trigger Majority / Test Pulses / Memory Occupancy / Voltage Level

COMMUNICATION INTERFACE

Optical Link

CAEN CONET proprietary protocol, up to 80 MB/s transfer rate

Daisy chainable: it is possible to connect up to 8/32 ADC modules to a single Optical Link Controller (Mod. A2818/A3818)

USB (NIM and Desktop direct, VME via V1718 bridge)

USB 2.0 compliant (transfer rate up to 30 MB/s)

VME

VME 64X compliant

Data transfer mode: BLT32, MBLT64 (70 MB/s using CAEN Bridge), CBLT32/64, 2eVME, 2eSST (up to 200 MB/s)

POWER CONSUMPTIONS

Desktop: 1.7 A @ 12 V (Typ.)

NIM: 3.9 A @ +6 V, 90 mA @ -6 V

VME: 4.5 A @ +5 V, 200 mA @ +12 V, 200 mA @ -12 V

Ordering Options

Code	Description	Form Factor
WDT5724BXAAA	DT5724B - 4 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C20, SE	Desktop
WDT5724CXAAA	DT5724C - 2 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C20, SE	Desktop
WDT5724FXAAA	DT5724F - 4 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, SE	Desktop
WDT5724GXAAA	DT5724G - 2 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, SE	Desktop
WN6724BXAAAA	N6724B - 4 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch,C20, SE	NIM
WN6724CXAAAA	N6724C - 2 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C20, SE	NIM
WN6724FXAAAA	N6724F - 4 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch,C20, SE	NIM
WN6724GXAAAA	N6724G - 2 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, SE	NIM
WV1724EXAAAA	V1724E - 8 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, SE	6U-VME64
WV1724GXAAAA	V1724G - 8 Ch. 14 bit 100 MS/s Digitizer: 512KS/ch, C20, SE	6U-VME64
WVX1724EXAAA	VX1724E - 8 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, SE	6U-VME64X
WPERS0172401	724 Customization - 10Vpp Input Range, SE	ALL
WPERS0172402	724 Customization - 500mVpp Input Range, SE	ALL
WFWDPPTFAAAA	DPP-PHA - Digital Pulse Processing for Pulse Height Analysis (8ch x724)	6U-VME64 VME64X
WFWDPPDAWXEA	DPP-DAW - Digital Pulse Processing with Dynamic Acquisition Window (8ch x724)	6U-VME64 VME64X
WFWDPPTFAD24	DPP-PHA - Digital Pulse Processing for Pulse Height Analysis (4/2ch x724)	Desktop NIM
WFWDPPDAWXED	DPP-DAW - Digital Pulse Processing with Dynamic Acquisition Window (4/2ch x724)	Desktop NIM

Accessories

A2818
PCI CONET Controller

A3818
PCI Express CONET2 Controller

A654
MCX to LEMO Cable Adapter

A659
MCX to BNC Cable Adapter

A317
Clock Distribution Cable

A318
SE to Differential Clock Cable Adapter

AI2700
Optical Fiber Series

Cables for CONET Optical Link Networks

DT4700
Clock Generator and FAN-OUT

(*) The minimum value may depend on the digitizer model, on the firmware or on the hardware downsampling mode (refer to AN6308 - Downsampling measurement with CAEN Digitizer 720/724/740/751 families)

(**) Trigger Logic and Trigger Time Stamp counter operate at 100 MHz (i.e. 10 ns or 1 ADC clock cycle), while the counter value is read at a frequency of 50 MHz (i.e. 20 ns).

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