CAEN Electronic Instrumentation

720 Digitizer Family

8/4/2 Ch. 12-bit 250 MS/s Digitizer

APPLICATIONS

- Nuclear and Particle Physics
- Dark Matter and Astroparticle Physics
- Fast Neutron spectroscopy, Fusion Plasma diagnostics
- Environmental monitoring, Homeland Security

FORM FACTOR

VME64 VME64X NIM DESKTOP

FUNCTIONS

ICH WV TS QDC PSD ZS

A cost- effective, general purpose choice

APPLICATION NOTES

- AN2086
- AN2503
- AN2506
- AN3250
- AN6308
- GD2783
- GD2827

Overview

The 720 is a family of CAEN Waveform Digitizers able to perform basic waveform recording and run online advanced algorithms (DPP) of charge integration and pulse shape discrimination. Data is read by a Flash ADC, 12-bit resolution and 250 MS/s sampling rate, which is well suited for mid-fast signals as the ones coming from liquid or inorganic scintillators coupled to PMTs or Silicon Photomultipliers. In the waveform recording mode, algorithms of zero suppression are also implemented to reduce the data throughput.

The acquisition can be channel independent and it is possible to make coincidence/anti-coincidence logic among different channels and external veto/gating. Multiple boards can be synchronized to build up complex systems.

In case of DPP mode, data can be saved in time-stamped list mode to support higher input rates and improving the throughput performances. Piled-up events can be rejected or saved for offline analysis. The acquisition in DPP mode is fully controlled by the CoMPASS software, which manages the algorithm parameters, builds plots and saves the relevant energy, time, and PSD spectra.

In case of waveform recording mode, the user can take advantage of the CAENScope and WaveDump software to access and save the waveforms. Libraries and demo software in C and LabView are available for integration and customization of specific acquisition systems.

720 family comes in three form factors: VME (8 input channels), NIM (4 or 2 input channels) and Desktop (4 or 2 input channels). The desktop form factor is also included in the Educational Kit for the readout of the SiPMs.

The communication to and from the board is provided through the following interfaces: USB (Desktop and NIM form factors), VMEbus (VME form factor), and Optical Link (all form factors).

Features

- 12-bit @ 250 MS/s
- Analog inputs on MCX coax. connectors
- VME64/VME64X (8 ch.), NIM (4 or 2 ch.) and Desktop (4 or 2 ch.) modules
- 2 Vpp input dynamic range with programmable DC offset adjustment
- Algorithms for Digital Pulse Processing (DPP)
- VME, USB and Optical Link communication interfaces
- Multi-board synchronization features
- Daisy chain capability
- Demo software tools, Control Software for waveform recording and DPP firmware, C and LabVIEW libraries

Firmware	Software	ICH	WV	TS	QDC	PSD	ZS
WAVEFORM RECORDING	WAVE DUMP CAEN, SCOPE CAEN		•	•			•
DPP PSD	CoMPASS CAEN	•	•	•	•	•	

Principle of Operation

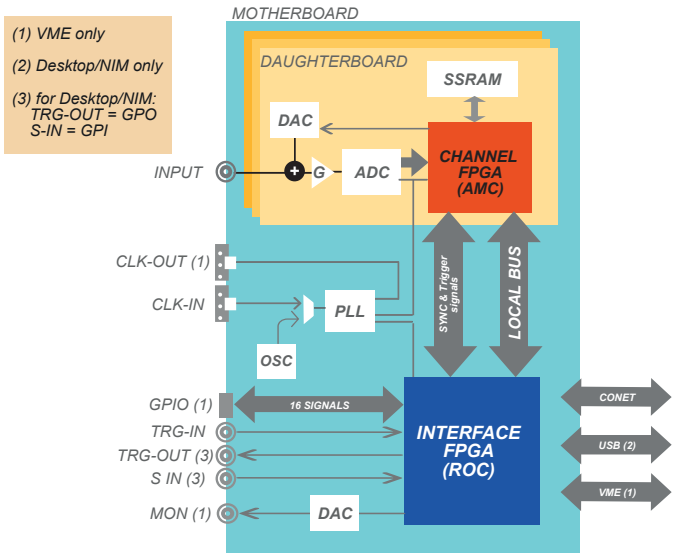
CAEN Waveform Digitizers are devices able to continuously acquire analog input signals, which are sampled by fast ADCs and stored into digital memories where they are avaiable for readout through different communication interfaces (USB, VMEBus, Optical Link). Depending on the FPGA firmware, the digitizer can work like an oscilloscope to acquire raw waveforms, or perform online processing to calculate parameters such as pulse height, charge, time stamp, pulse shape discrimination. In the latter case, the output data is a time-stamped list of parameters. Data reductions and zero suppression algorithms are also available. Digitization in CAEN digitizers is based on two main technics: **Flash ADC** and **Switched Capacitor Arrays**. Flash ADC are the fastest A/D converters, where the sampling and the analog-to-digital conversion are made practically at the same time. Flash ADC are so not affected by dead-time due to conversion. In the Switched Capacitor Arrays, the sampling and the A/D conversion take place at different times, thus introducing a dead-time. Despite of the dead-time, the Switched Capacitor Array Digitizers are able to sample the input pulse at very high frequency, up to 5 GS/s, with high channel density, while the highest Flash ADC frequency is 4 GS/s with a quite low number of channels. If compared to a commercial digital oscilloscope, the waveform digitizer presents a list of differences which make it an advanced instrument for many applications:

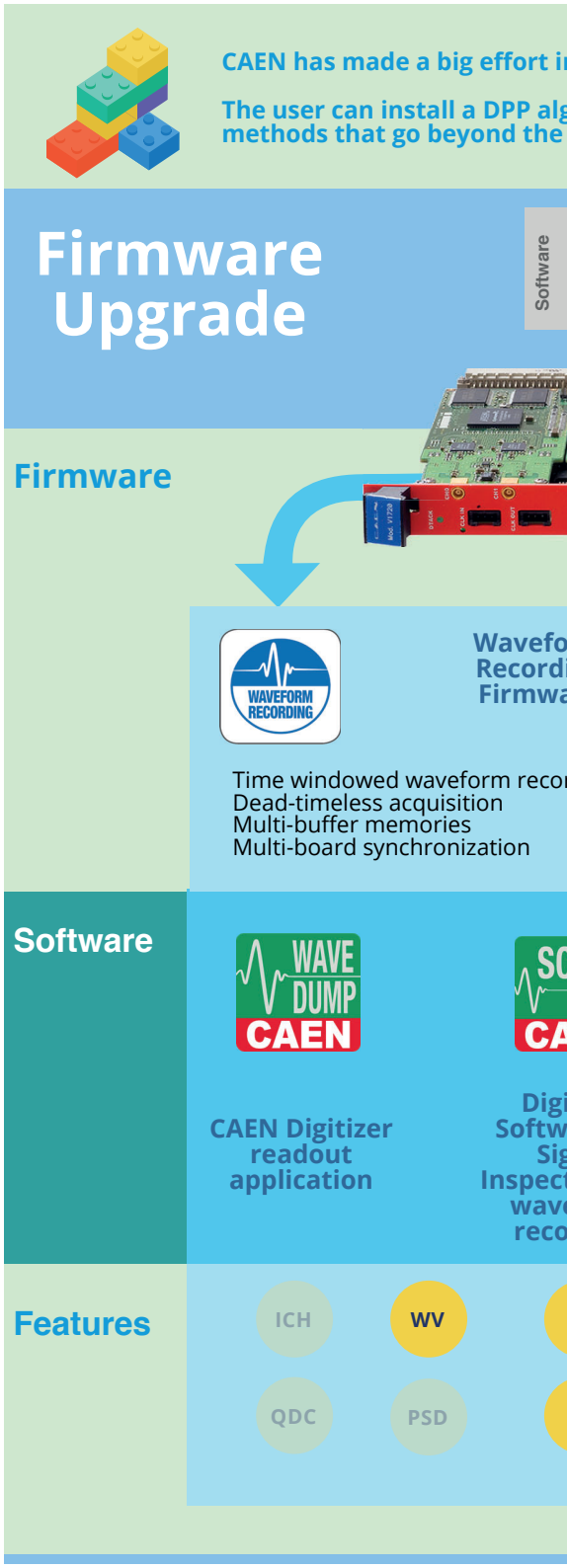
- Waveform recording with no dead-time due to conversion (Flash ADC digitizers)
- Independent channel self-triggering and event acquisition
- On-line digital pulse processing (DPP) algorithms
- Data reduction
- Multi-board synchronization for system scalability
- Communication interfaces with high bandwidth readout

The benefits of the digital approach are great stability and reproducibility, ability to reprogram and adjust the algorithms to the application, ability to preserve the information of the signal along the entire acquisition chain, flexibility, better correction of baseline fluctuation, pile-up, ballistic deficit, etc.. All in one board.

CAEN Digitizer block diagram:

- A motherboard which contains one FPGA for the readout interfaces and the services, and defines the form factor.





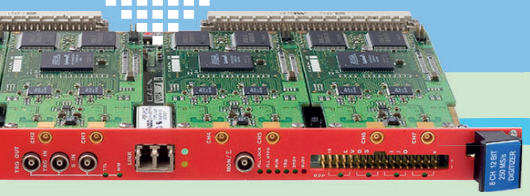
- One or more daughterboards which define the type of digitizer and contain the signal conditioning input stage, the ADCs, the FPGA for the data processing and the memories.

n developing algorithms for the Digital Pulse Processing (DPP).

gorithm on the FPGA of the digitizer (firmware upgrade), run it on-line and implement new acquisition simple waveform recording.

720 Digitizer Family

CAEN Upgrader — Firmware Upgrade Tool



Pulse Shape Discrimination

DPP PSD

Digitizer running DPP-PSD firmware becomes a digital replacement of dual gate QDC, discriminator and gate generator.

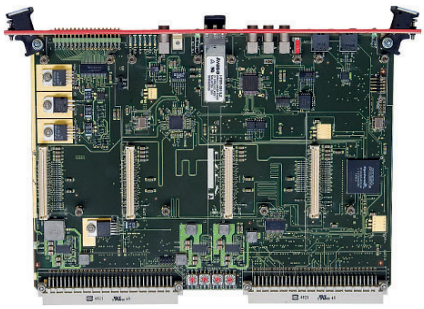
CoMPASS CAEN

Multiparametric DAQ Software for Physics Applications

ICH WV TS QDC PSD ZS

Feature Acronyms Legenda

- **ICH** — (**Independent channels**): the channels can trigger and acquire data independently and can be corelated using a user-defined (anti) coincidence logic criteria
- **WV** — (**Waveforms**): acquisition of a programmable number of ADC samples (raw waveforms)
- **TS** — (**Timestamp**): trigger coarse time stamp with low resolution (10-20 ns)
- **QDC** — (**Charge to Digital Converter**): gated integrator (charge)
- **PSD** — (**Pulse Shape Discrimination**): particle discrimination via double gated integration
- **ZS** — (**Zero Suppression**): acquisition of a programmable number of ADC samples with zero suppression



MOTHERBOARD

DAUGHTERBOARD

Technical Specifications

GENERAL

Form Factor
1-unit wide, 6U VME64/VME64X
1-unit wide NIM
154x50x164 mm^3 (WxHxD) Desktop

ANALOG INPUT

Channels
8 channels, single ended (VME)
4/2 channels, single ended (NIM, Desktop)

Impedance
50 Ω

Connector
MCX

Full Scale Range (FSR)
2 Vpp

Bandwidth
125 MHz

Offset
Programmable DAC for DC offset adjustment. Range: ±1 V

DIGITAL CONVERSION

Resolution
12 bits

Sampling rate
250 MS/s simultaneously on each channel
29.4 MS/s minimum by hardware downsampling (*)

ADC CLOCK GENERATION

Clock source: internal/external
On-Board PLL provides ADC sampling clock generation from an internal (50 MHz loc. oscillator) or external reference (50 MHz or 62.5 MHz; other options on request) on front panel CLK-IN connector.

MEMORY

1.25 MS/ch or 10 MS/ch Multi-Event Buffer divisible into 1 ÷ 1024 buffers with independent read and write access.
Programmable event size and pre- / post-trigger

TRIGGER

Trigger sources
Self-trigger: channel over/under threshold for either Common or Individual (DPP firmware only) trigger generation
External-trigger: Common by TRG-IN or Individual by LVDS connectors (DPP firmware only)
Software-trigger: Common by software command

Trigger propagation
TRG-OUT (VME) / GPO (NIM and Desktop) digital output

Trigger Time Stamp
Waveform recording firmware: 31-bit counter, 16 ns resolution, 17 s range (**); 48-bit extension by firmware
DPP-PSD Firmware: 32-bit counter, 4 ns resolution, 17 s range; 47-bit extension by firmware; 64-bit extension by software

SYNCHRONIZATION

Clock propagation
Daisy chain (VME only) by CLK-IN/CLK-OUT connectors
One-to-many clock distribution from an external clock source
Clock Cable delay compensation

Acquisition Synchronization
Sync Start/Stop by digital I/O (S-IN, TRG-IN or GPI input, TRG-OUT or GPO output)
External Trigger Time Stamp reset

LVDS I/O (VME only)

16 general purpose LVDS I/Os controlled by FPGA
Busy, Data Ready, Memory full, Individual Trig-Out and other functions can be programmed
An Input Pattern from the LVDS I/Os can be associated to each trigger as an event marker

ANALOG MONITOR (VME only)

12-bit/125 MHz DAC FPGA controlled output with four operating modes: Trigger Majority / Test Pulses / Memory Occupancy / Voltage Level

COMMUNICATION INTERFACE

Optical Link
CAEN CONET proprietary protocol, up to 80 MB/s transfer rate
Daisy chainable: it is possible to connect up to 8/32 ADC modules to a single Optical Link Controller (Mod. A2818/A3818)

USB (NIM and Desktop direct, VME via V1718 bridge)
USB 2.0 compliant
Transfer rate up to 30 MB/s

VME
VME 64X compliant
Data transfer mode: BLT32, MBLT64 (70 MB/s using CAEN Bridge), CBLT32/64, 2eVME, 2eSST (up to 200 MB/s)

POWER CONSUMPTIONS

Desktop: 1.5 A @ 12 V (Typ.)
NIM: 2.9 A @ +6 V, 90 mA @ -6 V
VME: 4 A @ +5 V, 200 mA @ +12 V, 200 mA @ -12 V

Ordering Options

Code	Description	Form Factor
WDT5720BXAAA	DT5720B - 4 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE	Desktop
WDT5720CXAAA	DT5720C - 2 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE	Desktop
WDT5720DXAAA	DT5720D - 4 Ch. 12 bit 250 MS/s Digitizer: 10MS/ch, C20, SE	Desktop
WDT5720EXAAA	DT5720E - 2 Ch. 12 bit 250 MS/s Digitizer: 10MS/ch, C20, SE	Desktop
WN6720BXAAAA	N6720B - 4 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE	NIM
WN6720CXAAAA	N6720C - 2 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE	NIM
WN6720DXAAAA	N6720D - 4 Ch. 12 bit 250 MS/s Digitizer: 10MS/ch, C20, SE	NIM
WN6720EXAAAA	N6720E - 2 Ch. 12 bit 250 MS/s Digitizer: 10MS/ch, C20, SE	NIM
WV1720EXAAAA	V1720E - 8 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE	6U-VME64
WV1720GXAAAA	V1720G - 8 Ch. 12 bit 250 MS/s Digitizer: 10MS/ch, C20, SE	6U-VME64
WVX1720EXAAA	VX1720E - 8 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE	6U-VME64X
WVX1720GXAAA	VX1720G - 8 Ch. 12 bit 250 MS/s Digitizer: 10MS /ch, C20, SE	6U-VME64X
WFWDPPNGAA20	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (8ch x720)	6U-VME64 VME64X
WFWDPPNGAD20	DPP-PSD Digital Pulse Processing for Pulse Shape Discrimination (4/2ch x720)	Desktop NIM

Accessories

A2818
PCI CONET Controller

A3818
PCI Express CONET2 Controller

A654
MCX to LEMO Cable Adapter

A659
MCX to BNC Cable Adapter

A317
Clock Distribution Cable

A318
SE to Differential Clock Cable Adapter

AI2700
Optical Fiber Series

Cables for CONET Optical Link Networks

DT4700
Clock Generator and FAN-OUT

(*) The minimum value may depend on the digitizer model, on the firmware or on the hardware downsampling mode (refer to AN6308 - Downsampling measurement with CAEN Digitizer 720/724/740/751 families)

(**) Trigger Logic and Trigger Time Stamp counter operate at 125 MHz (i.e. 8 ns or 1/2 ADC clock cycles), while the counter value is read at a frequency of 62.5 MHz (i.e. 16 ns).

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