CAEN
Tools for Discovery

A1702 - DT5702

32 Channel Silicon Photomultipliers Readout Front-End Board

Readout SiPM arrays for veto system of Liquid Argon Neutrino Experiments

Features

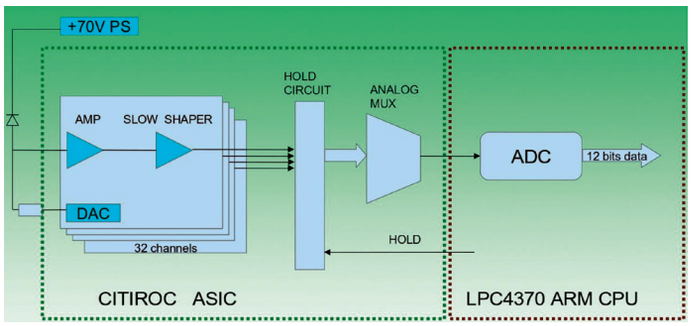
- Provides bias voltage in the range of 20-90 V individually adjustable for each of 32 SiPMs
- Amplification and shaping of the SiPMs output pulse on each of 32 channels
- Discrimination of shaped signal at configurable level from 0 to 50 SiPMs photo-electrons
- Providing basic coincidence of signals from each pair of adjacent even-odd channels
- Allows to trigger only on events that happen in coincidence with event in a group of other A1702 - DT5702 (event validation)
- Formation of the trigger for digitization of the signal amplitude
- Formation of the time stamp with respect to an input reference signal with 1 ns accuracy
- Digitization of signal amplitude of all 32 channels
- Data buffering
- Efficient back-end communication based on Ethernet standard
- Firmware upgrade via backend Ethernet link

Overview

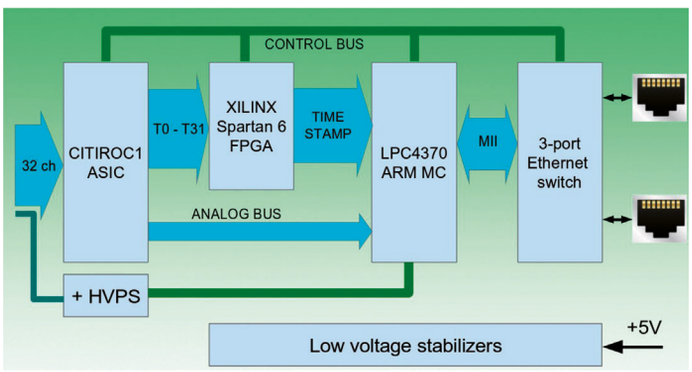
The A1702 - DT5702 Front-End Board is a custom design developed by the Albert Einstein Center for Fundamental Physics of the University of Bern for the readout of SiPM arrays used in the veto system of Liquid Argon Neutrino Experiments.

Given the increasing use of SiPM in Physics Experiments, this solution can become a valid approach for a variety of applications thanks to its flexibility and channel density.

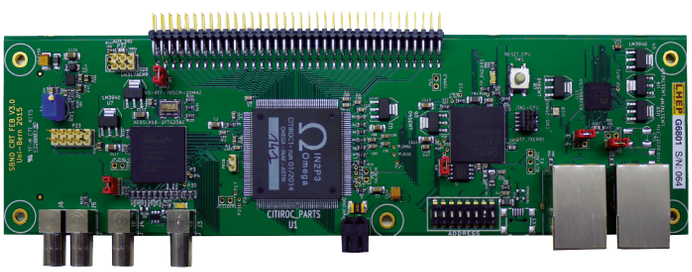
The analog input signal is processed by CITIROC a 32-channel ASIC from Weeroc. For each channel the chip provides charge amplifier with configurable gain, fast shaping with the peaking time of 15 ns and slow shaping with configurable peaking time in the range of 12.5 ns to 87.5 ns. Signals from the fast shapers are discriminated (programmable threshold) and produce digital signals (T0-T31) for event triggering. These 32 signals are routed to XILINX Spartan-6 FPGA chip, where the basic input coincidence and event triggering logic is realized. The analog signal for all channels can be stored in the ASIC Sample-and-Hold (S/H) circuit and multiplexed to a single analog output. This output is routed to the ADC (part of NXP LPC4370 ARM micro-controller chip).



Block-scheme of analog signal processing circuit.



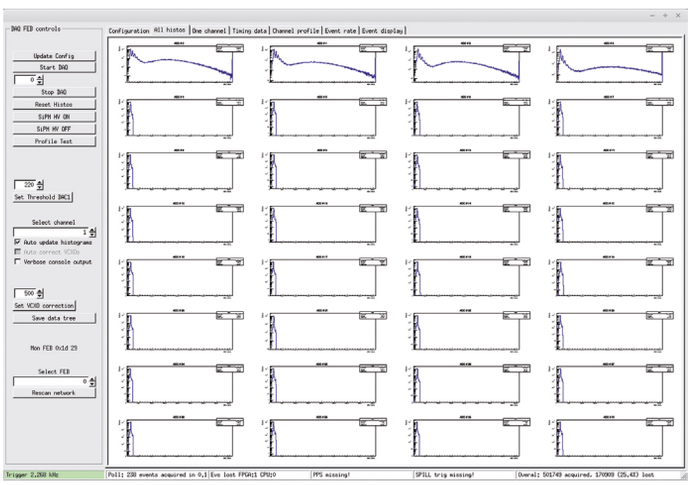
Block-scheme of the A17027 - DT5702.



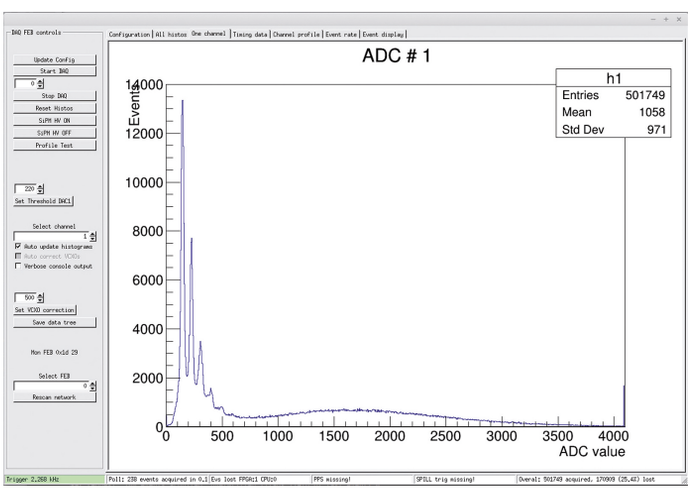
A1702 - Front-End Board.

Software

A simplified data acquisition program (FEBDAQMULT with GUI) is available in order to test performance of A1702-DT5702 boards. The code may serve as a template for more dedicated experiment-optimized DAQ software. The program is a CERN ROOT script, tested on Linux OS.



FEBDAQMULT GUI, 32-histograms per FEB summary display tab activated.



FEBDAQMULT GUI, single histogram tab activated.

All CAEN Control Software is available for free download on the web site.

Ordering Option

Code	Description
WA1702XAAAAA	A1702 - 32-channel SiPM readout Front-End Board
WDT5702XAAAA	DT5702 - 32-channel SiPM readout Front-End Board BOXED

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