Viareggio
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Introduction

The cores of x5202 boards are the 2 Citiroc-1A ASIC chips, as shown in Fig. 1. Citiroc-1A is a 32-channel front-end ASIC designed to readout SiPMs for scientific instrumentation applications. This ASIC allows the user to trigger down to $\frac{1}{3}$ photo-electron and provides the charge measurement with a good noise rejection and 1% linearity up to 2500 photo-electrons.

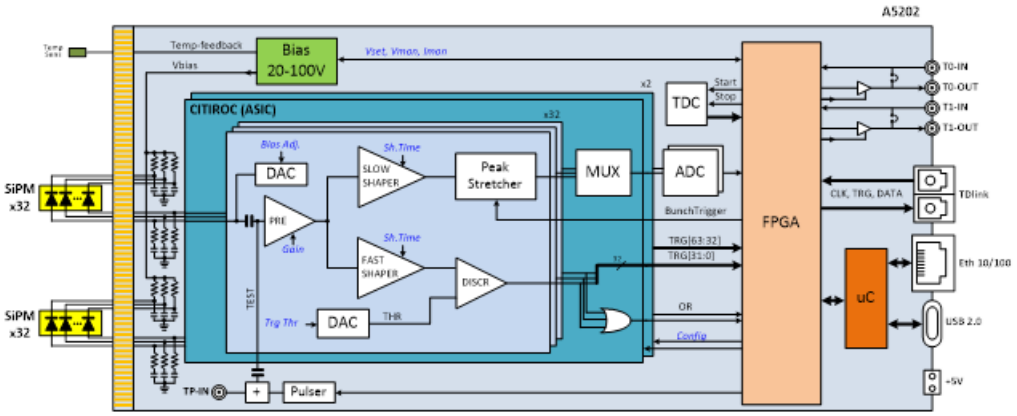

Fig. 1: 5202 Block Diagram.

Each of the 32 readout channels available in the chip integrates a classical readout chain made of Preamplifier (one for Low Gain and one for High Gain), Fast and Slow Shaper, a trigger line with a timing resolution of about $\sim$ 300 ps, a Peak Detector circuit and analog output MUX. Moreover, for each channel, a block for the SiPM bias regulation is available. A scheme of the chip is shown in Fig. 2.

The board has three different acquisition modes:

- Timing Mode
- Counting Mode
- Spectroscopy Mode

In Timing Mode and in Counting Mode each channel saves independently the time-trigger (Timestamp + Time over Threshold) or count information, coming from the Fast Shaper line, in a dedicated list.
In Spectroscopy Mode the signal coming from the SiPMs passes through the Slow Shaper line to generate the energy info. The Peak Stretcher is armed by the Bunch Trigger, which is common for all channels. Once armed, the Peak Stretcher follows the Slow Shaper signal and keeps the peak value. The “Hold” signal freezes the Peak Detector, which becomes irresponsive to any further pulses while waiting for the analog to digital conversion, as shown in Fig. 3. When all 64 channels have been converted, the “Reset” signal clears the Peak Stretcher and makes the chain ready for the acquisition of a new trigger.

The BunchTrigger may have different sources:

- external trigger connected to T0-IN or T1-IN (LEMO connectors)

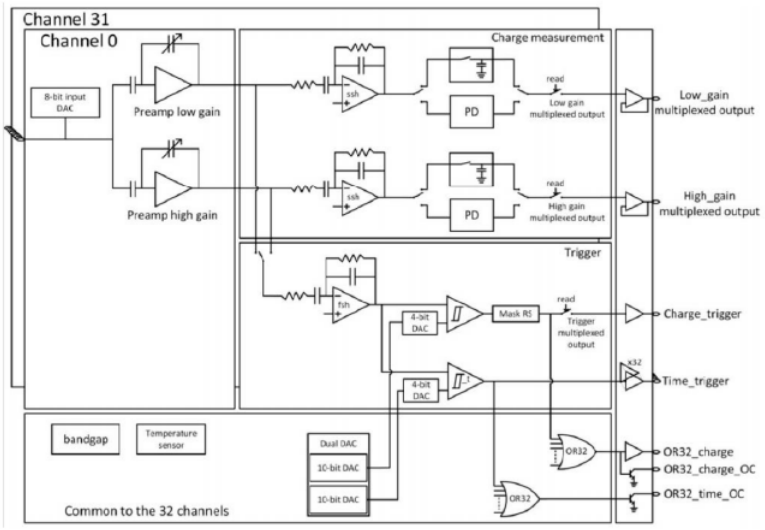

Fig. 2: Scheme of the Citiroc-1A ASIC chips, core of the x5202 boards.

- internal "T-OR", that is a signal produced by the Citiroc, making the logic "OR" of the channel self-triggers (fast shaper + discriminator)
- internal TLOGIC, generated by the FPGA that combines the self-triggers with a programmable logic (e.g. majority, coincidences, etc…).

In case of multiple boards, it is possible to propagate the internal trigger (either T-OR or TLOGIC) to T0-OUT or T1-OUT (LEMO outputs) and combine them externally to generate a "global system trigger" that eventually feeds the x5202 boards as an external trigger. It is also possible to implement a "wired OR" through the T0 (or T1) input/output: each board can drive a logic "1" to assert the trigger; all the boards connected in daisy chain will read "1" at the input. If no board is driving the line (high-Z), the 50 ohm termination keeps it to a logic "0". See the User Manual [**1**], section 8.4.6. for further details.
The trigger latency changes, depending on the selected trigger source.

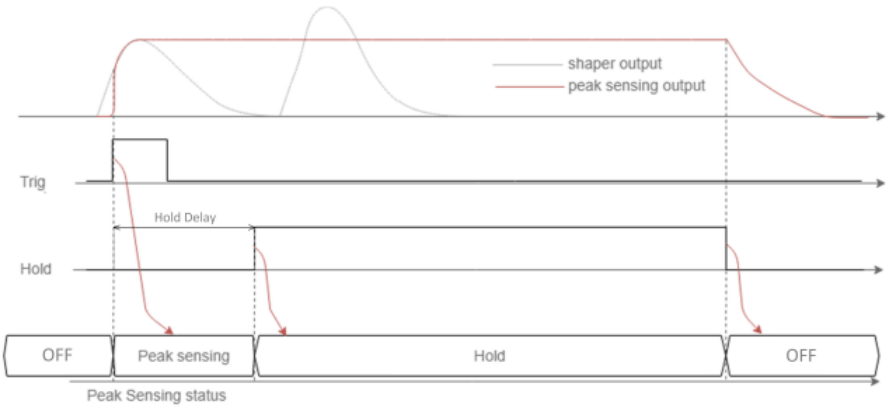

Fig. 3: CITIROC Peaking Sensing sequence.

The timing of the Bunch Trigger is crucial to sample the peak correctly: if it arrives after the peak of the slow shaper, the analog value converted by the ADC will be an underestimation of the actual peak height. Furthermore, the converted

value will be affected by the jitter of the trigger signal, with significant degradation of the amplitude resolution. The shaping time of the Slow Shaper can be programmed, therefore it is possible to counterbalance a longer trigger latency by increasing the peaking time of the Slow Shaper (up to 82.5 ns), even though this might result in a worse amplitude resolution since the best shaping time for the SiPM detectors is typically 25 ns. The best trade-off between these two components must be found according to the detector characteristics.

The aim of this test is to characterize the behavior of the Peak Sensing ADC as a function of the trigger latency, using different configurations for the trigger and for the Shaping Time (board in Spectroscopy Mode).

Experimental Setup

The setup is made of the following parts:

- DT5202 (PID 22686)
- A5251 (input adapter for MPPC matrix)
- Hamamatsu SiPM matrix S13361-3050AE-08
- LED pulser SP5601
- N108A (Cable Delay Line)

The LED driver generates a periodic light pulse (about 3 kHz) that illuminates the SiPM matrix. The LED driver also generates a trigger signal that is issued a few tens of ns before the light pulse. In the first test, the trigger from the LED driver, connected to the T0-IN, is used as a Bunch Trigger for the acquisition: this is a simple and safe way to guarantee that the Peak Detector converts all and only the pulses generated by the LED driver and not any other pulse due to the dark count or background noise. The spectrum acquired with the external trigger from the LED driver is the reference for the other tests. The amplitude of the light pulse has been set to get a single photon spectrum from a central pixel (Channel 50 of the DT5202), showing about 20 photon peaks (max height at about 10 photons). Fig. 4 shows the average pulse height (which is proportional to the emitted electron charge) acquired by each pixel of the matrix. The central spot is due to the light coming from the optical fiber connected to the LED driver.

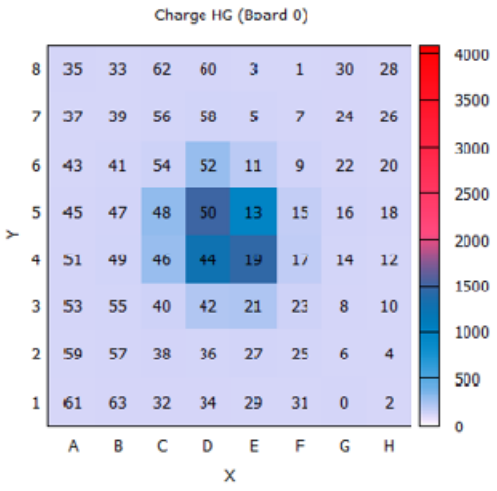

Fig. 4: HG charge-2D histogram.

Several tests have been run to estimate the energy resolution with different trigger sources and shaping times. The main settings for the acquisitions are:

- Acquisition mode = SPECTROSCOPY
- HG Gain = 50 (LG is not used)
- Shaping Time = 25 ns (unless otherwise indicated)
- Hold Delay = 100 ns
- HV Bias = 54 V
- All channels are enabled
- Preset Time = 30 s (run duration)

Study of the Energy Resolution of the DT5202 Board

Staircase

Before running the acquisition with the LED driver, it is important to acquire the "staircase" of the observed SiPM pixel (Channel 50). That will help to select a Discriminator threshold that will cut the noise and keep only the signal coming from the LED Driver. The plot in Fig. 5 shows the count rate of the self-trigger as a function of the discriminator threshold. The steps due to the single photon counting are clearly visible. The region below 175 threshold value unit (from now tvu) is noise. From 175 to 190 tvu is the flat region corresponding to "one photon" counting, etc...

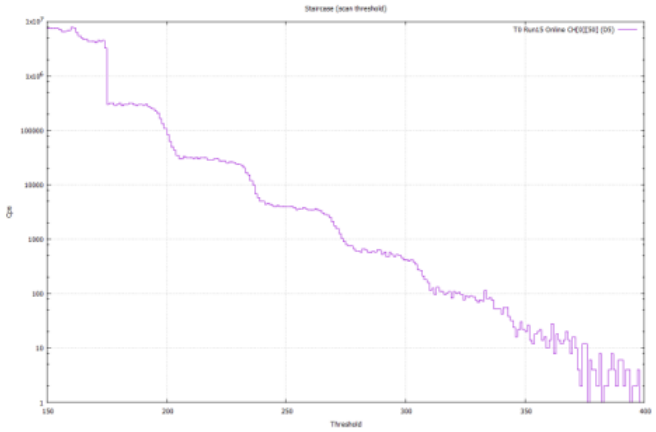

Fig. 5: Staircase of channel 50 of the DT5202.

Results

External Trigger

In the first test (used as reference for the following) the Bunch Trigger is generated by the LED pulser and is connected to the T0-IN of the DT5202. Results are shown in Fig. 6. The distribution is centred in about bin 1000 of the PHA High Gain histogram. The resolution allows to recognize single photoelectrons (the first peak represent one photon counts, etc..)

Internal OR of 64 Channels

In the second test, the Bunch Trigger is the T-OR signal, that is the logic OR of the 64 self-triggers generated by the Citiroc chip by means of the fast shapers and discriminators. The threshold of the discriminator is set to 300 tvu, which

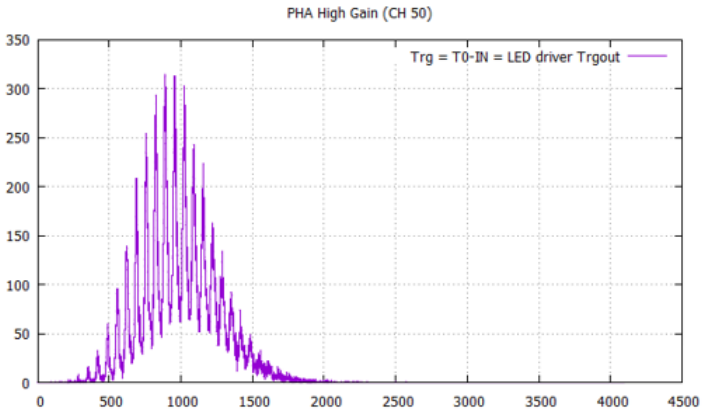

Fig. 6: Energy Spectrum with the LED Driver Trigger as BunchTrigger.

corresponds to about 4 photons, according to the staircase (as shown in Fig. 5). Therefore, the T-OR signal can be generated, in some cases, by the dark count of any pixel in the SiPM matrix. As a consequence, some events are not correlated to the light pulse of the LED driver and channel 50 may convert a "zero" signal. This explains the high peak on the left of Fig. 7, at the pedestal position.

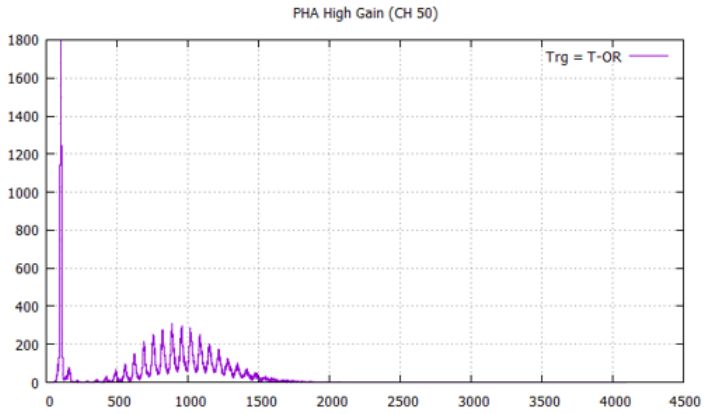

Fig. 7: Energy Spectrum with the OR of 64 channels as BunchTrigger.

Internal OR of 64 Channels with Higher Discriminator Threshold

The test has been repeated with a discriminator threshold set to 450 tvu, which is above the dark count noise (see figure 5). The acquired spectrum in Fig. 8, is almost equal to the reference shown in Fig. 6.

Internal Majority Trigger

In this test, the BunchTrigger is issued when there are at least 2 channels firing at the same time. The threshold is still 300 tvu, but the probability to have a dark count pulse of 4 photoelectrons on two different channels at the same time is extremely low, so the trigger is only given by the light pulses produced by the LED driver hitting two pixels. In fact the results shown in Fig.9 are quite similar to what shown in the reference test, Fig.6. This test shows that the time the

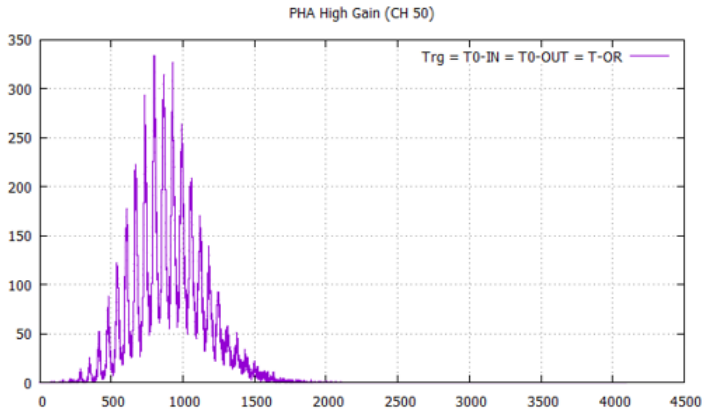

Fig. 8: Energy Spectrum with the OR of 64 channels as BunchTrigger with a Discriminator threshold of 450 tvu.

FPGA takes to calculate the majority, which results in higher latency, is still irrelevant and there is no visible effect in the calculation of the amplitude of the signal by the Peak Stretcher.

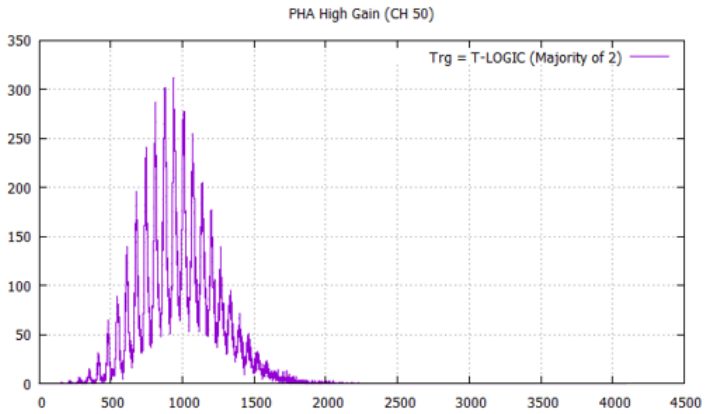

Fig. 9: Energy Spectrum with the Internal Majority of 2 channels as BunchTrigger.

External Majority Trigger

This test is similar to the one described in the previous section, with the only difference that the TLOGIC signal, that is the Majority of 2 calculated by the FPGA, is outputted to T0-OUT externally, connected to T0-IN with a 5 ns cable, and finally the T0-IN is used as a trigger for the acquisition. As shown in Fig. 10, the trigger latency is too high and the acquired spectrum is significantly affected: the average peak height (centroid) is reduced and the amplitude resolution is so degraded that the single photoelectrons peaks are completely smeared out. This means that the sum of the delays (majority calculation + T0-OUT output delay + external cable + T0-IN input delay) is too high.

External OR of 64 Channels

Similar to what was done in section ”External Majority Trigger (TLOGIC)”, this test shows the effect of the propagation of the T-OR signal through the T0-OUT and T0-IN of the DT5202 board. An external cable of 5 ns is used to connect T0-OUT

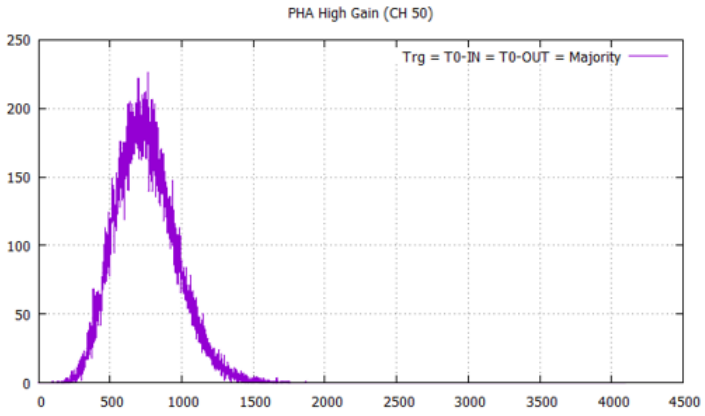

Fig. 10: Energy Spectrum with the Majority of 2 channels via T0-OUT and T0-IN as BunchTrigger.

to T0-IN. As shown in Fig. 11, there is no visible effect in the acquired spectrum between this acquisition and the one described in section ”Internal OR of 64 Channels”, showing that the T-OR logic is faster than the Majority logic.

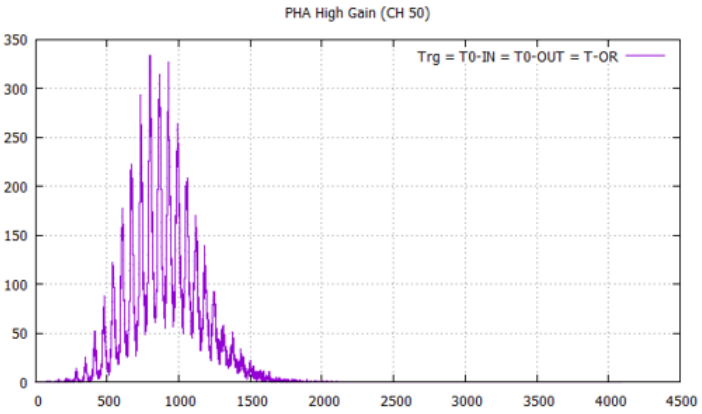

Fig. 11: Energy Spectrum with the External OR of 64 channels via T0-OUT and T0-IN as BunchTrigger.

External OR of 64 Channels (Different Delays)

The effect of the increasing propagation delay between T0-OUT and T0-IN has been studied using the programmable external delay line N108A. The Discriminator threshold has been set to 450 tvu in order to remove the pedestal, as shown in section ”Internal OR of 64 Channels with Higher Discriminator Threshold”. Plots in Fig. 12 show the progressive degradation of the resolution (peak smearing) as well as the lost of gain, due to the incorrect peak sampling (armed on the falling edge of the slow shaper). The spectrum starts to lose resolution when the external delay is 10 ns, even though it is possible to have the single photon count resolution up to 14 ns. For higher delay values, the resolution doesn’t allow to resolve the single photon counts, but the amplitude (position of the centroid) is still at the same value. For delays > 64 ns the board is not able to detect any signal.

External Trigger with different Shaping Times

The variation of the energy resolution has been studied as a function of the shaping time of the Slow Shaper. In general, the energy resolution decreases for longer shaping times; on the other hand, higher shaping times should tolerate better

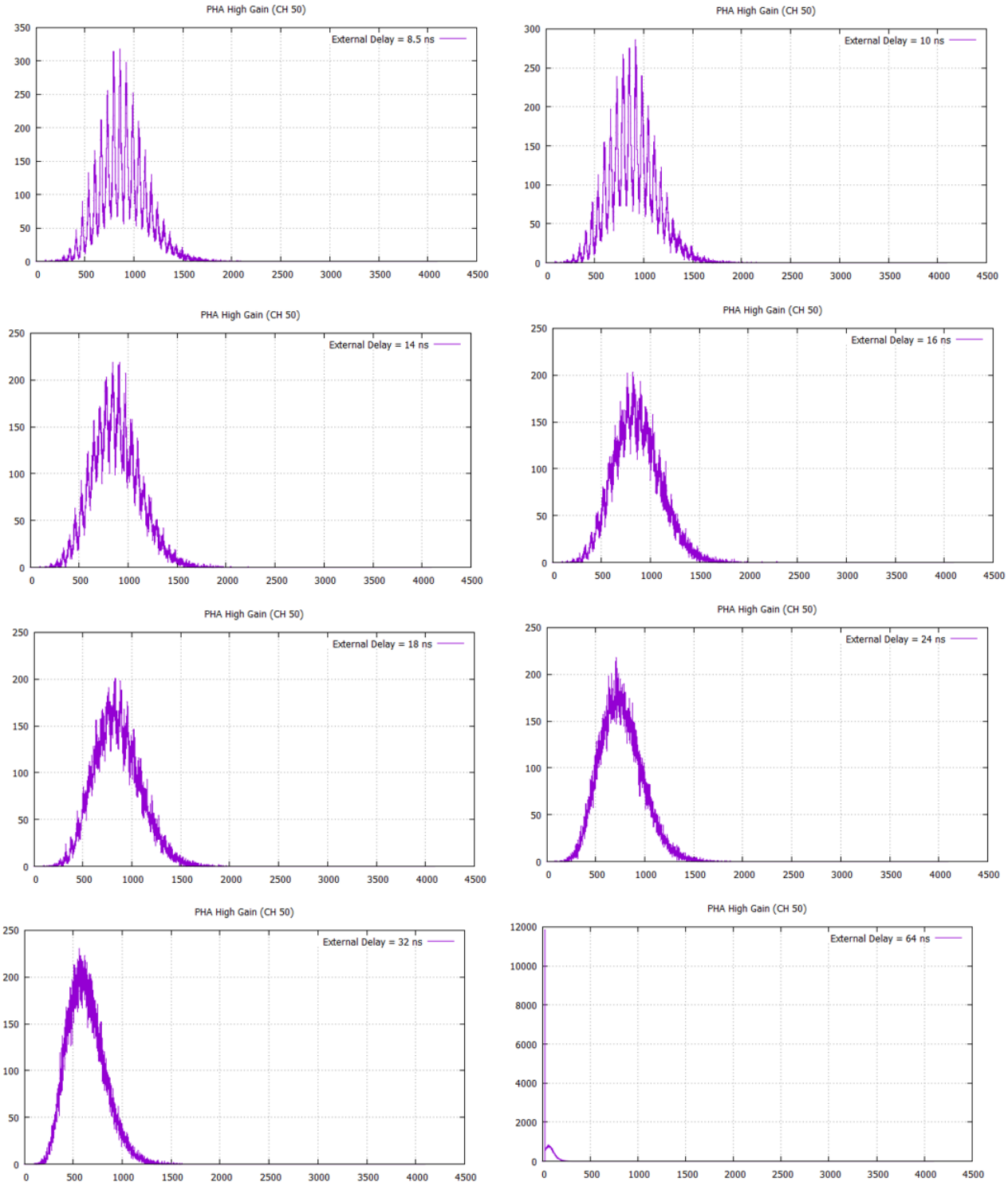

Fig. 12: Energy spectrum with external OR of 64 channels as BunchTrigger with different external delays.

the trigger latency, since there is a longer peaking time. The plots in Fig. 13 show the spectra taken at different shaping times. The Bunch Trigger is the TRG-OUT of the LED driver connected to the T0-IN of the DT5202. Typically, the fastest shaping time (12.5 ns) tends to oscillate and it is not recommended, although in this test the effect is not visible. Shaping time at 25 ns is typically the best setting, and it has been used in all the previous runs. The loss of the single photon

resolution at higher shaping times is well visible, but it is not as bad as observed when the trigger arrives after the peaking time. Therefore, choosing a longer shaping time when the trigger latency is long, is certainly beneficial.

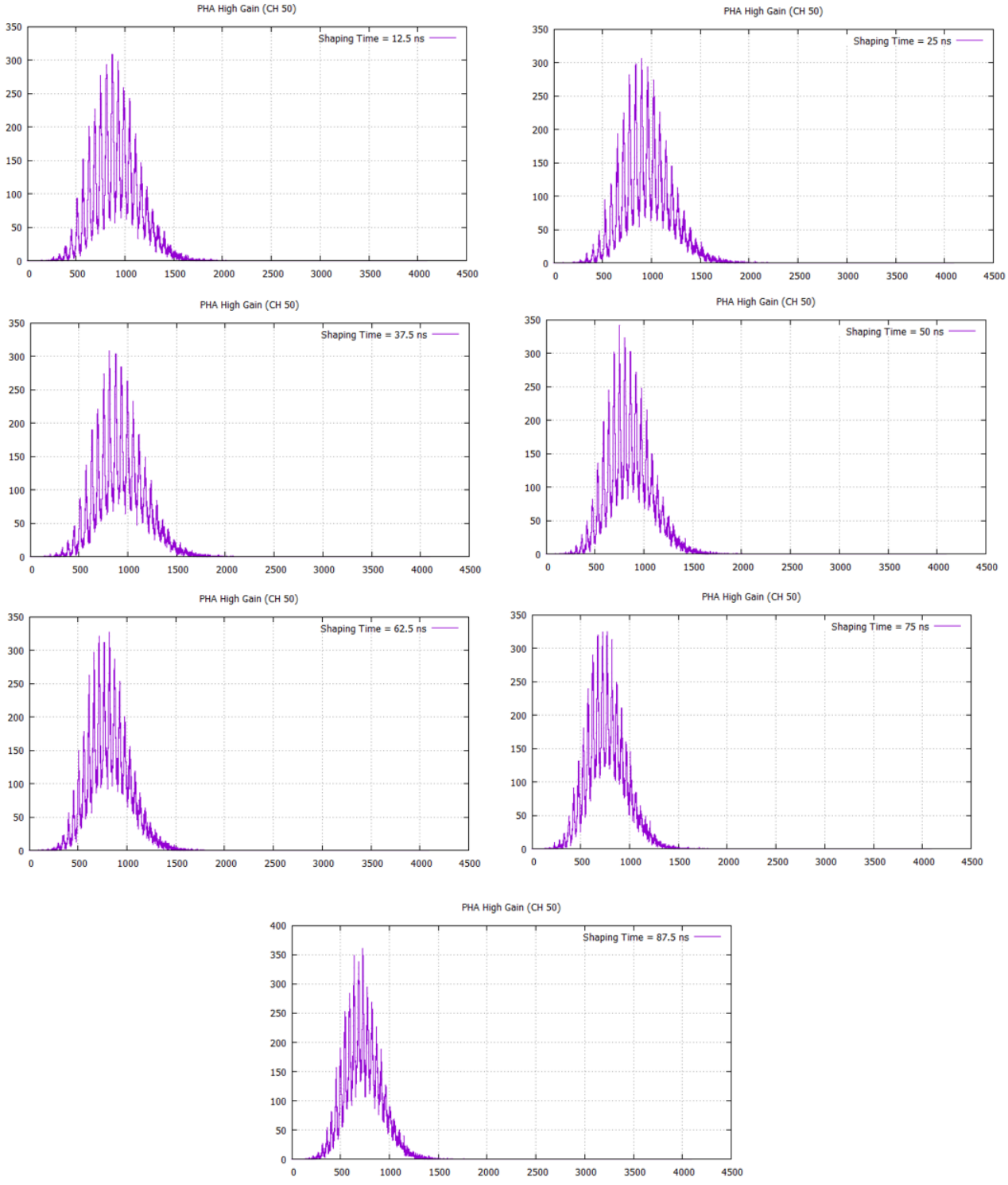

Fig. 13: Energy spectrum at different shaping times with the LED Driver External Trigger as BunchTrigger.

External OR with Longest Shaping Times

In this paragraph we show the effects of the trigger latency with the longest shaping time (82.5 ns). The external OR of 64 channels with a programmable delay was used as BunchTrigger. As shown in Fig. 14, board keeps the single photo-electrons resolution even with a trigger latency of 64 ns, with respect to the 14 ns measured in section ”External OR of 64 Channels (Different Delays)” with a shaping time of 25 ns.

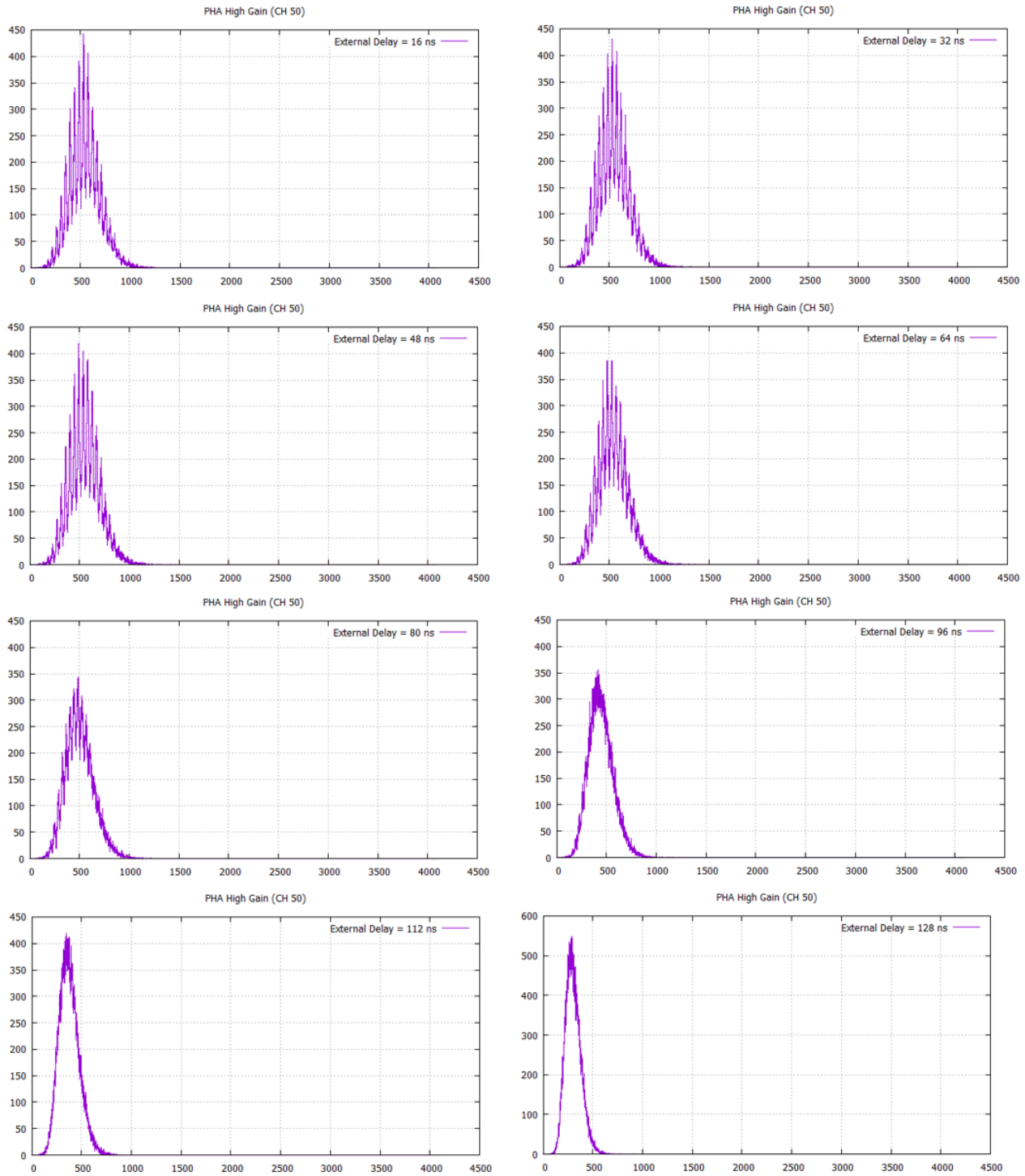

Fig. 14: Energy spectrum with External OR of 64 Channels as BunchTrigger and Shaping Time of 82.5 ns.

Conclusions

The effect of the trigger latency has been tested in various conditions. The use of the T-OR signal generated by the CITIROC chips as the basis for a more complex multi-board trigger logic is possible, even in the case where an external trigger logic introduces an extra delay of some tens of ns. For a shaping time of 25 ns, that is the typical setting for SiPM, the maximum external delay is rather small ($\sim$14 ns), but it can be increased up to $\sim$64 ns by selecting the highest shaping time (82.5 ns), still keeping the single photoelectrons resolution. Depending on the detector characteristics, the best trade-off between shaping time and immunity to the increasing trigger latency must be found. It was not possible to test the Wired-OR logic because a second SiPM matrix was missing, but the results of this test lead us to believe that it works properly, at least for a small number of boards connected in daisy chain.

References

[**1**] UM7945 – FERS-5200 A5202/DT5202 User Manual.

CAEN
Tools for Discovery

CAEN SpA
Via Vetraia 11
55049 – Viareggio Italy
Tel +39.0584.388.398
Fax +39.0584.388.959

info@caen.it www.caen.it

www.caen.it