Application Note AN6308
Downsampling measurements with CAEN Digitizer 720/724/740/751 families

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Abstract

In this Application Note we present the results of measurements performed with CAEN Digitizers families 720, 724, 740, 751, in order to evaluate the possibility of reaching lower sampling frequencies.
The reasons for downsampling are a wide variety, depending on the use of the Digitizer for a particular application. However the simplest reason for downsampling is to reduce the amount of data throughput.
We explored measurements with boards equipped with Waveform Recording or Digital Pulse Processing (DPP) firmware. Using different configurations we found out the clock frequencies for which the digitizer has a proper operating. In particular, we verified the coherent sampling of the input signal and the stability of the data acquisition for each tested clock frequency.

Introduction

Some of the CAEN Digitizers (as 720,724,740,751 series) provide the possibility to operate in downsampling mode. There are two ways to operate the Digitizer at sampling frequencies lower than the nominal one:

- The **decimation**, operating at the **firmware level**, for 724 and 740 series with Waveform Recording and DPP (x740D) firmware. The decimation is a firmware option based on the programmability of a decimation factor n. During the acquisition, the firmware processes the digitized input waveforms calculating an averaged value of the "decimated" 2^n consecutive samples. The self-trigger is then issued as soon as the averaged value exceeds the programmed threshold. Software trigger and external trigger are not affected by decimation option. While *the real sampling frequency doesn't change*, the decimation effect is to **change the rate of the data written into the digitizer memory**. Being a firmware feature it is guaranteed a proper operation of the Digitizer even with high decimation factors.

- The **hardware downsampling**, realized in three different ways:
  - basing on the **internal** 50 MHz oscillator as clock reference, program the PLL to provide different clock frequencies to the ADCS (see later for more details).
  - basing on an **external** reference clock, program the PLL as in the previous case (not verified because this option is used to synchronize the ADCs with an external signal and not for downsampling).
  - basing on an external reference clock, program the PLL to drive that signal directly to the clock frequency of the ADCs (**Bypass mode**).

The hardware downsampling, since the ADC sampling frequency is really lowered, does not guarantee a proper operating of the board at all the theoretical reachable frequencies. This is the reason why we decided to investigate the operation of the hardware-firmware-software chain under hardware downsampling conditions, trying to understand the minimum sampling frequency at which data acquisition is still possible.

In this Application Note we report the results of measurements performed with CAEN Digitizers V1720, V1724, V1740, V1740D and V1751, equipped with the Waveform Recording firmware and/or with a DPP firmware. Although **the decimation is the recommended way to reach low sampling frequencies**, that possibility is supported only by x724, x740 and x740D boards equipped with Waveform Recording or DPP firmware (see [**1**] and [**2**] for more details). Moreover the decimation, as explained above, is not a true downsampling mode. For these reasons it is useful to understand the performances of CAEN Digitizers, when running at a lower frequency with respect to the default sampling.

In the following we report all the results of measurements performed with our particular setup. We will highlight, for each board, the sampling frequencies which passed the data acquisition test. The failure conditions are linked to general bugs in the data acquisition (for example, a Digitizer not triggering), to a wrong acquisition of the input signal (for example if a signal contains spikes or if it is not sampled in the proper way) or to instabilities of the board during the measurements.
In conclusion we give some general advices, valid for each tested Digitizer family, based on our specific tests. In Tab. **1** and **2** we report the firmware and software revisions used for our measurements.

FW/Digitizer	V1720	V1724	V1740	V1740D	V1751
Waveform recording	4.14_0.14	4.14_0.14	4.15_0.12	4.15_0.12	4.14_0.7
DPP-PHA		4.15_128.36			
DPP-PSD	4.9_131.11				4.11_132.8
DPP-QDC				4.15_135.10	

Tab. 1: Digitizer firmware used for the measurements presented in the Application Note.

FW/SW	WaveDump rel. 3.8.1	MC^2 Analyzer rel. 1.0.23	PSD Control Software rel. 1.3.5	QDC Demo Software rel. 1.0
Waveform recording	All boards			
DPP-PHA		V1724		
DPP-PSD			V1720, V1751	
DPP-QDC				V1740D

Tab. 2: CAEN software used for the data acquisition with boards equipped with different firmware. All listed firmware and software are available on the CAEN website. Refer to [**3**],[**4**],[**5**] and [**6**] for the software management.

Measurements setup

As mentioned above, we used two main measurements setup for each board, one using the internal clock generator and one using an external clock source. Fig. **1** reports a simplified scheme of the digitizer clock synthesis and distribution. We report here a brief description of the hardware components and their operation. We will see later how to modify the clock configuration with **CAENUpgrader**.

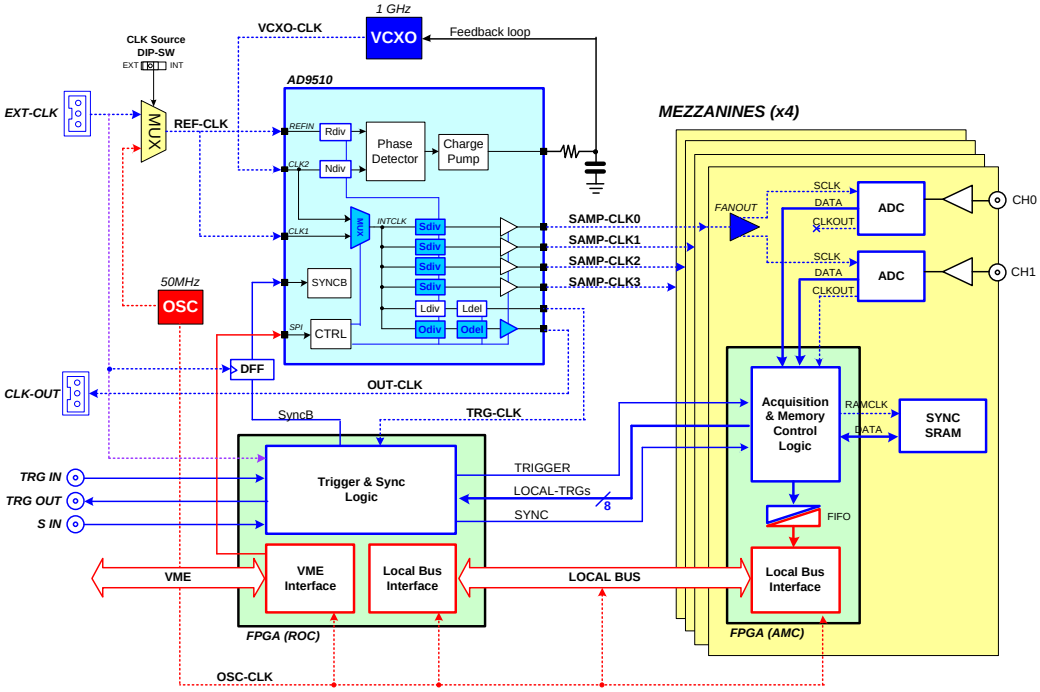

Fig. 1: Representation of the clock signal synthesis and distribution for a V1724 CAEN Digitizer

In a CAEN Digitizer the clock management is provided by a PLL (Phase-locked Loop) circuit and a Clock Distributor. The PLL can receive a reference clock from either an internal oscillator (50 MHz) or an external clock source through the clock input (CLK-IN) connector. A dip switch on the VME board allows to select the clock generator (INT or EXT, see Fig. **2**). The dip switch does not guarantee itself the correct programming of the PLL, therefore, when switching from INT to EXT clock and vice versa, the PLL must be reprogrammed.
The role of the PLL is therefore to align the phase of a Voltage Controlled Crystal Oscillator (VCXO) to the reference one. The generated clock is passed to the Clock Distributor, which splits the clock signal in different branches, sending each branch to board subsystems (FPGA, ADCs). The remaining branch is sent to CLK-OUT connector. The Clock Distributor can send different sub multiples of the VCXO frequency to each branch.

Concerning the communication with the boards, we used the CAEN USB Bridge V1718, running the readout software under Windows 10 - 64bit OS.

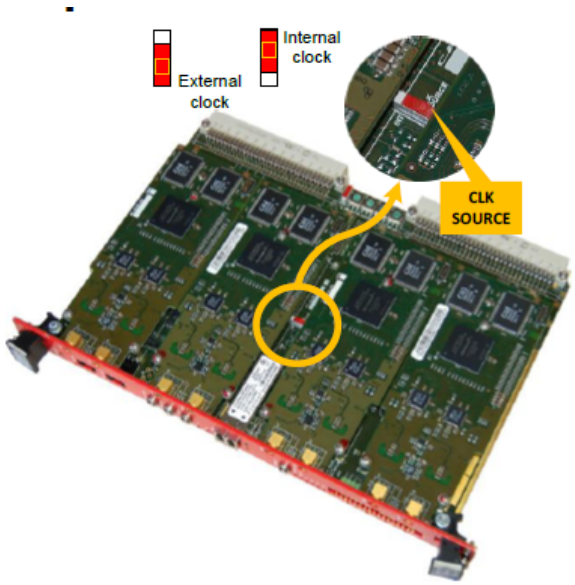

Fig. 2: The clock source dip switch on a CAEN VME Digitizer board

Downsampling using the internal clock

In order to implement the downsampling using the internal clock setup, it is required to program the PLL using **CAENUpgrader** (available on CAEN web site) through the following steps:

- Set the CLK dip switch of the VME board to INT (not required for DT/NIM form factors).
- Open CAENUpgrader and select ”Upgrade PLL”, the Board Model and click on ”new”. The PLL configuration menu will open (see Fig. **4**).
- Read the VCXO frequency from the board, which automatically sets the correct value in the GUI.
- Select the desired ADC sampling frequency (see Fig. **5**).
- Click on ”save”. A .rbf file will be generated to upgrade the PLL.
- Click on ”Upgrade” in the main menu of CAENUpgrader to upgrade the PLL frequency and reboot the board. After the reboot the ”PLL LOCK” LED of the Digitizer must be on, otherwise repeat the procedure.

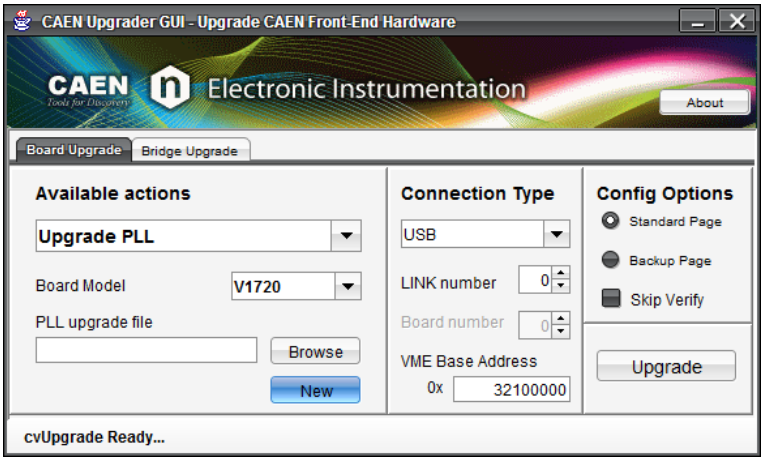

Fig. 3: CAENUpgrader main menu to configure a V1720 Digitizer PLL upgrade

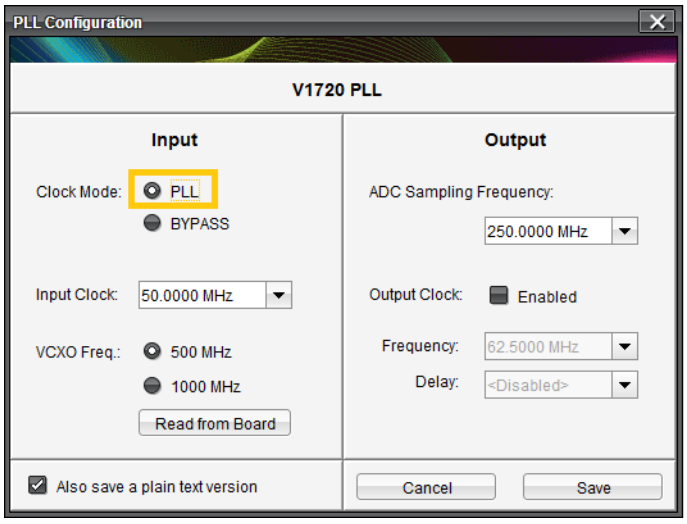

Fig. 4: CAENUpgrader PLL Configuration menu for a V1720 Digitizer

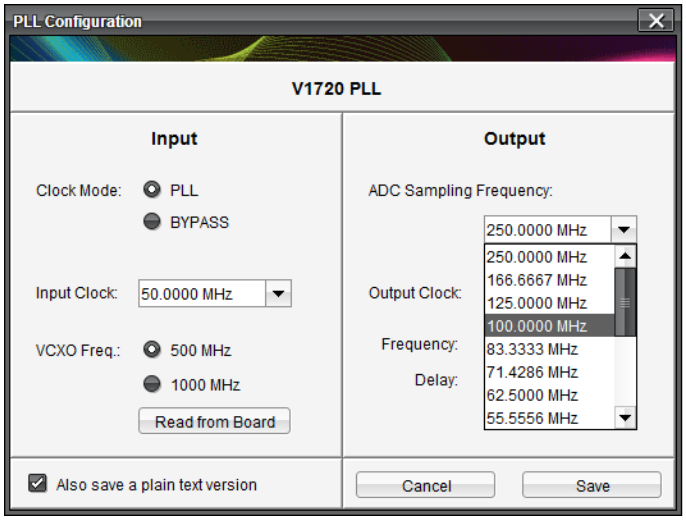

Fig. 5: ADC sampling frequency configuration for a V1720 Digitizer

With this setup the clock is generated through the internal PLL circuit, therefore it is sufficient to provide an analog signal to the board input to begin the data acquisition.
For each board, we tested all the theoretically admissible ADC sampling frequencies, which are listed in CAENUpgrader.

Downsampling using the external clock and Bypass mode

An alternative setup to perform downsampling is to use an external clock source and program the PLL in Bypass mode. To use this setup it is necessary to program the PLL in Bypass mode using CAENupgrader (the PLL circuit is bypassed, and the external clock is simply splitted by the internal Clock Distributor and directly provided to the ADCs). Perform the steps listed below:

- Set the CLK dip switch of the VME board to EXT
- Open CAENUpgrader and select ”Upgrade PLL”, the Board Model and click on ”new”. The PLL configuration menu will open.
- Select the Bypass option[1](see Fig. **6**).

[1] the x740 family does not support the Bypass mode.

- Click on ”save”. A .rbf file will be generated to upgrade the PLL.
- Click on ”Upgrade” to set the PLL in Bypass mode and reboot the board. After the reboot the ”PLL LOCK” LED of the Digitizer must be off, while the ”PLL BYPSS” LED will turn on (if it does not happen repeat the upgrade procedure).

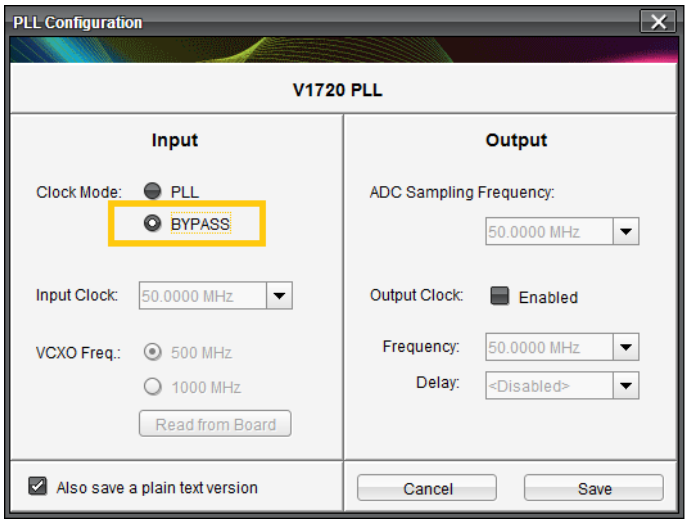

Fig. 6: Bypass mode configuration in CAENUpgrader for a V1720 Digitizer

With this configuration you need to **connect an external clock source to the CLK-IN** connector of the board. The CLK-IN accepts only standard differential signals as LVDS, ECL, PECL, LVPECL, MCL. The clock signal must have a Z_{diff}= 100 Ω and the jitter must be less than 100 ppm. A signal of this type can be generated by a commercial clock unit responding to the listed requirements or by a function generator. It is recommended to use a differential signal among the types listed above because of their better quality.
If you are not able to generate differential signals, you can use a CAEN A318 cable adapter to convert a single-ended LEMO input into the differential standard supported by the CLK-IN input connector of CAEN Digitizers. In this way it is possible to use a single-ended signal with amplitude of about 1 V_{pp} (for example a NIM signal) as external clock reference. For our purposes, we used the second setup, sending to the CLK-IN a square wave with amplitude of 1 V_{pp}, as shown in Fig. **7**. The frequencies of the external clock were chosen accordingly to the frequencies reported in CAENUpgrader ver. 1.6.3 for the ADC sampling.

Acquisition test

We performed different acquisition tests with V1720, V1724, V1740, V1740D, V1751 Digitizers using four different firmware/clock combinations:

- Board equipped with Waveform Recording firmware, Internal Clock
- Board equipped with DPP firmware, Internal Clock
- Board equipped with Waveform Recording firmware, External Clock and Bypass Mode
- Board equipped with DPP firmware, External Clock and Bypass Mode

We remark that the results given in this Application Note are valid for the last official firmware revision available at the date of the test. In particular the firmware and software versions used for each digitizer are listed in Tab. **1** and **2**.
To evaluate the success or the failure of the test we send to all board channels a **square pulse with negative polarity, frequency of 1 kHz and width of about 1 µs** (see Fig. **8**) and perform a data acquisition of that signal. We tested all the clock frequencies available in CAENUpgrader for each board. For each clock frequency, we performed event acquisition,

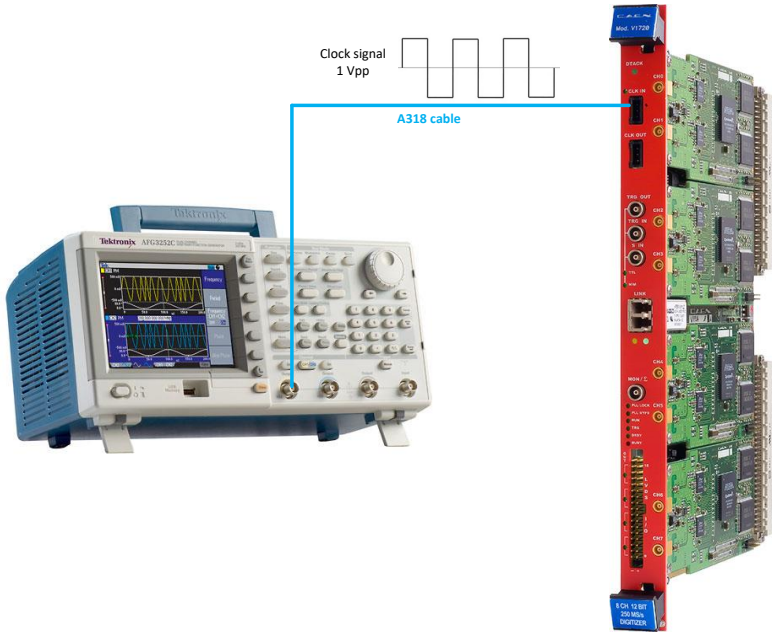

Fig. 7: Connection setup to operate with an external clock with a VME Digitizer

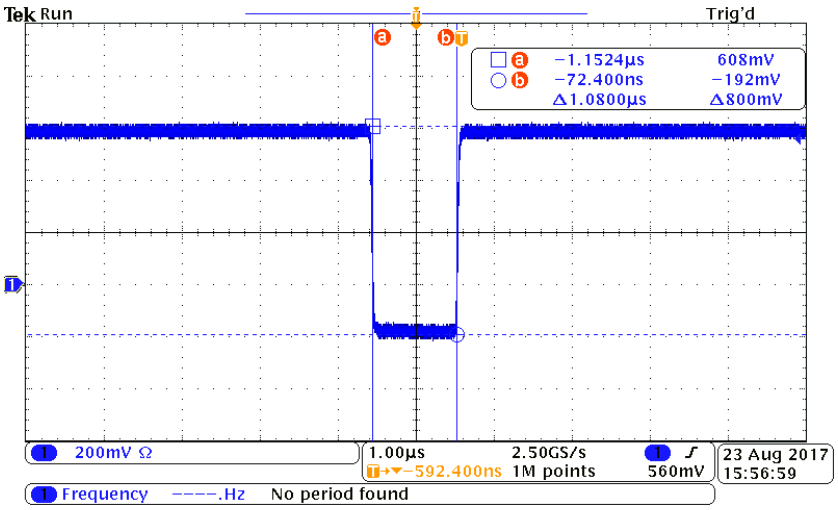

Fig. 8: Oscilloscope screenshot of the square pulse waveform used as input signal.

checking the coherence of the data with the new sampling frequency [2] and the communication stability over a few minutes of acquisition. In addition, when using a board equipped with a DPP firmware, we performed the acquisition in LIST mode too, checking the visualization of the histogram and verifying whether the board fell into the BUSY state.

[2] In CAEN Readout softwares, when changing the clock frequency, the plotted pulse width is scaled accordingly to the new sampling frequency. Example: using a V1720, which has a standard sampling frequency of 250 MHz, the plotted pulse width w is scaled according to the following formula:

$$w = T \cdot \frac{f}{250MHz} \quad (1)$$

where T is the set pulse width (in our case 1µs) and f the clock frequency expressed in MHz. If this equation is satisfied we can conclude that the sampling of the input signal is coherent with the set clock frequency.

Results

In this section we outline the results of the measurements performed with CAEN Digitizers. To be schematic we will report the results in tables, where the success of the acquisition test is indicated for each setup and each clock frequency. A green thick indicates a successful test, responding to the criteria indicated in the previous paragraph. A red cross indicates a failure.

V1720				
Clock frequency (MHz)	TEST1 FW Waveform Recording Internal clock - PLL	TEST2 FW DPP Internal clock - PLL	TEST3 FW Waveform Recording External clock - Bypass	TEST4 FW DPP External clock - Bypass
166.6667	X	X	X	X
125.0000	✓	✓	✓	✓
100.0000	✓	✓	✓	✓
83.3333	✓	✓	✓	✓
71.4286	✓	✓	✓	✓
62.5000	X	✓	✓	✓
55.5556	✓	✓	X	✓
50.0000	✓	✓	X	✓
45.4545	✓	✓	X	✓
41.6667	✓	✓	X	✓
38.4615	✓	✓	X	✓
35.7143	✓	✓	X	✓
33.3333	✓	✓	X	✓
31.2500	✓	✓	X	✓
29.4118	X	✓	X	✓

Tab. 3: Results of the downsampled data acquisition for the CAEN Digitizer V1720.

V1724				
Clock frequency (MHz)	TEST1 FW Waveform Recording Internal clock - PLL	TEST2 FW DPP Internal clock - PLL	TEST3 FW Waveform Recording External clock - Bypass	TEST4 FW DPP External clock - Bypass
83.3333	✓	✓	✓	✓
71.4268	✓	✓	✓	✓
62.5000	✓	✓	✓	✓
55.5556	✓	✓	✓	✓
50.0000	✓	✓	✓	✓
45.4545	✓	✓	✓	✓
41.6667	✓	✓	✓	✓
38.4615	✓	✓	✓	✓
35.7143	✓	✓	✓	✓
33.3333	✓	✓	✓	✓
31.2500	✓	✓	✓	✓
29.4118	✓	✓	✓	✓
27.7778	✓	✓	✓	✓
26.3158	✓	✓	✓	✓
25.0000	✓	✓	✓	✓
23.8095	✓	✓	✓	✓
22.7273	✓	✓	✓	✓
21.7391	✓	✓	✓	✓
20.8333	✓	✓	✓	✓
20.0000	✓	✓	✓	✓
19.2308	✓	✓	✓	✓
18.5185	✓	✓	✓	✓
17.8571	✓	✓	✓	✓
17.2414	✓	✓	✓	✓
16.6667	✓	✓	✓	✓
16.1290	✓	✓	✓	✓

Tab. 4: Results of the downsampled data acquisition for the CAEN Digitizer V1724.

V1740				
Clock frequency (MHz)	TEST1 FW Waveform Recording Internal clock - PLL	TEST2 FW DPP Internal clock - PLL	TEST3 FW Waveform Recording External clock - Bypass	TEST4 FW DPP External clock - Bypass
55.5556	X			
50.0000	✓			
45.4545	X			
41.6667	X			
38.4615	X			
35.7143	X			
33.3333	X			
31.2500	X			
29.4118	X			
27.7778	X			
26.3158	X			
25.0000	X			
23.8095	X			
22.7273	X			
21.7391	X			
20.8333	X			
20.0000	X			
19.2308	X			
18.5185	X			
17.8571	X			
17.2414	X			
16.6667	X			
16.1290	X			

Tab. 5: Results of the downsampled data acquisition for the CAEN Digitizer V1740. Only a test with the Waveform Recording firmware and the internal clock setup is supported by this board.

V1740D				
Clock frequency (MHz)	TEST1 FW Waveform Recording Internal clock - PLL	TEST2 FW DPP Internal clock - PLL	TEST3 FW Waveform Recording External clock - Bypass	TEST4 FW DPP External clock - Bypass
55.5556	X	✓		
50.0000	X	✓		
45.4545	X	✓		
41.6667	X	✓		
38.4615	X	✓		
35.7143	X	✓		
33.3333	X	✓		
31.2500	X	✓		
29.4118	X	✓		
27.7778	X	✓		
26.3158	X	✓		
25.0000	X	✓		
23.8095	X	✓		
22.7273	X	✓		
21.7391	X	✓		
20.8333	X	✓		
20.0000	X	✓		
19.2308	X	✓		
18.5185	X	✓		
17.8571	X	✓		
17.2414	X	✓		
16.6667	X	✓		
16.1290	X	✓		

Tab. 6: Results of the downsampled data acquisition for the CAEN Digitizer V1740D. Only the internal clock setup is supported by this board.

V1751				
Clock frequency (MHz)	TEST1 FW Waveform Recording Internal clock - PLL	TEST2 FW DPP Internal clock - PLL	TEST3 FW Waveform Recording External clock - Bypass	TEST4 FW DPP External clock - Bypass
500.0000	✓	✓	X	X
3333.3333	✓	X	X	X
250.0000	✓	✓	X	X

Tab. 7: Results of the downsampled data acquisition for the CAEN Digitizer V1751.

Conclusion

In this conclusive paragraph we summarize the results of our measurements. This summary can be considered as a guideline to use CAEN Digitizer families x720, x724, x740, x751 with a lower sampling frequency than the default one. A graphical summary of all the measurements results is reported in Fig. **9**. Given these results we can draw up a list of advices for those users interested in lowering the sampling frequency of their Digitizers:

- **720 family**: for clock frequencies from 125 MHz to 29.4118 MHz data acquisition should be always possible with a board mounting a DPP-PSD firmware. When using the Waveform Recording firmware, the Bypass mode is not supported for frequencies lower than 62.5 MHz, while we suggest to use PLL mode only from 125 MHz to 71.4268 MHz.
- **724 family**: the downsampling should be always possible from 83.333 MHz to 16.1290 MHz. Moreover the Decimation function is supported by this family, both with the Waveform Recording or the DPP-PHA firmware.
- **740 family**: it is recommended to use the Decimation function with the Waveform Recording firmware, while, if mounting a DPP-QDC firmware, it is possible to use the PLL downsampling mode. The Bypass mode is not supported.
- **751 family**: use **only** the PLL mode, avoiding to use a clock frequency of 333.333 MHz when mounting a DPP-PSD firmware. The Bypass mode is not supported.

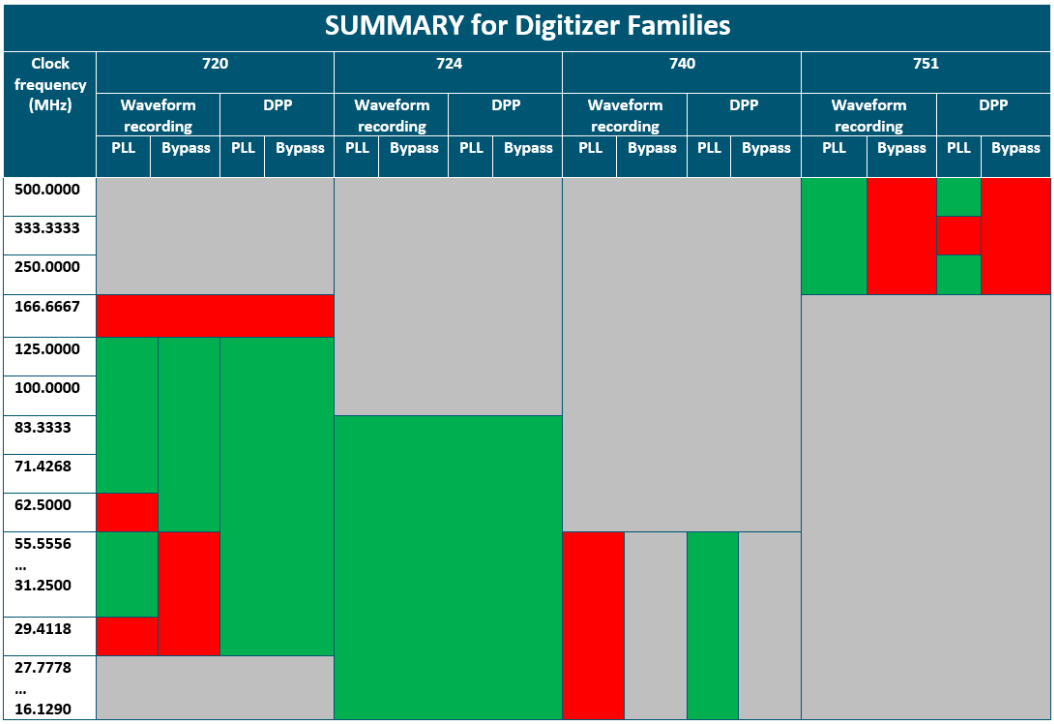

Fig. 9: Summary of the results of downsampling measurements performed on 720/724/740/751 Digitizer families.
Colors meaning:
Red = acquisition test failed.
Green= acquisition test passed.
Grey = not supported.

References

[**1**] UM3248 – V1724 & VX1724 User Manual.

[**2**] V1740 & VX1740 User Manual.

[**3**] UM2091 – CAEN WaveDump User Manual.

[**4**] UM2580 – DPP-PSD User Manual.

[**5**] UM3182 – DPP-PHA and MC2Analyzer User Manual.

[**6**] UM4874 – DPP-QDC User Manual.

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