Application Note AN5995
Dead Time characterization of the x725-x730 Digitizer Family with DPP-PSD

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Introduction

The aim of this measurement is to characterize the dead-time of the x725 and x730 digitizer families running DPP-PSD firmware. The algorithm can self-trigger on the input pulses, open an integration gate of programmable width, and provide time stamp and charge (integral) of the pulses. Optionally, it is also possible to save a portion of the waveform, but in this case the dead time will be higher.

Test Setup

- DT5730 with DPP-PSD firmware Rev. 4.11_136.11
- Pulse Generator Tektronix AFG3102; Burst Mode with N-Cycles = 2, Trigger Interval = 1 ms (1 KHz).
- Software: digiTES ver. 4.3.3.

Main settings in the config file:

```
AcquisitionMode         LIST
RecordLength            20
PreTrigger              4
DiscrMode               LED
TriggerThreshold        100
TrgHoldOff              0
TTFsmoothing            1
GateWidth               4
ShortGateWidth          2
PreGate                 2
```

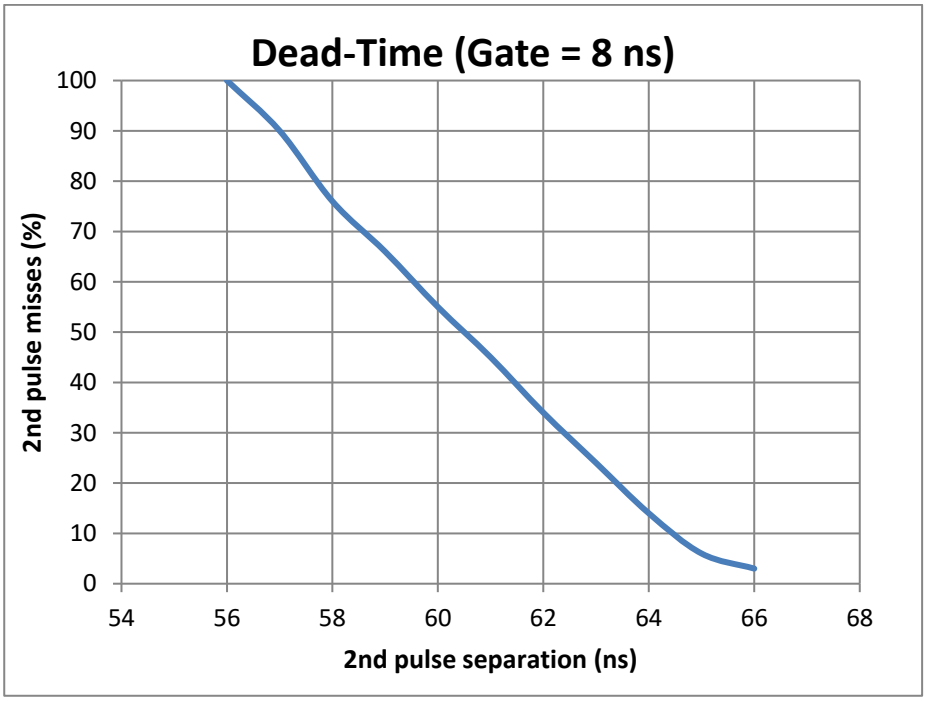
Disable on-line time stamp interpolation (option in sysvars.txt):

```
FineTstampMode          2
```

For every trigger, the pulser generates 2 pulses separated by a time **Tp** (set by “period” in the generator). When Tp is higher than the dead time of the digitizer, both pulses are acquired and the count rate reported by the software is 2 KHz. The time Tp is decreased until the digitizer starts to miss the 2nd pulse. The dead time is defined as the time Td for which the digitizer misses the 2nd pulse 50% of the times, thus the count rate is 1.5KHz.

Results

The following plot shows the number of 2nd pulse misses (in percent) as a function of the pulse separation Td. Below 56 ns, the 2nd pulse is always missed. At ~61 ns, 50% are missed. Considering that the integration gate is 8 ns, the intrinsic dead time of the algorithm is about ~53 ns.



The intrinsic dead time is almost independent of the gate settings: when the gate width increases, the total dead time increases by the same amount, but only every 8 ns (16 ns for 725 series), which is given by the clock frequency of the FPGA internal logic. For example, the dead time (50% of 2nd pulse missed) remains constant for Gate Width = 8, 10, 12, and 14 ns; when Gate Width = 16 ns, the dead time increases by 8 ns and it remains constant for Gate Width = 16, 18, 20, and 22 ns. Values must be multiplied by 2 for 725 series.
The dead time is independent on the PreGate.
In conclusion, the total dead time can be calculated by the following formula:

1. For the x730 family:
   DeadTime = 53 ns + GateWidth + (GateWidth % 8)
   (where % is the C operator, that is remainder after division)
2. For the x725 family:
   DeadTime = 53 ns + GateWidth + (GateWidth % 16)
   (where % is the C operator, that is remainder after division)

This measurement is made with disabled waveforms (Acquisition Mode = LIST), Trigger Hold-Off set to zero and disabled on-line timing interpolation (Extras Selection != 2). When the interpolation is enabled, the minimum dead time is 156 ns.

In MIXED mode (readout of waveform) the dead time is also function of the “Record Length” and “Pre Trigger”. For small values of Record Length, the dead time does not change significantly. For instance, RecordLength = 24 samples (48 ns) and PreTrigger = 10 samples (20 ns) give a dead time of ~68 ns. For RecordLenght = 64 samples (128 ns) and PreTrigger = 24 samples (48 ns), the total dead time is ~150 ns.

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