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Abstract

Digital sampling technique has become common in many applications as homeland security and nuclear medicine as well as in research fields as nuclear and particle physics. Digital sampling devices can represent multichannel oscilloscopes, but at the same time they can implement in Field Programmable Gate Arrays (FPGAs) algorithms traditionally operated by analogic devices. These algorithms can operate data reduction through programmable on-board computation.

In the present note we focus our attention on the techniques for time measurement. We will describe one of the algorithms typically used for this measurements, it implementation and their performances, which are obtained in some benchmark tests.

Introduction

Traditional analog devices as the Constant Fraction Discriminators (CFDs) and Time-to-Digital Converters (TDCs) can be very competitive in terms of channel density and cost. For these reasons highly segmented detectors are often read out by analog devices, which have custom made specification to guarantee a perfect match with the experimental requirements. Despite these advantages, in some applications the requirement of simultaneous measurement of energy and time poses the practical issue of complex device connections. On the contrary, digital acquisition systems are directly connected to front-end electronics converting analog signals to digital information. This may result eventually in a system with less cables, less signal distortion and potentially more convenient. Digital data is processed by real time FPGA algorithms, which replace traditional analog modules.

In some applications the implementation of a digitizer for time measurements is profitable or even necessary:

- Applications that require an excellent timing resolution of the whole chain, of the order of few ps;
- Simultaneous acquisition of time and energy information: digitizers can do both;
- Online walk correction with integrated charge or amplitude;
- Bursts of very close pulses (e.g. Free Electron Lasers), since digitizer can integrate memories and operate without dead time.

We now proceed with a brief description of the digital CFD (dCFD) method and the contributions to the time measurement uncertainty. We then report some experimental tests we conducted with radiation detection devices and analog function generators. Finally some considerations are drawn.

Time Stamp Determination

Time measurements consist in marking the time when the signal crossed a determined amplitude. Digital acquisition systems convert detector signals in a sequence of digitized samples regularly spaced in time. This conversion reduces the time information in a discrete quantity, which poses a limit in the resolution of the measurement of threshold crossing time. To overcome this limitation, interpolation methods may be used, which approximate the signal shape with analytic functions. These methods require the digital data of the sampled waveform and high transfer bandwidth is needed to transfer it. For this reason FPGA processing with simple algorithms may satisfy many applications where high signal rates do not allow the waveform data transfer.

Time stamp of analog signals is traditionally obtained with CFD modules, which function is documented in several nuclear textbooks e.g. [1][2]. The CFD technique sets the time stamp of a pulse at the moment when the amplitude reaches a fixed fraction of the full amplitude. This choice of the pulse arrival time is generally not dependent on the pulse amplitude, therefore pulses over a wide dynamic range can be discriminated with a low time jitter. Our firmware intends to exploit these advantages of a CFD technique using a digital sampling device. At the same time we implement a simple linear interpolation between two points to eliminate the time degradation due to the clock granularity.

The **digital Constant Fraction Discriminator** can be computed from sampled data in the following way.

1. Transform the sampled data points (S_i) subtracting the sample delayed by "*d*" from a fraction *"k"* of the sample S_i

$$S_i \rightarrow S_i^{'} = k \cdot S_i - S_{i-d}$$

k = fraction (0<k<1)
d = delay

2. Set a threshold to arm the search of the zero crossing.
3. Find the zero crossing identifying the two consecutive samples across it.
4. Compute a linear interpolation using the two points and find the intersection with the zero axis.

The choice of *k* and the *d* has to be taken to optimize the resolution obtained. There is no a priori condition which guarantees the best result. In several application the optimal setting is obtained with a fraction of about 20% of the signal amplitude and a delay corresponding to the time lapse between the 20% threshold and the peak of the signal.

Following the previous procedure the time resolution can be approximated with the equation

$$\sigma_t \leq \sigma_{tot}\left[\left|\frac{dS'}{dt}\right|_{S'=0}\right]^{-1}$$

$$\sigma_{tot}^2 = \left(1+k^2\right)\cdot\left(\sigma_e^2 + \frac{1}{12\cdot 4^{ENOB}}\right) \qquad (1)$$

σ_e = standard deviation of the electronic noise

ENOB = Effective Number of Bits of the ADC converter

k = CFD fraction

S' = analog signal after the CFD transformation

$$S_{(t)} \rightarrow S'_{(t)} = k\cdot S_{(t)} - S_{(t-\Delta t)}$$

The previous equations hold in case there is no rise time dependency on other parameters, like the signal amplitude or the event rate.

The time stamp resolution in Eq. (1) has been estimated assuming a signal linear shape around the zero crossing. The non-linearity of the signal may cause resolution degradation since the lack of synchronization between the sampling clock and the signal translates in a random interpolation error. The contribution depends on the shape of the signals and may easily be higher than the resolution due to sampling rate as reported in Eq. (1). The effect of the non-linearity can be quantified with e.g. Monte Carlo method with a proper modelling of the analog signal shape.

In some applications, the linear interpolation of two points, in step 4, can be substituted by a linear regression on more data points. This choice can be taken when several sampling points are taken in the signal leading edge, and the amplitude variation between two consecutive samplings around the zero crossing (expressed in least significant bits), is much lower than the ADC dynamics. When this happens a linear regression on several data points may represent a good tradeoff between the linear approximation of the CFD around the zero crossing and the interpolation accuracy.

Experimental Measurements

Experimental Setup with Plastic Scintillators and Photomultiplier Tubes

This section reports the measurements of the relative time between signals generated by scintillation in an organic scintillator. The detector assemblies used for these measurements are two R4607A-27 manufactured by Hamamatsu Photonics K.K.. The PMTs belonging to the assemblies are 10-Stage Head-on tubes, biased with photocathode negative potential set to -1.6 kV. The scintillators used for radiation detection are of type EJ-232, manufactured by Eljen Technology. Some of the relevant specifications of the scintillation material are reported here.

- Light Output, % Anthracene 55
- Wavelength of Max. Emission, nm 370
- Rise Time, ns 0.35
- Decay Time, ns 1.6
- Polymer Base Polyvinyltoluene
- Refractive Index 1.58

For the measurement of the time resolution a ^{60}Co radioactive source was used. This source generates a two photon emission in cascade, which for our purpose are considered in coincidence. The signal from the PMTs was sampled with CAEN digitizers V1751 and V1761. Full details of these digitizers and the relative product families can be found in the CAEN website www.caen.it in the Waveform Digitizers section. Some details are reported in brief here.

Digitizer	ADC bits	Analog Inputs	Sampling Rate (MS/s)	Analog Bandwidth (MHz)	Dynamics
V1751	10	8-4	1000-2000	500	1 Vpp
V1761	10	2	4000	1000	1 Vpp

One PMT signal is represented in the picture below. The pictures is taken with a screenshot from the oscilloscope Tektronix MSO 4101, 5 GS/s with 1 GHz of bandwidth.

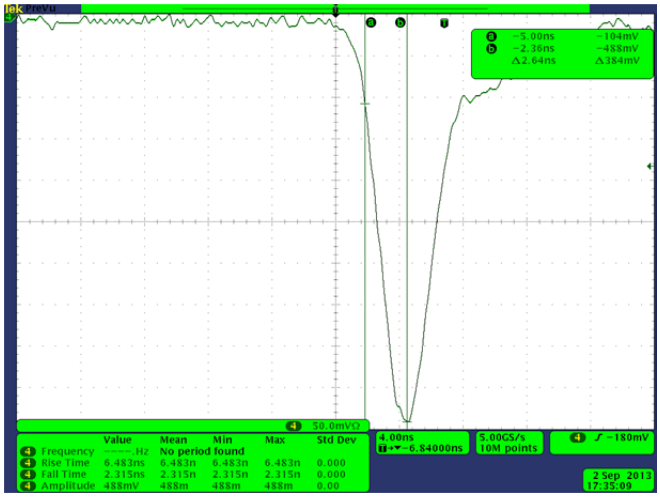


Fig. 1: PMT signal profile (Tektronix MSO 4101, 5 GS/s with 1 GHz of bandwidth) . the signal has a leading edge of about 2.3 ns between the 10% and 90% of the signal amplitude.

From the previous picture it is possible to see that the signal has a leading edge of about 2.3 ns between the 10% and 90% of the signal amplitude.

For our time measurements we set a CFD fraction of 50% and we choose the delay to find the best time resolution, corresponding usually to about 2-3 ns. We found an optimized condition for time measurement when the CFD fraction was set to 50%. Starting from the previous condition we set a delay consistent with this choice, corresponding to about 2-3 ns. The picture below shows the digital CFD obtained with a waveform digitized by the V1751 at a sampling frequency of 1 GS/s. The delay was set to 3 samples.

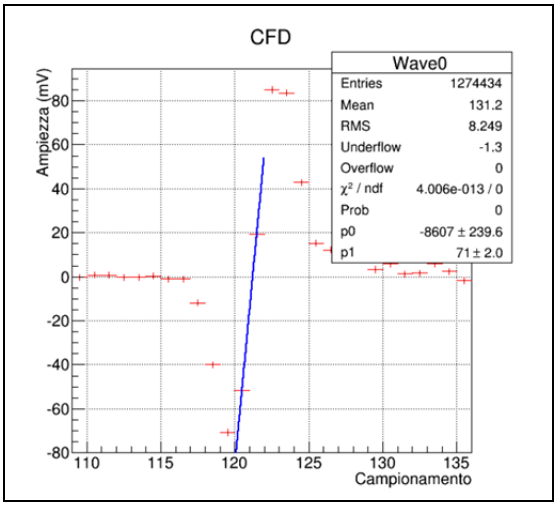


Fig. 2: digital CFD obtained with a waveform digitized by the V1751 at sampling frequency of 1 GS/s. The delay was set to 3 samples.

The study done on the time measurement is based on an offline analysis based on the CERN ROOT 5.34 [3] framework. The time stamps measured with couples of coincident signals are subtracted to obtain the measurement of relative time. The relative time is represented in a histogram and a Gaussian curve is interpolated on the measured distribution. The picture below (Fig. 3) represents the result obtained with the V1751 at a sampling frequency of 1 GS/s.

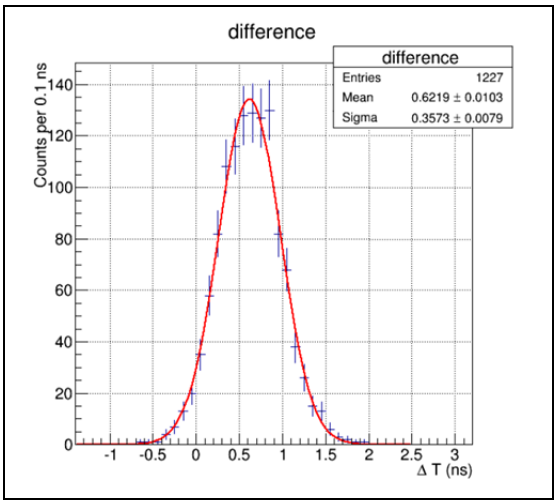


Fig. 3: Relative time result obtained with V1751 at a sampling frequency of 1 GS/s.

The best resolution obtained with two points interpolation is summarized in the table below.

Digitizer	Sampling Rate	Resolution (ps)
V1751	1 GS/s	357.3 ± 7.9
V1751	2 GS/s	354.2 ± 6.3
V1761	4 GS/s	353.5 ± 7.7

The results above express the overall resolution of the two detector assemblies and the relative acquisition chains. The intrinsic uncertainty of the detector assemblies is affected by time jitter linked to the PMT transit time, which may be of the order of few hundreds of ps. Taking this in account, the results in the table may be strongly dominated by the PMT transit time jitter. In the next sections we will describe measurements accomplished with different experimental setups, with lower intrinsic time jitter. These measurements will be a more stringent test for the performances of digitizer algorithms.

Setup with Arbitrary Function Generator

The time measurement has been accomplished using the analog outputs of the Pattern Generator Agilent 81110A. The pulse emission was driven by external trigger signals at a repetitive rate of 1 kHz and the signals were taken from the Trigger Output (TTL logic) and the Analog Output. The pattern generator provides pulses with 0.8 and 1.6 ns transition time through the Analog Output and pulses with 0.8 ns transition time through the Trigger Output.

The first set of time measurements is obtained with data taken by waveform digitizers, so the Trigger Output of the generator was attenuated to match the dynamic range of the digitizer input stages. The Trigger Output was used as start of the time measurement. The picture below represents the start (blu) and stop (red) signals sampled by the Tektronix oscilloscope DPO 3054, 2.5 GS/s with 500 MHz bandwidth.

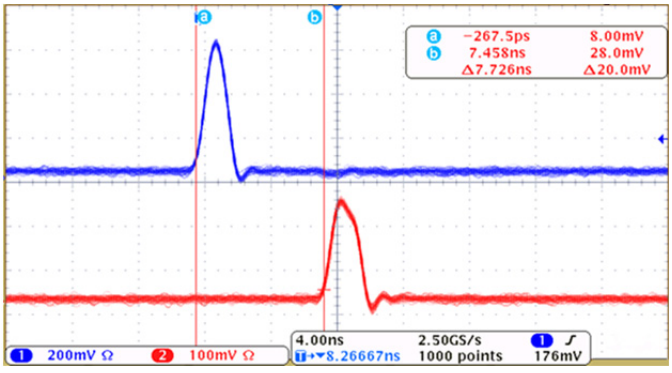


Fig. 4: Start (blu) and Stop (red) signals sampled by Tektronix oscilloscope DPO 3054, 2.5 GS/s - 500 MHz bandwidth.

The start signal has an amplitude of about 950 mV, while the stop signal of about 600 mV.

The digitizers used for this set of measurements were the DT5751, the V1761 and the DT5742. The first unit is a desktop digitizer embedding the same acquisition channels of the V1751 digitizer described in the previous section. We used the DT5751 digitizer setting the acquisition to 2 GS/s. The DT5742 is a desktop digitizer with 16 acquisition channels, which sample signals through the

DRS4 chip [4]. The DRS4 chip is a switched capacitor array, which can sample the input signal at a frequency of 5 GHz. The sampling is done loading charge on the capacitor array, then the conversion to digital, which requires about 180 µs, is done with an external ADC. The DRS4 chip needs both amplitude and time calibration to obtain the best performances. The time calibration for these measurements were accomplished by the Werner Siemens Imaging Centre of Tubingen.

For our time measurements we set a CFD fraction of 100% and we choose the delay of about 2 ns. This unusual choice of the parameters allows to have the maximum slope at the zero crossing. In equation [1] you can notice that the maximization of the slope, expressed by the term $\left|\frac{dS'}{dt}\right|$, minimize the effect of the uncertainty due to noise and quantization error. The picture below shows the dCFD obtained with a waveform digitized by the DT5751 at a sampling frequency of 2 GS/s.

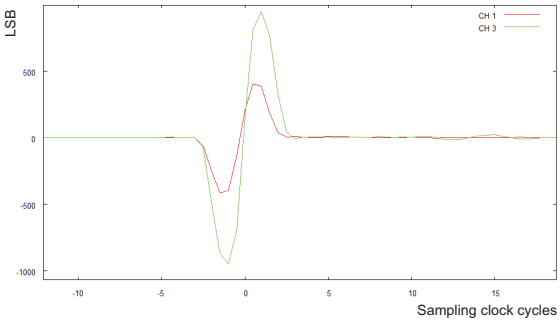


Fig. 5: dCFD obtained with a waveform digitized by DT5751 (sampling frequency: 2 GS/s).

The online time measurement is obtained finding the two points of the CFD traces across the zero and interpolating them with a line to find the higher resolved zero crossing. The delay between the start signal and the stop signal ranged between 0 and 5.5 ns, in steps of 1.1 ns. The time difference between start and stop has been measured with the resolution, expressed in standard deviation, which is reported below.

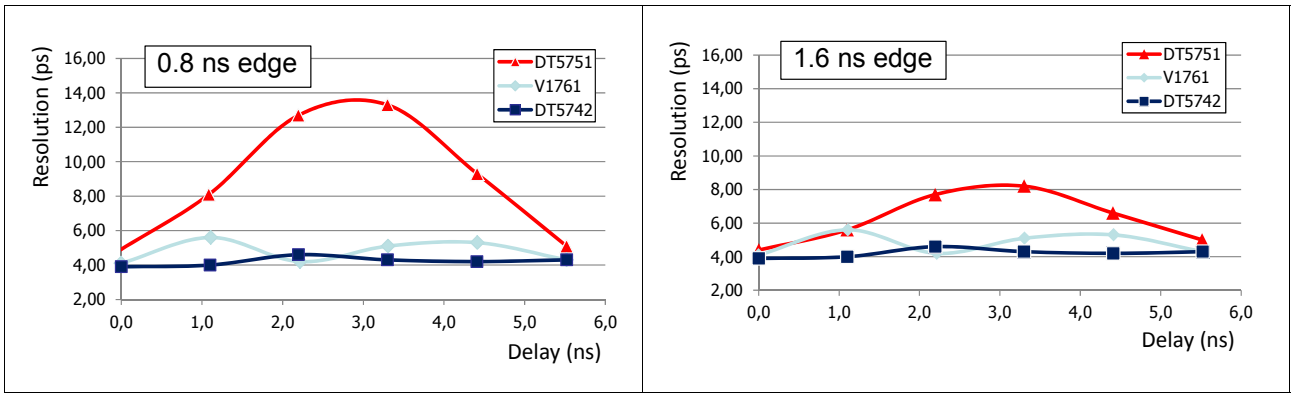


Fig. 6: DT5751, V1761 and DT5742 measurement resolution (ps) as function of start-stop delay (ns) for 0.8 ns and 1.6 ns transition time (Analog output)

It can be noticed that the time resolutions of the DT5742 and the V1761 are similar, the first resolution is less than 5 ps and the second less than 6 ps. The DT5751 performs significantly worse than the others, especially when the signal transitions are 0.8 ns. This result is due to high uncertainty contribution given by the linear interpolation, which approximates the coarse digital CFD.

A repetitive pattern can be noticed in the previous picture. This is degradation of the performances due to the interpolation process which imply a straight line approximation of the input signal. When the delay between signals differ by a integer multiple of the sampling frequency, the interpolation error is cancelled out by the time difference (start and stop time are measured with the same systematic error). Generally, this cancellation does not happen when the start and stop channel signals are out of phase.

The second set of measurements is obtained with an analog acquisition chain made of a CFD manufactured by Ortec, model 935, and a TDC CAEN, model V1290N. The polarity of the Trigger Output of the generator 81110A is inverted by mean of a wideband transformer and used as start signal of the TDC measurement. The amplitude of that signal corresponds approximately to the standard of the NIM logic. The inverted Analog Output of the generator generated pulses with 1 V amplitude was then used as CFD input. Two logic outputs of the CFD are then used to trigger the TDC measurement and to stop the time measurement. The picture below shows a sketch of the hardware setup.

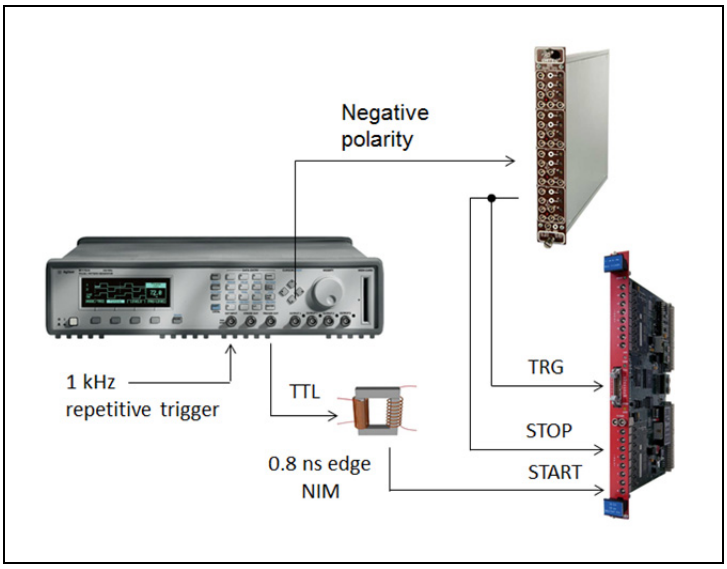


Fig. 7 Hardware setup of the second set of measurements.

The delay of the stop signal is spread over the range between 0 and 25 ns to test the integral nonlinearities of the TDC fine counter. The resolution obtained with the 0.8 ns and 1.6 ns transient signal are shown below.

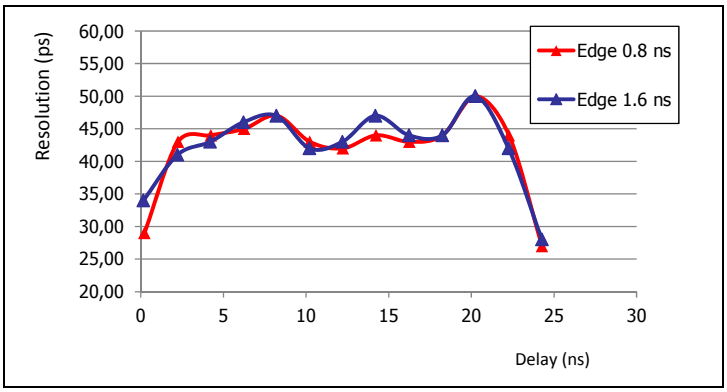


Fig. 8: Second set of measurement resolution (ps) as a function of start-stop delay (ns) for 0.8 ns and 1.6 ns transition time (Analog output).

Similar performances are obtained with the 0.8 ns and the 1.6 ns transition time. Most of the time measurements have a standard deviation between 40 and 50 ps (spreading from 30 to 50 ps), result which is slightly higher that the TDC intrinsic resolution, of 35 ps. The overall result of this commercial analog acquisition chain is significantly poorer than the one obtained with the digital acquisition system previously presented.

Setup with Silicon Pixel detectors

Time jitter measurements have been conducted in collaboration with Dr. Nicolò Cartiglia at Department of Physics of the University of Turin. The detector setup is composed by two Silicon pixel detectors, 300 µm thick, irradiated by the microwave emission of a Nd:YAG laser. The silicon sensors are first prototypes for the development of Low-Gain Avalanche Detectors (LGAD)[5]. Those are intended to generate a controlled, low gain charge avalanche through a high electric field within the silicon bulk. The laser emission is propagated through an optical fiber and then split in two branches receiving approximately the same light intensity. The two branches were terminated on the surface of the two silicon detectors.

The detectors were biased with a potential of 700 V and the signal was amplified by wideband preamplifier with factor 52 dB. The signal from the PMTs was sampled with CAEN digitizers V1751 and DT5730. The latter is a standalone desktop module. Some details on the devices are reported in brief here.

Digitizer	ADC bits	Analog Inputs	Sampling Rate (MS/s)	Analog Bandwidth (MHz)	Dynamics
V1751	10	8-4	1000-2000	500	1 Vpp
DT5730	14	8	500	250	2-0.5 Vpp

The digitizers of the 730 family integrate in their firmware algorithms for Pulse Shape Discrimination (DPP-PSD) a dCFD trace. This trace can be used for channel individual triggers and is computed onboard selecting the delay and the fraction, which has 4 possible values: 0.25, 0.5, 0.75 and 1. The firmware algorithm computes a linear interpolation of two points across the dCFD zero crossing.

In the following part of this section some results will be given, obtained with algorithms similar to the one implemented in the firmware. More information on the DPP-PSD firmware can be found on the relative user manual on CAEN website www.caen.it.

The CAEN digitizer V1751 was set to acquire data with sampling frequency of 1 GS/s and 2 GS/s in two separate data takings. A couple of sampled waveforms are shown in the picture below, setting the V1751 at 2 GS/s. In the plot the abscissa indicates the index of the ADC sampling and on the ordinate the amplitude of the signal expressed in units of LSBs.

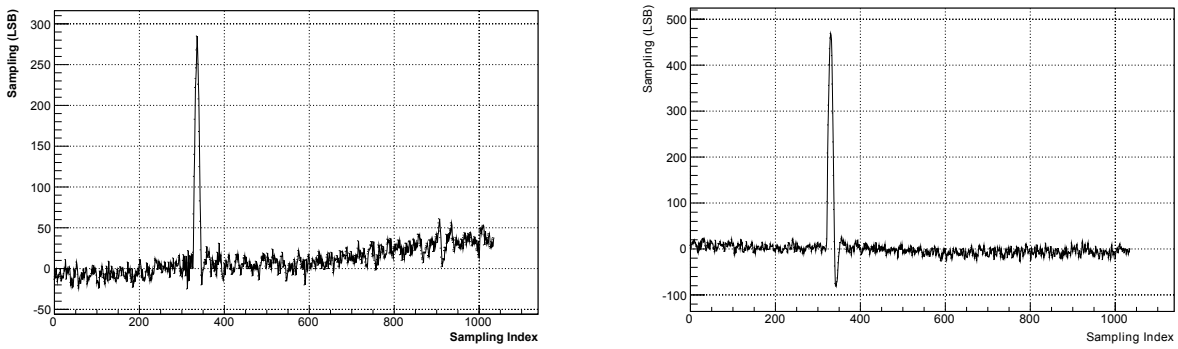


Fig. 9: Sampled waveforms using V1751 at 2 GS/s

The first group of signals are considered as start signal, while the others, the one with an accentuate undershoot, are considered stop signals. The detector pulses have a rise time (10-90% transition) of about 4.5 ns and the picture below shows them with higher detail.

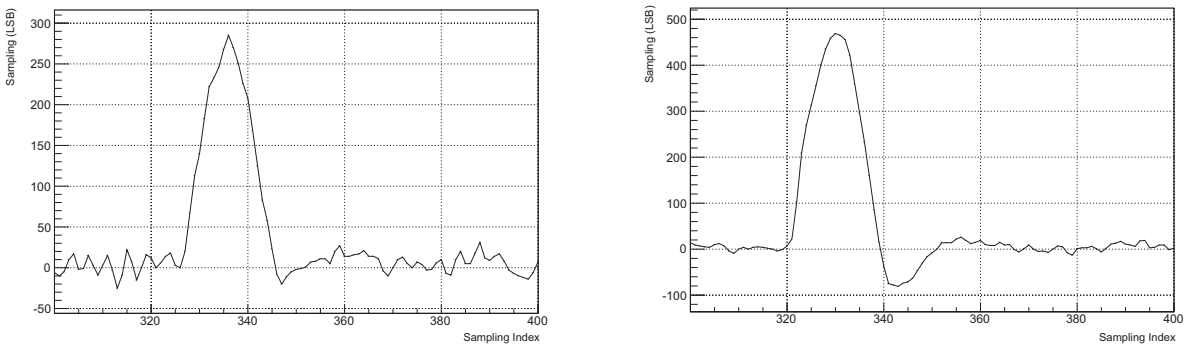


Fig. 10: Sampled waveforms using V1751 at 2 GS/s (Peaks detail)

The baseline of the signal has fluctuations which are of the order of 8.7 LSBs for the start signals and about 8.1 LSBs for the stop signals. Start signals are about 300 LSBs high, while the stop signals are about 500 LSBs. This give a signal over noise ratio of about 35 for start signals and 40 for stop ones. The observed signal amplitudes are about 2.5 and 4 times the expected 125 mV generated from minimum ionizing particles in LGAD with the same acquisition setup.

The study done on the time measurement is based on an offline analysis based on the Cern ROOT 5.34 framework [3]. We first reject events with large baseline fluctuations (if one sample differ by more than 30 LBSs the average computed on a group of previous samplings, for a total of 25 ns). Then we compute the baseline interpolating with a line data points before and after the detector signal. We subtract the baseline and compute the dCFD setting different delays and the fractions. In this analysis we compute the zero crossing interpolating 2 or more data point across the dCFD zero with a line. An example of the result of these algorithms on the digitized information is shown in the pictures below. The dCFD traces in the picture were acquired with the V1751 at 2 GS/s, the CFD delay was set to 4 ns and the fraction to 0.5.

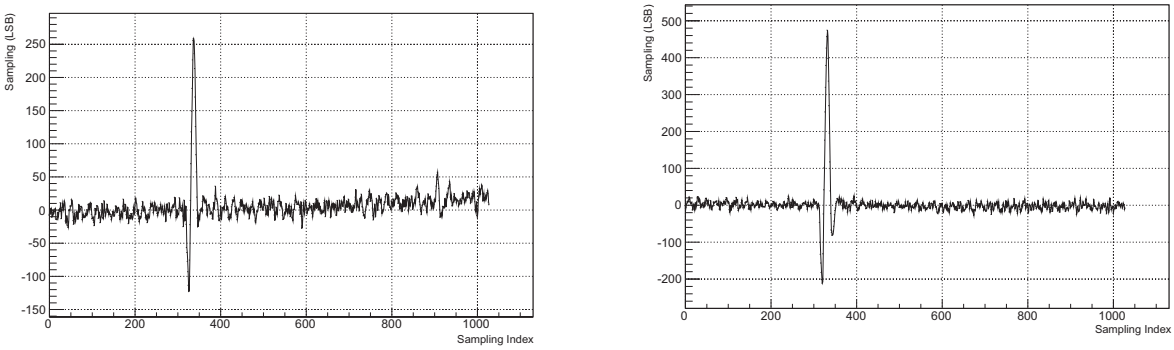


Fig. 11: dCFD traces acquired with the V1751 at 2 GS/s (CFD delay set to 4 ns and fraction to 0.5).

The dCFDs traces with the interpolated lines (in red) are shown in the picture below. The line is obtained with an interpolation of 4 sampling points close to the zero crossing: 2 negative and 2 positive samplings.

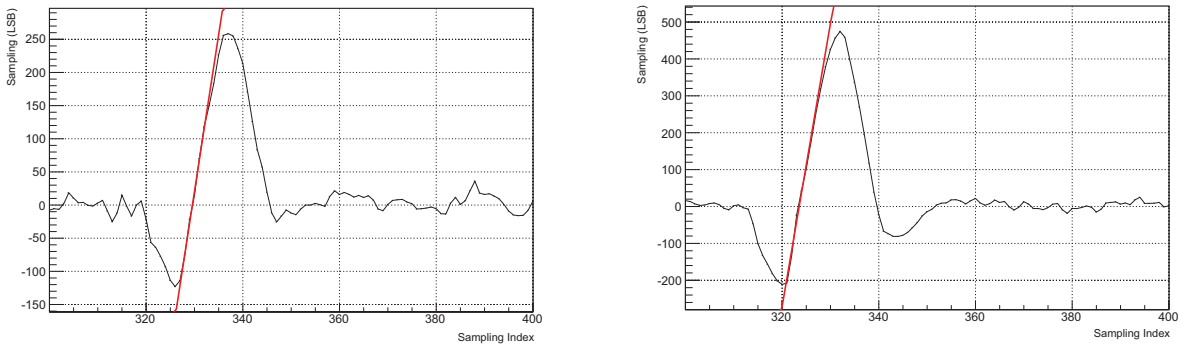


Fig. 12: dCFDs traces with interpolated lines (red)

The pulse time stamps are estimated for the two channels with the method just described. They are then subtracted to obtain the relative time. As example we report the distribution of the relative time between two pulses measured with a dCFD delay of 4 ns and a fraction of 0.5, using a sampling frequency of 2 GS/s. The distribution of 10,000 events is fitted with a Gaussian function, whose parameters are reported in the picture.

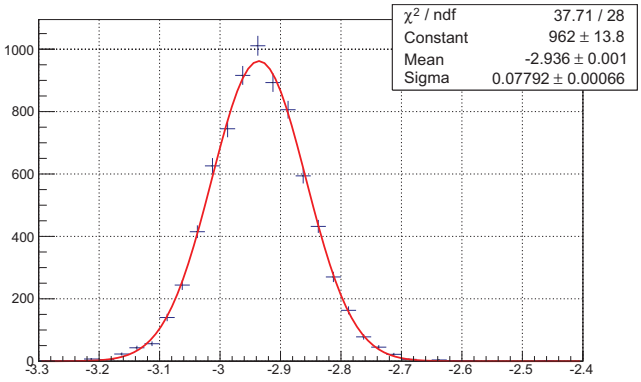
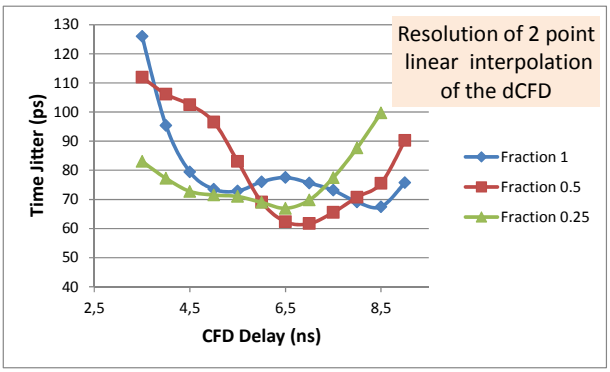
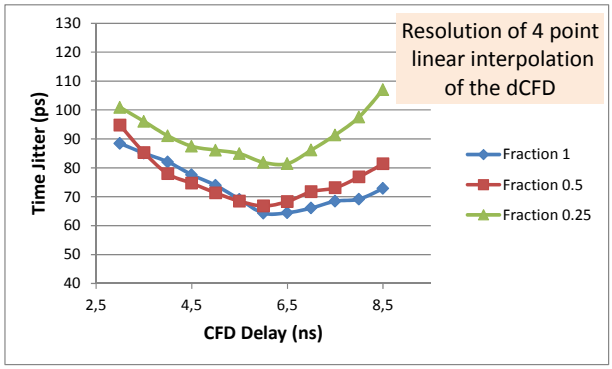
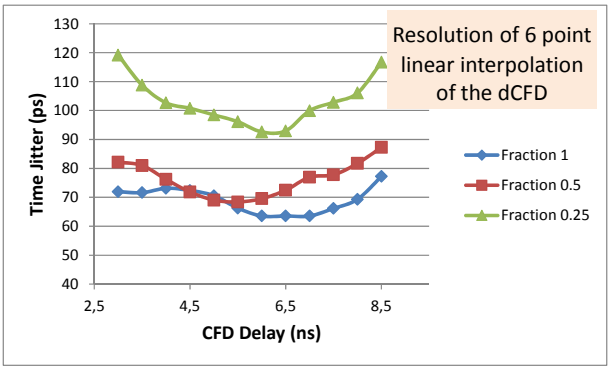


Fig. 13: Distribution of the relative time between two pulses measured with a dCFD delay of 4 ns and a fraction of 0.5, (sampling frequency of 2 GS/s). The distribution of 10,000 events is fitted with a Gaussian function, whose parameters are reported in the picture.

We report below the time resolution that is given by the interpolation of a Gaussian function on the time distribution. We analyze the resolution changing the parameters used for the dCFD and the number of points used for the linear fit around the zero crossing. The results obtained with the linear fit over 2, 4 and 6 points are represented in the pictures below.







Smallest resolutions:

Resolution	Interpolation	CFD fraction	delay
61.7 ± 0.5 ps	2 point	0.5	7 ns
64.4 ± 0.5 ps	4 point	1	6 ns
63.5 ± 0.5 ps	6 point	1	6 ns

Fig. 14: Results obtained with the linear fit over 2, 4 and 6 points (V1751 at 2 GS/s).

We conducted a similar analysis on the data taken at a sampling frequency of 1 GS/s. With the first data sample we obtain a resolution of 68.2 ± 0.7 ps, achieved with a dCFD delay of 5 ns and a fraction of 1, using liner interpolation over four points around the zero crossing.

We analyzed the data acquired with the DT5730 and made a study similar to the one described before. The dynamic range of the device was set via software to 2 Vpp. The waveforms acquired with this device are shown in the picture below.

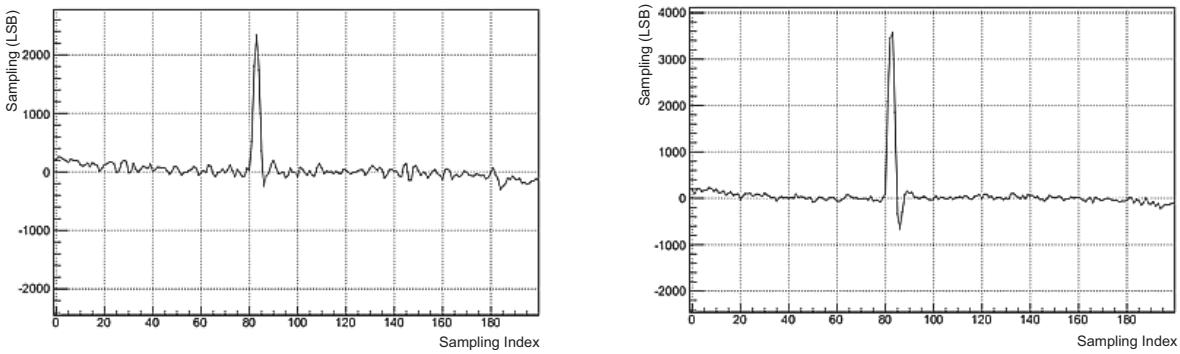
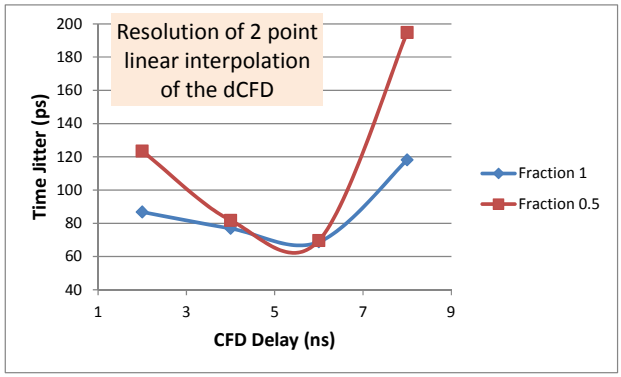


Fig. 15: Sampled waveforms using DT5730 at 500 MS/s

We analyze the resolution changing the parameters used for the dCFD and we report the time resolution that is given by the interpolation of a Gaussian function on the time distribution. The results obtained with the linear fit over two points are represented in the picture below.



Smallest resolution:

Resolution	Interpolation	CFD fraction	delay
68.8 ± 1.6 ps	2 point	1	6 ns

Fig. 16: Results obtained with the linear fit over 2 points (DT5730 at 500 MS/s).

The smallest resolution achieved with the DT5730 data method is 68.8 ± 1.6 ps, obtained CFD fraction of 1 and a delay of 6 ns. It is possible to notice that in spite of the reduction of the sampling frequency to 500 MS/s, the measured time jitter increases by 20% only.

Conclusions

The algorithms described in the present note can be easily embedded into the data acquisition software and provide accurate time measurements, which can reach few picosecond resolution.

Digitizers are capable to measure time stamps with higher accuracy compared to commercial analog solution composed by CFD and TDC modules. This difference in time resolution emerges significantly when experimental setup have low time jitter between pulses, of the order of some tens of picoseconds. This has been shown before in the experimental setup with function generators. Also the switching capacitor technology is highly competitive in terms of cost and provide performances comparable to fast ADC chips, but at present time can be limited by analog-to-digital conversion dead time.

References

[1] "Radiation Detection and Measurement", G. F. Knoll, Edited by John Wiley & Sons, Inc..
[2] "Techniques for Nuclear and Particle Physics Experiments" 2nd ed. 1994, W.R. Leo, Edited by Springer-Verlag
[3] Software and documentation available at http://root.cern.ch/
[4] Development of High Speed Waveform Sampling ASICs", http://www.psi.ch/drs/DocumentationEN/nsni10.pdf
[5] N. Cartiglia et al., arXiv:1312.1080v2

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